Chapter 6

MMIC Fabrication and Measurement

This chapter presents the performance characterisation of four prototype MMICs fabricated in this thesis: two 15GHz single-ended injection-lockable VCOs, a 24GHz differential cross-coupled VCO and a 1/6 synchronous static frequency prescaler operating at 24GHz. On-wafer measurement was carried out in the High Speed IC Laboratory at the ETH Zürich during a three week return trip to Switzerland. Measured results are compared to the simulated predictions and state-of-the-art data reported in the literature.

6.1   Fabrication

The IBM 0.18μm SiGe BiCMOS7WL process was identified at the research planning phase as the optimal fabrication technology because of its lower cost, availability and highly refined state in terms of device model accuracy and design kit maturity. Refer to Section 2.5 for an overview of SiGe BiCMOS and the IBM technology.

The three VCO circuits, ET15G, ET15G_V2 and XC24G were submitted for fabrication by the ETH Zürich as part of a Multiple Project Wafer (MPW) run. The frequency prescaler, SDIV6 was submitted by the Technical University of Dresden (TUD) also in a MPW run. Figure 6.1 shows the fabricated MPW wafer samples. Note that scribe lines[9] have been incorporated into the ETHZ chip, enabling sawing of the die into its constituent chips. This facilitates individual chip separation for bonded test board measurement if desired. The

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[9]Scribe lines consist of crack-stop structures placed in channels separating adjacent chip boundaries. The channel width is sufficient for the saw blade to pass through while possible stress fractures or damage to the wafer edge are mitigated via the crack-stop structure.

absence of scribe lines on the TUD MPW sample limits the testability to on-wafer probing only.

<div align="center">(a)   (b)</div>
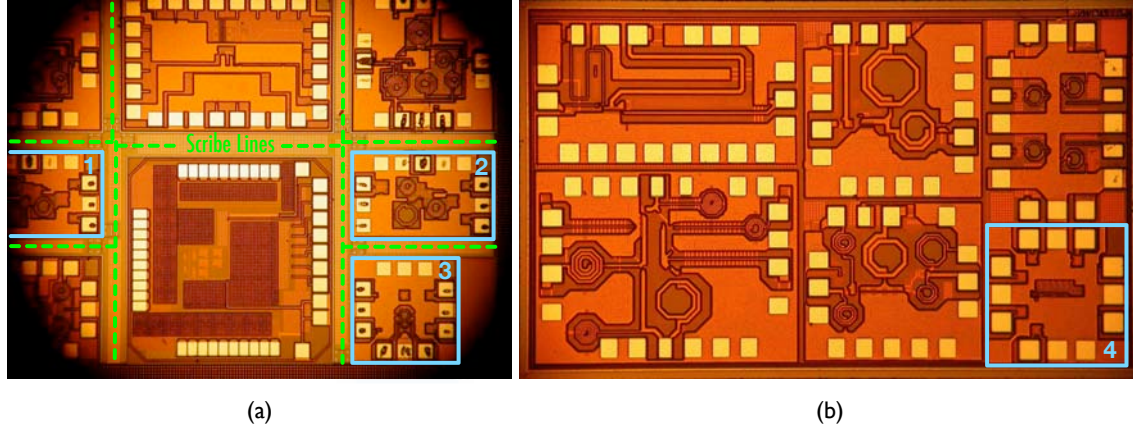
Figure 6.1. Fabricated IBM SiGe BiCMOS chip dies submitted by: (a) the Swiss Federal Institute of Technology Zürich and (b) the Technical University of Dresden. (1) 15GHz single-ended VCO, ET15G. (2) 15GHz single-ended VCO, ET15G_V2. (3) 24GHz differential VCO, XC24G. (4) 24GHz $1/6$ synchronous static frequency prescaler, SDIV6.

Refer to Appendix D for high resolution photographs of the individual fabricated MMICs. VCOs ET15G_V3 and BT15G were not submitted for fabrication due to their poor simulated performance and MPW area and cost limitations.

6.2   On-Wafer Measurement

The High Speed IC Laboratory facilities of the IfE ETHZ were utilised to perform on-wafer measurement of the fabricated MMICs. Figure 6.2 shows the probe station and peripheral equipment used to capture RF spectrum and DC data. The extremely high fidelity probes are manually aligned to make electrical contact with chip bond pads and viewed using the attached microscope. Wafer probes in GND–Signal–GND and Signal–GND–Signal configurations were used to connect to RF input and output pads, while DC–GND–DC probes were used to connect to bias supply pads. The exact configurations are further illustrated in the test apparatus diagrams of Section 6.3, 6.5 and 6.6.

Figure 6.2(a) depicts three sample MPW dies bonded to a copper plate for measurements in triplicate. This plate provides better suction to the vacuum table, making it easier to achieve good electrical contact between the probes and chip bond pads. Measuring multiple chip samples allows validation of performance data and investigation of manufacturing yield and the effects of wafer process variation. The heat sinking capability of the plate also helps
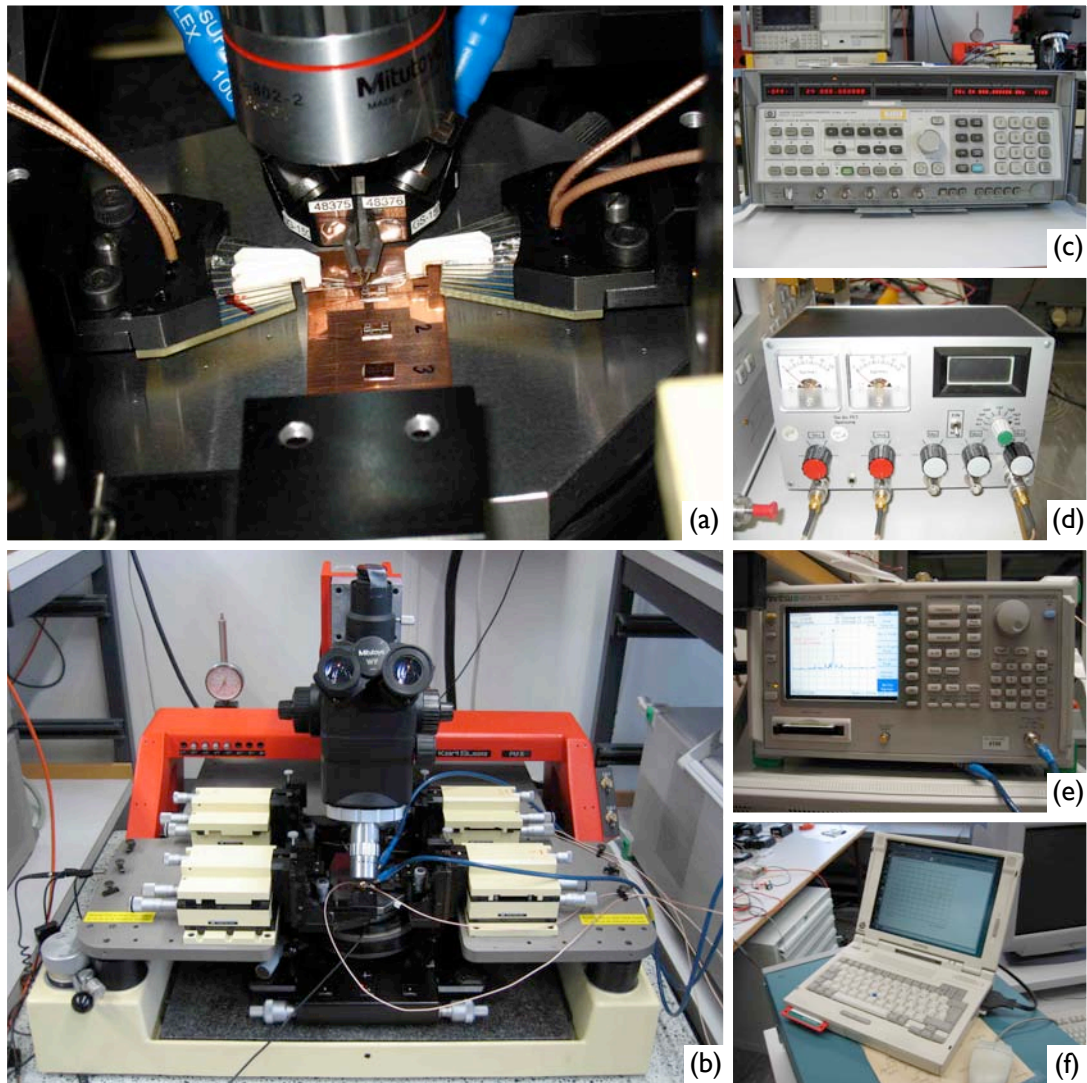
Figure 6.2. ETHZ IfE High Frequency IC Laboratory equipment used to carry out on-wafer chip measurement. (a) Close up of DC supply probes (left and right) and Picco RF probe (top) contacting a MPW chip sample. (b) Karl Suss PM8 wafer probe station. (c) HP 8340B frequency synthesiser. (d) Battery powered DC supply. (e) Anritsu MS266BC 40GHz spectrum analyser. (f) SoftPlot data acquisition and plotting software.

to mitigate temperature gradient increases as a result of high power consumption, therefore improving the consistency of measurement data over the test duration. This is particularly important for the VCO circuits where transistor junction temperature changes have a direct impact on the centre resonant frequency.

VCO measurements were carried out using the battery powered DC supply, shown in Figure 6.2(d). The power pack eliminates the introduction of mains power supply noise into the VCO via the power rails and subsequent substrate coupled noise. In effect, giving a more accurate measurement of the inherent VCO noise performance by minimising the effect of external noise sources.

Measurement of the 24GHz differential VCO required an additional Hewlett-Packard (HP) digital power supply to provide a fixed current to the differential pair and output buffers. The digitally controlled power supply was also used to provide all DC inputs to the 1/6 frequency prescaler, where power consumption is much higher and noise behaviour characterisation is of lower priority compared to the division ratio and input signal sensitivity.

The HP 8340B frequency synthesiser of Figure 6.2(c) provides the input clock signal to the frequency prescaler and is capable of generating signals from 10MHz to 26.5GHz with output power between -20dBm and 7.4dBm. These power levels correspond to signals with approximately 32mV to 741mV amplitude.

The laptop and SoftPlot data acquisition software shown in Figure 6.2(f) were used to capture frequency spectrum data directly from the the Anritsu MS266BC 40GHz spectrum analyser of Figure 6.2(e). The manually recorded measurement data presented in this thesis is attached in Appendix C, however captured frequency spectrum are not included due to their large file size.

6.2.1   Soft-start Power Application

To avoid damaging the MMICs during power-up, the DC biasing inputs were ramped from zero to their intended operating values whilst monitoring current flow. Monitoring or setting current limits ensures that current flow does not exceed safe levels to maintain electrical integrity. Possible fabrication errors which result in open or short circuits can be identified using this technique, without causing irreversible damage to the entire MPW die. Although the soft-start method does not assimilate real world power-up conditions including transients, latch-up effects and so on, it was used to minimise the risk of damaging the small number of chips available for testing.

6.2.2   De-imbedding Measurement Equipment

To determine actual circuit performance from the raw on-wafer measurement data, it is necessary to de-imbed the losses contributed by the measurement equipment. SMA cables, hybrid couplers, attenuators and wafer probes all have frequency dependent power transmission losses, typically specified in dB. In the single-ended measurement system, the process of de-imbedding simply involves adding/subtracting the amount of loss associated with each device in the output/input signal path, to the raw spectral data recorded in dBm. This is most efficiently performed using MATLAB and operating on the raw data as matrices.

Differential measurements are achieved using hybrid couplers, which add an additional level of complexity to the de-imbedding process. In this case, the cable losses in each differential path vary and must be treated separately until the hybrid coupler interface where the incident signal power is combined or divided. Figure 6.3 illustrates the differential measurement input and output signal paths while the following expressions show how the de-imbedding technique is implemented in MATLAB. Given the known input signal power, P_{in}, the power incident
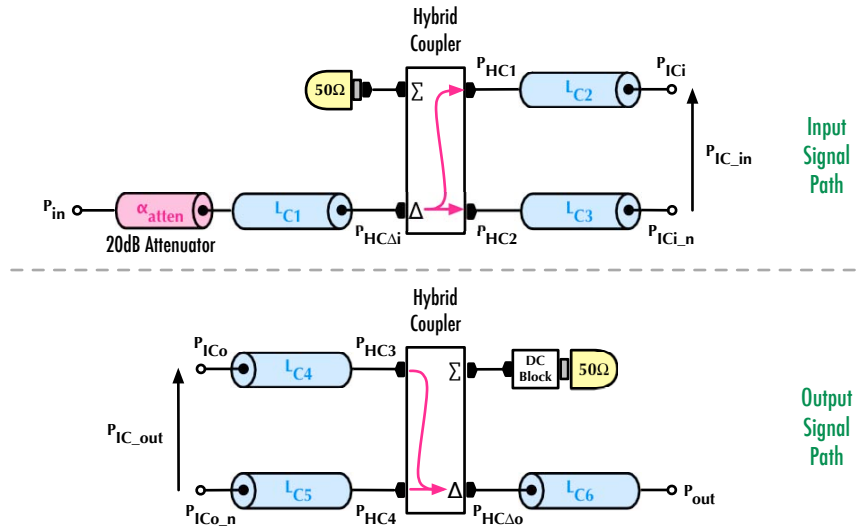
Figure 6.3. Differential wafer measurement input and output signal paths including attenuation (α_{atten}), cable losses (L_{C1}–L_{C6}) and power combing/dividing.

at the hybrid coupler input, $P_{HC\Delta i}$ can be expressed in dBm as,

$$P_{HC\Delta i} = P_{in} - \alpha_{atten} - L_{C1}. \tag{6.1}$$

The equally divided hybrid coupler output can be expressed as,

$$P_{HC1} = P_{HC2} = P_{HC\Delta i} - 10\log_{10}(1/2) \tag{6.2}$$

$$\approx P_{in} - \alpha_{atten} - L_{C1} - 3. \tag{6.3}$$

P_{HC1} and P_{HC2} represent the same amount of power and their respective voltage signals have equal amplitude, however they are $180°$ out of phase. This generates a differential signal composed of P_{ICi} and P_{ICi_n}. Accounting for a second level of cable losses gives the expressions for the signal power incident on each chip input pad,

$$P_{ICi} = P_{HC1} - L_{C2} \tag{6.4}$$

$$\approx P_{in} - \alpha_{atten} - L_{C1} - L_{C2} - 3 \tag{6.5}$$

$$P_{ICi\_n} = P_{HC2} - L_{C3} \tag{6.6}$$

$$\approx P_{in} - \alpha_{atten} - L_{C1} - L_{C3} - 3. \tag{6.7}$$

The signal powers in dBm can be expressed in terms of voltage amplitude as,

$$P_{ICi} \ (dBm) = 10 \cdot \log_{10} \left(\frac{\left(\frac{V_{ICi\_RMS}^2}{50} \right)}{1 \times 10^{-3}} \right) \tag{6.8}$$

$$= 10 \cdot \log_{10} \left(\frac{\left(\frac{V_{ICi\_amp}}{\sqrt{2}} \right)^2}{50 \times 10^{-3}} \right) \tag{6.9}$$

$$= 10 \cdot \log_{10} \left(\frac{V_{ICi\_amp}^2}{0.1} \right) \tag{6.10}$$

and similarly,

$$P_{ICi\_n} \ (dBm) = 10 \cdot \log_{10} \left(\frac{V_{ICi\_n\_amp}^2}{0.1} \right). \tag{6.11}$$

Therefore, voltage signal amplitude is defined by,

$$V_{ICi\_amp} \ (V) = \sqrt{\frac{10^{(P_{ICi}/10)}}{10}} \equiv \sqrt{\frac{P_{ICi} \ (mW)}{10}} \tag{6.12}$$

$$V_{ICi\_n\_amp} \ (V) = \sqrt{\frac{10^{(P_{ICi\_n}/10)}}{10}} \equiv \sqrt{\frac{P_{ICi\_n} \ (mW)}{10}}. \tag{6.13}$$

The differential signal amplitude can now be calculated by adding the voltage amplitudes since the signal paths are assumed to be exactly $180°$ out of phase,

$$V_{IC\_in\_amp} = V_{ICi\_amp} + V_{ICi\_n\_amp} \tag{6.14}$$

$$= \sqrt{\frac{10^{(P_{ICi}/10)}}{10}} + \sqrt{\frac{10^{(P_{ICi\_n}/10)}}{10}} \tag{6.15}$$

where P_{ICi} and P_{ICi_n} are in dBm. The differential input power is then given by,

$$P_{IC\_in} \ (dBm) = 10 \cdot \log_{10} \left(\frac{\left(\frac{V_{IC\_in\_amp}}{\sqrt{2}} \right)^2}{50 \times 10^{-3}} \right) \tag{6.16}$$

$$= 10 \cdot \log_{10} \left(\sqrt{10^{(P_{ICi}/10)}} + \sqrt{10^{(P_{ICi\_n}/10)}} \right)^2. \tag{6.17}$$

Working backwards from the recorded spectrum analyser data, P_{out}, determines the actual differential output power at the chip pads, P_{IC_out}. The signal power at the output of the hybrid coupler due to the summation of signal voltage amplitudes at its inputs can be expressed in dBm as,

$$P_{HC\Delta o} = P_{out} + L_{C6}. \tag{6.18}$$

Assuming hybrid coupler inputs are half the output power $P_{HC\Delta o}$ then,

$$P_{HC3} = P_{HC4} = P_{HC\Delta o} - 10\log 10(1/2) \tag{6.19}$$

$$\approx P_{out} + L_{C6} - 3. \tag{6.20}$$

Individual chip pad powers are then determined by adding the losses of the differential cables resulting in,

$$P_{ICo} = P_{HC3} + L_{C4} \tag{6.21}$$

$$\approx P_{out} + L_{C4} + L_{C6} - 3 \tag{6.22}$$

$$P_{ICo\_n} = P_{HC4} + L_{C5} \tag{6.23}$$

$$\approx P_{out} + L_{C5} + L_{C6} - 3. \tag{6.24}$$

The differential pad output signal is then calculated by adding the voltage amplitudes of the composite signals, which are assumed to be $180°$ out of phase and expressed as,

$$V_{ICo\ amp}\ (V) = \sqrt{\frac{10^{(P_{ICo}/10)}}{10}} \equiv \sqrt{\frac{P_{ICo}\ (mW)}{10}} \tag{6.25}$$

$$V_{ICo\_n\ amp}\ (V) = \sqrt{\frac{10^{(P_{ICo\_n}/10)}}{10}} \equiv \sqrt{\frac{P_{ICo\_n}\ (mW)}{10}}. \tag{6.26}$$

The summation takes the same form as Eq. (6.15), with the input power expressions replaced with the output power expressions,

$$V_{IC\_out\ amp} = V_{ICo\ amp} + V_{ICo\_n\ amp} \tag{6.27}$$

$$= \sqrt{\frac{10^{(P_{ICo}/10)}}{10}} + \sqrt{\frac{10^{(P_{ICo\_n}/10)}}{10}}. \tag{6.28}$$

Finally, the de-imbedded output power can be expressed in Watts as,

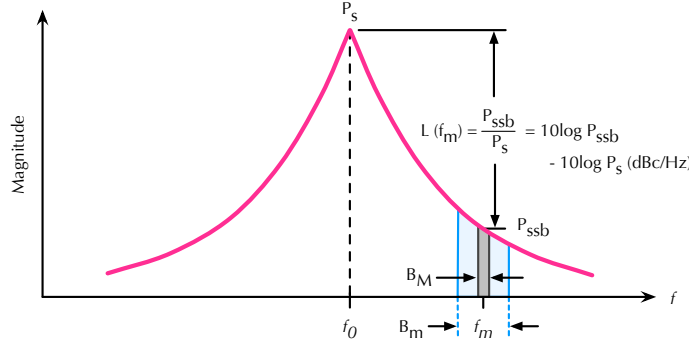$$P_{IC\_out}\ (W) = \frac{\left(\frac{V_{IC\_out\ amp}}{\sqrt{2}}\right)^2}{50} \tag{6.29}$$

or in dBm as,

$$P_{IC\_out}\ (dBm) = 10 \cdot \log_{10}\left(\frac{\left(\frac{V_{IC\_out\ amp}}{\sqrt{2}}\right)^2}{50 \times 10^{-3}}\right) \tag{6.30}$$

$$= 10 \cdot \log_{10}\left(\sqrt{10^{(P_{ICo}/10)}} + \sqrt{10^{(P_{ICo\_n}/10)}}\right)^2. \tag{6.31}$$

6.2.3 Phase Noise Measurement

Phase noise data quoted in this thesis is measured using the direct measurement technique described in [43] and illustrated in Figure 6.4. The technique involves measuring the sin-

Figure 6.4. Direct phase noise measurement technique using the centre frequency spectral power, P_s and the single side band noise power, P_{ssb} measured at $f_m - f_0 = 1\text{MHz}$ offset and normalised to a 1Hz bandwidth. B_m = the measured bandwidth and B_M = the equivalent 1Hz bandwidth.

gle side band noise power, P_{ssb} in a 1Hz bandwidth, relative to the spectral power at the fundamental frequency, P_s. This is in accordance with Eq. (2.9) and can be expressed as,

$$\mathcal{L}(f_m) = \frac{P_{ssb}}{P_s} \tag{6.32}$$

where power values are in Watts, or expressed in dBc/Hz as,

$$\mathcal{L}(f_m) = 10 \log P_{ssb} - 10 \log P_s. \tag{6.33}$$

Furthermore, since power levels on the spectrum analyser are displayed in dBm, calculating the phase noise is as simple as,

$$\mathcal{L}(f_m) = P_{ssb} \ (dBm) - P_s \ (dBm) \tag{6.34}$$

assuming a measurement bandwidth of 1Hz. However, accurate capture of high frequency spectrum on screen requires much higher measurement bandwidths or spectrum analyser resolution bandwidths (RBWs). The measured noise power, P_m at the offset must then be normalised to the 1Hz noise bandwidth using the normalisation scale factor,

$$SF_{BW} = 10 \log \frac{B_m}{B_M} \tag{6.35}$$

where B_m is the measurement bandwidth and B_M is the equivalent 1Hz noise bandwidth. The normalised single side band noise power in dBm then becomes,

$$P_{ssb} = P_m - SF_{BW}. \tag{6.36}$$

Therefore the final expression for directly measured phase noise in dBc/Hz is,

$$\mathcal{L}(f_m) = P_m - SF_{BW} - P_s. \tag{6.37}$$

6.3   15GHz Single-ended VCO [ET15G] Measurement

On-wafer measurement of the 15GHz single-ended VCOs was performed using instrumentation configured in accordance with Figure 6.5. All measurements were systematically performed on three ET15G chips from three separate MPW dies. The key features of the test
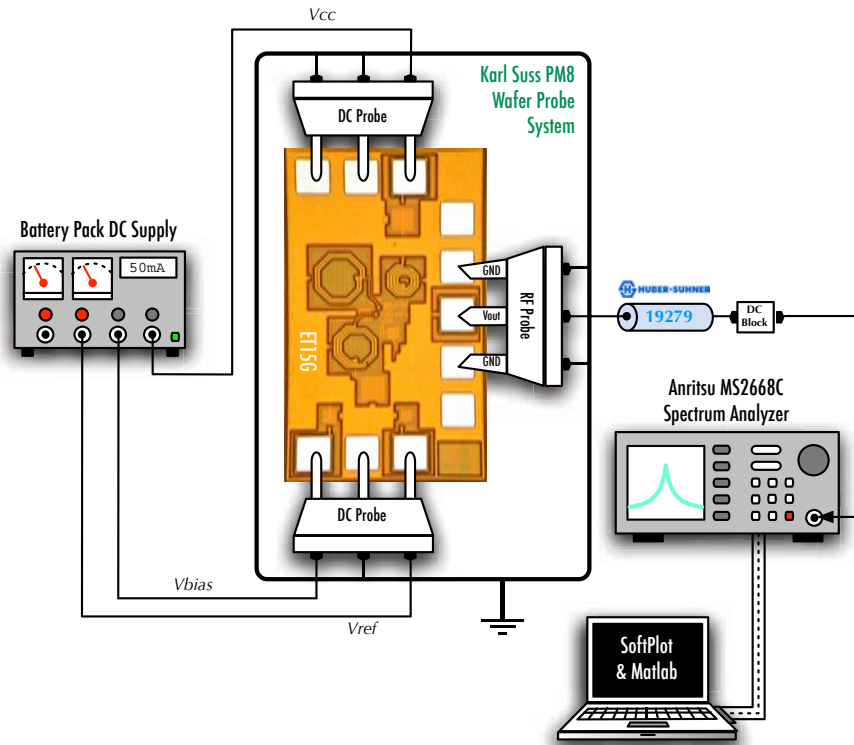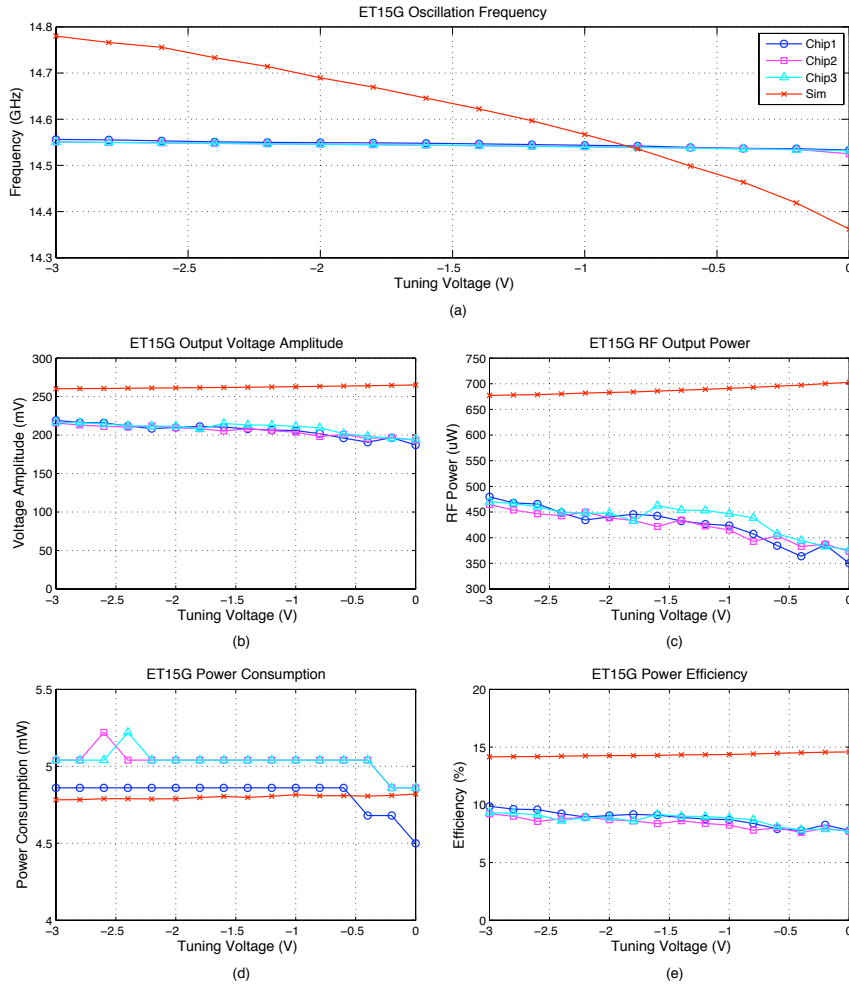

Figure 6.5. Test instrumentation setup used to perform on-wafer characterisation of the two 15GHz single-ended VCOs, ET15G and ET15G_V2. The apparatus enables measurement of frequency, spectral power and DC power consumption data.

apparatus are the battery powered DC supply unit which eliminates mains power supply noise, minimum length coaxial cable for output signal connectivity to reduce signal loss, and data acquisition capability to accurately capture VCO spectral data. The IC is orientated 90° clockwise to align with the probe stations RF output probe fixture. Mounting the RF probes on the left and right hand sides of the apparatus aided connectivity with input and measurement equipment and minimisation of cable losses due to decreased cable length.

Basic VCO operation was confirmed with the application of DC supply voltages resulting in an oscillatory output signal observed on the spectrum analyser. VCO tuning behaviour was investigated by stepping the tuning voltage, V_{tune} from -3V to 0V in $+0.2$V increments and recording: output frequency, peak output spectral power and DC power supply current. The raw measurement data was de-imbedded and manipulated to determine the VCO frequency tunability, output voltage amplitude, RF output power, DC power consumption and power conversion efficiency characteristics displayed in Figure 6.6.

Figure 6.6. ET15G output characteristics measured over the tuning range $V_{tune} = -3 \quad 0V$ in $+0.2V$ increments: (a) oscillation frequency, (b) voltage amplitude, (c) RF output power, (d) DC power consumption and (e) power conversion efficiency.

Although simulated and measured centre frequencies are approximately the same, the average measured tuning range of the three ET15G VCOs is 23.6MHz, compared to 417.8MHz predicted by post-layout circuit simulations. This is a reduction of approximately 94% in the

fabricated circuit. All three chip samples exhibit this severe degradation of tuning capability, suggesting that a common layout issue may be the cause. However, the exact origin of this problem remains unresolved. The ET15G frequency tuning characteristic exhibits good continuity, however the limited range will likely significantly impact the phase range of the resultant phase shifting network.

The output amplitude decreases as the tuning voltage approaches zero, however it exhibits relatively linear behaviour with a mean value of 206.78mV. Although less than post-layout simulation results, the output swing is deemed more than sufficient for the application, since amplifiers are used at the output.

The RF output power generated by the VCO naturally has the same characteristic shape as the output voltage amplitude and ranges from 350–480μW. DC power consumption remains relatively constant over tuning voltage variation but falls for $V_{tune} \geq -0.6$V. The maximum recorded DC power consumption is 5.22mW. The accuracy of current consumption measurements is limited by the single decimal point ammeter accuracy on the DC supply unit. As a result, the measured characteristic has low granularity in comparison to simulated power consumption results, however they are in reasonable agreement. Using the measured DC power consumption and RF output power, the VCO power conversion efficiency can be calculated. The fabricated VCO exhibits an efficiency figure between $7.68 - 9.87\%$ over the tuning range.

ET15G frequency spectrum were captured at the tuning voltage limits, $V_{tune} = 0$V and -3V for the three MPW dies and displayed in Figure 6.7. All of the spectral plots exhibit the three distinct slope regions (modulated $1/f$ noise, resonator noise and noise floor) in the frequency side skirts as theorised in Leeson's oscillator phase noise model illustrated in Figure 2.10. Close-in frequency spurs appear symmetrically around the fundamental in the spectrum of chip 2 and 3 at $V_{tune} = -3$V. They represent discrete short-term causal effects such as harmonics, while the sidebands are the result of continuous nondeterministic random device noise and interference [43]. Table 6.1 shows the phase noise directly measured from each frequency spectrum at 1MHz offset from the fundamental. The measured data shows very good agreement with simulated post-layout extracted results.

The E-tuned VCO topology allows tuning by varying the transistor bias current as well as via the varactor voltage. This effectively changes the base-emitter junction capacitance and hence the frequency of the resonant loop. The highest measured ET15G frequency under default DC biasing was achieved by chip 1 at 14.556GHz, with $V_{tune} = -3V$. An alternative bias setup was investigated such that the VCO would generate an output at 15GHz. Figure 6.8 shows the 15GHz spectrum produced at the operating point: $V_{cc} = 2.13$V, $V_{bias} = 0.93$V and $V_{tune} = 0$V. Simulation and measurement therefore indicate that ET15G
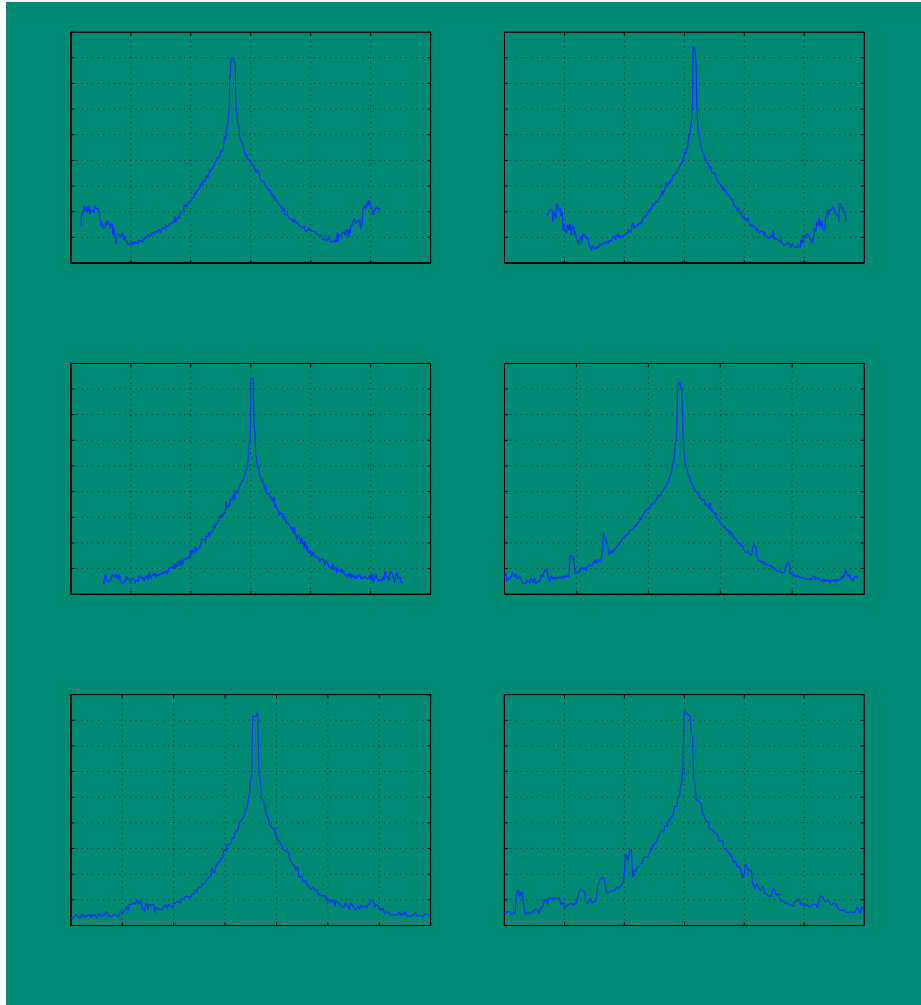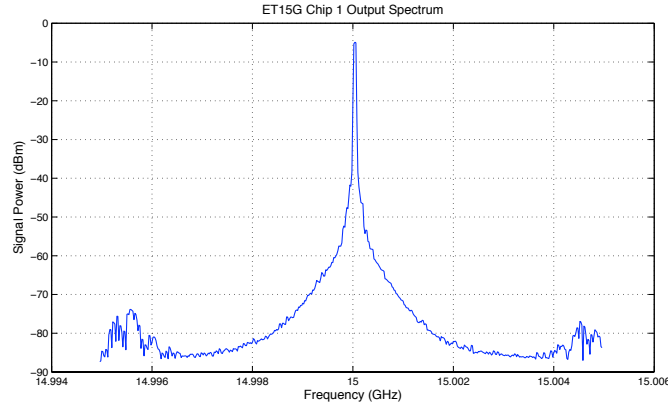
Figure 6.7. ET15G measured output frequency spectrum at $V_{tune} = 0V$ and $-3V$ for: (a) & (b) chip 1, (c) & (d) chip 2, and (e) & (f) chip 3.

Table 6.1. ET15G direct phase noise measurements at 1MHz offset from the fundamental, for chips 1–3 and chip 1* under modified bias conditions to operate at 15GHz. Simulated post-layout extracted phase noise figures are included for comparison.

$MMIC$	V_{tune} (V)	$\mathcal{L}(\Delta\omega = 1MHz)$ (dBc/Hz)				
		$Chip\ 1$	$Chip\ 2$	$Chip\ 3$	$Chip\ 1^*$	$Simulated$
ET15G	-3	-92.02	-89.62	-90.39	–	-90.92
	0	-87.22	-90.75	-88.48	-87.08	-90.23

is functionally suitable for implementation into the phase shifter network, however the tuning range is very limited. Refer to Table 6.3 for a comparison of ET15G performance against post-layout simulation, ET15G_V2 performance and state-of-the-art VCOs fabricated in similar technologies.



Figure 6.8. ET15G frequency spectrum under modified bias conditions such that the output is at 15GHz: $V_{cc} = 2.13V$, $V_{bias} = 0.93V$ and $V_{tune} = 0V$.

6.4   15GHz Single-ended VCO [ET15G_V2] Measurement

The test equipment configuration shown in Figure 6.5 was also used to measure the performance of the ET15G_V2 15GHz single-ended VCO. All measurements were systematically performed on three ET15G_V2 chips on three separate MPW dies.

Basic VCO operation was confirmed with the application of DC supply voltages resulting in an oscillatory output signal observed on the spectrum analyser. VCO tuning behaviour was investigated by stepping the tuning voltage, V_{tune} from $-3V$ to $0V$ in $+0.2V$ increments and recording: output frequency, peak output spectral power and DC power supply current. The raw measurement data was de-imbedded and manipulated to determine the VCO frequency tunability, output voltage amplitude, RF output power, DC power consumption and power conversion efficiency characteristics displayed in Figure 6.9.

The average measured tuning range is 230.7MHz, compared to 486.5MHz predicted by post-layout circuit simulation. Therefore, less than 50% simulated tuning range is actually achieved in the fabricated circuit, while the tuning characteristic is also shifted down by as much as 2GHz. ET15G_V2 tuning range is approximately a factor of ten greater than the recorded tuning range of ET15G despite similar simulated tuning ranges. Unlike ET15G, the tuning characteristic of ET15G_V2 does not exhibit a smooth transition from maximum to minimum
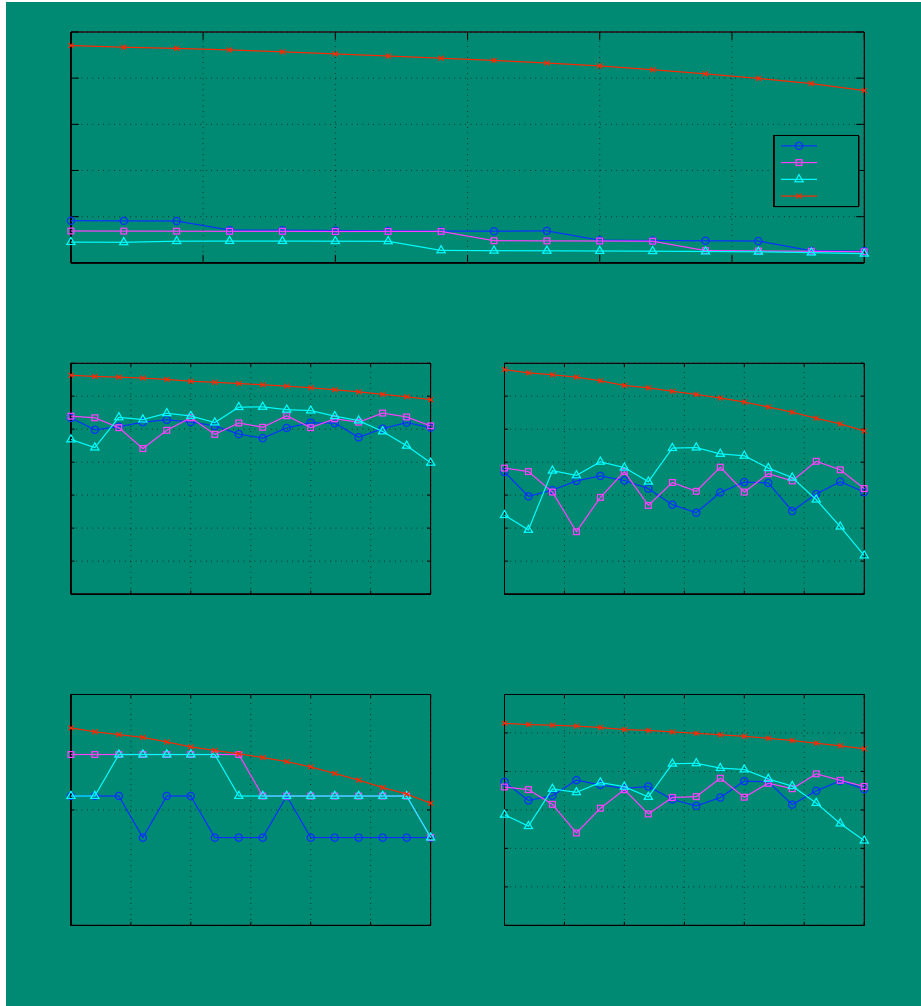
Figure 6.9. ET15G_V2 output characteristics measured over the tuning range $V_{tune} = -3 \quad 0V$ in $+0.2V$ increments: (a) oscillation frequency, (b) voltage amplitude, (c) RF power, (d) power consumption and (e) power conversion efficiency.

frequency. Instead, there are multiple step transitions in the oscillation frequency which complicate the accurate tuning of the VCO around these points. Essentially the sensitivity to V_{tune} in these regions is greatly increased.

The measured oscillation amplitude has an average value of 102.6mV and fluctuates minimally over the tuning voltage range. As such, the RF output power also remains relatively flat with a calculated average of 105.7μW. The output voltage and power are both less than post-layout simulations predict. In comparison to ET15G, this VCO has approximately half the signal amplitude and therefore a quarter of the RF power output.

DC current measurements identify a maximum power consumption of 3.24mW, recorded by chips 2 and 3. This is approximately 2mW less than that consumed by ET15G and approximately equal to the mean of the post-layout simulated characteristic. ET15G_V2 exhibits a power conversion efficiency between 2.2–4.2%, down from approximately 5% predicted by post-layout simulations. This is also about half the efficiency of ET15G, suggesting that the circuit parameter modifications to ET15G_V2 and their associated resistive losses have impacted transistor current gain and hence the ability to convert DC power into oscillatory output energy.

ET15G_V2 frequency spectrum were captured at the tuning voltage limits, $V_{tune} = 0V$ and $-3V$ for each of the three MPW dies and displayed in Figure 6.10. All of the spectral plots
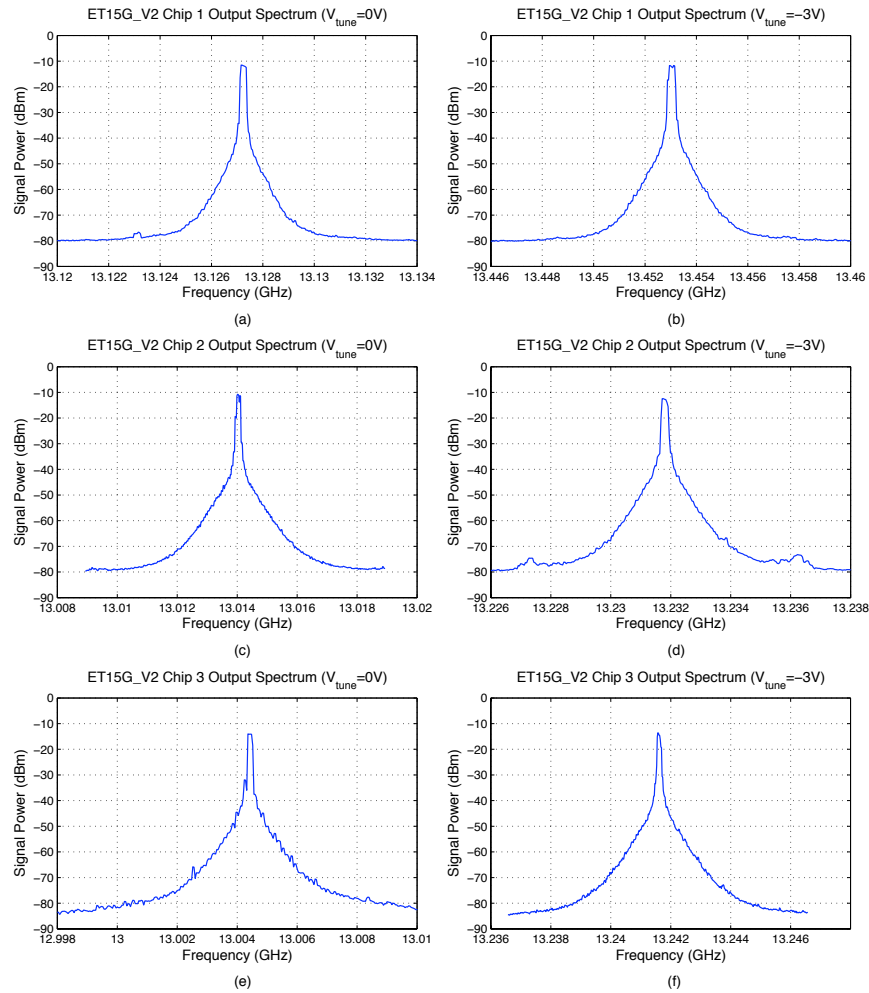
Figure 6.10. ET15G_V2 measured output frequency spectrum at $V_{tune} = 0V$ and $-3V$ for: (a) & (b) chip 1, (c) & (d) chip 2, and (e) & (f) chip 3.

exhibit the three distinct slope regions (modulated $1/f$ noise, resonator noise and noise floor)

in the frequency side skirts as theorised in Leeson's oscillator phase noise model illustrated in Figure 2.10. The close-in frequency spurs that appeared in ET15G spectrum are no longer present, suggesting the harmonic clarity of the VCO has been improved. Table 6.2 shows the phase noise directly measured from each frequency spectrum at 1MHz offset from the fundamental. The measured data shows consistently worse phase noise performance for $V_{tune} = -3$V and up to 16.54dBc/Hz more noise than post-layout extracted results.

Table 6.2. ET15G_V2 direct phase noise measurements at 1MHz offset from the fundamental, for chips 1–3 and chip 1* under modified bias conditions to operate at 15GHz. Simulated post-layout extracted phase noise figures are included for comparison.

$MMIC$	V_{tune} (V)	$\mathcal{L}(\Delta\omega = 1MHz)$ (dBc/Hz)				
		$Chip\ 1$	$Chip\ 2$	$Chip\ 3$	$Chip\ 1^*$	$Simulated$
ET15G_V2	-3	-71.24	-78.73	-74.88	-86.19	-87.78
	0	-75.04	-83.44	-88.96	–	-84.42

The highest measured ET15G_V2 frequency under default DC biasing was achieved by chip 1 at 13.456GHz, with $V_{tune} = -3$V. An alternative bias setup was investigated such that the VCO would generate an output at 15GHz. Figure 6.11 shows the highest obtainable ET15G_V2 frequency at 14.095GHz, produced at the operating point: $V_{cc} = 2.31$V, $V_{bias} = 0.95$V and $V_{tune} = -3$V. Measurement data therefore indicates that ET15G_V2 may not be functionally suitable for integration into the phased shifter network due to inaccurate frequency synthesis.
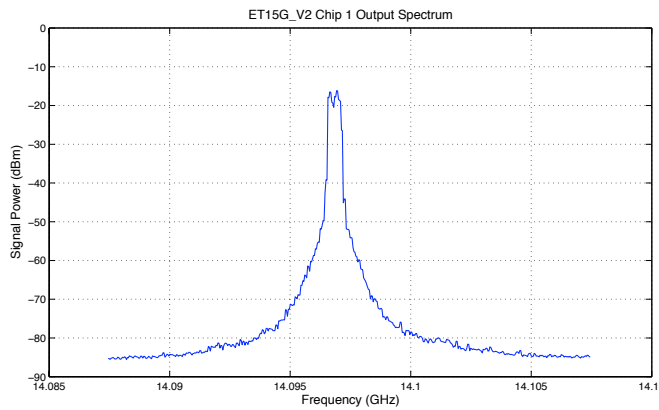
Figure 6.11. ET15G_V2 frequency spectrum under modified bias conditions: $V_{cc} = 2.31V$, $V_{bias} = 0.95V$ and $V_{tune} = -3V$.

Table 6.3 summarises the measured performance metrics of both 15GHz single-ended VCOs fabricated in IBM SiGe 0.18μm BiCMOS technology as part of this thesis. Average values are calculated over the tuning range for each metric. The mean is then determined to provide a more accurate representation of VCO performance over multiple MPW dies rather than the measured performance of a single chip. The results are also compared against post-layout analog extracted simulation data and reported state-of-the-art VCO designs in similar technologies.

Table 6.3. Summary of ET15G and ET15G_V2 measured performance, post-layout simulation and comparison to current state-of-the-art VCOs. Phase noise is quoted at 1MHz ([†]100kHz) offset from the fundamental.

Ref.	Technology, f_t Topology, Size (μm^2)	f_{osc} (GHz)	f_Δ (MHz)	P_{out} (dBm)	P_{DC} (mW)	$\mathcal{L}(\Delta\omega)$ (dBc/Hz)
ET15G	0.18μm SiGe BiCMOS, 60GHz					
	Single-ended E-tuned, 1038×630	14.541	22.6	-3.70	4.958	-89.75
	Analog Extracted Simulation	14.571	417.8	-1.63	4.800	-90.58
ET15G_V2	0.18μm SiGe BiCMOS, 60GHz					
	Single-ended E-tuned, 1038×630	13.230	230.7	-9.80	3.064	-78.72
	Analog Extracted Simulation	15.110	486.5	-7.96	3.219	-86.10
[4]	0.25μm SiGe BiCMOS, 47GHz Single-ended E-tuned	15.15	1100	–	–	-75[†]
[44]	0.18μm SiGe BiCMOS, 200GHz Differential LC, 1000×1200	16.45	3150	2.5	3.338	-100
[45]	InGaP/GaAs HBT, 30GHz Differential LC, 1000×800	14.80	1600	-0.83	–	-115
[37]	AlGaAs/GaAs HBT, 85GHz Single-ended B-tuned, 1800×1200	15.6	600	-4	75	-110
[46]	0.09μm RF CMOS, 200GHz Differential LC, 340×700	15.27	496	-10	5.76	-105
[6]	0.25μm SiGe BiCMOS, 47GHz Single-ended B-tuned	4.8	400	-3.5	2.16	-110

6.5   24GHz Differential VCO [XC24G] Measurement

Figure 6.12 shows the configuration of test instrumentation used to obtain single-ended measurement data for the 24GHz differential cross-coupled VCO, XC24G. All measurements were systematically performed on three XC24G chips on three separate MPW dies. The apparatus uses a differential Signal–GND–Signal RF probe to connect to the output pads v_{out} and
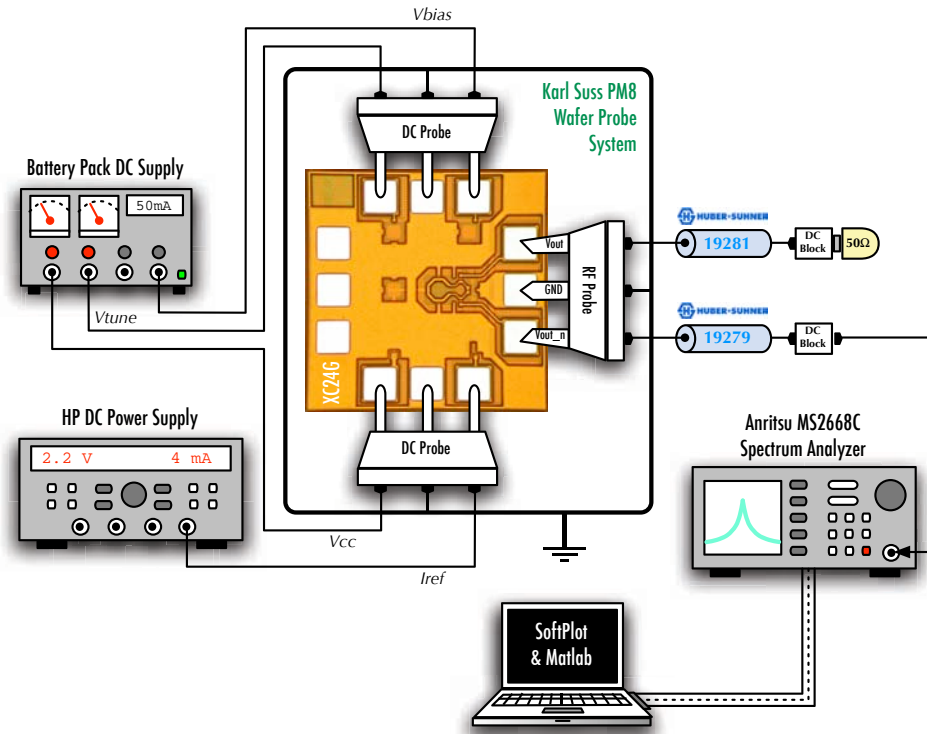
Figure 6.12. Test instrumentation setup used to perform on-wafer characterisation of the 24GHz differential VCO, XC24G. The apparatus enables measurement of frequency, spectral power and DC power consumption data.

v_{out_n}. v_{out_n} connects to the spectral analyser via a minimum length SMA cable and DC blocker. To present a balanced load to the VCO, an SMA cable of the same length (and hence similar frequency dependent losses), a DC blocker and 50Ω termination are attached to the complementary differential signal, v_{out}. Since the spectrum analyser has a standard 50Ω input impedance, the VCO sees an output impedance equivalent to that used during pre and post-layout test bench simulation. Without such a setup, the operational symmetry of the cross-coupled VCO core may be interrupted, causing unbalanced frequency pulling and producing unwanted phase error and harmonics in the output. However, the EF output buffers incorporated into the design should greatly reduce the influence of external loading on VCO performance.

Basic VCO operation was confirmed with the application of DC supply voltages, resulting in an oscillatory output signal observed on the spectrum analyser. VCO tuning behaviour was investigated by stepping the tuning voltage, V_{tune} from 1.8V to 4.8V in +0.2V increments and recording: output frequency, peak output spectral power and DC power supply current. The raw measurement data was de-imbedded and manipulated to determine the VCO frequency

tunability, output voltage amplitude, RF output power, DC power consumption and power efficiency characteristics displayed in Figure 6.13.
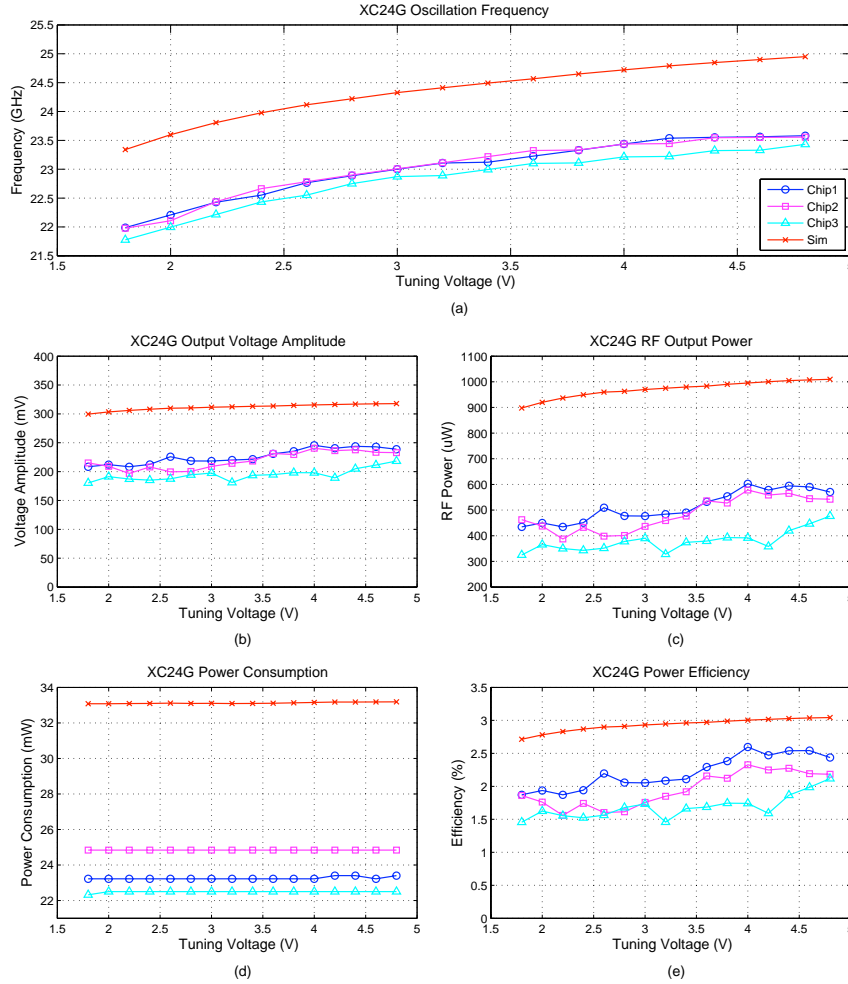
Figure 6.13. XC24G output characteristics measured over the tuning range $V_{tune} = 1.8$ $4.8V$ in $+0.2V$ increments: (a) oscillation frequency, (b) voltage amplitude, (c) RF power, (d) power consumption and (e) power conversion efficiency.

The tuning range characteristic shows an almost linear transition between the minimum and maximum resonant frequencies with an average range of 1.61GHz over the three measured chips. This is the same range as predicted by post-layout simulations however the centre frequency has shifted downward from 24.145GHz to 22.719GHz. Chip 1 and 2 tuning characteristics are practically identical, while chip 3 shows a further downward frequency shift of approximately 200MHz. The chosen differential topology and device selection obviously provides far greater frequency tunability in comparison to any of the single-ended VCO topologies investigated in this thesis, despite operating at the higher frequency of 24GHz.

The measured performance also correlates much better with post-layout simulated performance. It can be seen that the effectiveness of the varactors in the differential configuration is significantly improved and the layout parasitics do not cause degradation of performance to the same extent.

The output signal amplitude varies between 180–246mV over the three measured chips, which is down from post-layout simulations of greater than 300mV. However, this is still well above the specified frequency prescaler input voltage level of 100mV with additional margin for interconnection losses between the two circuits, assuming they are on the same die or connected via bond wires. In fact, Section 6.6 reveals that at 24GHz the fabricated prescaler will accurately divide an input signal amplitude of less than 10mV.

VCO RF output power was measured from 325–603μW over the tuning range with a gradual increase as V_{tune} approaches 4.8V. All VCO samples display a similar trend, albeit at approximately half the output power predicted by post-layout simulation. DC power consumption is basically flat over the tuning range with an average of 23.53mW, approximately 10mW lower than the simulated average consumption. The positive slope of the RF power characteristic without significant increase in DC power consumption suggests that varactor capacitance variation at the HBT collector nodes is effecting transistor gain and hence the output swing into the EF buffers. The DC power consumption is large in comparison to the single-ended VCO topologies but justifiable when considering the number of active transistors in the VCO core, active current mirror structure and output buffer amplifiers. Oscillator power efficiency is low due to the high DC power consumption and ranges between 1.46% and 2.6%.

XC24G frequency spectrum were captured at the tuning voltage limits, $V_{tune} = 1.8$V and 4.8V for each of the three MPW dies and displayed in Figure 6.14. Output frequency drift made it difficult to capture high resolution VCO spectral content. The presence of spurious output frequencies is evident in all spectral diagrams, but perhaps more prominent in the sidebands of chip 2 and 3. Leeson's oscillator phase noise model illustrated in Figures 2.10 is harder to recognise in these plots, however Figure 6.14(a) does demonstrate this type of phase noise behaviour. Table 6.4 shows the phase noise directly measured from each frequency spectrum at 1MHz offset from the fundamental. The measured data shows up to 12.14dBc/Hz worse phase noise performance than post-layout extracted results, however the accuracy of the measured results is limited as they do not take into account the reduction of common mode noise in the real differential output.

The highest measured XC24G frequency under default DC biasing was achieved by sample chip 1 at 23.581GHz, with $V_{tune} = 4.8$V. An alternative bias setup was investigated such that the VCO would generate an output at 24GHz. Figure 6.15 shows the frequency spectrum
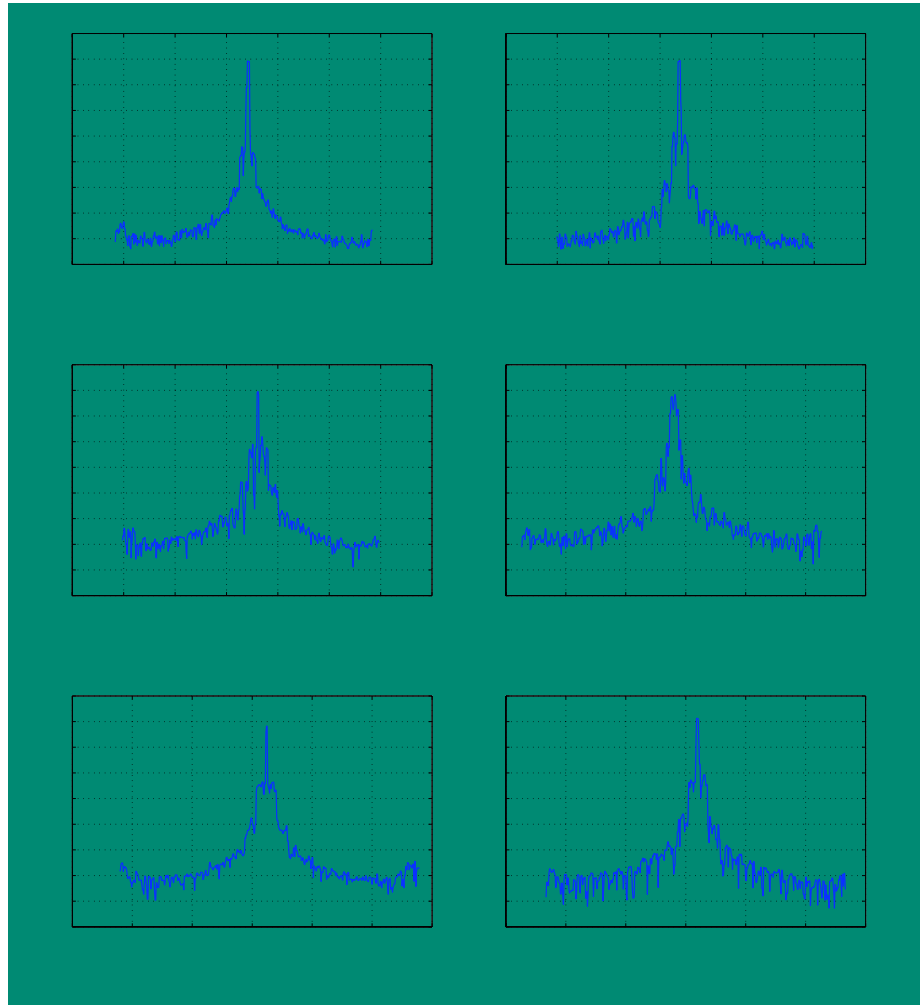
Figure 6.14. XC24G measured output frequency spectrum at $V_{tune} = 1.8V$ and $4.8V$ for: (a) & (b) chip 1, (c) & (d) chip 2, and (e) & (f) chip 3.

Table 6.4. XC24G direct phase noise measurements at 1MHz offset from the fundamental, for chips 1–3. Simulated post-layout extracted phase noise figures are included for comparison.

MMIC	V_{tune} (V)	$\mathcal{L}(\Delta\omega = 1MHz)$ (dBc/Hz)			
		Chip 1	Chip 2	Chip 3	Simulated
XC24G	1.8	-82.95	-88.61	-89.28	-95.09
	4.8	-82.47	-82.09	-90.01	-93.59

produced at the modified bias point; V_{cc} = 2.2V, V_{bias} = 1V, I_{ref} = 4mA and V_{tune} = 5.46V. The fundamental frequency is located at 23.99GHz, however since the tuning voltage
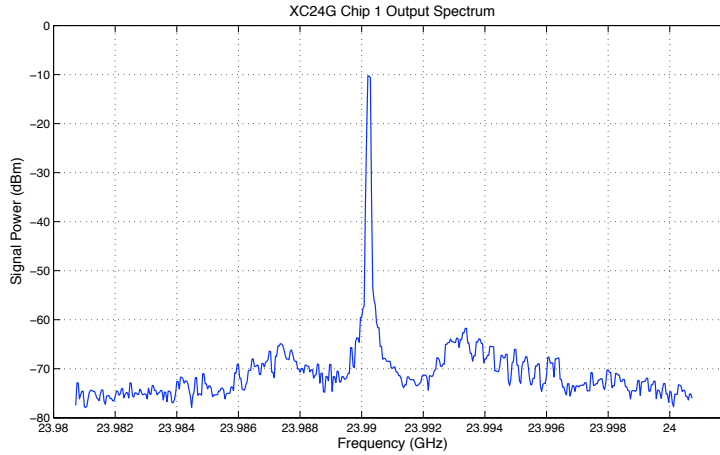
Figure 6.15. XC24G frequency spectrum under modified bias conditions: V_{cc} = 2.2V, V_{bias} = 1V, I_{ref} = 4mA and V_{tune} = 5.46V.

is already beyond the recommended varactor potential, it is not possible to find an operating point where the tunable range is centred around 24GHz. This means that a practical PLL for 24GHz automotive SRR utilising this VCO could only operate up to 24GHz before potentially losing frequency lock, provided that the tuning voltage is allowed to exceed the varactor potential specification.

Table 6.5 summarises the measured performance metrics of the 24GHz differential cross-coupled VCO fabricated in IBM 0.18μm SiGe BiCMOS technology. Mean values are calculated over the tuning range for each metric and then averaged over the multiple MPW dies. The results are compared against post-layout analog extracted simulation data and reported state-of-the-art VCO designs in similar technologies.

6.6   1/6 Frequency Prescaler [SDIV6] Measurement

On-wafer measurement of the frequency prescaler was carried out using both single-ended and differential techniques. The test instrumentation setup for single-ended prescaler measurement is illustrated in Figure 6.16. The input clock signal is provided by the HP 8340B frequency synthesiser, capable of generating signals from 10MHz to 26.5GHz with output power between -20dBm and 7.4dBm. These power levels correspond to signals with amplitude approximately 31.6mV to 741.3mV. Given that post-layout simulations of prescaler

Table 6.5. Summary of XC24G measured performance, post-layout simulation and comparison to current state-of-the-art VCOs. Phase noise is quoted at 1MHz ([†]100kHz) offset from the fundamental ([‡]PLL phase noise).

Ref.	Technology, f_t Topology, Size (μm^2)	f_{osc} (GHz)	f_Δ (GHz)	P_{out} (dBm)	P_{DC} (mW)	$\mathcal{L}(\Delta\omega)$ (dBc/Hz)
XC24G	0.18μm SiGe BiCMOS, 60GHz Differential LC, 776×776 Analog Extracted Simulation	22.719 24.145	1.61 1.611	-3.45 -0.13	23.53 33.12	-85.90 -94.34
[47]	0.18μm CMOS, 45GHz 12GHz VCO + f-doubler, 680×850 Complementary LC, 640×850	25.1 21.6	3 1.5	-18.8 -4.2	11 45	-99.9 -101.7
[48]	0.15μm GaAs mHEMT, 120GHz 12GHz Push-Push, 1800×2000	23.55	1.4	9	220	-92
[49]	0.25μm SiGe BiCMOS, 92GHz Differential LC, 550×650	24.85	2.3	-9	6.6	-100
[50]	Infineon SiGe B7HF, 75GHz Differential LC, 890×890	24.4	1.0	-10	21.6	-89
[51]	0.8μm ATMEL SiGe1, 50GHz 8GHz VCO + f-tripler, 300×600	23.5	0.42	-10	180	-80[†]
[52]	0.13μm SiGe BiCMOS, 166GHz Differential LC	22.75	4.7	-0.8	14.5	-104.3[‡]

input sensitivity reveal a minimum of -44.61dBm, it is necessary to incorporate a 20dB attenuator at the signal generator output to produce the lower power levels required to investigate the measured input sensitivity performance. The clock signal is then connected via a minimum length SMA cable and differential Signal–GND–Signal RF probe to the v_{clk} input. The complementary differential input, v_{clk_n}, is also connected to a SMA cable of the same length, however it is terminated by a 50Ω load. This ensures that the prescaler is presented with a balanced input impedance. The digital HP power supply unit connects to the bias pads via DC wafer probes to provide the bias signals: $V_{cc} = 4.2$V, $V_{ref\_clk} = 2$V and $V_{ref} = 2.4$V. A current limit of $I_{ref} = 4$mA is set for the V_{ref} supply to avoid current mirror output fluctuations due to voltage supply noise and chip temperature effects. Such fluctuations would directly effect the bias current supply to each ECL D-latch and EF level shifter within the synchronous static prescaler core, as well as the double EF output buffer. The output is connected to the spectrum analyser and data acquisition system in a similar manner to the input. However in this case, v_{out} is terminated by a 50Ω load and the complementary differential output v_{out_n} is the measured signal.
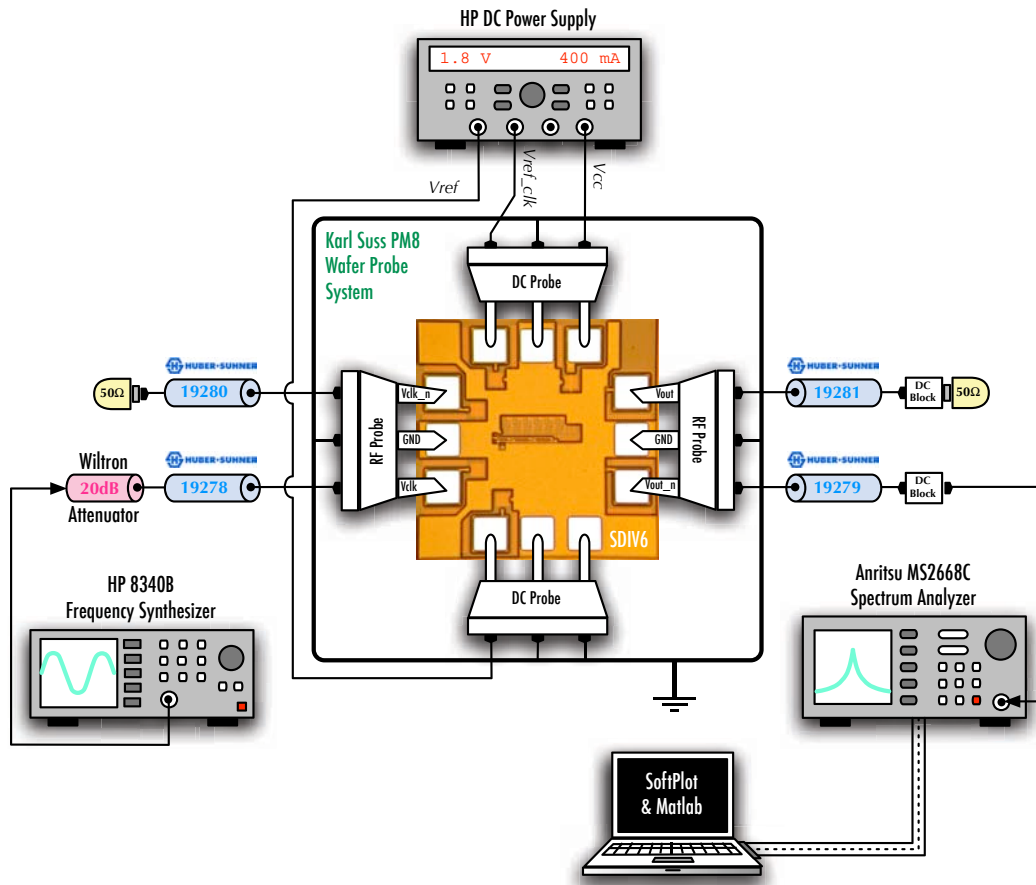
Figure 6.16. Test apparatus used to perform single-ended on-wafer characterisation of the 1/6 synchronous static frequency prescaler, SDIV6. The test setup enables measurement of frequency, spectral power and DC power consumption data.

While the single-ended measurement technique is a commonly used method of evaluating the performance of fabricated frequency dividers of a differential signal nature [26, 25, 22], differential prescaler measurement was also undertaken. Due to time limitations, differential measurement was only performed on a single MPW sample, chip 1. The aim is to verify the accuracy of single-ended measurement data and identify any significant performance differences when the prescaler is excited by a true differential input. It is envisaged, that a true differential signal may improve the switching transition speed of the ECL D-latches by driving both sides of the clock current steering differential pair harder. This mechanism controls the track and hold differential stage transitions. The differential output spectrum is also expected to display better noise floor due to the elimination of common mode components, generated both on-wafer and by external test rig sources. The test setup for differential frequency prescaler measurement is illustrated in Figure 6.17. The frequency synthesiser and
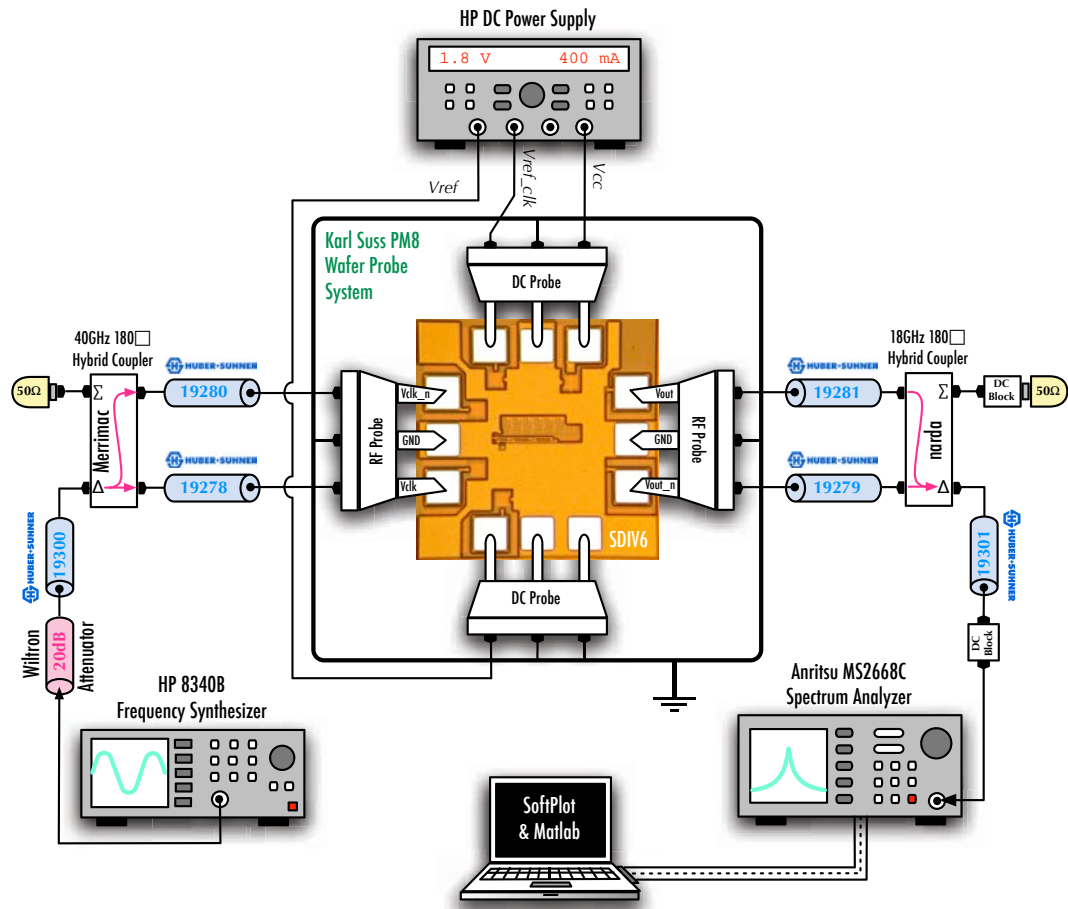
Figure 6.17. Test apparatus used to perform differential on-wafer characterisation of the 1/6 synchronous static frequency prescaler, SDIV6. The test setup enables measurement of frequency, spectral power and DC power consumption data.

spectrum analyser are both single signal output and input devices respectively. As such, it is necessary to split the input into a differential signal and combine the differential output for measurement. This is achieved using 180° hybrid couplers. A hybrid coupler can be configured to output either the sum or the difference of its input signals. In the presented configuration, the input hybrid coupler splits the signal from the frequency synthesiser into two equal signals each of half the input power in Watts, or approximately 3dB less than the input power in dB, and 180° out of phase. Conversely, the output hybrid coupler produces the difference of the two output signals which are in opposite phase orientation, therefore essentially adding their respective signal powers. The addition of hybrid couplers in the test apparatus complicates the data analysis required in the de-imbedding process as documented in Section 6.2.2. Compounding this is the additional stage of cabling required, causing further

signal attenuation. Additionally, signals in each differential path suffer different attenuation due to the variation of frequency dependent cable losses. This effect becomes more prominent at high frequency and potentially unbalances the symmetry of the composite differential signals and their relative phase relation to each other. The remainder of the differential test setup is reused from the single-ended equipment configuration.

Self oscillation of the prescaler was observed with the application of DC bias voltages for all three MPW chip samples. The spectral plots of Figure 6.18 represent the self generated oscillations measured at the prescaler output in the absence of an input signal. All self-
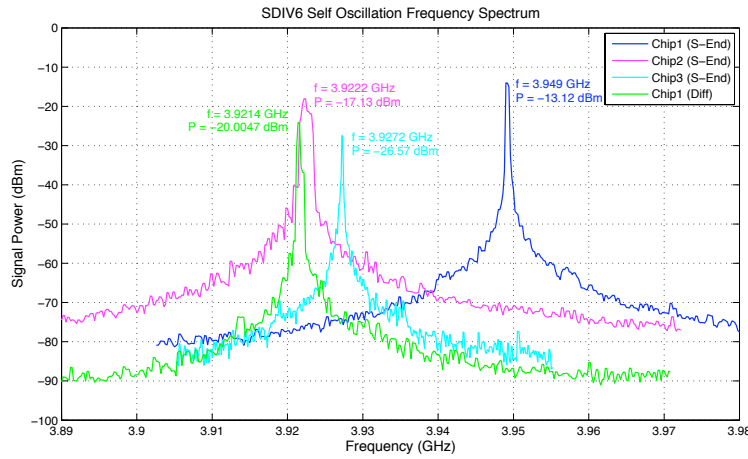
Figure 6.18. Measured SDIV6 self-oscillation frequency spectrum using single-ended (chips 1–3) and differential (chip 1) measurement techniques.

oscillation frequencies are within 80MHz of the designed output divided frequency of 4GHz, given a 24GHz input signal. The circuits natural tendency to oscillate at this frequency explains the very low voltage required to drive the prescaler at 24GHz. Essentially, when $v_{clk} = 0$V, the current distribution through each D-latch is symmetrical with $v_{out} \approx 0$V. Thus, the prescaler core contains multiple cascaded D-latches behaving like non-inverting differential amplifiers with a wired inversion feedback path creating a phase shift of $180°$ (or π). When the total loop phase shift is 2π, the Barkhausen criterion are met and the circuit oscillates.

To confirm that the prescaler exhibits accurate divide-by-6 functionality, a 24GHz input signal was applied to the input pads in both single-ended and differential test setups. Due to the limited output power capability of the signal generator at 24GHz and the inclusion of the attenuator, the specified input clock amplitude of 100mV[10] (or -10dBm) could not be reached. Instead, the maximum achievable amplitude was approximately 58.88mV (or

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[10]100mV per differential input, where $v_{clk\_n} = -v_{clk}$.

-14.6dBm)[11]. The combined frequency spectrum of Figure 6.19(a) shows that despite the reduced input amplitude, accurate 1/6 division is exhibited by each measured chip, producing an exact 4GHz output from the 24GHz input. The plots also demonstrate the mutual accuracy of both single-ended and differential measurement techniques. Figure 6.19(b) shows
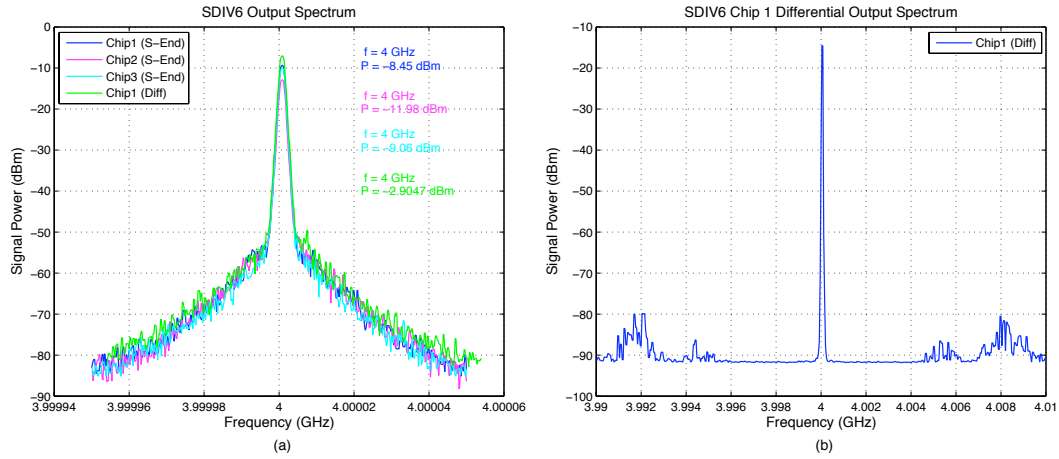
Figure 6.19. (a) Measured SDIV6 single-ended (chip 1–3) and differential (chip 1) output frequency spectrum given an input clock signal of -14.6dBm power (equivalent to 59mV voltage amplitude) at 24GHz. (b) Measured SDIV6 chip 1 differential output frequency spectrum including the associated frequency components out to 10MHz from the fundamental.

a differentially measured output spectrum of chip 1 including frequencies out to 10MHz from the centre frequency at 4GHz. Additional frequency components are observed from approximately ±4.5MHz offset from the fundamental.

The next phase of testing investigated the sensitivity of the prescaler, to gain an understanding of the signal levels required to maintain an accurate division ratio over a broad input frequency range, including the designed frequency of 24GHz. The input sensitivity characteristic is typically the dominant means of quantifying a frequency dividers performance. By varying the input signal provided from the frequency synthesiser in both frequency and power, the minimum power necessary to produce an output at $f_{clk}/6$ was recorded. Collating the results and plotting against the input frequency gives the measured input sensitivity characteristic shown in Figure 6.20.

The characteristic is classically displayed in decibels however additional insight can be gained by expressing the characteristic in Volts since these are the units typically used when specifying the input and output signal requirements of PLL building blocks. A differential input of 100mV at 24GHz was assumed during prescaler design and simulation and is considered to

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[11]This assumes 20dBm fixed attenuation and an estimated 2dB cable loss at 24GHz.
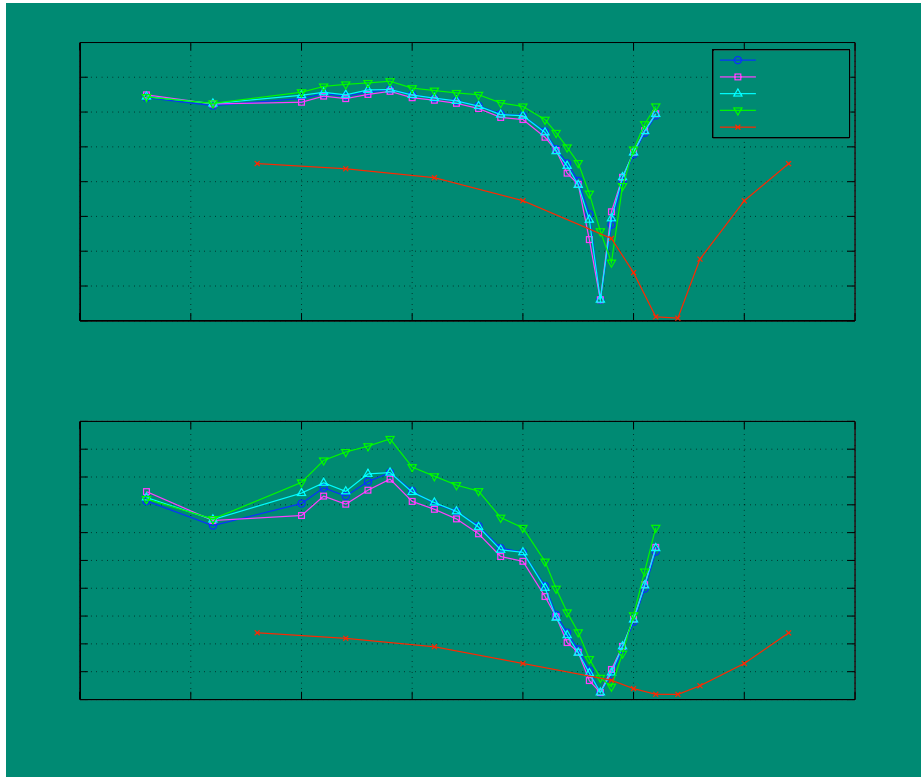
Figure 6.20. Measured SDIV6 single-ended and differential input sensitivity: (a) in dBm, and (b) in mV. Simulated post-layout analog extracted input sensitivity is included for comparison.

be a realistic representation of the input levels within a PLL, on chip. The input sensitivity plot indicates that a 1/6 division factor is achieved over the entire measured frequency range 3–26GHz for an input of this magnitude. In fact, provided the input is at least 81.56mV (-11.77dBm) according to single-ended data, and 93.71mV (-10.56dBm) according to differential data, the prescaler functionality is assured between 3–26GHz. Mentally extrapolating the characteristic[12], one could hypothesise accurate prescaler division up to 30GHz for a 100mV (-10dB) input. Unfortunately, due to equipment limitations the upper frequency limit of operation could not be determined. The low-frequency response stops at 3GHz and is limited by the slew-rate of the sinusoidal input signal. Table 6.6 contains the observed minimum input power and voltage points and the frequency at which they occur. Alternatively, these points can be viewed as the points of maximum prescaler sensitivity. The data reveals that at 24GHz, a signal of amplitude 10.8mV will be divided accurately irrespective of whether it is a single-ended or differential type input. The characteristic is consistent with the general shape of SiGe static frequency dividers recently reported in the literature [29, 53, 26, 54, 24, 55]. Included in the input sensitivity plots is the simulated post-layout

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[12]Assuming a similar levelling off curve at higher input frequencies, akin to post-layout simulation.

Table 6.6. Maximum measured prescaler input sensitivity and comparison to simulated post-layout analog extracted data.

| MMIC	Data Type	P_{clk} (dBm)	v_{clk} (mV)	f_{clk} (GHz)
	Single-ended Measurement	-41.98	2.518	23.5
SDIV6	Differential Measurement	-36.62	4.664	24
	Extracted Simulation	-44.61	1.859	27

analog extracted characteristic indicating a narrowing of the notch style frequency response. The post-layout results predict a much greater sensitivity over the frequency range 8–32GHz and suggest that a signal of 24mV (-22.4dBm) would be sufficient to drive the prescaler. The measured minimum also occurs 4GHz lower in frequency than the simulated minimum of 1.859mV (-44.61dBm) at 27GHz.

The RF output power was measured during input sensitivity testing and presented in Figure 6.21, along with the calculated output voltage assuming a 50Ω load. Ideally, with an output buffer amplifier incorporated in the prescaler design, the output voltage and hence power would remain relatively constant over the entire operational frequency range. Thus providing a consistent and large enough signal to drive the following circuitry amidst temperature and process fluctuations. In practice however, this is difficult to achieve given the nonlinear relationship between the required input power and the frequency. The output power ranges between -27.01dBm (14.11mV) and -8.65dBm (116.8mV) under single-ended operation and between -19.16dBm (34.83mV) and -3.54dBm (210.3mV) under differential operation. The output power peaks at the intended output frequency of 4GHz and is the result of a 24GHz input signal of only 4.664mV (-36.62dBm). The differential output voltage characteristic is approximately twice as large, or 6dBm larger in terms of power, as the single-ended measurement between 2.167GHz and 4GHz. Fluctuation in the differential output characteristic may be attributed to variation in the 180° phase relationship between v_{out} and v_{out_n}, caused by inconsistent cable losses before the hybrid coupler. It may also be the result of an identical effect after the hybrid coupler at the prescaler input. These losses become even more prominent at the input as frequency increases towards the maximum 26GHz.

DC current consumption was also recorded during input sensitivity testing for bias supplies, V_{cc} and V_{ref_clk}. V_{ref} is current limited to $I_{ref} = 4mA$ by the power supply and is therefore constant throughout the test. Figure 6.22 shows the total chip current and power consumption versus the output frequency. All three MPW samples exhibit relatively constant current consumption and only vary within approximately 3mA over the measurement range. It is not possible to directly measure the power consumption of the individual D-latches and output
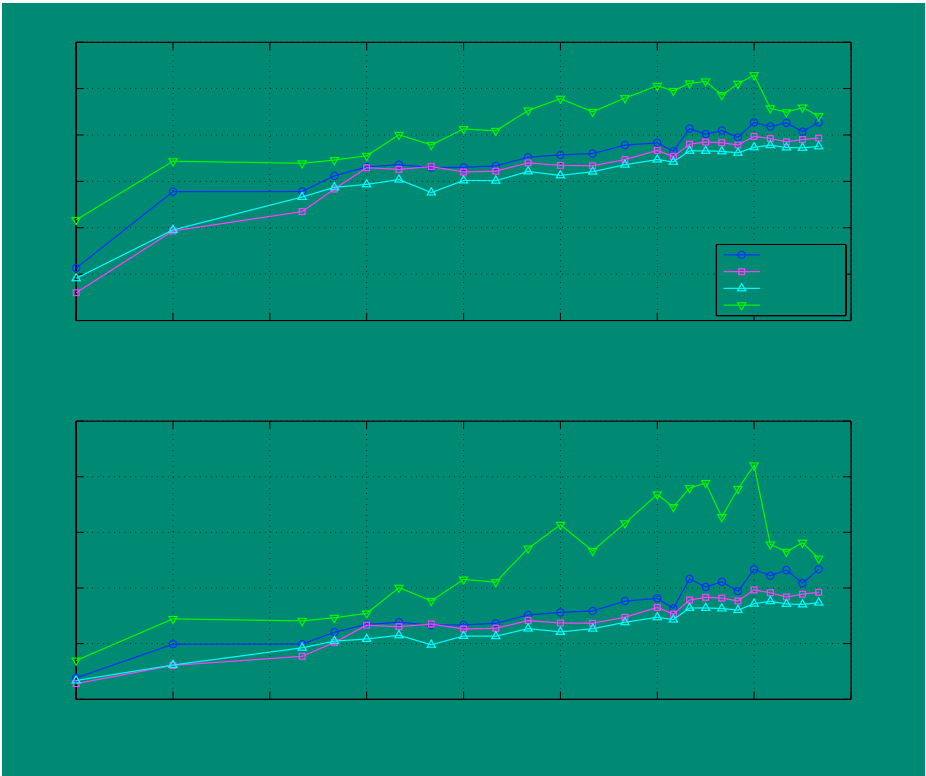
Figure 6.21. Measured SDIV6 single-ended and differential: (a) output power in dBm, and (b) output voltage in mV, recorded during input sensitivity testing.
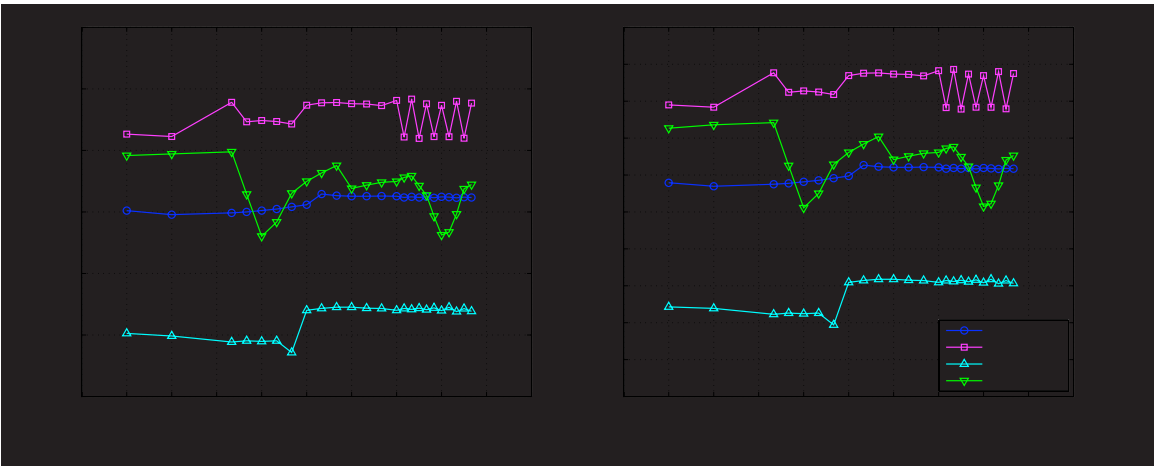
Figure 6.22. Measured SDIV6 single-ended and differential: (a) current, and (b) power consumption during input sensitivity testing.

buffer amplifier internal to the fabricated prescaler, however an estimate can be made using the total chip data and assuming that the EF output buffer tail bias current is an exact replica of the current mirror current, $I_{ref} = 4$mA set by the DC power supply limit. The differential double-stage EF output buffer is therefore estimated to consume 16mA or 67.2mW. The following expression can then be used to estimate the current and power consumed per D-latch in mA and mW respectively,

$$I_{D-latch} \ (mA) \approx \frac{\overline{I_{V_{CC}}} - 16}{6} \tag{6.38}$$

$$P_{D-latch} \ (mW) \approx V_{CC} \cdot I_{D-latch} \tag{6.39}$$

where $\overline{I_{V_{CC}}}$ is the mean measured current supplied to the divider core and output buffer by the DC bias voltage V_{cc}, over the input sensitivity test frequency range. Table 6.7 shows the estimated per D-latch current and power consumption, measured total chip consumption and post-layout simulated results of the same quantities. In summary, the measured

Table 6.7. Estimated prescaler D-latch and mean total chip current and power consumption measured during input sensitivity testing. Simulated schematic values are also included for comparison.

MMIC	*Data*	*Chip 1* *(S-End)*	*Chip 2* *(S-End)*	*Chip 3* *(S-End)*	*Chip 1* *(Diff)*	*Simulated*
SDIV6	$I_{D-latch} \ (mA)$	12.034	12.467	11.399	12.092	15.071
	$P_{D-latch} \ (mW)$	50.543	52.486	47.877	50.786	63.398
	$I_{Total} \ (mA)$	92.35	95.12	88.54	92.70	112.972
	$P_{Total} \ (mW)$	380.35	391.99	364.35	381.81	467.340

prescaler draws a mean total current of 92.70mA under differential excitation, with an estimated per latch current draw of 12.092mA. This is approximately 18–20% lower than the results predicted by analog extracted simulations.

Table 6.8 summarises the measured performance metrics of the 24GHz synchronous static 1/6 frequency prescaler fabricated in IBM 0.18μm SiGe BiCMOS technology. The results are compared against post-layout analog extracted simulation data and reported state-of-the-art frequency divider designs in similar technologies.

Table 6.8. Summary of SDIV6 measured performance, post-layout simulation and comparison to the current state-of-the-art frequency dividers.

Ref.	*Technology, f_t* *Topology, Size (μm^2)*	$P_{clk_{min}}$ (dBm)	$f_{P_{clk_{min}}}$ (GHz)	f_{BW} (GHz)	P_{Total} (mW)	f_{clk}/f_{out}
SDIV6	0.18μm SiGe BiCMOS, 60GHz Sync. Static ECL, 776×776 Analog Extracted Simulation	 -36.62 -44.61	 24 27	 3–26 8–32	 381.81 467.34	24/4
[56]	0.5μm SiGe HBT, 80GHz Dynamic Regenerative, 220×170 Async. Static ECL, 450×200	 -4 –	 24 –	 23.7–24.9 <12.5	 132 66	 24/12 12/1.5
[50]	Infineon SiGe B7HF, 75GHz Async. Static ECL, 890×890	 -44	 21	 7–28	 82.6	 24/0.75
[23]	0.25μm SiGe:C BiCMOS, 190GHz Dynamic Regenerative , 370×475 Static ECL, 380×475 Async. Dynamic + 4 Static, 655×475	 -18 -33 -14	 13 30 24	 22–93 5–50 25–76	 175 217.5 1010	 2 2 32
[22]	0.25μm SiGe:C BiCMOS, 200GHz Static ECL, 1000×500 Dynamic Regenerative , 1000×500	 -24 -1.4	 50 80	 18–71.5 24–103	 140 195	 2 2
[25]	0.15μm SiGe:C Bipolar, 200GHz Async. Static ECL, 550×450 Dynamic Regenerative , 550×450	 -19 -19	 70 41	 2–86.2 35–110	 900 310	 32 2
[57]	0.13μm SiGe BiCMOS, 230GHz Static ECL w/ EF, 515×473 Static ECL w/o EF, 502×360	 -22 -42	 66 77	 2–80 18–100	 145 122	 2 2
[53]	0.18μm SiGe BiCMOS, 120GHz Async. Static E^{2}CL	 -29	 41	 2–51	 4056	 8
[58]	0.25μm SiGe:C BiCMOS, 190GHz Dynamic Regenerative , 295×475	 -18	 25	 22–93	 175	 2
[59]	0.15μm GaAs PHEMT, 95GHz Dynamic Regenerative , 3000×1500	 –	 –	 5.7%	 100	 28/14
[60]	0.5μm InP DHBT, 301GHz Static ECL w/ L-peaking, 493×473	 -36	 87	 3–152	 659.8	 2

Chapter 7

Conclusion

This chapter summarises the outcomes of the thesis with respect to the research motivations and discusses the scope of possible future work.

7.1 Thesis Conclusions

The use of negative resistance theory has been demonstrated in the design of two 15GHz single-ended injection-lockable VCOs (ET15G and ET15G_V2) fabricated in an IBM 0.18μm SiGe BiCMOS technology with $f_t = 60$GHz. A Colpitts based emitter-tuned topology has been implemented allowing injection-locking via the output port. The simulated and measured performance metrics are summarised in Table 7.1. ET15G exhibits slightly better

Table 7.1. Simulated and measured performance metrics of the SiGe VCO MMICs developed in this thesis for frequency synthesis in mm-wave devices.

Chip	Data Type	f_{osc} (GHz)	f_Δ (GHz)	P_{out} (dBm)	P_{DC} (mW)	η (%)	$\mathcal{L}(\Delta\omega)$ (dBc/Hz)
ET15G	Measured	14.541	0.0226	-3.70	4.958	8.63	-89.75
	Simulated	14.571	0.4178	-1.63	4.800	14.33	-90.58
ET15G_V2	Measured	13.230	230.7	-9.80	3.064	3.45	-78.72
	Simulated	15.110	486.5	-7.96	3.219	4.98	-86.10
XC24G	Measured	22.719	1.61	-3.446	23.528	1.95	-85.90
	Simulated	24.145	1.611	-0.129	33.122	2.933	-94.34

performance than ET15G_V2 in terms of frequency accuracy and phase noise, however both circuits suffer significant reduction in tuning range from predicted post-layout simulation results. As such, both circuits are unable to be tuned to 15GHz under the designed bias

and tuning voltage specifications. An alternative biasing setup for ET15G has generated an output at 15GHz, rendering it suitable for implementation in the intended Ka-Band antenna beam-forming network.

The suitability of SiGe BiCMOS technology in the emerging automotive SRR market has been demonstrated through the design of a differential cross-coupled VCO (XC24G) and multi-stage synchronous static frequency prescaler (SDIV6) for PLL based frequency synthesis at 24GHz. Both MMICs are fabricated in an IBM 0.18μm SiGe BiCMOS process with $f_t = 60$GHz and exhibit excellent performance. Negative resistance theory and statistical process variation analysis techniques have been utilised in the VCO design and functional verification. The importance of statistical manufacturing process variation analysis for SiGe MMIC design has been highlighted, and its applicability in the academic research environment where such rigours are seldom considered. Measured 24GHz VCO performance metrics are summarised in Table 7.1, indicating good tuning range and a centre frequency approximately 1.3GHz lower than required. Under modified bias conditions, 24GHz output was achieved, therefore making the VCO suitable for automotive SRR applications. The synchronous static 1/6 frequency prescaler exhibits one of the best broadband input sensitivity characteristics reported in the literature to date, with more than adequate output power and hence driving capability. A summary of prescaler performance appears in Table 7.2. A differential mea-

Table 7.2. Simulated and measured performance metrics of the SiGe prescaler MMIC developed in this thesis for frequency synthesis in mm-wave devices. Note – input sensitivity, P_{clk} is quoted for a 4GHz output frequency only and may not represent the minimum observed.

Chip	*Data Type*	P_{clk} (dBm)	f_{BW} (GHz)	P_{out} (dBm)	P_{DC} (mW)
SDIV6	Measured	-36.62	3–26	-3.54	381.81
	Simulated	-33.18	8-32	1.83	467.34

surement technique has been successfully implemented, showing good agreement with more commonly used single-ended frequency divider characterisation. Although prescaler power consumption is high, accumulation of signal jitter has been minimised. Given the VCO output level and the prescaler input sensitivity, interoperability within the intended 24GHz PLL for UWB automotive SRR is guaranteed with minimal system phase noise impact.

While measured results show reasonable agreement with post-layout simulations for all MMICs, VCO frequency is particularly susceptible to discrepancies or deficiencies in the accuracy of

device and parasitic modelling at mm-wave frequencies. Coupled with the small tuning capability of the VCOs, makes it difficult to achieve the desired oscillation frequency in a single prototyping wafer run.

In conclusion, through verified chip prototyping, this thesis confirms the practicability of recent SiGe BiCMOS technology advances for the implementation of low-cost integrated frequency synthesis circuits in mm-wave devices.

7.2   Future Directions

Design tool licensing restrictions and limited time to perform physical chip measurement have prevented further investigation into some of the open questions identified in this research. The following is a list of potential future work within the project scope.

- Isolation of the cause of the significant discrepancy between simulated and measured 15GHz VCO tuning capability. Further investigation could indicate the existence of a possible design or layout fault.

- The differential on-wafer measurement technique used in the frequency prescaler characterisation could also be applied to the differential 24GHz VCO. Comparison with single-ended measurement data would provide verification of results and closer modelling of the simulated system.

- The upper frequency limit of prescaler operation was unable to be determined due to the 26.5GHz output limit of the HP 8340B frequency synthesiser used as the input clock source for testing. A higher frequency device could be used to determine this important characteristic.

- It would be interesting to investigate the effects of temperature variation on SiGe MMIC performance and compare to competing mm-wave technologies. Temperature effects on 24GHz automotive SRR circuits are particularly relevant given the extreme environmental and atmospheric conditions in which they would be expected to operate in reliably.

- Integration of the differential VCO and frequency prescaler with the remaining PLL components shown in Figure 1.3 in a SoC would be the obvious next step towards an operational 24GHz UWB automotive SRR receiver. The ultimate goal being a full 24GHz SRR system developed in low-cost SiGe technology for the automotive market.

- This thesis has proven the suitability of the moderate performance IBM BiCMOS7WL technology for MMIC design up to 24GHz. However, a higher performance SiGe technology with $f_t > 60$GHz (IBM BiCMOS7HP with $f_t = 120$GHz or BiCMOS8HP with $f_t = 200$GHz for example) could provide performance gains in terms of VCO tunability, lower power operation, higher device gain and broader prescaler operational frequency. Therefore, the cost versus performance benefits of a higher f_t SiGe technology could be investigated.

Appendix A

Schematics

This appendix contains the final optimised circuit schematics of the MMICs designed and tested in this thesis. The layout cell views submitted for fabrication were generated from these schematics.
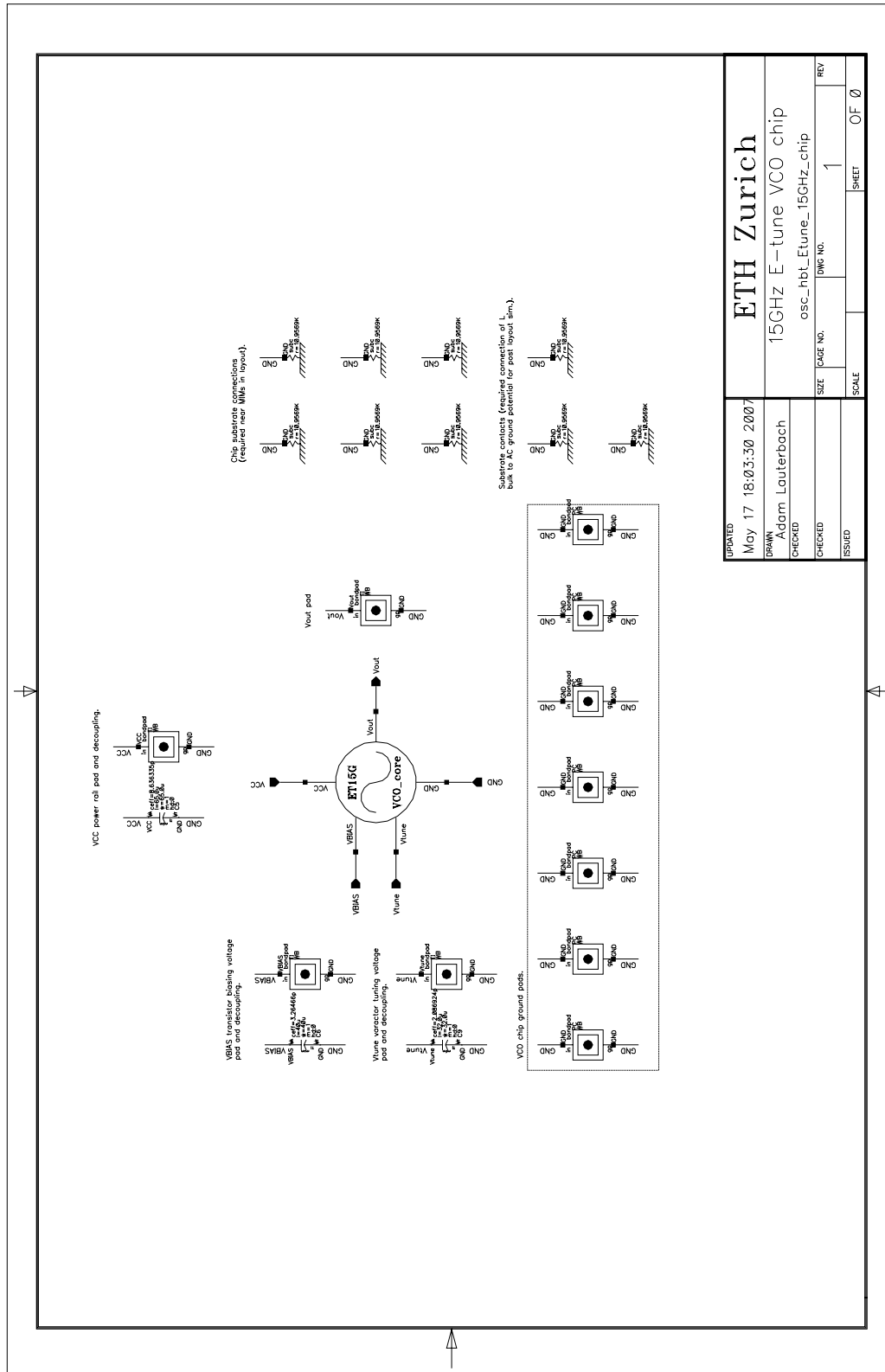
Figure A.1. ET15G 15GHz E-tuned single-ended VCO top level schematic including VCO core, bond pads, substrate ties and power supply decoupling capacitors.

Figure A.2. ET15G 15GHz E-tuned single-ended VCO core schematic utilising the tuning varactor connected to the emitter of the transistor.
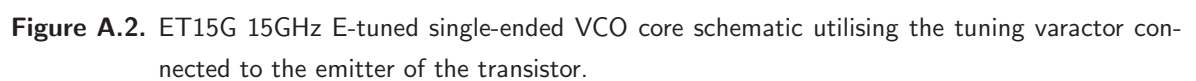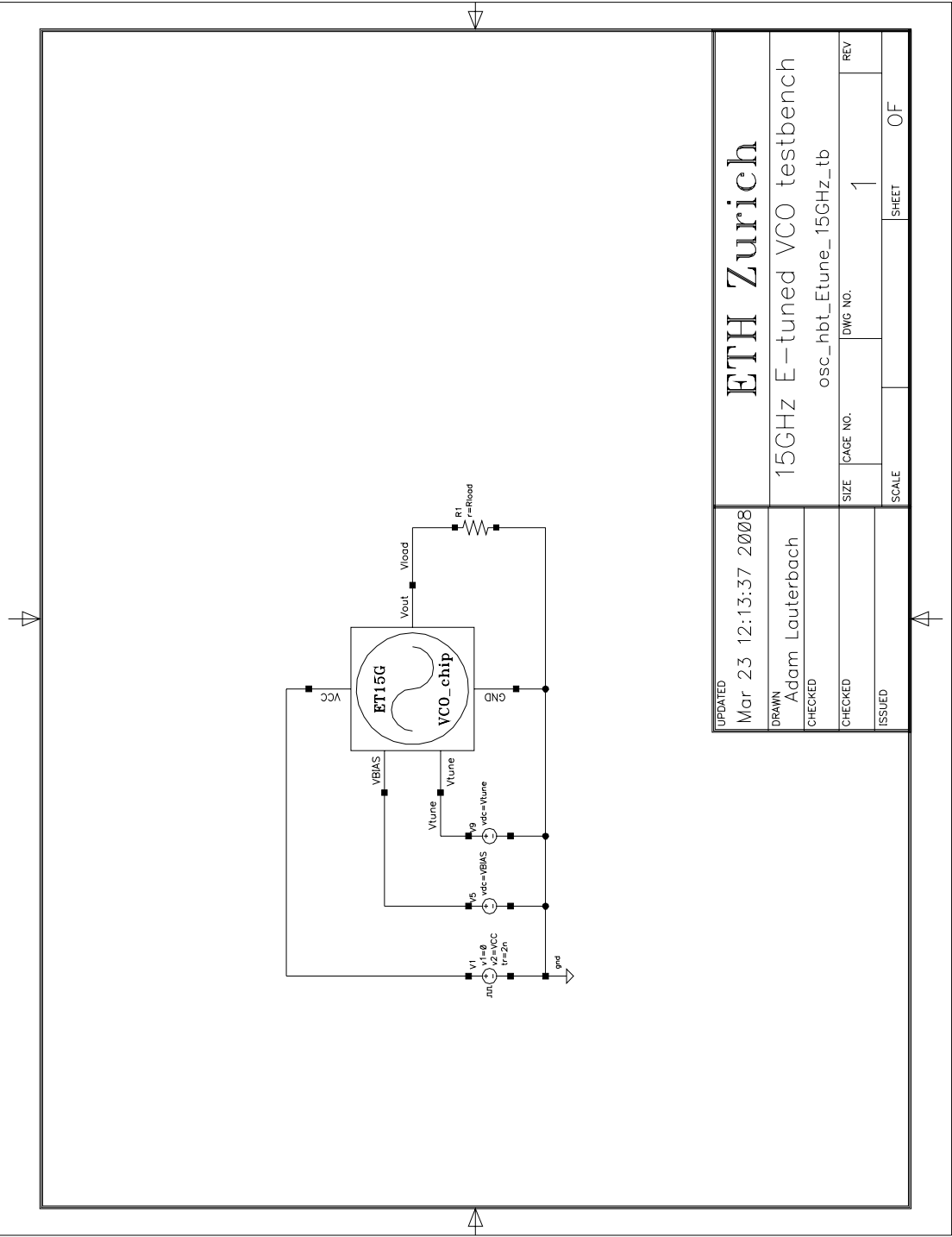
Figure A.3. ET15G 15GHz E-tuned single-ended VCO test bench schematic used to simulate pre-layout schematic and post-layout analog extracted VCO performance.

Figure A.4. ET15G_V2 15GHz E-tuned single-ended VCO top level schematic including VCO core, bond pads, substrate ties and power supply decoupling capacitors.

Figure A.5. ET15G_V2 15GHz E-tuned single-ended VCO core schematic utilising the tuning varactor connected to the emitter of the transistor.

Figure A.6. ET15G_V2 15GHz E-tuned single-ended VCO test bench schematic used to simulate pre-layout schematic and post-layout analog extracted VCO performance.
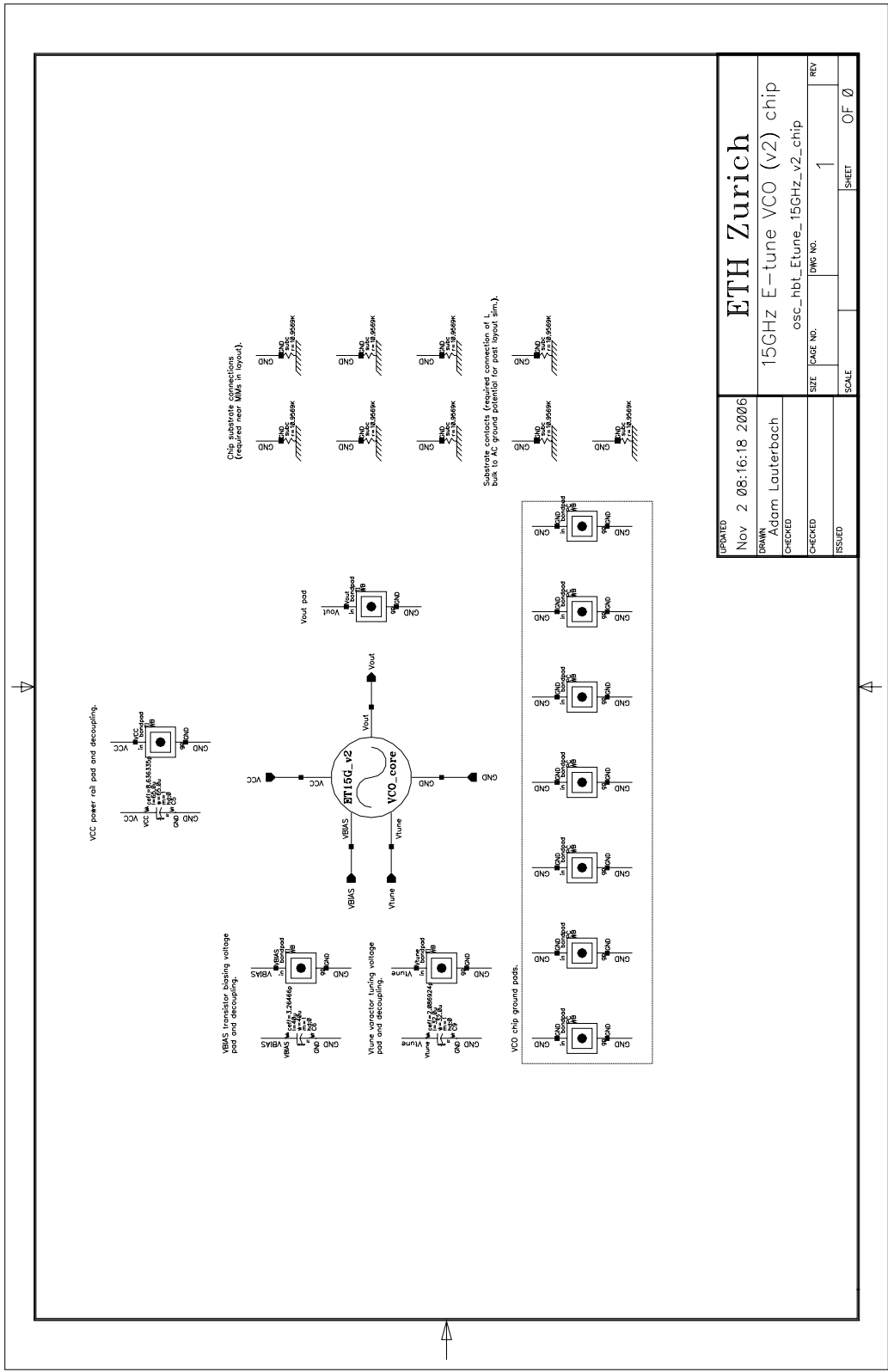
Figure A.7. ET15G_V3 15GHz E-tuned single-ended VCO top level schematic including VCO core, bond pads, substrate ties and power supply decoupling capacitors.
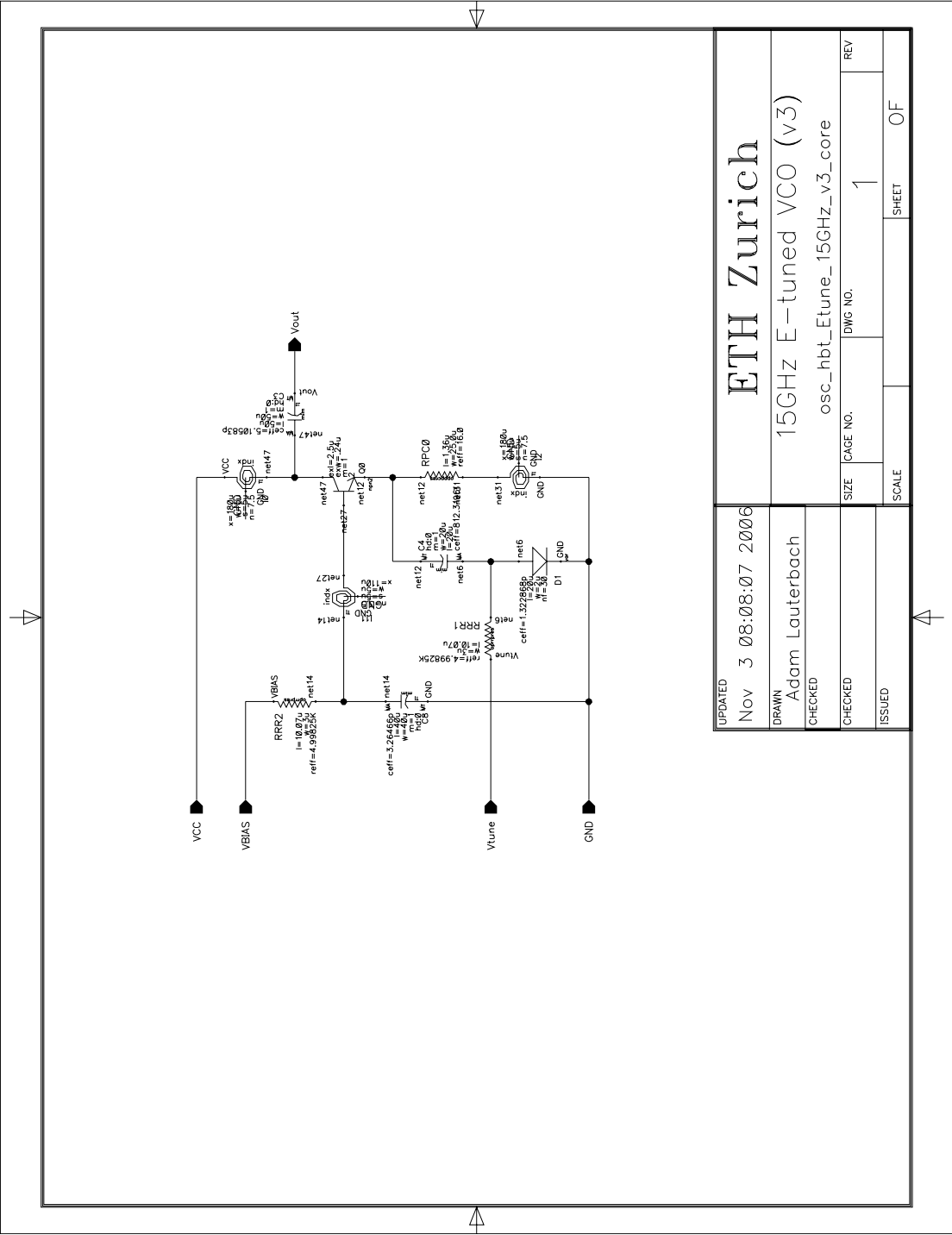
Figure A.8. ET15G_V3 15GHz E-tuned single-ended VCO core schematic utilising the tuning varactor connected to the emitter of the transistor.
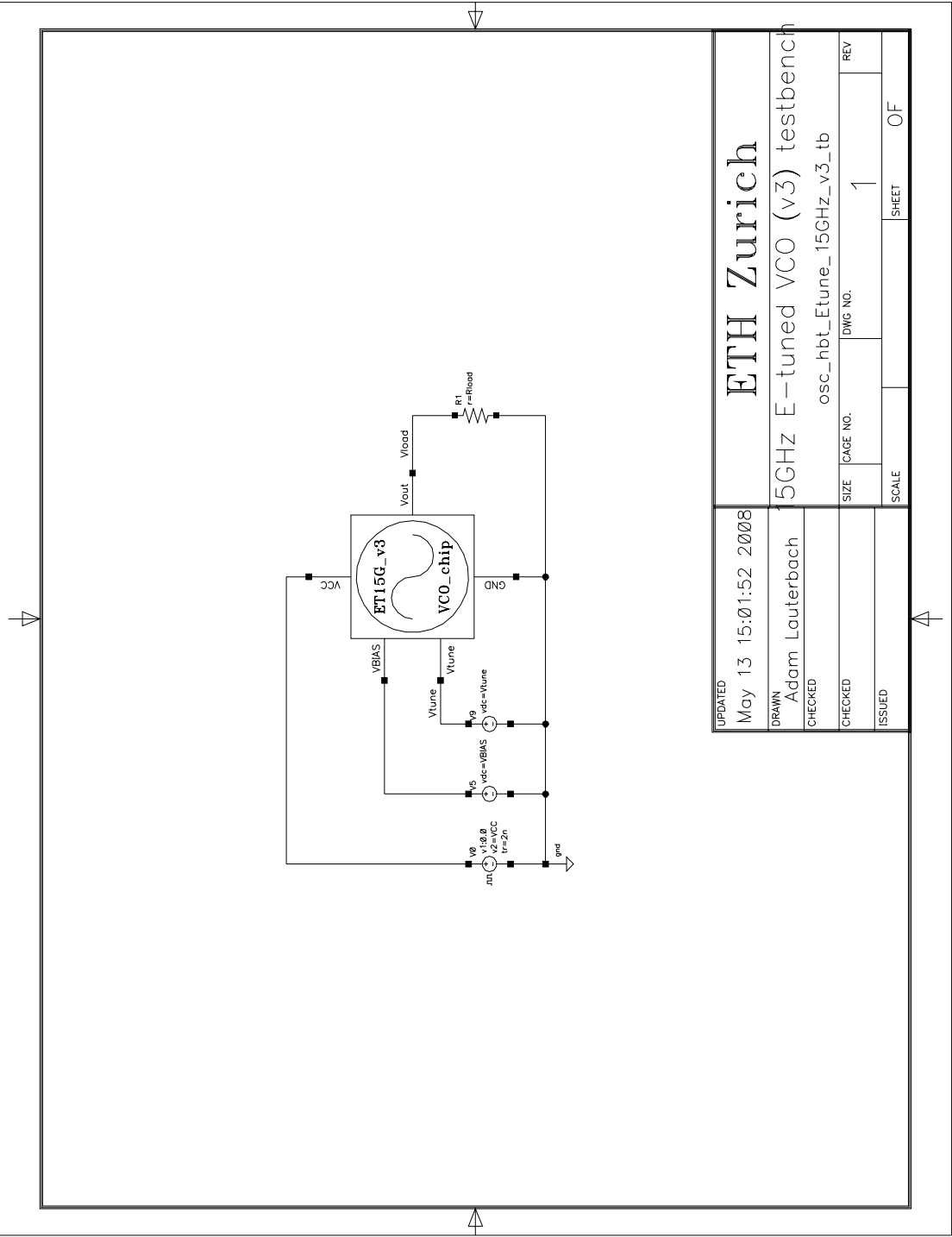
Figure A.9. ET15G_V3 15GHz E-tuned single-ended VCO test bench schematic used to simulate pre-layout schematic and post-layout analog extracted VCO performance.
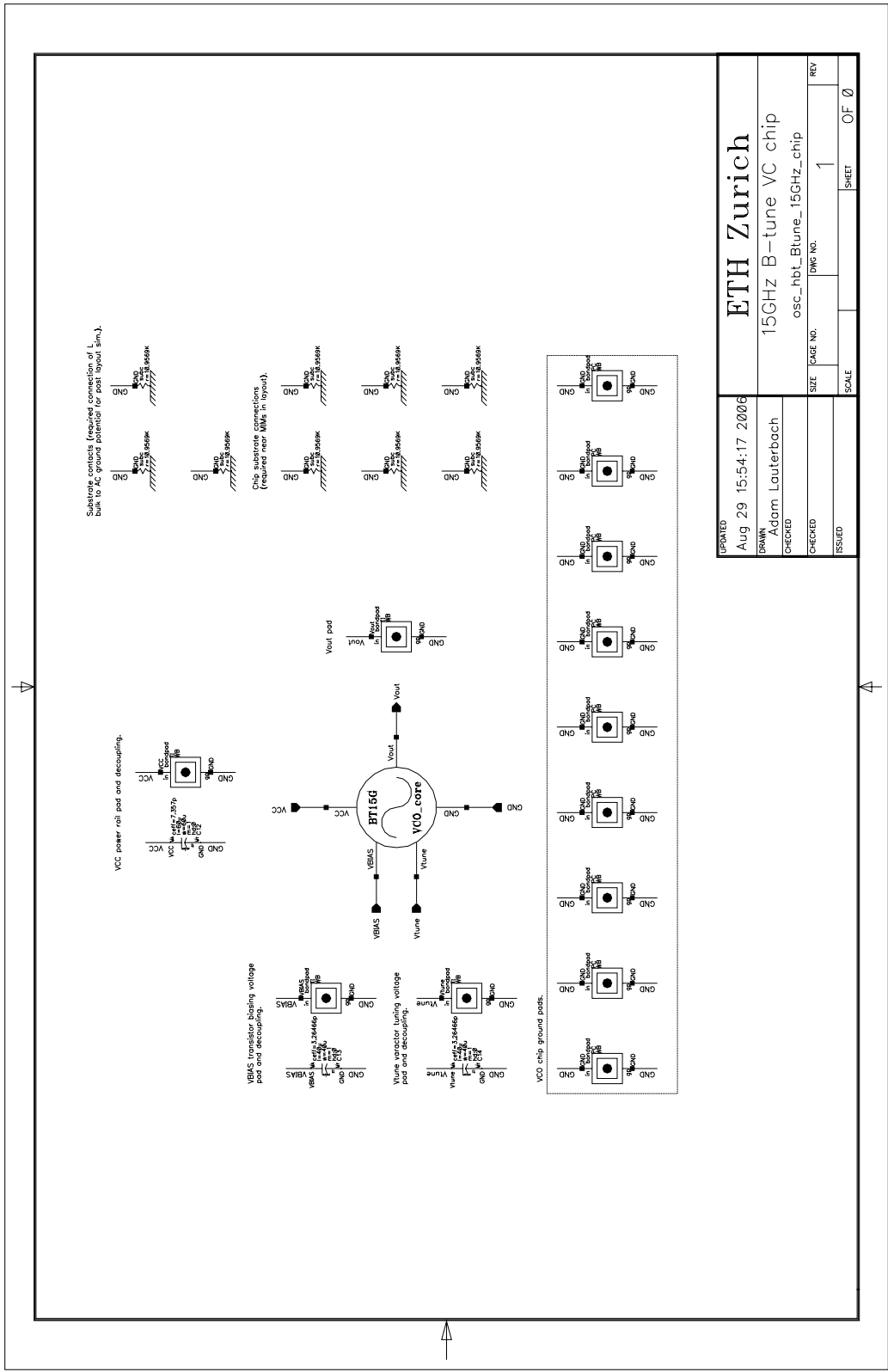
Figure A.10. BT15G 15GHz B-tuned single-ended VCO top level schematic including VCO core, bond pads, substrate ties and power supply decoupling capacitors.
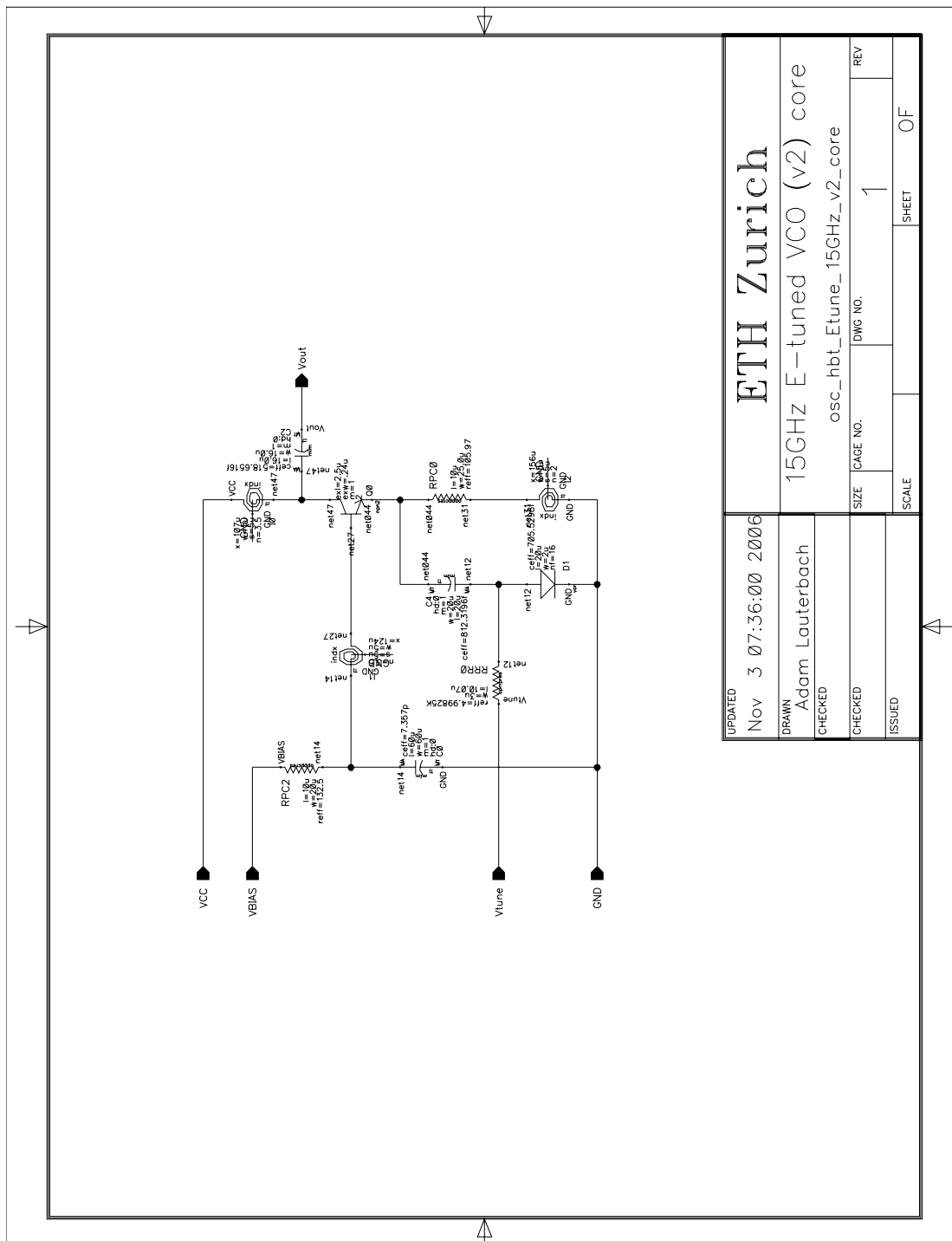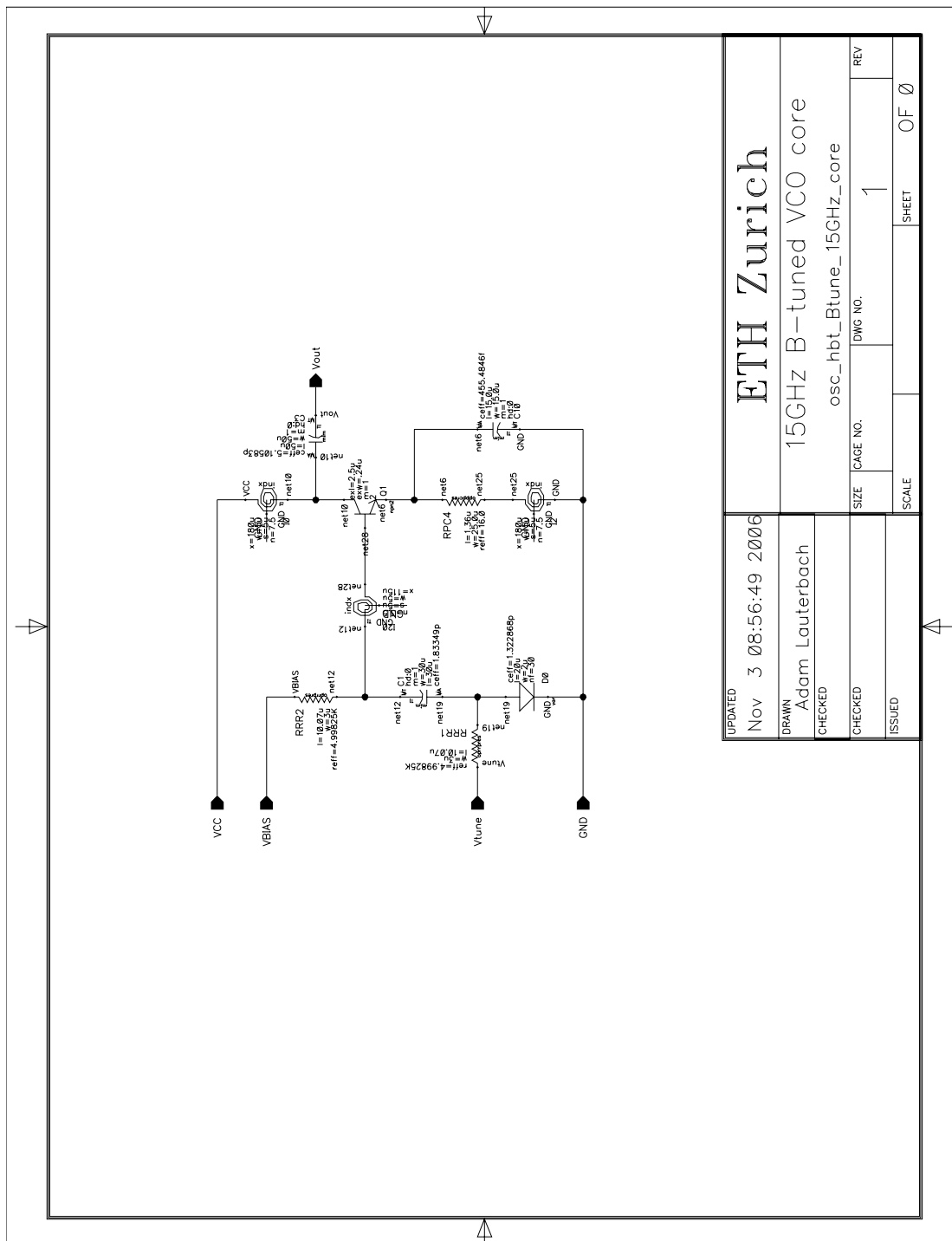
Figure A.11. BT15G 15GHz B-tuned single-ended VCO core schematic utilising the tuning varactor connected to the base of the transistor.
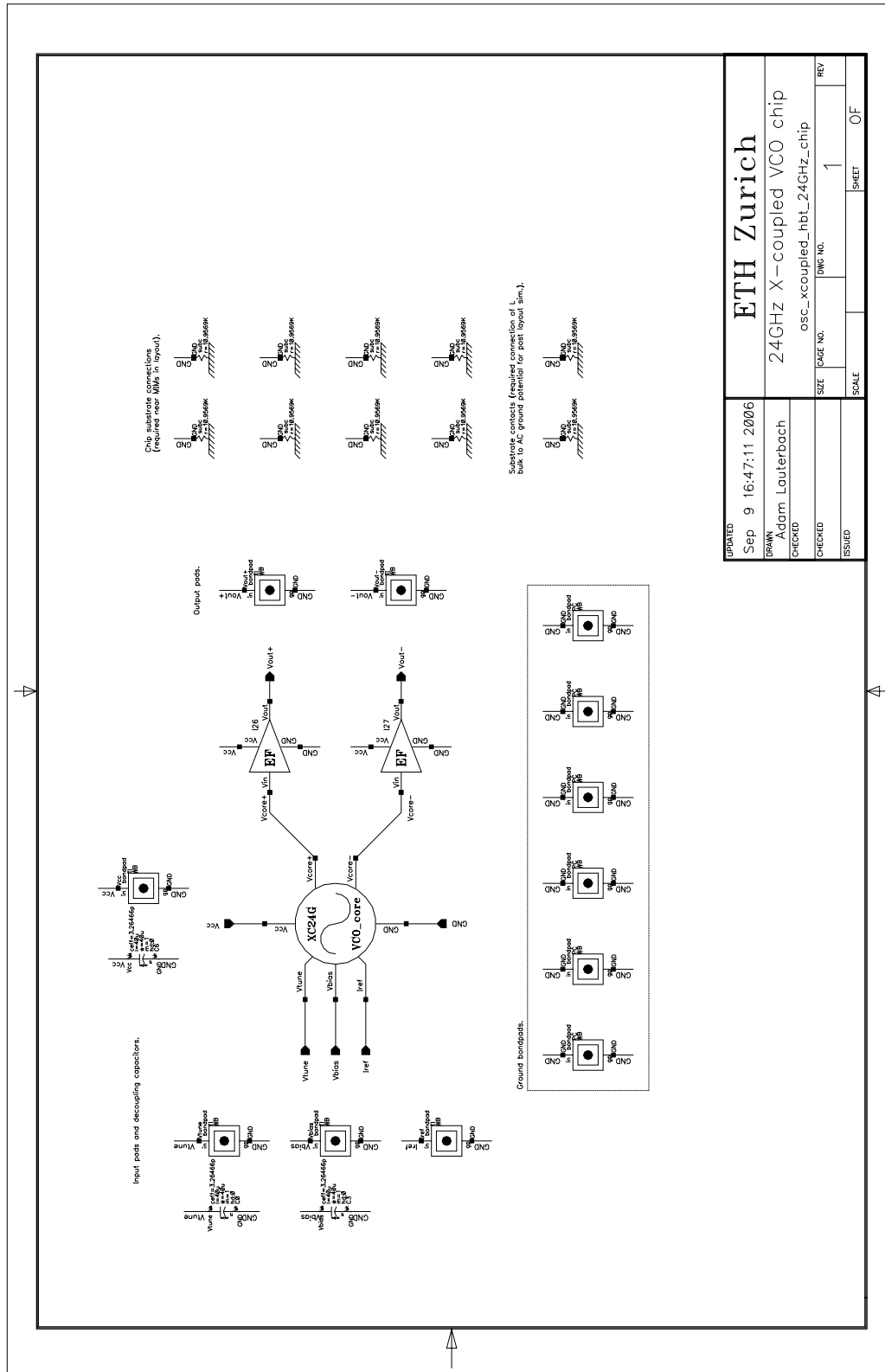
Figure A.12. BT15G 15GHz B-tuned single-ended VCO test bench schematic used to simulate pre-layout schematic and post-layout analog extracted VCO performance.
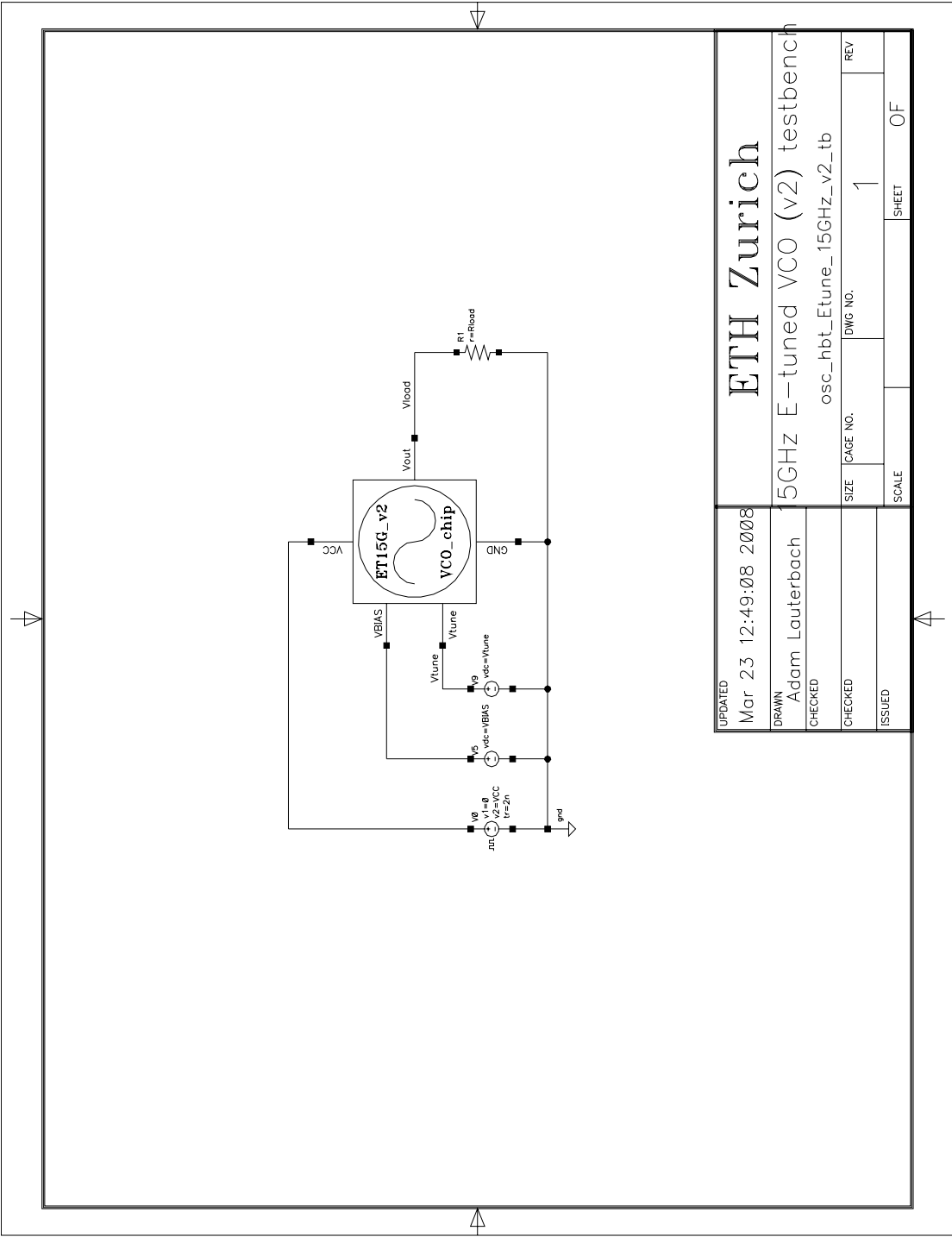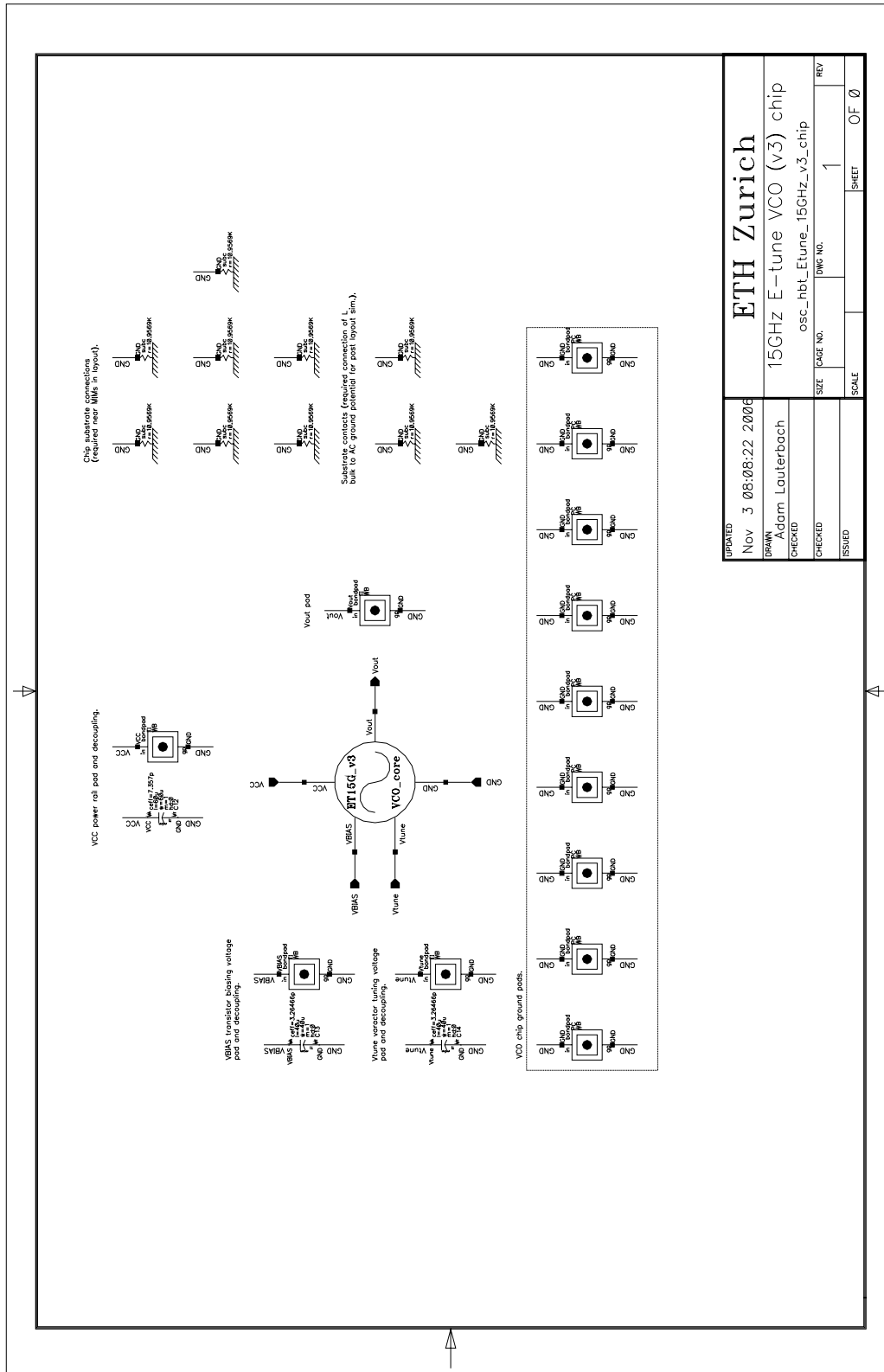
Figure A.13. XC24G 24GHz differential cross-coupled VCO top level schematic including VCO core, output buffer amplifiers, bond pads, substrate ties and power supply decoupling capacitors.
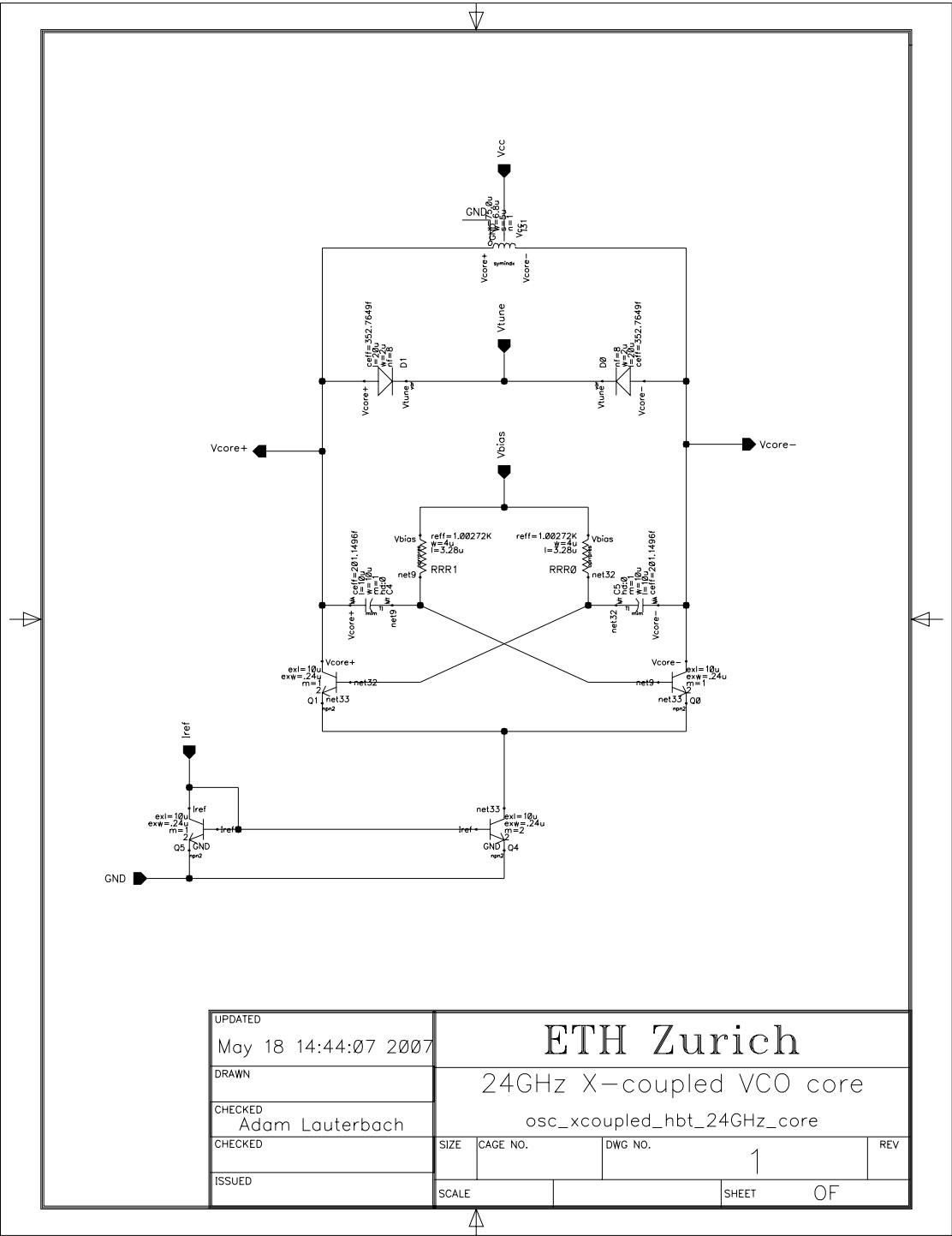
Figure A.14. XC24G 24GHz differential cross-coupled VCO core schematic combining the capacitive cross-coupled differential pair, current mirror bias and resonant tank comprising symmetrical inductor and tuning varactors.
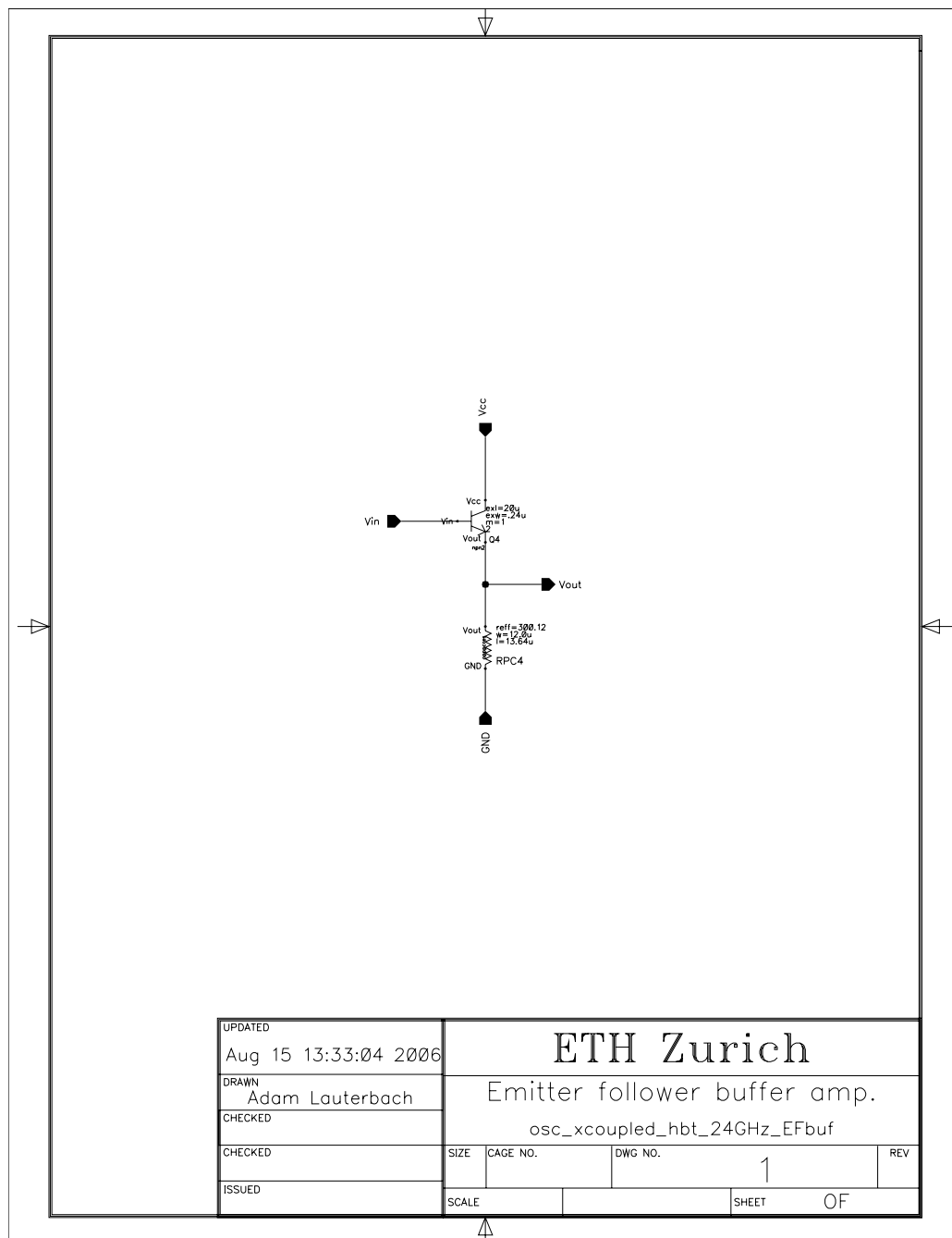
Figure A.15. XC24G 24GHz differential cross-coupled VCO emitter-follower output buffer schematic.
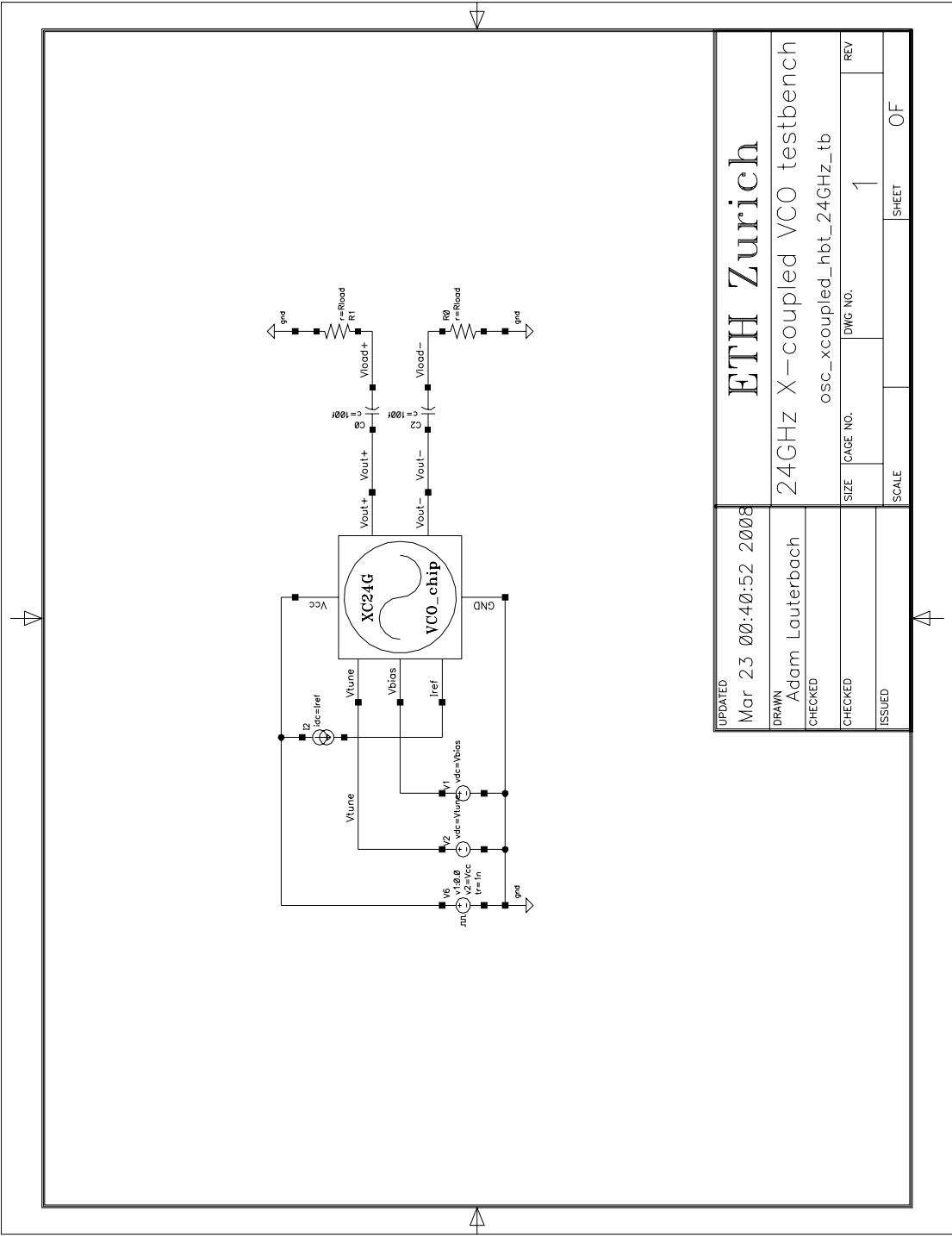
Figure A.16. XC24G 24GHz differential cross-coupled VCO test bench schematic used to simulate pre-layout schematic and post-layout analog extracted VCO performance.

Figure A.17. SDIV6 1/6 frequency prescaler top level schematic including 3-stage DFF synchronous static divider core, output buffer amplifier, current mirror supply, bond pads, substrate ties and power supply decoupling capacitors.
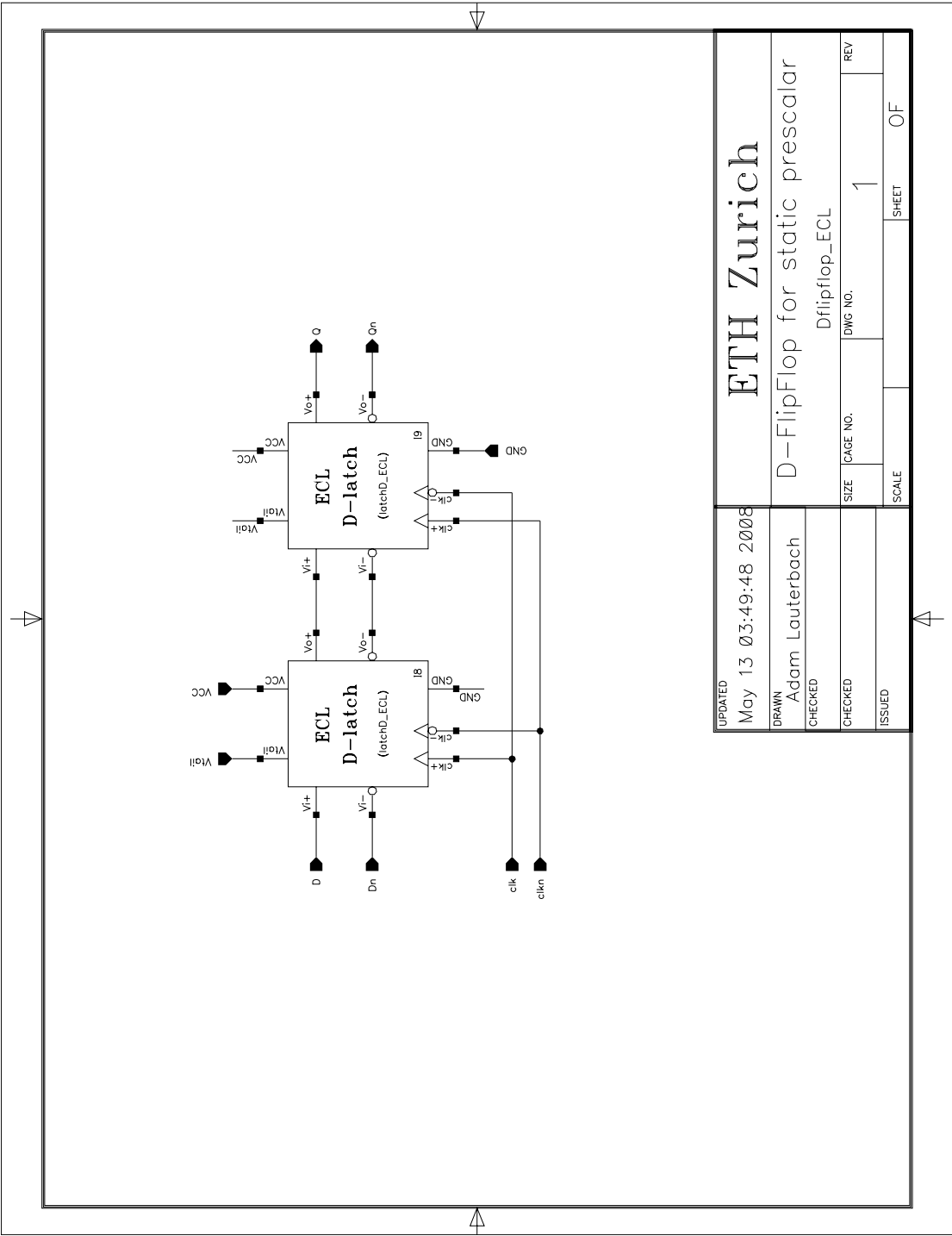
Figure A.18. SDIV6 1/6 frequency prescaler negative edge triggered DFF schematic constructed from two master-slave ECL D-latches.
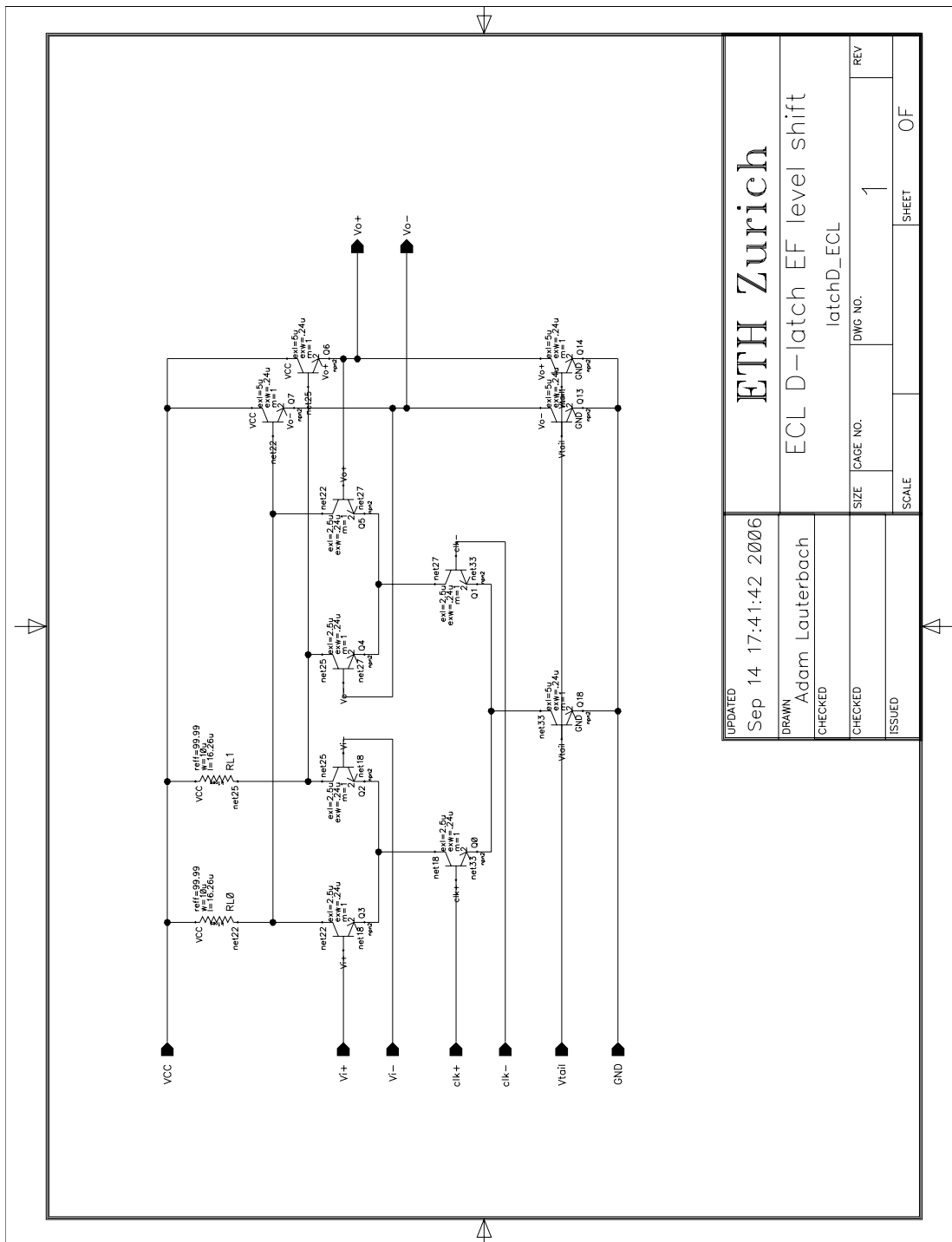
Figure A.19. SDIV6 1/6 frequency prescaler D-latch schematic comprising track and hold stages, current steering differential pair, emitter-follower output level shifters and tail current supply transistors.
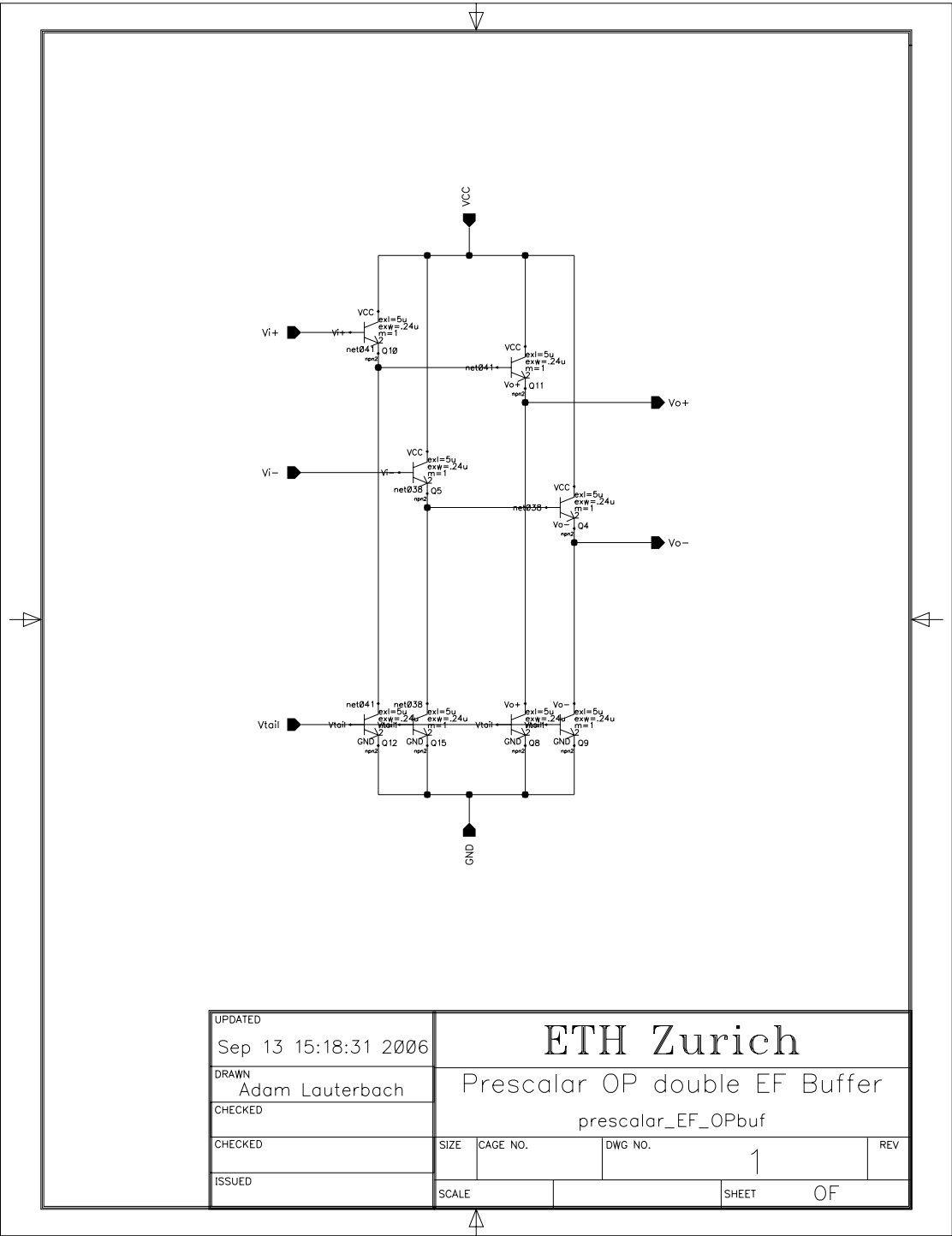
Figure A.20. SDIV6 1/6 frequency prescaler double emitter-follower output buffer schematic including bias current transistors.
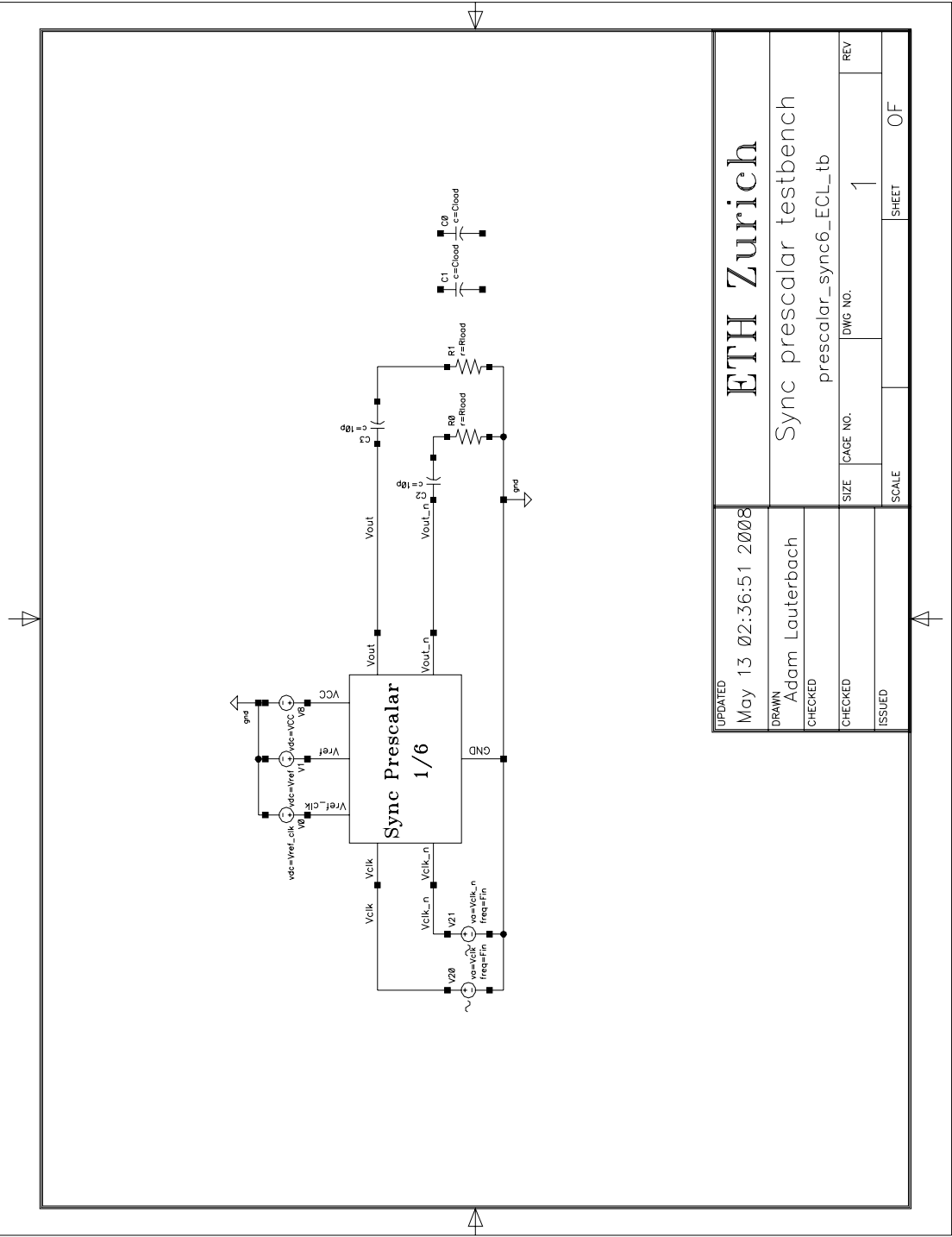
Figure A.21. SDIV6 1/6 frequency prescaler test bench schematic used to simulate pre-layout schematic and post-layout analog extracted prescaler performance.

Figure A.22. Combined XC24G 24GHz VCO and SDIV6 1/6 frequency prescaler test bench schematic used to simulate a bonded chip environment.
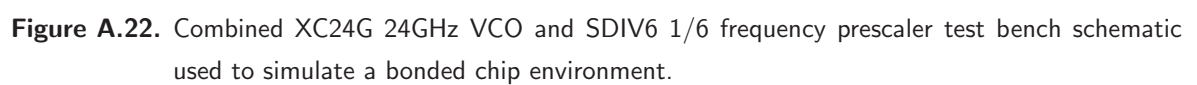
Appendix B

SDIV6 Layout Cell Views

This appendix contains additional layout cell views of the SDIV6 1/6 synchronous static frequency prescaler core, ECL D-latch, DFF and EF output buffer.

(a)

(b)
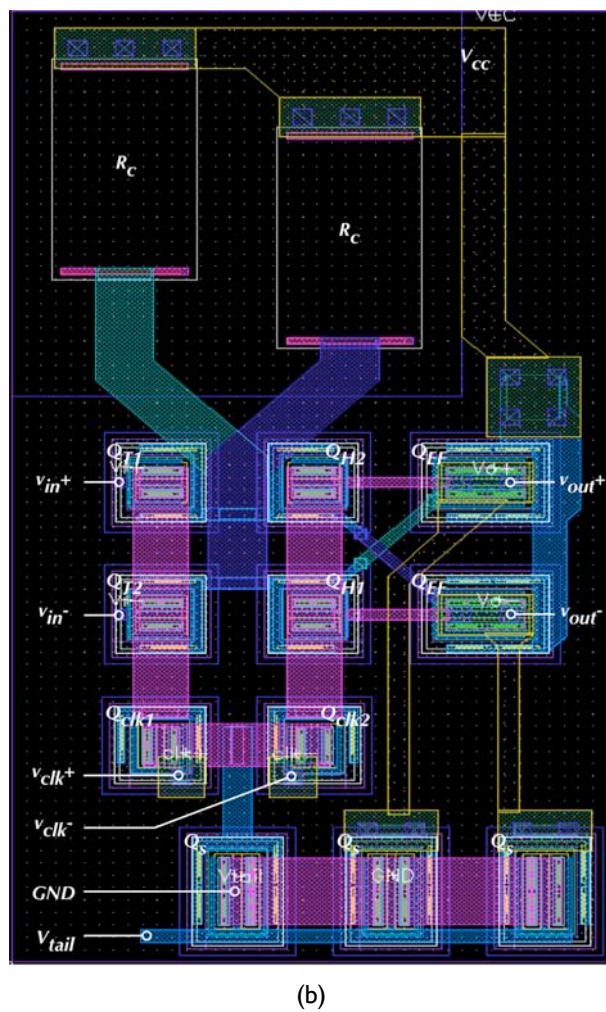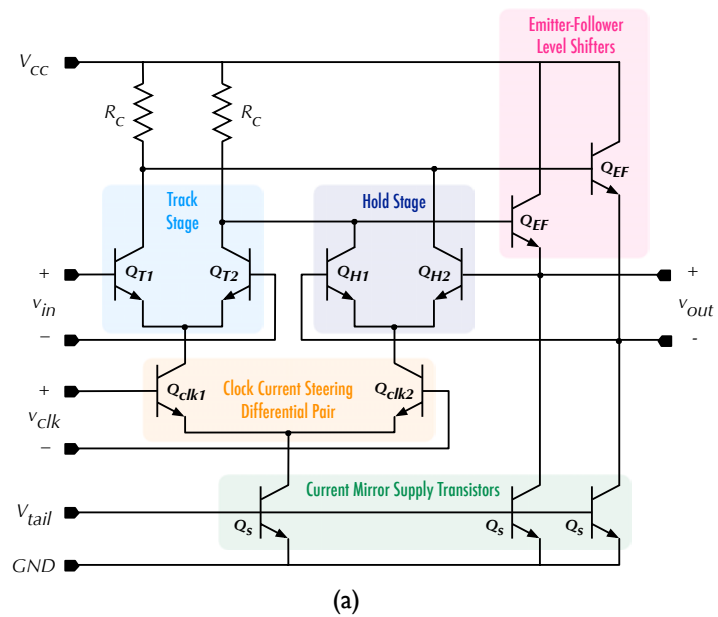
Figure B.1. SDIV6 D-latch: (a) schematic and (b) layout cell view before metal density fill and without poly-Si (Rx) and deep trench isolation (Ti) mesh.
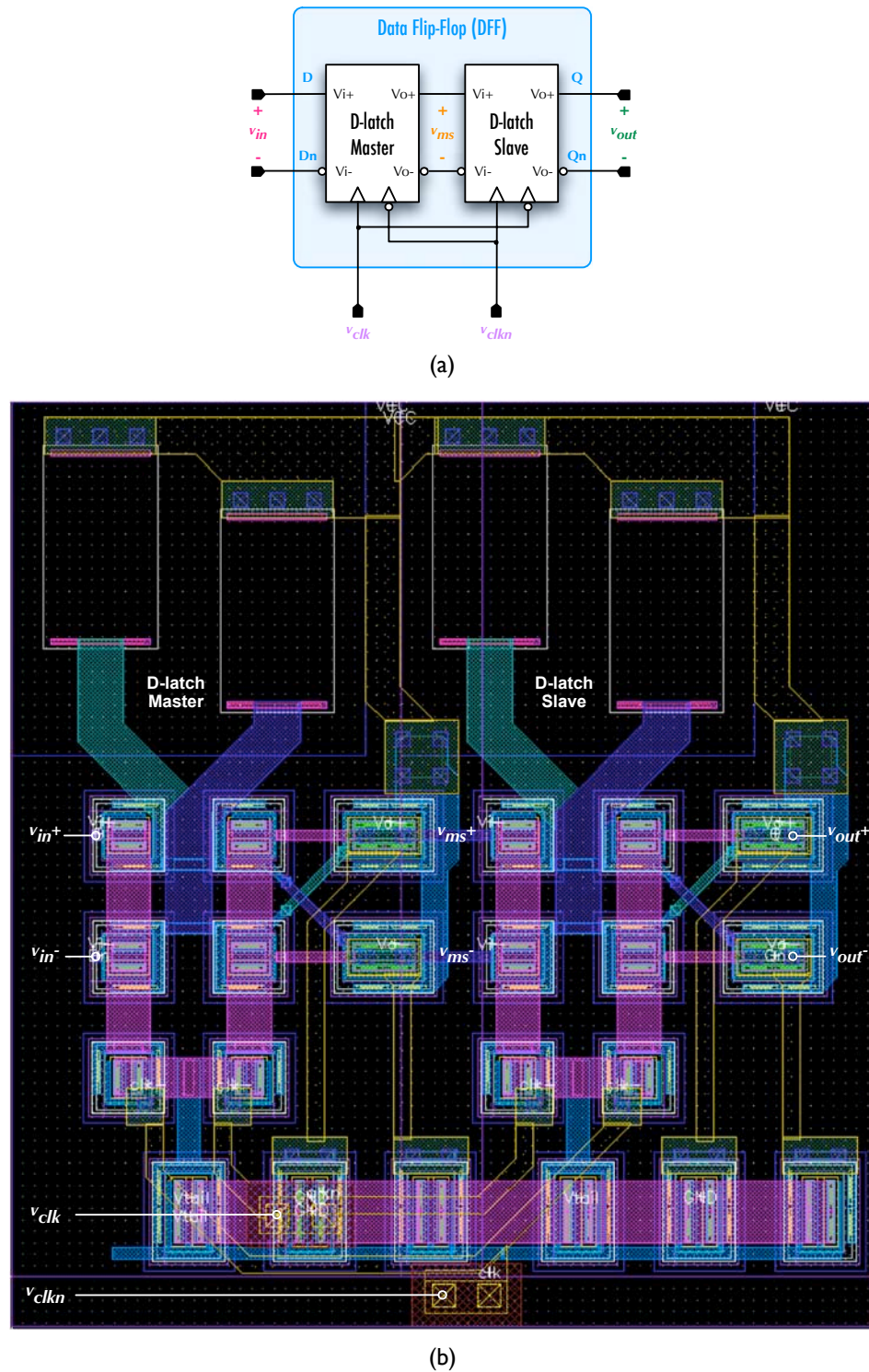
Figure B.2. SDIV6 DFF: (a) schematic and (b) layout cell view before metal density fill and without Rx and Ti mesh.
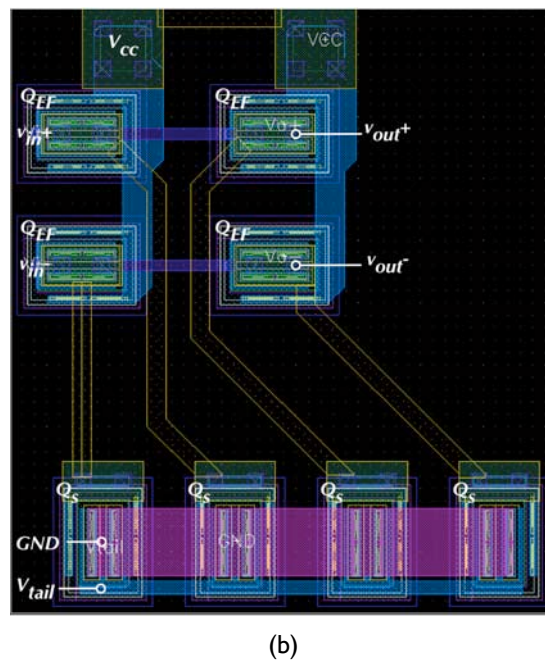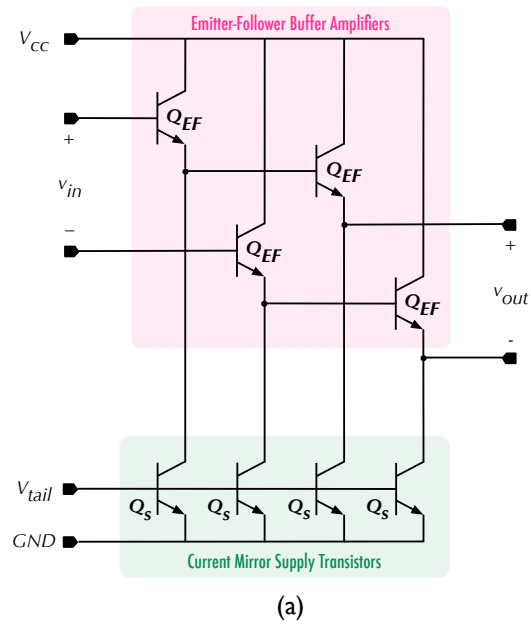
Figure B.3. SDIV6 EF output buffer: (a) schematic and (b) layout cell view before metal density fill and without Rx and Ti mesh.
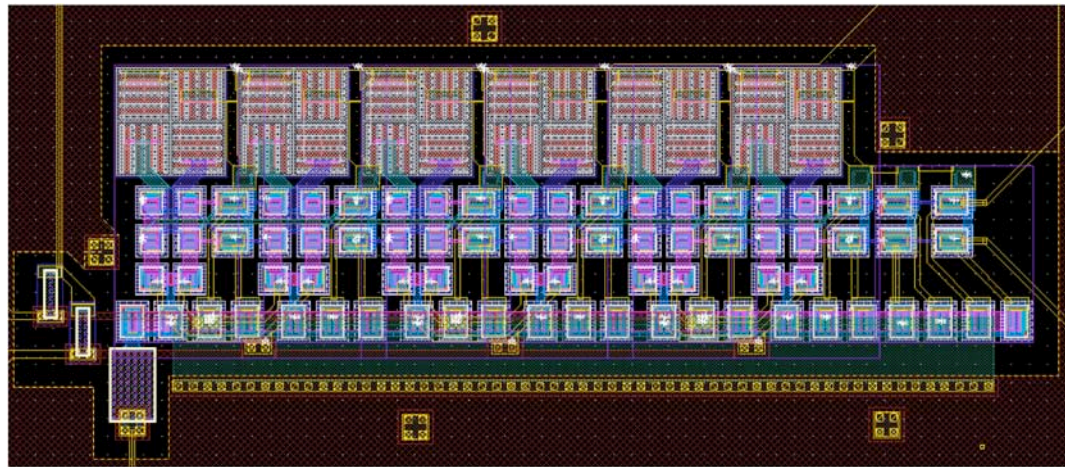
(a)
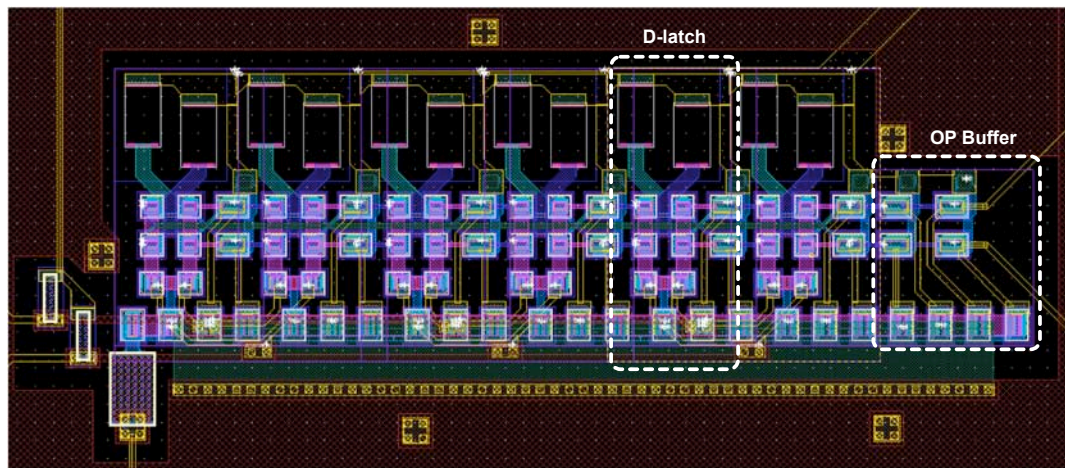
(b)
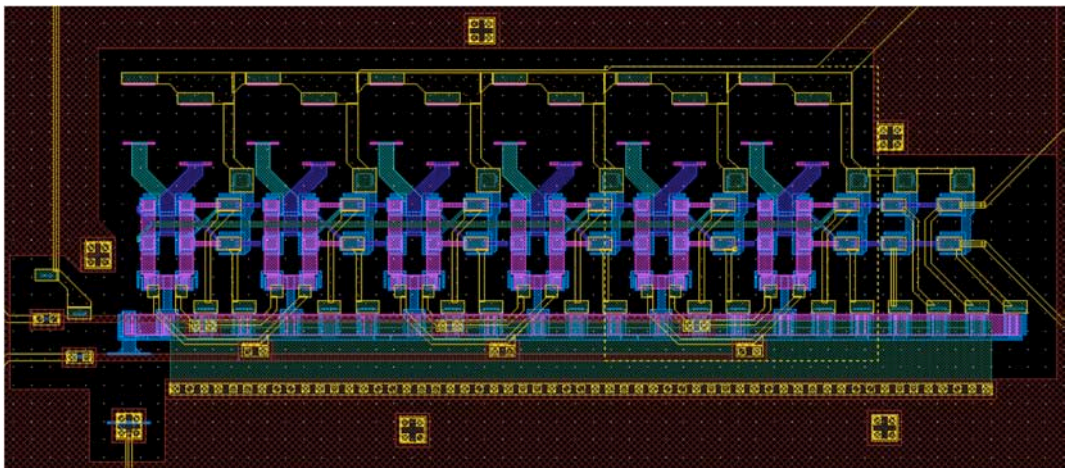
(c)

Figure B.4. SDIV6 core layout cell views before metal density fill: (a) full, (b) without Rx and Ti mesh, and (c) metal only.

Appendix C

Measurement Data

This appendix contains the manually recorded on-wafer measurement data presented in Chapter 6.

Table C.1. ET15G chip 1 tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1V$, $V_{tune} = 0V$ to $-3V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
0	14.5332	-6.14	2.5
-0.2	14.5362	-5.71	2.6
-0.4	14.537	-5.97	2.6
-0.6	14.539	-5.73	2.7
-0.8	14.542	-5.48	2.7
-1	14.5436	-5.31	2.7
-1.2	14.5452	-5.28	2.7
-1.4	14.5466	-5.22	2.7
-1.6	14.5480	-5.12	2.7
-1.8	14.5488	-5.09	2.7
-2	14.5492	-5.14	2.7
-2.2	14.55	-5.2	2.7
-2.4	14.551	-5.06	2.7
-2.6	14.5532	-4.9	2.7
-2.8	14.5552	-4.88	2.7
-3	14.5562	-4.77	2.7

Table C.2. ET15G chip 2 tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1V$, $V_{tune} = 0V$ to $-3V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
0	14.525	-5.86	2.7
-0.2	14.5347	-5.7	2.7
-0.4	14.5361	-5.75	2.8
-0.6	14.5377	-5.52	2.8
-0.8	14.53917	-5.64	2.8
-1	14.54031	-5.4	2.8
-1.2	14.54151	-5.32	2.8
-1.4	14.54267	-5.2	2.8
-1.6	14.54379	-5.33	2.8
-1.8	14.54479	-5.21	2.8
-2	14.54579	-5.16	2.8
-2.2	14.54675	-5.05	2.8
-2.4	14.54779	-5.12	2.8
-2.6	14.54871	-5.08	2.9
-2.8	14.5497	-5.01	2.8
-3	14.55075	-4.91	2.8

Table C.3. ET15G chip 3 tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1V$, $V_{tune} = 0V$ to $-3V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
0	14.5317	-5.82	2.7
-0.2	14.5339	-5.75	2.7
-0.4	14.5357	-5.62	2.8
-0.6	14.5375	-5.48	2.8
-0.8	14.5387	-5.16	2.8
-1	14.5399	-5.08	2.8
-1.2	14.5415	-5.02	2.8
-1.4	14.5425	-5.01	2.8
-1.6	14.5437	-4.93	2.8
-1.8	14.5447	-5.22	2.8
-2	14.5457	-5.07	2.8
-2.2	14.5467	-5.07	2.8
-2.4	14.5477	-5.05	2.9
-2.6	14.5485	-4.95	2.8
-2.8	14.5497	-4.89	2.8
-3	14.5507	-4.86	2.8

Table C.4. ET15G chips 1–3 direct phase noise measurement at 1MHz offset from the carrier.

MPW	V_{tune} (V)	$P_m - P_s$ (dBm)	B_m (kHz)	B_M (Hz)	SF_{BW}	$\mathcal{L}(f_m)$ (dBc/Hz)
Chip 1	-3	-52.02	10	1	40	-92.02
	0	-47.22				-87.22
Chip 2	-3	-49.62	10	1	40	-89.62
	0	-50.75				-90.75
Chip 3	-3	-50.39	10	1	40	-90.39
	0	-48.48				-88.48
Chip 1 @ 15GHz	0	-47.08	10	1	40	-87.08

Table C.5. ET15G_V2 chip 1 tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1V$, $V_{tune} = 0V$ to $-3V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
0	13.126	-11.5	1.6
-0.2	13.131	-11.24	1.6
-0.4	13.2366	-11.55	1.6
-0.6	13.239	-12.02	1.6
-0.8	13.2418	-11.27	1.6
-1	13.245	-11.25	1.6
-1.2	13.346	-11.51	1.7
-1.4	13.3425	-12.07	1.6
-1.6	13.3441	-11.84	1.6
-1.8	13.3471	-11.41	1.6
-2	13.3505	-11.21	1.7
-2.2	13.3537	-11.1	1.7
-2.4	13.3551	-11.22	1.6
-2.6	13.4537	-11.45	1.7
-2.8	13.4547	-11.61	1.7
-3	13.4561	-11.01	1.7

Table C.6. ET15G_V2 chip 2 tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1V$, $V_{tune} = 0V$ to $-3V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
0	13.120	-11.41	1.6
-0.2	13.125	-10.96	1.7
-0.4	13.128	-10.77	1.7
-0.6	13.133	-11.22	1.7
-0.8	13.235	-11.05	1.7
-1	13.237	-11.50	1.7
-1.2	13.238	-10.90	1.7
-1.4	13.240	-11.48	1.7
-1.6	13.3402	-11.26	1.8
-1.8	13.341	-11.86	1.8
-2	13.340	-11.00	1.8
-2.2	13.3415	-11.64	1.8
-2.4	13.3422	-12.67	1.8
-2.6	13.343	-11.50	1.8
-2.8	13.344	-11.00	1.8
-3	13.345	-10.92	1.8

Table C.7. ET15G_V2 chip 3 tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1V$, $V_{tune} = 0V$ to $-3V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
0	13.099	-13.56	1.6
-0.2	13.111	-12.50	1.7
-0.4	13.12	-11.70	1.7
-0.6	13.123	-11.14	1.7
-0.8	13.126	-10.92	1.7
-1	13.128	-10.65	1.7
-1.2	13.130	-10.61	1.7
-1.4	13.132	-10.48	1.7
-1.6	13.135	-10.49	1.7
-1.8	13.233	-11.24	1.8
-2	13.235	-10.91	1.8
-2.2	13.236	-10.78	1.8
-2.4	13.236	-11.09	1.8
-2.6	13.234	-10.98	1.8
-2.8	13.223	-12.61	1.7
-3	13.225	-12.14	1.7

Table C.8. ET15G_V2 chips 1–3 direct phase noise measurement at 1MHz offset from the carrier.

MPW	V_{tune} (V)	$P_m - P_s$ (dBm)	B_m (kHz)	B_M (Hz)	SF_{BW}	$\mathcal{L}(f_m)$ (dBc/Hz)
Chip 1	-3	-31.24	10	1	40	-71.24
	0	-35.04				-75.04
Chip 2	-3	-38.73	10		40	-78.73
	0	-33.44	100	1	50	-83.44
Chip 3	-3	-34.88	10	1	40	-74.88
	0	-48.96				-88.96
Chip 1 @ 15GHz	0	-46.19	10	1	40	-86.19

Table C.9. XC24G chip 1 single-ended tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1.4V$, $I_{ref} = 4mA$, $V_{tune} = 1.8V$ to $4.8V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
1.8	21.9871	-11.56	12.9
2.0	22.2081	-11.41	12.9
2.2	22.4281	-11.56	12.9
2.4	22.5511	-11.4	12.9
2.6	22.7661	-10.87	12.9
2.8	22.887	-11.15	12.9
3.0	23.000	-11.16	12.9
3.2	23.1081	-11.09	12.9
3.4	23.1211	-11.04	12.9
3.6	23.227	-10.68	12.9
3.8	23.3301	-10.51	12.9
4.0	23.4371	-10.14	12.9
4.2	23.5381	-10.32	13.0
4.4	23.5537	-10.20	13.0
4.6	23.5607	-10.23	12.9
4.8	23.5813	-10.38	13.0

Table C.10. XC24G chip 2 single-ended tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1.4V$, $I_{ref} = 4mA$, $V_{tune} = 1.8V$ to $4.8V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
1.8	21.9776	-11.29	13.8
2.0	22.1078	-11.53	1 3.8
2.2	22.4376	-12.06	13.8
2.4	22.6638	-11.58	13.8
2.6	22.7832	-11.94	13.8
2.8	22.8992	-11.91	13.8
3.0	23.0068	-11.54	13.8
3.2	23.1126	-11.32	13.8
3.4	23.2176	-11.16	13.8
3.6	23.3248	-10.65	13.8
3.8	23.332	-10.72	13.8
4.0	23.4366	-13.32	13.8
4.2	23.4430	-10.47	13.8
4.4	23.5456	-10.42	13.8
4.6	23.5506	-10.58	13.8
4.8	23.5570	-10.60	13.8

Table C.11. XC24G chip 3 single-ended tuning data: $V_{cc} = 1.8V$, $V_{bias} = 1.4V$, $I_{ref} = 4mA$, $V_{tune} = 1.8V$ to $4.8V$.

V_{tune} (V)	f_{osc} (GHz)	P_{out} (dBm)	$I_{V_{cc}}$ (mA)
1.8	21.7764	-12.82	12.4
2.0	21.9972	-12.31	12.5
2.2	22.2152	-12.50	12.5
2.4	22.4326	-12.59	12.5
2.6	22.5516	-12.48	12.5
2.8	22.7496	-12.17	12.5
3.0	22.8724	-12.03	12.5
3.2	22.8908	-12.78	12.5
3.4	22.9954	-12.21	12.5
3.6	23.1008	-12.15	12.5
3.8	23.1100	-12.00	12.5
4.0	23.2130	-12.01	12.5
4.2	23.2214	-12.40	12.5
4.4	23.3218	-11.71	12.5
4.6	23.3286	-11.44	12.5
4.8	23.4318	-11.16	12.5

Table C.12. XC24G chips 1-3 direct phase noise measurement at 1MHz offset from the carrier.

MPW	V_{tune} (V)	$P_m - P_s$ (dBm)	B_m (kHz)	B_M (Hz)	SF_{BW}	$\mathcal{L}(f_m)$ (dBc/Hz)
Chip 1	1.8	-42.95	10	1	40	-82.95
	4.8	-42.47				-82.47
Chip 2	1.8	-48.61	10	1	40	-88.61
	4.8	-42.09				-82.09
Chip 3	1.8	-49.28	10	1	40	-89.28
	4.8	-50.01				-90.01

Table C.13. SDIV6 chip 1 single-ended input sensitivity data: $V_{cc} = 4.2V$, $V_{ref\_clk} = 2V$, $V_{ref} = 2.4V$ ($I_{ref} = 4mA$).

F_{clk} (GHz)	P_{clk} (dBm)	$I_{V_{cc}}$ (mA)	$I_{V_{ref\_clk}}$ (mA)	F_{out} (GHz)	P_{out} (dBm)
0.6	14.7	88.36	0.199	0.1	-38.65
1	13.95	88.12	0.197	0.166667	-35.44
3	7.7	87.85	0.192	0.5	-24.95
6	6.85	87.75	0.162	1.0	-16.72
10	8.1	87.82	0.148	1.6666	-16.7
11	8.95	87.85	0.15	1.83336	-15.01
12	8.6	87.9	0.145	2.0	-14.05
13	9.2	87.95	0.143	2.16667	-13.81
14	9.55	88.02	0.144	2.3333	-14.13
15	9.1	88.09	0.142	2.5	-14.10
16	8.55	88.44	0.140	2.66667	-13.94
17	8.2	88.39	0.140	2.83334	-13.02
18	7.5	88.37	0.140	3.0	-12.76
19	6.5	88.37	0.140	3.16666	-12.62
20	6.25	88.38	0.134	3.33334	-11.70
21	4.0	88.37	0.139	3.5	-11.46
21.5	1.45	88.33	0.139	3.58334	-12.37
22	-0.40	88.35	0.14	3.66668	-10.22
22.5	-2.9	88.33	0.139	3.85002	-10.83
23	-7.7	88.35	0.138	3.83334	-10.44
23.5	-20	88.32	0.139	3.91668	-11.16
24	-9.2	88.35	0.139	4.0	-9.56
24.5	-2.9	88.34	0.139	4.08334	-10.0
25	0.9	88.32	0.138	4.16668	-9.61
25.5	4.2	88.34	0.139	4.25002	-10.54
26	6.7	88.33	0.138	4.3334	-9.55

Table C.14. SDIV6 chip 2 single-ended input sensitivity data: $V_{cc} = 4.2V$, $V_{ref\_clk} = 2V$, $V_{ref} = 2.4V$ ($I_{ref} = 4mA$).

F_{clk} (GHz)	P_{clk} (dBm)	$I_{V_{cc}}$ (mA)	$I_{V_{ref\_clk}}$ (mA)	F_{out} (GHz)	P_{out} (dBm)
1	14.10	90.40	0.137	0.1667	-35.53
3	8.10	90.38	0.147	0.5	-27.62
6	7.10	90.31	0.140	1.0	-20.95
10	7.55	91.42	0.141	1.6667	-18.87
11	8.6	90.79	0.139	1.8334	-16.44
12	8.25	90.84	0.13	2.0	-14.14
13	8.85	90.8	0.138	2.1667	-14.32
14	9.3	90.72	0.137	2.3334	-14.02
15	8.65	91.33	0.137	2.5	-14.6
16	8.3	91.41	0.135	2.6667	-14.52
17	7.85	91.42	0.135	2.83336	-13.62
18	7.1	91.38	0.136	3.0	-13.89
19	6.0	91.37	0.137	3.16666	-13.93
20	5.7	91.32	0.136	3.33337	-13.26
21	3.15	91.49	0.135	3.5	-12.27
21.5	1.25	90.30	0.135	3.5834	-12.94
22	-1.8	91.53	0.136	3.6667	-11.90
22.5	-3.4	90.25	0.137	3.75	-11.68
23	-11.35	91.38	0.135	3.8333	-11.74
23.5	-20	90.31	0.136	3.9167	-11.99
24	-7.35	91.33	0.135	4.0	-11.06
24.5	-2.4	90.31	0.135	4.0834	-11.29
25	1.2	91.46	0.136	4.1667	-11.64
25.5	4.5	90.26	0.134	4.25	-11.41
26	6.95	91.40	0.136	4.3334	-11.25

Table C.15. SDIV6 chip 3 single-ended input sensitivity data: $V_{cc} = 4.2V$, $V_{ref\_clk} = 2V$, $V_{ref} = 2.4V$ ($I_{ref} = 4mA$).

| F_{clk}	P_{clk}	$I_{V_{cc}}$	$I_{V_{ref\_clk}}$	F_{out}	P_{out}
(GHz)	(dBm)	(mA)	(mA)	(GHz)	(dBm)
0.6	14.75	84.21	0.233	0.1	-39.09
1	14.15	83.10	0.236	0.166667	-36.35
3	7.85	83.83	0.221	0.5	-26.06
6	7.15	83.82	0.146	1.0	-20.85
10	8.55	83.63	0.142	1.66667	-17.30
11	9.15	83.67	0.140	1.83334	-16.25
12	8.8	83.65	0.140	2.0	-15.94
13	9.5	83.67	0.141	2.166667	-15.42
14	9.55	83.29	0.138	2.33332	-16.81
15	9.05	84.66	0.141	2.5	-15.52
16	8.6	84.72	0.144	2.66666	-15.54
17	8.2	84.76	0.141	2.83334	-14.55
18	7.45	84.76	0.142	3.0	-14.97
19	6.4	84.73	0.141	3.16667	-14.57
20	6.25	84.72	0.140	3.33332	-13.81
21	3.85	84.66	0.141	3.50001	-13.26
21.5	1.15	84.72	0.140	3.58334	-13.51
22	-0.75	84.69	0.140	3.66667	-12.63
22.5	-3.5	84.73	0.139	3.75001	-12.63
23	-8.5	84.68	0.140	3.83333	-12.68
23.5	-20	84.74	0.139	3.91667	-12.83
24	-8.3	84.65	0.141	4.0	-12.24
24.5	-2.4	84.76	0.139	4.08334	-12.01
25	1.15	84.62	0.139	4.16667	-12.26
25.5	4.45	84.72	0.138	4.25	-12.30
26	6.9	84.63	0.139	4.33334	-12.14

Table C.16. SDIV6 chip 1 differential input sensitivity data: $V_{cc} = 4.2V$, $V_{ref\_clk} = 2V$, $V_{ref} = 2.4V$ ($I_{ref} = 4mA$).

| F_{clk} (GHz)	P_{clk} (dBm)	$I_{V_{cc}}$ (mA)	$I_{V_{ref\_clk}}$ (mA)	F_{out} (GHz)	P_{out} (dBm)
0.6	14.5	89.07	0.218	0.1	-39.50
1	13.45	89.42	0.212	0.16667	-37.99
3	4.9	89.58	0.252	0.5	-22.93
6	4.40	89.74	0.144	1.0	-16.6
10	6.3	89.81	0.143	1.66665	-16.82
11	7.4	88.42	0.153	1.83332	-16.48
12	7.7	87.06	0.149	2.0	-16.02
13	7.9	87.53	0.14	2.16667	-13.75
14	8.15	88.46	0.146	2.3333	-14.84
15	7.6	88.85	0.145	2.5	-13.13
16	7.25	89.12	0.147	2.66666	-13.32
17	6.9	89.36	0.146	2.83332	-11.13
18	6.65	88.62	0.142	3.0	-9.86
19	5.6	88.73	0.14	3.16665	-11.27
20	5.1	88.82	0.142	3.3333 3	-9.79
21	3.2	88.85	0.141	3.5	-8.47
21.5	1.3	88.98	0.14	3.58333	-9.02
22	-0.4	89.03	0.142	3.66667	-8.58
22.5	-2.65	88.71	0.141	3.75	-8.37
23	-7.05	88.4	0.14	3.83332	-9.86
23.5	-12.45	87.72	0.139	3.91666	-8.61
24	-16.95	87.11	0.139	4.0	-7.69
24.5	-5.95	87.2	0.142	4.083337	-11.27
25	-0.7	87.79	0.139	4.16666	-11.7
25.5	3.25	88.61	0.14	4.2500008	-11.18
26	5.8	88.75	0.14	4.33332	-12.11

Appendix D

MMIC Die Photos

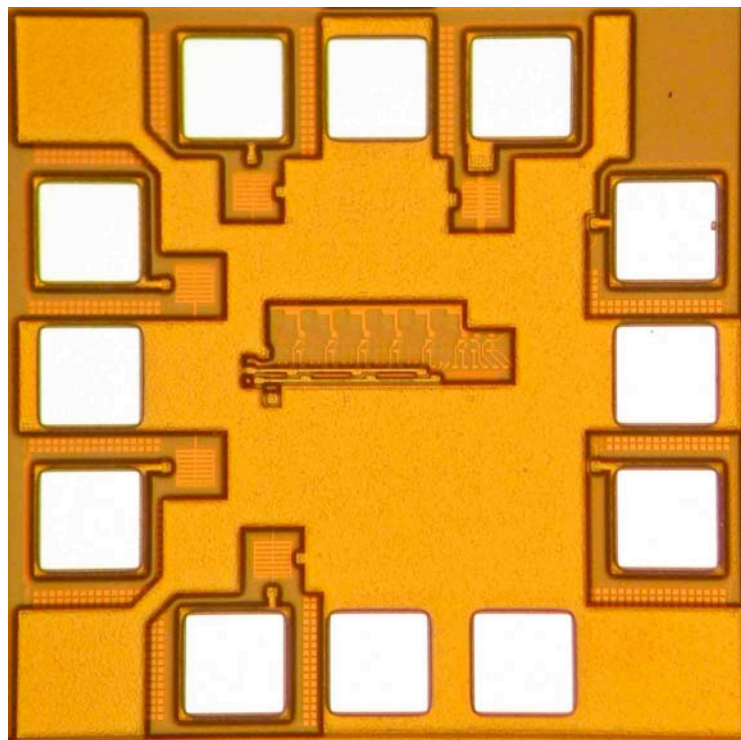This appendix contains photographs of the four fabricated MMIC dies – ET15G, ET15G_V2, XC24G and SDIV6.
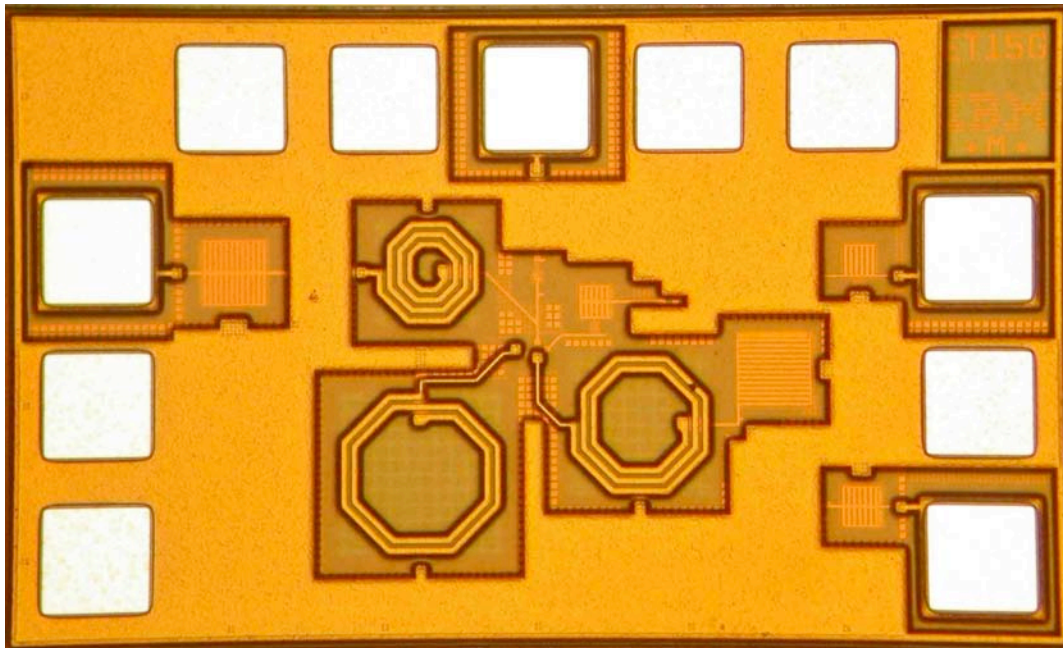
Figure D.1. ET15G 15GHz single-ended VCO die photo.
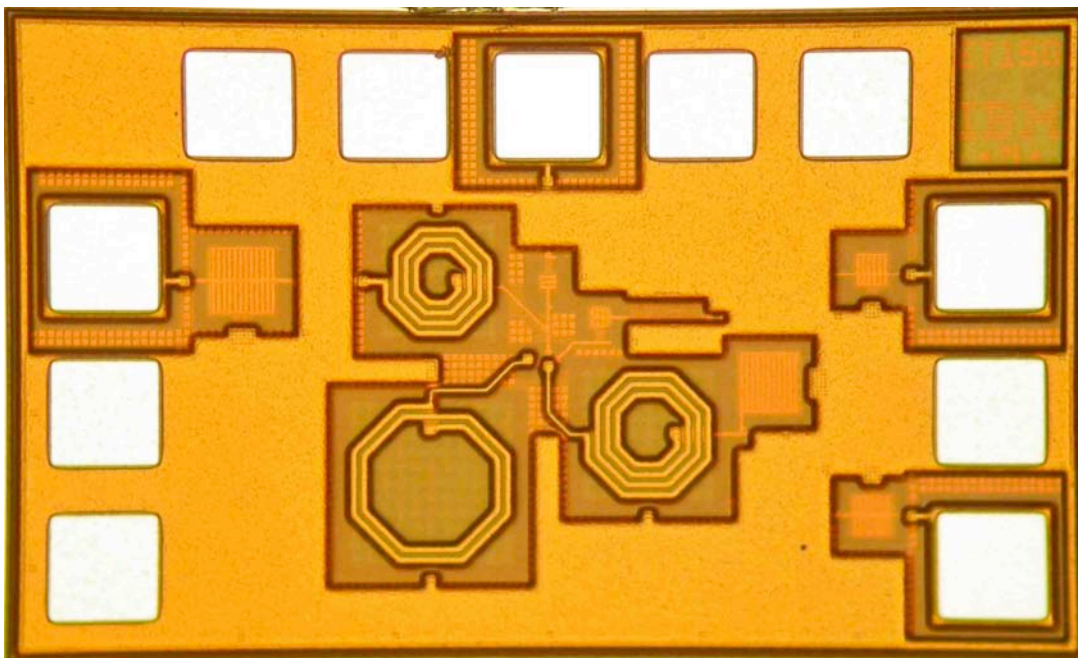
Figure D.2. ET15G_V2 15GHz single-ended VCO die photo.
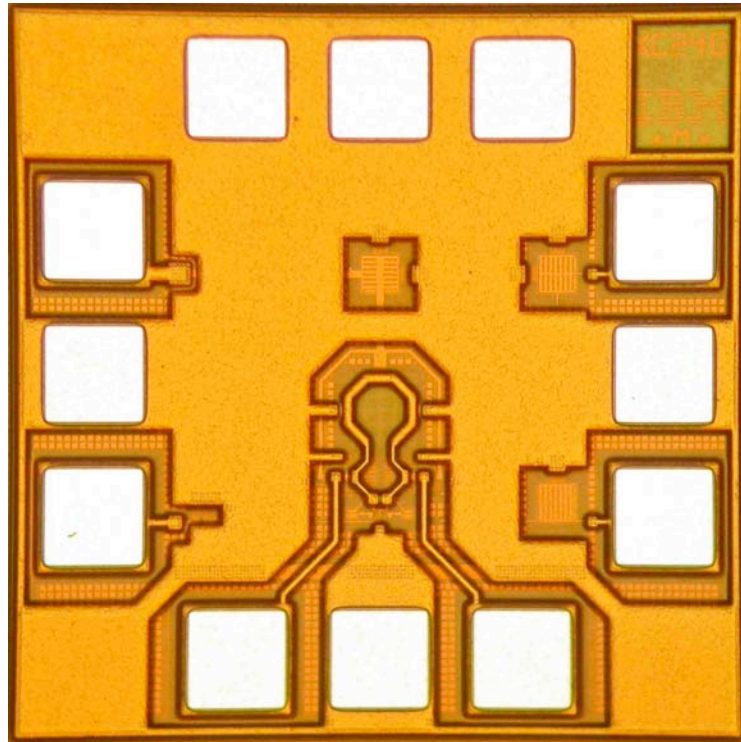
Figure D.3. XC24G 24GHz differential cross-coupled VCO die photo.

Figure D.4. SDIV6 1/6 synchronous static frequency prescaler die photo.

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