

# Chapter 1

## Introduction

This chapter introduces the research topic by delineating the technological background and motivating factors. An overview of the structure and content of the thesis is then described, including the original contributions of this work.

### 1.1 Background

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Advances in SiGe BiCMOS technology has caused a revolution in low-cost MMIC design. Until recently, III-V compound semiconductors<sup>1</sup>, namely Gallium Arsenide (GaAs) or Indium Phosphide (InP), have dominated Silicon (Si) based technologies in millimeter-wave (mm-wave) applications due to their superior electron velocity and mobility. Transistors fabricated in these materials can operate at extremely high frequencies with high gain and power, and comparatively low noise generation. However, manufacturing costs of these technologies in terms of materials and complexity are excessive in comparison to standard silicon wafer fabrication, and they do not enable efficient integration of digital logic and high-speed analog circuitry in a full System-on-Chip (SoC) approach. The relatively lossy substrate (with resistivity 1-20Ωcm compared to 1000Ωcm for GaAs [1]) and poor transistor performance in the mm-wave band renders current standard Radio Frequency (RF) Complementary Metal Oxide Semiconductor (CMOS) processes impracticable for the design of MMICs, therefore paving the way for SiGe innovation.

The addition of high-speed SiGe HBTs to commercial bulk CMOS processes has realised devices with transition frequency<sup>2</sup>,  $f_t$  up to 300GHz [2, 3]. Thus, combating the presence of the lossy silicon substrate and leveraging the economic benefits and high density SoC

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<sup>1</sup>Extrinsic semiconductors containing group II, IV or VI dopant atoms to alter electron and hole carrier concentrations at thermal equilibrium.

<sup>2</sup>Transistor unity short circuit current gain frequency.

## 1.2 Motivation

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integrability to yield an ideal technology for high volume, low-cost RF and mixed-signal applications.

The catalysts for increased interest in SiGe BiCMOS include the availability of unlicensed Industrial, Scientific and Medical (ISM) frequency bands in combination with the proliferation of high frequency devices such as mobile phones, Wireless Local Area Networks (WLANs), Bluetooth devices, UWB communications and so on. Traditional mm-wave applications in industry and military such as satellite communications, microwave point-to-point links and radar could also benefit from higher levels of integration and reduced product Bill Of Materials (BOM).

## 1.2 Motivation

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The motivation for this thesis has been sculptured not only by the potential to advance the field of low-cost SiGe MMIC design, but also by the realistic constraints of technology availability for prototype fabrication, funding, facilities, and of course, time. The material presented in this thesis is the result of a one year research scholarship to the Institute for Electronics (IfE) at the Swiss Federal Institute of Technology Zürich (ETHZ). During this time, research goals were defined by the opportunity to combine collaborative work on existing projects with the emerging field of automotive radar – specifically, the development of SiGe circuits for frequency synthesis. The two motivating themes are detailed in the following subsections.

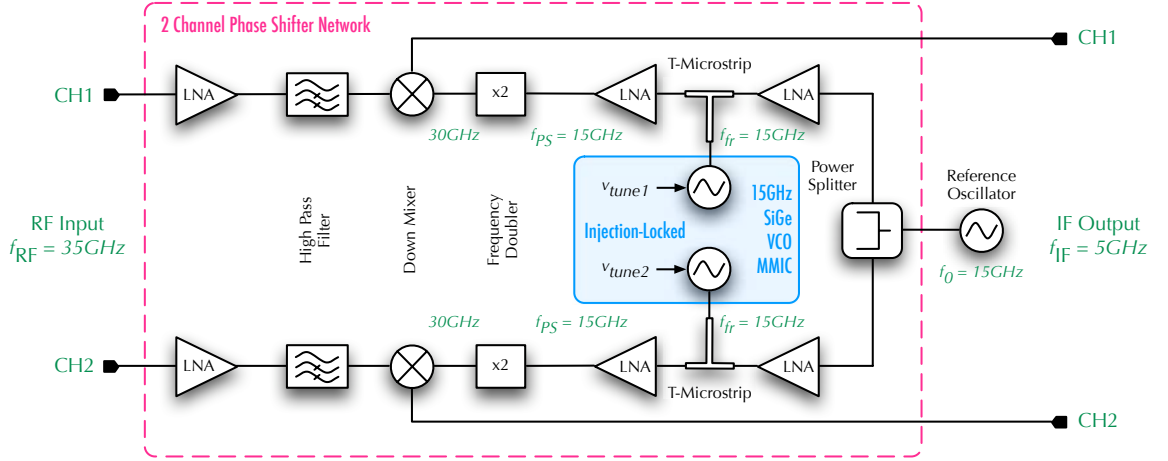
### 1.2.1 15GHz Injection-Lockable VCO

The first task was the design and fabrication of a single-ended injection lockable VCO operating at 15GHz for application in a 30GHz continuously tunable phase shifter [4]. The resultant phase shifter shall be implemented in the next revolution of the active electronic Ka-Band<sup>3</sup> antenna beam-forming network of [5], depicted in Figure 1.1. The VCO topology shall be modelled on the original topology similar to that presented in [6] and updated from the IBM SiGe BiCMOS6HP technology ( $f_t = 47\text{GHz}$ ) to the faster IBM SiGe BiCMOS7WL technology ( $f_t = 60\text{GHz}$ ).

VCO performance targets include accurate 15GHz output synthesis and optimised linear tuning range. Oscillator quality factor (Q) and phase noise are less critical since the slave injection locked VCO adopts similar performance to the high Q reference VCO signal. Thus

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<sup>3</sup>Microwave frequency band 26.5–40GHz.



**Figure 1.1.** Block diagram representation of the active electronic Ka-Band antenna beam-forming phase-shifting network based on the injection-locked local oscillators developed in this thesis.

in a locked state, the VCO signals are constant in frequency and exhibit excellent phase noise. A continuous tuning characteristic of the free-running VCO is vital as it defines the phase tuning continuity of the phase shifter.

The achievable phase shift of the injection-locked VCO relative to the reference oscillator is controlled by the tuning voltage ( $v_{tune}$ ) and can be expressed as,

$$\Delta\phi = \arcsin\left(\frac{2 \cdot (f_0 - f_{fr}(v_{tune}))}{\Delta f_{locking}}\right) \quad (1.1)$$

$$\approx \arcsin\left(\frac{(f_0 - f_{fr}(v_{tune}))}{f_0} \cdot \sqrt{\frac{P_{VCO}}{P_{inj}}} \cdot Q_{ext}\right), \quad (1.2)$$

where  $f_0$  is the reference signal frequency,  $f_{fr}$  is the free running VCO frequency,  $P_{VCO}$  is the VCO output power,  $P_{inj}$  is the injected power and  $Q_{ext}$  is the VCO external quality factor. The VCO is locked to the reference when  $f_{fr}$  is within the locking range approximated by,

$$\Delta f_{locking} = \left(\frac{2f_0}{Q_{ext}} \cdot \sqrt{\frac{P_{VCO}}{P_{inj}}}\right) \quad (1.3)$$

and resulting in the locking limits,  $f_{min,max} = f_0 \pm \Delta f_{locking}/2$ . It follows from Eq. (1.1) that a maximum phase shift of  $180^\circ$  is achievable when  $f_{fr}$  is within the locking range,  $f_{min} \leq f_{fr} \leq f_{max}$ .

### 1.2.2 24GHz Circuits for Short Range Automotive Radar

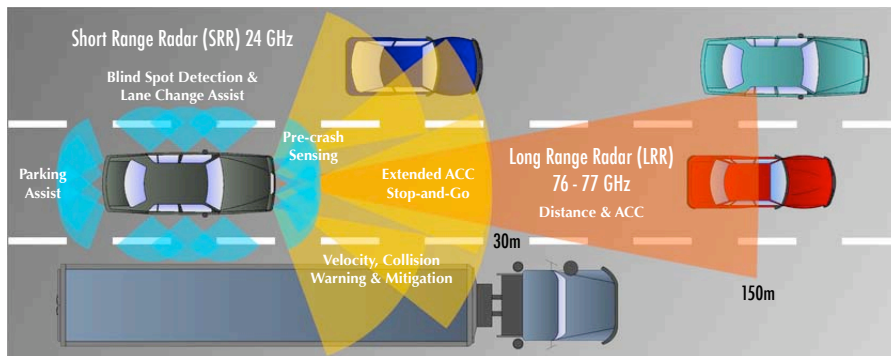
Vehicular radar has been identified as the next major step forward in intelligent comfort and safety systems to greatly reduce injury and fatality rates in road accidents. While luxury

## 1.2 Motivation

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brands such as Mercedes-Benz and BMW are now introducing such systems, the development of low-cost radar solutions, driving broad adoption of the technology into low-end automotive markets, is still in its infancy.

SiGe BiCMOS technology has been identified as the ideal marriage between performance and cost constraints for high volume automotive radar production [7, 8]. Figure 1.2 illustrates the concepts of automotive radar and its division into the facets of Long Range Radar (LLR) and SRR.

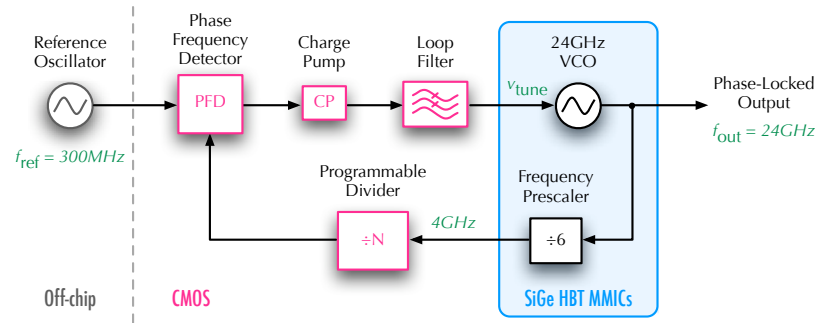


**Figure 1.2.** Application of SiGe MMIC technology to automotive radar. LLR (red) at 76-77GHz penetrates up to 150m and is used for distance measurement/warning and Autonomous Cruise Control (ACC) systems. SRR (yellow) with a range up to 30m at 24GHz perform velocity measurement, collision warning and mitigation, extending ACC to include advanced stop-and-go functionality. Additional encircling SRR sensors (blue) provide safety and comfort functions including blind spot detection, parking assist, lane change assist and pre-crash readying.

A worldwide regulation has been established for the operation of automotive LRR in the 76-77GHz band, however frequency allocation for UWB SRR has not yet reached international harmony. Despite the Federal Communications Commission's (FCC) adoption of the 24GHz UWB radar sensor approach, the European Communications Committee (ECC) has granted only temporary introduction of vehicular SRR at 24Hz, transitioning to 79GHz by 2013. The Strategic Automotive Radar frequency Allocation (SARA) Group is a consortium of automotive and component manufacturers supporting the standardised development of SRR devices in the 24GHz range and recognises the operational modes described in [9].

In this light, the second task of the thesis was the design of a 24GHz differential VCO and 1/6 frequency divider (or prescaler) in IBM 0.18 $\mu$ m SiGe BiCMOS technology, capable of extending the operational range of an existing 4GHz CMOS phase-locked loop (PLL) to 24GHz for potential SRR applications. The existing PLL was developed for UWB radio communications as part of a concurrent IfE project [10]. Figure 1.3 shows the system level

integration of the SiGe MMICs designed in this thesis, with the CMOS components of the original work to form the SRR PLL.



**Figure 1.3.** System level block diagram of the 24GHz PLL suitable for UWB automotive SRR applications. The contributions of this thesis include the 24GHz VCO and 1/6 frequency prescaler.

### 1.3 Thesis Overview and Contributions

This thesis has two distinct motivations; firstly, an active electronic Ka-band antenna beam-forming network, and secondly, 24GHz UWB automotive SRR. The common thread that defines the scope of work carried out with respect to these two topics, is the rigorous development of low-cost SiGe circuits for frequency synthesis in millimeter-wave devices.

On a practical level, this research has achieved the MMIC design, simulation, fabrication and measurement of two 15GHz single-ended injection-lockable VCOs, a 24GHz differential cross-coupled VCO and a 24GHz synchronous 1/6 static frequency divider.

The original contributions and thesis structure are organised as follows.

**Chapter 1 – Introduction** This chapter provides the topical background and research motivation including current developments, along with a summary of the structure and original contributions presented in this thesis.

**Chapter 2 – Design Theory and Process Technology** This chapter summarises the relevant theory of frequency synthesis pertaining to PLL implementation. In particular, it presents comprehensive treatment of the oscillator and frequency divider PLL subcomponents in terms of topologies, circuit analysis, and functionality. A system level view of phase noise mechanisms and models is also given. Finally, attributes of the IBM SiGe technology used for MMIC prototyping are discussed.

**Chapter 3 – 15GHz Oscillator Implementations** This chapter documents the rigorous design, layout and simulation of four potential 15GHz single-ended SiGe VCOs for future

implementation in the 30GHz continuous tunable phase shifter described in [4]. Two separate topologies; the emitter-tuned (E-tuned) and base-tuned (B-tuned) are investigated, and their performance characteristics compared.

The main contribution of this chapter is the application of negative resistance theory to the analytical design of single-ended SiGe VCOs at 15GHz.

**Chapter 4 – 24GHz Oscillator Implementation** This chapter documents the rigorous design, layout and simulation of a 24GHz differential cross-coupled SiGe VCO suitable for frequency synthesis applications in UWB automotive SRR systems. The effects of process variation and device mismatch on critical performance metrics and fabrication yield are also investigated through Monte Carlo simulation.

The main contributions of this chapter are the application of negative resistance theory to the analytical design of differential cross-coupled SiGe VCOs at 24GHz and the investigation of the effects of wafer manufacturing variations on VCO performance – a necessary aspect of commercial, high volume MMIC design almost always neglected in the literature.

**Chapter 5 – Frequency Prescaler Implementation** This chapter documents the rigorous design, layout and simulation of a synchronous SiGe Emitter Coupled Logic (ECL) based static 1/6 frequency divider operating at 24GHz, suitable for frequency synthesis applications in UWB automotive SRR systems. The effects of process variation and device mismatch on critical divider performance metrics are again investigated through Monte Carlo simulation.

The main contributions of this chapter are the successful implementation of a multi-stage synchronous static frequency divider topology at 24GHz in a SiGe technology with moderate  $f_t = 60\text{GHz}$ , for minimal PLL phase noise contribution – a design approach yet to be explored in the literature, and the investigation of the effects of wafer manufacturing variations on divider performance – a necessary aspect of commercial, high volume MMIC design almost always neglected in the literature.

**Chapter 6 – MMIC Fabrication and Measurement** This chapter reports the on-wafer measurement methodology and results for the four fabricated MMICs. VCO measurements include output time domain waveforms, frequency spectra, frequency and power characteristics over tuning range and phase noise using a single-ended test setup. Frequency divider measurements include self oscillation and divided output spectrum, input sensitivity, power output and DC power consumption, obtained using both single-ended and differential test setups. The measured results are also compared against analog extracted post-layout schematic simulations and the current state-of-the-art.

The main contribution of this chapter is the use of both single-ended and differential measurement techniques to confirm the accuracy of frequency divider performance characteristics – typically only single-ended measurement techniques are used to assess the performance of differential circuits in the literature.

**Chapter 7 – Conclusion** This chapter summarises the principle outcomes of the thesis and advises areas of future research.

**Appendix A – Schematics** This appendix contains the final optimised circuit schematics of the MMICs designed and simulated in Chapters 3, 4 and 5.

**Appendix B – SDIV6 Layout Cell Views** This appendix contains additional layout cell views of the frequency prescaler core, ECL Data-latch (D-latch), Data Flip-Flop (DFF) and emitter-follower (EF) output buffer designed in Chapter 5.

**Appendix C – Measurement Data** This appendix contains the manually recorded on-wafer measurement data presented in Chapter 6.

**Appendix D – MMIC Die Photos** This appendix contains photographs of the four fabricated MMIC dies.





# Chapter 2

## Design Theory and Process Technology

This chapter presents theoretical analyses of frequency synthesis pertaining to PLL implementation and the two building blocks designed in this thesis – the VCO and frequency prescaler. Common mm-wave circuit topologies are explored and the attributes which have influenced system design choices presented in later chapters. A system level view and VCO specific discussion on phase noise mechanisms and models is also given. The chapter then closes with an overview of the relevant characteristics of the IBM SiGe BiCMOS process technology used for MMIC fabrication.

### 2.1 PLL Frequency Synthesis

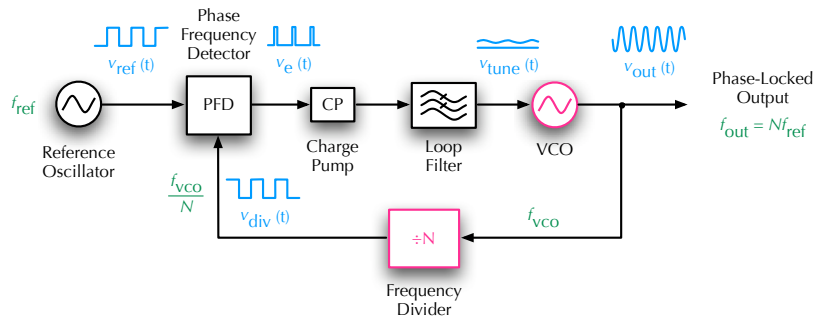
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Frequency synthesisers are essential components in RF systems, providing precisely controlled sources for frequency conversion and continuous or pulsed carrier generation. Modern wireless system synthesisers demand frequency stability, low noise performance and sufficiently wide tuning range to accurately access the designated frequency bands in multichannel communication or radar standards. Phase-locked loops are often used for this purpose.

PLLs incorporate feedback control to allow a voltage controlled oscillator to accurately track the phase of a stable reference oscillator and generate a periodic output at a multiple of the reference source. The integer-N PLL block diagram of Figure 2.1 represents the indirect frequency synthesis method and indicates the signals presented to each sub-circuit.

The PLL ensures accurate local oscillator (LO) synthesis by tuning the VCO proportional to the phase error between the divided VCO output,  $v_{div}(t)$ , and a stable reference signal,  $v_{ref}(t)$ . The charge pump (CP) and low-pass filter (LPF) translate the phase difference pulse

## 2.2 Oscillator Analysis



**Figure 2.1.** Integer-N PLL block diagram, indicating the feedback frequency control mechanism used to achieve phase-lock to a high quality reference oscillator.

train signal,  $v_e(t)$ , from the phase frequency detector (PFD) into a tuning voltage,  $v_{tune}(t)$ , which alters the capacitance of the VCO resonant tank and hence its centre frequency to achieve the locked state. The loop filter also controls the dynamic properties of the PLL frequency response including; modulation bandwidth, rise time, overshoot and stability.

There are three characteristics of PLLs that are of particular importance in practical systems.

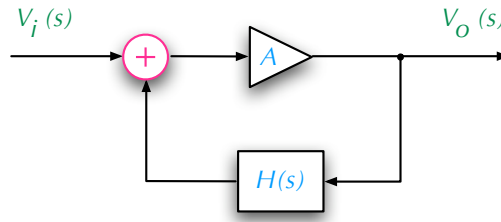
1. Capture range is the range of input frequency for which the loop can achieve lock.
2. Lock range is the input frequency range over which the loop will remain locked – usually larger than the capture range.
3. Settling time is the time taken for the loop to lock onto a new frequency – changing between multiple frequency channels for instance.

The phase noise characteristic of a PLL is similar to that of the reference source and influenced by the phase noise and spurious behaviour of the VCO.

## 2.2 Oscillator Analysis

### 2.2.1 Linear Feedback Analysis

At the most fundamental level, an electrical oscillator relies on circuit nonlinearity and the presence of noise to generate a periodic output voltage or AC waveform from DC power. The circuits are designed to be both unstable, which is generally achieved through feedback, and self-sustaining. The operation of an oscillator can be described by the linear feedback circuit of Figure 2.2. The output voltage<sup>4</sup> of this positive feedback system can be expressed as



**Figure 2.2.** Sinusoidal oscillator linear feedback model.

$$V_o(s) = AV_i(s) + H(s)AV_o(s), \quad (2.1)$$

where  $A$  is the amplifier voltage gain and  $H(s)$  is a frequency dependent feedback network. Further manipulation yields the overall closed loop transfer function

$$\frac{V_o(s)}{V_i(s)} = \frac{A}{1 - AH(s)}. \quad (2.2)$$

A self-sustaining mechanism arises when the denominator of Eq. (2.2) becomes zero,  $H(s_0) = +1$  at a particular frequency  $s_0$ . To produce constant amplitude at the output  $s_0$  must be purely imaginary,  $H(s_0 = j\omega_0) = +1$ . These conditions for steady state oscillation must be simultaneously met and are known as the Nyquist or Barkhausen criterion:

1. The loop gain,  $H(j\omega_0)$ , must equal unity and,
2. The total phase shift around the positive feedback loop,  $\angle H(j\omega_0)$  must be equal to zero or a multiple of  $360^\circ$ .

In most RF oscillators the feedback network consists of an LC tank (or resonant tank), the most commonly recognised being Hartley, Colpitts, Clapp and Pierce circuits. The sharpness of an oscillators output frequency response is significantly influenced by the quality factor of the LC tank while the component values determine the operation frequency. Therefore, the design of the feedback network is critical for narrowband operation.

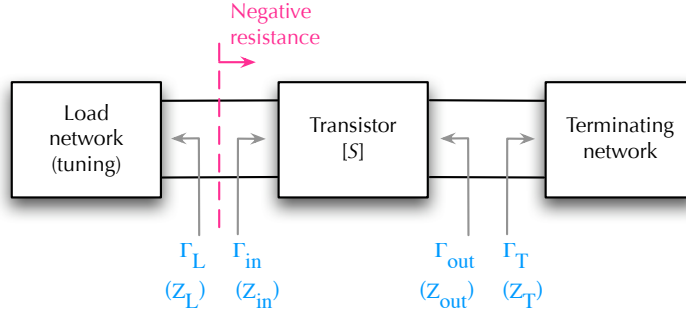
### 2.2.2 Negative Resistance ( $-g_m$ ) Oscillators

Most of today's integrated RF oscillators fall into the category of negative resistance oscillators. They incorporate as few active devices (Bipolar Junction Transistor (BJT), Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or IMPact ionisation Avalanche

<sup>4</sup>Note – although voltage is used in the explanation of the linear feedback model, the analysis is equally valid for current, waves, etc.

## 2.2 Oscillator Analysis

Transit-Time (IMPATT) diode) as possible to minimise noise and passive resonators using transmission line elements or lumped LC devices. A transistor oscillator can be viewed as a one-port negative resistance network by terminating the potentially unstable transistor with an impedance,  $Z_T$  designed to force the device into its unstable region. Consider the transistor circuit of Figure 2.3 where  $Z_{in} = R_{in} + jX_{in}$  is the current (or voltage) and frequency dependent input impedance of the transistor. The passive load impedance  $Z_L = R_L + jX_L$



**Figure 2.3.** Two-port negative resistance transistor oscillator circuit structure, indicating the reflection coefficients and associated impedances looking into each connection interface.

is chosen to match  $Z_{in}$  so that applying Kirchoff's voltage law to the one-port equivalent results in

$$(Z_L + Z_{in})I = 0. \quad (2.3)$$

When oscillation occurs,  $I$  is nonzero which implies the following conditions:

$$R_L + R_{in} = 0 \quad (2.4)$$

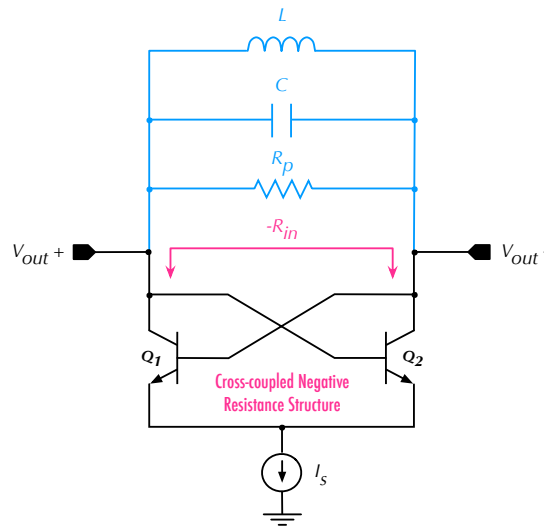
$$X_L + X_{in} = 0. \quad (2.5)$$

Eq. (2.5) sets the oscillation frequency while Eq. (2.4) implies  $R_{in} < 0$  since the load is passive,  $R_L > 0$ . A positive resistance means energy dissipation whereas a negative resistance implies an energy source. From Eq. (2.3), for steady state oscillation  $Z_L = -Z_{in}$ , which in terms of the reflection coefficients  $\Gamma_L$  and  $\Gamma_{in}$  can be expressed as

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{-Z_{in} - Z_0}{-Z_{in} + Z_0} = \frac{Z_{in} + Z_0}{Z_{in} - Z_0} = \frac{1}{\Gamma_{in}}. \quad (2.6)$$

Thus, the reflection coefficient theory  $\Gamma_L \Gamma_{in} = 1$  is an instance of the linear feedback analysis in which  $\Gamma_L = H(s)$  and  $\Gamma_{in} = A$ . For oscillations to occur at the intended frequency  $f_0$ , the transistor must have sufficient negative resistance such that  $R_{in}(f_0) + R_L < 0$ . The presence of noise or power supply transients will then cause oscillation to build up. As the current increases,  $R_{in}$  must become less negative until a point where  $R_{in} + R_L = 0$  and a stable oscillatory state is reached at  $f_0$ .

There are numerous possible RF oscillator circuits utilising the transconductance ( $g_m$ ) of bipolar or field-effect transistors to generate negative resistance in conjunction with different resonant networks. The cross-coupled pair of Figure 2.4 is an example of a negative resistance BJT based oscillator where the impedance seen at the collector of  $Q_1$  and  $Q_2$  is calculated as  $R_{in} = -2/g_m$  [11]. Therefore, if  $R_{in}$  is greater than or equal to the equivalent parallel resistance  $R_p$  of the tank, the circuit oscillates.



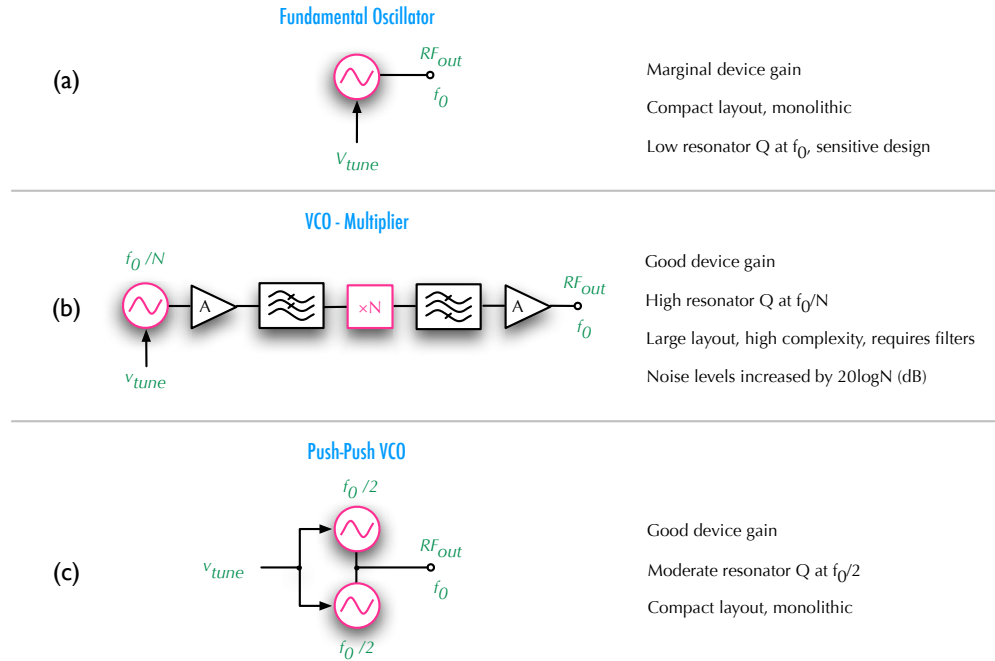
**Figure 2.4.** Cross-coupled pair differential oscillator indicating the generation of negative input resistance.

Oscillator frequency control can be achieved by changing the inductance or capacitance of the tank circuit or by varying the bias currents for transistor oscillators which alters the contribution of device parasitic impedance to the LC network. The latter approach, however, results in output voltage amplitude changes as tuning is performed – an undesired outcome. While it is possible to get tunable discrete inductors, voltage-controlled capacitors (varactors) are the only feasible tuning device for integrated circuits. A varactor is a diode (or diode connected BJT/MOSFET) whose junction capacitance can be controlled by the DC reverse bias voltage applied across the device. Generally varactors appear either in series or parallel with a capacitor in the feedback network to offer a fine tuning range about the natural resonant frequency. As the DC bias is varied the oscillator centre frequency shifts in response, hence the term, voltage-controlled oscillator. The capacitance range of the varactors dictates the available tuning range of the oscillator.

## 2.2 Oscillator Analysis

### 2.2.3 Microwave Oscillator Designs

There are currently three main approaches to MMIC oscillator design at mm-wave frequencies. The topological block diagrams are shown in Figure 2.5 along with their basic implementation characteristics. Fundamental VCOs simply generate an output at the desired frequency, how-



**Figure 2.5.** The three basic mm-wave VCO implementations: (a) fundamental oscillators directly generate the desired output frequency, (b) VCO-multipliers isolate higher order harmonics from a lower fundamental VCO frequency, and (c) push-push VCOs add second harmonics of lower odd mode VCO frequencies.

ever they are only feasible if the device technology has sufficient gain at that frequency. Until recently, silicon based integrated technologies have not presented enough gain at microwave frequencies.

VCO-multipliers incorporate a VCO designed to operate at a more modest frequency  $f_0/N$  (typically  $f_0/2$  or  $f_0/3$ ) and employ a frequency multiplier to convert the signal to the millimeter-wave realm. While active device gain and resonator Q are much better at the lower centre frequency, the additional circuitry required to isolate the desired higher order harmonic increases complexity, chip area and output noise levels.

Push-push VCO designs consist of two fundamental frequency oscillators operating at  $f_0/2$  in odd mode so that the fundamental frequencies add out of phase, cancelling, and the second harmonics add in phase, thus producing the required output. The performance of this

topology is heavily reliant on the anti-phase accuracy of both oscillators and therefore layout symmetry and device matching are paramount.

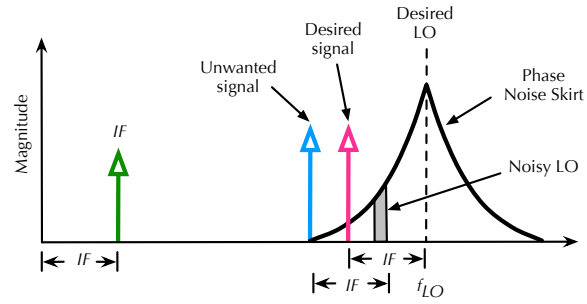
## 2.3 Phase Noise

Oscillator circuits are susceptible to noise just like all analog circuits. However, the amount of noise produced by a frequency synthesiser or oscillator is critically important in practice because it can seriously degrade the performance of a wireless system.

### 2.3.1 System Level View

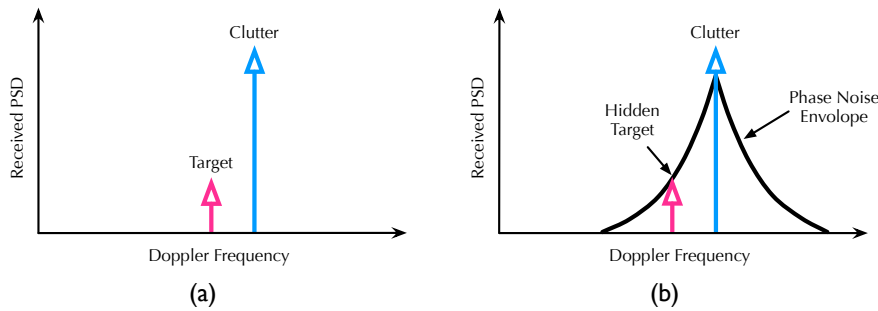
Noise injected via the oscillators constituent devices (active and passive) or by external means may influence both the centre frequency and the amplitude of the output signal. Amplitude changes can, in general, be neglected because there exists circuit techniques for eliminating such disturbances. The short-term random deviation of frequency can be alternatively viewed as random variation of the period or deviation of the zero crossing points of the output waveform from its ideal position along the time axis. This phenomenon is more commonly known as phase noise in the analog design world or jitter in the digital design world and has more serious implications than amplitude inaccuracies.

Phase noise not only adds to the overall noise level (minimum synthesiser output noise floor) but in digital systems, clock jitter directly affects timing margins of logic circuits hence limiting system speed. In analog RF systems, a generic transceiver for instance, phase noise in the LO leads to corruption of both the downconverted and upconverted signals by translating undesired nearby signals to the frequency of interest, thus limiting detection sensitivity, selectivity, channel bandwidth and output purity of the transceiver. Modern digital modulation schemes such as Phase Shift Keying (PSK) and Quadrature Amplitude Modulation (QAM) used in WLAN systems are particularly affected by the presence of phase noise, introducing uncertainty during signal detection and degrading the Bit Error Rate (BER). Figure 2.6 illustrates how phase noise effects the selectivity of a receiver by down-converting signals adjacent to the desired signal frequency. The figure assumes a heterodyne architecture with LO at  $f_{LO}$  to translate the desired signal to an intermediate frequency (IF). Unfortunately, a nearby unwanted signal can be down converted to the same IF due to the LO's phase noise spectrum. The portion of phase noise spectrum leading to this conversion is situated at an offset from the carrier equal to the IF from the unwanted signal – a process known as reciprocal mixing. Essentially resulting in spectral overlapping and significant degradation of the wanted signal.



**Figure 2.6.** Illustration of how LO phase noise can lead to the reception of an undesired signal close to the frequency of the desired signal in a heterodyne receiver architecture.

In terms of radar systems, internally generated phase noise degrades sensitivity and target detection performance. The presence of phase noise sidebands around the carrier and hence the reflected signal (or echo) spectrum from large returns such as clutter<sup>5</sup> can completely obscure the echo from smaller targets in close proximity. This potentially makes the smaller target indistinguishable from the received noise, as illustrated in Figure 2.7. The measure of



**Figure 2.7.** Receiver power spectral density (PSD) of (a) an ideal radar exhibiting no phase noise where the target and clutter can be differentiated by their Doppler frequencies, and (b) a radar with phase noise where the target is rendered indiscernible from the broadened clutter spectrum.

a radar's ability to discern moving target signals superimposed on clutter signals is known as Sub-Clutter Visibility (SCV). The extent of clutter spread is dependent on the level of the clutter signal, the radar's phase noise characteristic and the target range [12].

The specific effects of phase noise on radar performance depends on the type of radar implemented, for example Frequency Modulated Continuous Wave (FMCW), pulsed, UWB and so on. [13, 14] have studied the effects of transmitter phase noise on FMCW based radar and identify a broadening of the clutter velocity spectrum, increased velocity and range measurement errors and reduced SCV.

<sup>5</sup>Unwanted radar reflections from ground, sea, atmospheric conditions, urban objects, jamming etc.



In Doppler radar systems, frequency shifts in the reflected signal are used to determine the velocity of moving objects. As such, small Doppler frequency shifts from slow moving targets close to the carrier signal demand a high level of close-in carrier phase noise purity to be detectable. The phase noise requirements become more relaxed as the target speed and proximity to the carrier increase due to the larger Doppler frequency shifts.

### 2.3.2 Phase Noise Mechanisms

The characterisation of phase and frequency fluctuations in electrical oscillator circuits has been the subject of many detailed studies in recent times [15, 16, 17, 18, 19, 20]. Complex mathematical models have been presented, however they are often only applicable to specific classes of oscillators because of the simplifications assumed. Modern Computer Aided Design (CAD) tools can simulate the presence of phase noise however they rely on the accuracy of the available design kit device models and still have limited ability to model the nonlinear nature of oscillator noise sources. Nevertheless, phase noise in oscillators is spawned from noise sources divided into two main categories – device noise and interference. Device noise encompasses thermal, shot and flicker noise (or  $1/f$  noise) along with the  $Q$  of resonant devices. Interference on the other hand arises from substrate noise (LO leakage, self mixing, nonlinear device harmonic components, etc.) and supply noise.

The output of an ideal sinusoidal oscillator can be expressed as,

$$v_o(t) = A \cos[\omega_{LO}t + \phi], \quad (2.7)$$

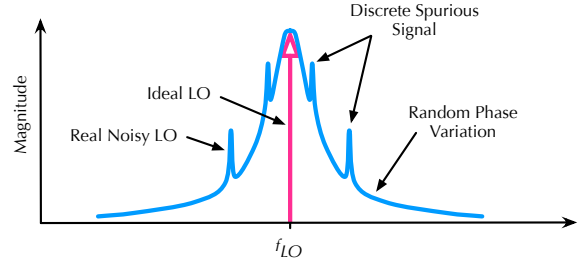
where  $A$  is the amplitude,  $\omega_{LO}$  ( $= 2\pi f_{LO}$ ) is the frequency, and  $\phi$  is the fixed phase of the signal. The frequency spectrum of such a signal would consist of a pair of Dirac delta functions<sup>6</sup> (impulses) at  $\pm f_{LO}$ , as shown only in the positive frequency region in Figure 2.8. In reality, however, the output voltage of a typical oscillator or frequency synthesiser is more accurately defined as

$$v_o(t) = V_o[1 + A(t)] \cos[\omega_{LO}t + \phi(t)], \quad (2.8)$$

where  $A(t)$  represents the amplitude fluctuations of the output, and  $\phi(t)$  represents the phase variation of the output waveform. A consequence of the time varying amplitude and phase is the addition of sidebands in the oscillators output spectrum around the centre frequency,  $f_{LO}$ . This effect is also shown in Figure 2.8. The discrete spikes represent spurious signals due to oscillator harmonics or mixer products. Phase noise due to random fluctuations caused by device noise and interference appear as a broad continuous distribution localised about the output signal.

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<sup>6</sup>A function  $\delta(x)$  that equals infinity at one value of  $x$  and zero elsewhere.



**Figure 2.8.** Frequency spectrum of an ideal oscillator consisting of a delta function at the operating frequency  $f_{LO}$  and a practical oscillator indicating the presence of spurious noise frequency peaks and noise sidebands around the operating frequency.

Phase noise is defined as the ratio of power in one phase modulation sideband to the total signal power per unit bandwidth (1Hz) at a given offset,  $\Delta\omega$  from the signal frequency. This leads to the general definition for single-sideband phase noise spectral density, denoted as  $\mathcal{L}(\Delta\omega)$ ,

$$\mathcal{L}(\Delta\omega) = 10 \log \left[ \frac{P_{sideband}(\omega_{LO} + \Delta\omega, 1Hz)}{P_{carrier}} \right]. \quad (2.9)$$

This definition includes the effect of both amplitude and phase fluctuations and has units of decibels relative to the carrier power per Hertz, dBc/Hz.

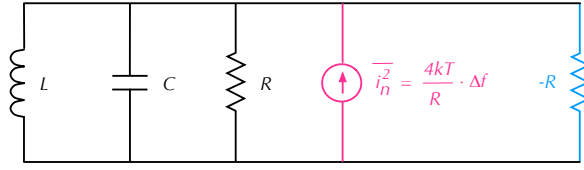
The advantage of this figure-of-merit (FOM) is its ease of measurement, however since it indicates the cumulative effect of both amplitude and phase noise it does not provide information about the severity of each noise source separately. Knowing the specific contributions of amplitude and phase variations greatly benefits the designer in devising noise reduction mechanisms.

### Leeson's Oscillator Phase Noise Model

One of the classical oscillator phase noise models on which many of the new theories are based is the linear time invariant (LTI) model described by Leeson. Leeson's model approximates the noise power spectral density of tuned tank oscillators, assuming that the oscillator is a linear positive feedback system as previously discussed in Section 2.2.1.

Initially, consider the oscillator system as a ideal oscillator with the only noise contribution coming from the lossy tank, as shown in Figure 2.9. The tank resistance has to be compensated by the active device generating negative resistance  $-R$ . The noise current source associated with this lossy tank conductance can be expressed by the mean-square value,

$$\overline{i_n^2} = S_n(f) \cdot \Delta f = \frac{4kT}{R} \cdot \Delta f \quad (2.10)$$



**Figure 2.9.** Oscillator noise model with LC resonant tank, loss resistance, associated noise current source and active device generating negative resistance.

where  $S_n(f)$  represents the noise spectral density,  $k$  is Boltzmann's constant ( $1.38 \times 10^{-23}$  Joules/Kelvin),  $T$  is the temperature and  $R$  is the tank resistance. This noise current source converts to a voltage noise source when multiplied by the effective tank impedance. During oscillation the unstable active device will generate sufficient negative resistance to exactly cancel the positive resistance of the tank. Therefore, the effective impedance seen by the noise current source is that of a perfectly lossless parallel LC network that can be approximated for small offset frequency  $\Delta\omega$  from the centre frequency as,

$$Z(\omega_{LO} + \Delta\omega) \approx j \cdot \frac{\omega_{LO} L}{2 \frac{\Delta\omega}{\omega_{LO}}} \quad (2.11)$$

provided that  $\Delta\omega \ll \omega_{LO}$ . This expression can be rewritten incorporating the unloaded tank quality factor,

$$Q = \frac{R}{\omega_{LO} L} = \frac{1}{\omega_{LO} G L}, \quad (2.12)$$

revealing the magnitude of the tank impedance as,

$$Z(\omega_{LO} + \Delta\omega) = \frac{1}{G} \cdot \frac{\omega_{LO}}{2Q\Delta\omega}. \quad (2.13)$$

The spectral density of the mean-square noise voltage can then be determined by multiplying the spectral density of the mean-square noise current by the squared magnitude of the tank impedance,

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot Z^2 = 4kTR \left( \frac{\omega_{LO}}{2Q\Delta\omega} \right)^2. \quad (2.14)$$

Note that increasing resonator  $Q$  reduces the noise density and that the output noise power spectral density falls as the inverse-square of the offset frequency.

Normalising the mean-square noise voltage density of Eq. (2.14) to the mean-square oscillator voltage and representing the result as a ratio in decibels gives the following equation for the normalised single-sideband noise spectral density,

$$\mathcal{L}(\Delta\omega) = 10 \log \left[ \frac{2kT}{P_{LO}} \cdot \left( \frac{\omega_{LO}}{2Q\Delta\omega} \right)^2 \right]. \quad (2.15)$$

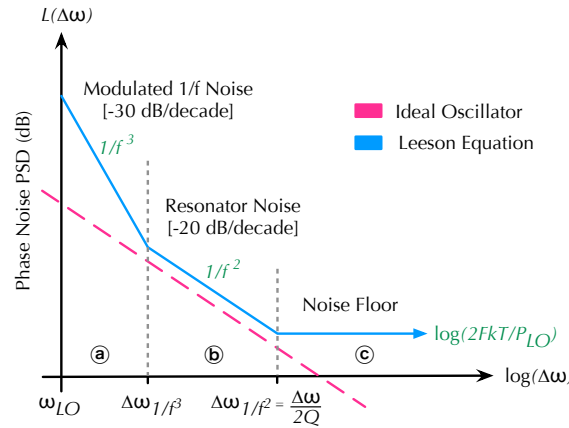
## 2.3 Phase Noise

The above equation allows us to draw some important conclusions about the RLC resonant tank of an ideal oscillator; improving tank  $Q$  and increasing the LO signal power are essential for low phase noise design. According to Leeson, this expression alone is insufficient for describing the complete phase noise spectrum of an oscillator, however it does represent the region proportional to  $1/f^2$  shown graphically in Figure 2.10 with a theoretical slope of -20 dB/decade.

Now considering additive flicker ( $1/f$ ) and thermal noise from the active devices within the oscillator core or associated buffer amplifiers, the phase noise expression (referred to as Leeson's equation) becomes,

$$\mathcal{L}(\Delta\omega) = 10 \log \left[ \frac{2FkT}{P_{LO}} \cdot \left( 1 + \left( \frac{\omega_{LO}}{2Q\Delta\omega} \right)^2 \right) \cdot \left( 1 + \frac{\Delta\omega_{1/f^3}}{\Delta\omega} \right) \right] \quad (2.16)$$

where  $P_{LO}$  is the oscillator output power,  $\Delta\omega$  is the LO offset frequency,  $Q$  is the loaded quality factor of the tank and  $\omega_{LO}$  is the LO frequency.  $F$  is an empirical fitting parameter (often referred to as the device noise factor) determined from measurements and accounts for the increased noise in the  $1/f^2$  region when compared to that predicted by the ideal oscillator assumption. The parameter  $\Delta\omega_{1/f^3}$  is the boundary between the  $1/f^2$  and  $1/f^3$  regions and is equal to the  $1/f$  corner of the active device noise. At around the resonator 3dB bandwidth



**Figure 2.10.** Leeson's LTI oscillator phase noise model predicting three typical regions relative to the centre frequency  $\omega_{LO}$  on a logarithmic scale: (a) Additive  $1/f$  active device noise contribution. (b) Passive resonant tank generated noise. (c) Thermal noise floor of resistive oscillator losses.

$\Delta\omega/2Q$  offset from the LO centre frequency, the phase noise spectrum flattens off revealing the spectral noise floor.

The Leeson model provides a realistic interpretation of the generalised oscillator phase noise spectrum, however it relies heavily on the measured fitting parameters and therefore has

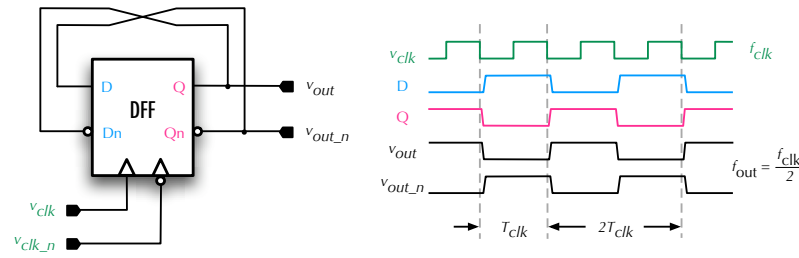
limited predictive power. Nevertheless, several insights can be gained from Leeson's equation into phase noise reduction techniques including; maximising LO power or equivalently the output voltage swing, maximising resonator  $Q$  and utilising active devices with low  $1/f$  flicker noise to reduce the close-in phase noise component and noise floor.

## 2.4 Frequency Dividers

There are essentially two types of mm-wave frequency divider topologies prevalent in the literature and suitable for MMIC PLL implementation – the static and the dynamic.

### 2.4.1 Static Divider

Static frequency dividers are based on the conventional Data Flip-Flop topology with negative feedback as shown in Figure 2.11, including switching signal waveforms. The differential



**Figure 2.11.** Block diagram of the DFF based 1/2 static frequency divider element and principle of operation waveforms.

input signal is applied to the clock ports of the DFF while the negative feedback mechanism produces an output at  $f_{out} = f_{clk}/2$ , provided that the propagation delay through the DFF and feedback wiring is less than the input period,  $T_{clk}$ .

The DFFs are constructed from two master-slave connected Data-latches operating on opposite clock phases. The D-latches are typically designed using fully differential ECL [21, 22, 23] or double emitter-coupled logic (E<sup>2</sup>CL) [24, 25, 26], in bipolar transistor implementations. The difference being that E<sup>2</sup>CL has a second level of emitter-followers at the output of the D-latch to increase switching speed and provide additional level shifting, at the expense of increased power consumption and higher supply voltage requirements. Inductive peaking can also be introduced in the latch resistor loads to improve switching speeds however this significantly increases chip area.

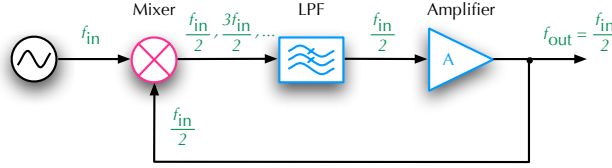
The lower operational frequency limit for static dividers is usually restricted by the slew rate of the input clock signal, while the upper limit is defined by the maximum propagation delay

## 2.4 Frequency Dividers

through each of the DFFs and associated wiring. As such, static dividers typically have broader operational frequency ranges compared to dynamic topologies.

### 2.4.2 Dynamic Divider

Dynamic frequency dividers on the other hand, work on the principle of regenerative frequency division shown in Figure 2.12. The design involves applying the input signal to a mixer,



**Figure 2.12.** System level diagram of the dynamic regenerative divider mechanism.

reproducing the fundamental signal along with a signal at half its frequency. A low-pass filter then removes the fundamental frequency while a feedback mechanism injects the half frequency signal back into the mixer. The output frequency is therefore  $f_{out} = f_{in}/2$ . The feedback loop frequency response dictates the maximum divider operating frequency, where at high frequencies the loop gain is insufficient to sustain operation. The minimum operating frequency limit occurs when the low-pass filter can no longer suppress the  $3f_{in}/2$  harmonic component [27].

Common MMIC dynamic divider implementations [28, 25] utilise double balanced active mixers such as the Gilbert cell mixer, in which case low-pass filtering and amplification are unnecessary due to the low-pass frequency response of the mixer gain.

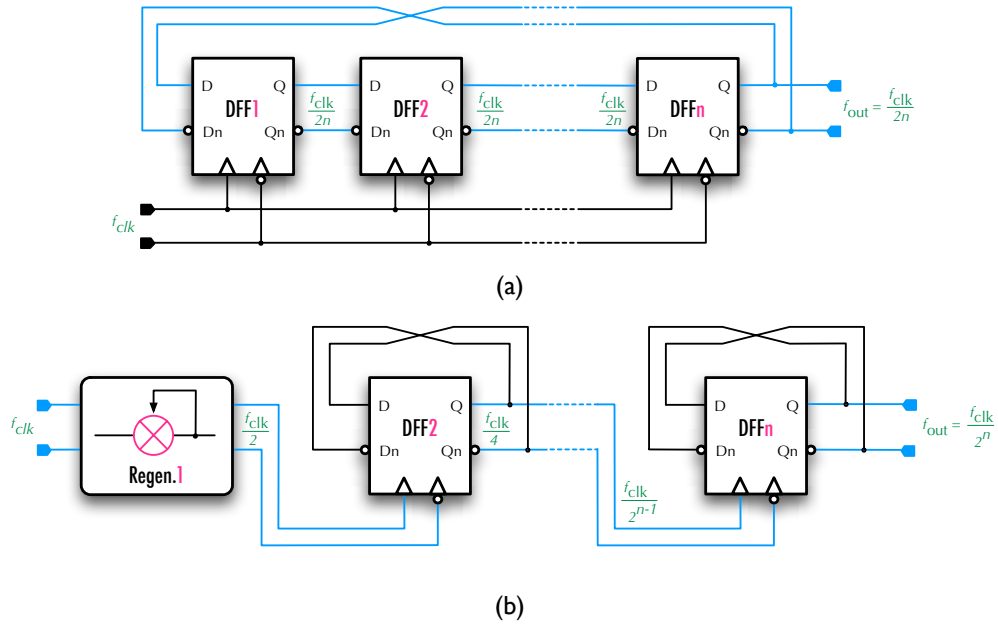
In comparison, dynamic divider circuits are faster and consume less power than static dividers [29]. However at the more modest frequency of 24GHz compared to those reported, both static and dynamic dividers should be realisable.

### 2.4.3 Higher Order Division

Higher order frequency division ratios can be achieved both synchronously or asynchronously.

Synchronous higher order division can only be achieved using multiple static DFF divider stages in a chain with negative feedback from the final stage to the first, as shown in Figure 2.13(a). Assuming  $n$ -stages, the output frequency of a synchronous divider chain is defined by the expression,

$$f_{out} = \frac{f_{clk}}{2^n}. \quad (2.17)$$



**Figure 2.13.** Block diagram representation of (a) synchronous and (b) asynchronous divider topologies.

Each DFF stage is clocked at the high input signal frequency, placing high driving capability requirements on the input source and tight timing requirements on the DFFs and associated layout wiring delays. This also results in high power consumption compared to asynchronous designs. Propagation delays and hence clock jitter do not accumulate in synchronous dividers since the output of each DFF stage is simply a time shifted version of the divided output signal with identical frequency. The synchronous divider topology possesses similar broadband operation to the static 1/2 divider element, therefore making it suited to PLL implementation where phase noise minimisation and broad band operation are critical. Assuming however, that sufficiently fast ECL logic can be achieved with the available fabrication technology.

Asynchronous higher order division can be achieved using any combination of cascaded static or dynamic 1/2 divider stages as illustrated in Figure 2.13(b). Assuming  $n$ -stages, the output frequency of an asynchronous divider is defined by,

$$f_{out} = \frac{f_{clk}}{2^n}. \quad (2.18)$$

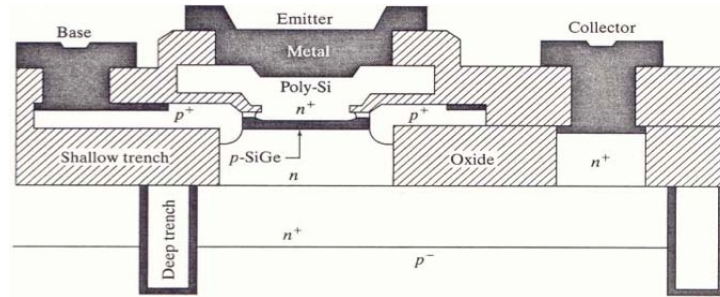
In the asynchronous configuration, each successive stage operates at half the frequency of its predecessor, relaxing the speed constraints at each stage further down the chain. This results in low power operation compared to synchronous methodologies. Essentially the performance of the first stage determines the maximum operating frequency of an asynchronous divider. Given the higher frequency and lower power consumption of dynamic dividers, a common approach is to implement the first stage dynamically and subsequent stages using dynamic

## 2.5 SiGe Process Technology

or static divider stages [23, 30]. The main disadvantage of the asynchronous design is that timing delays and jitter accumulate with each additional stage, leading to increased phase noise on top of the input source phase noise characteristic.

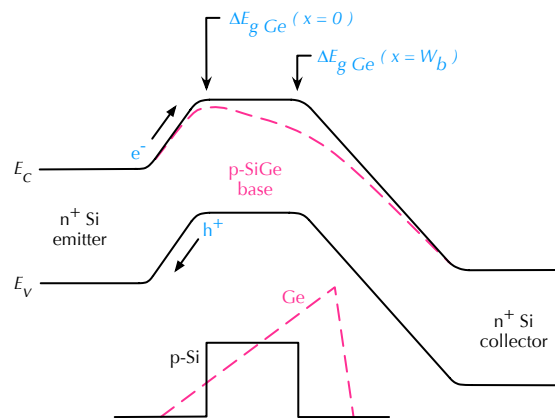
## 2.5 SiGe Process Technology

SiGe BiCMOS is a successful integration of SiGe HBTs with conventional Si CMOS to yield a technology ideal for high performance mixed signal Very Large Scale Integration (VLSI). Traditional Si homojunction BJTs use materials with the same bandgap, whereas SiGe heterojunction devices use bandgap engineering to alter the bandgap in the base region by implantation of the SiGe alloy as shown in Figure 2.14. With reference to Figure 2.15, the



**Figure 2.14.** Cross-section diagram of a typical SiGe HBT indicating the presence of Germanium in the base region to reduce the material bandgap [31].

epitaxial Germanium (Ge) concentration in the base is graded so that the bandgap is narrower at the collector than at the emitter. Tapering of the bandgap in the base induces an electric



**Figure 2.15.** Energy band diagram for a typical Si BJT and a graded-base SiGe HBT [32].

field that accelerates the injected electrons, thus reducing base transit times and improving



frequency response [32]. Reduction of the bandgap at the emitter-base junction also lowers the potential barrier to injection from the emitter to the base, exponentially increasing the collector current density and hence current gain. Hole injection into the base region is limited by the large potential barrier in the valence band allowing higher doping concentrations in the base. This creates higher electron mobility while maintaining gain.

### 2.5.1 IBM BiCMOS7WL

The IBM BiCMOS7WL 0.18 $\mu\text{m}$  SiGe BiCMOS process with seven metal interconnect layers has been used for low volume MMIC prototyping in this thesis. Detailed technical information regarding device structure, modelling and fabrication requirements can be found in the official documentation [33, 34], however this section will give a brief overview of the features and particular device characteristics relevant to the ensuing circuit design.

#### Active Devices

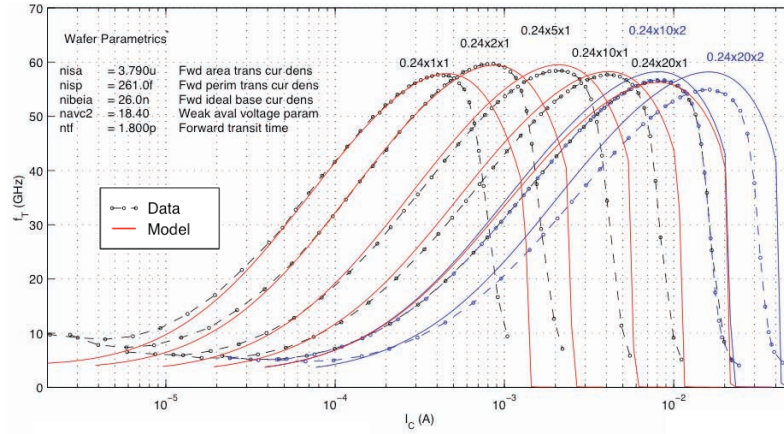
The fastest transistors offered in this technology for RF applications are the high performance NPN Si/SiGe HBT family with  $f_t = 60\text{GHz}$ . They support single and dual emitter stripe configurations with fixed emitter width  $W_e = 0.24\mu\text{m}$  and scaleable emitter length  $L_e$  to achieve the required current rating. Nominal electrical parameters for a single emitter high- $f_t$  NPN transistor of size  $0.24\mu\text{m} \times 4.2\mu\text{m}$  are shown in Table 2.1. Although both single

**Table 2.1.** Nominal electrical parameters of a high- $f_t$  NPN transistor of size  $0.24\mu\text{m} \times 4.2\mu\text{m}$  and single emitter stripe [33].

<i>Electrical Parameter</i>	<i>Value</i>	<i>Conditions</i>
Base-emitter voltage, $V_{BE}$	0.737V	$I_C = 10\mu\text{A}$ , $V_{CB} = 0\text{V}$
Current gain, $\beta$	140	$V_{BE} = 0.72\text{V}$ , $V_{CB} = 0\text{V}$
Peak transition frequency, $f_t$	60GHz	$V_{CB} = 1\text{V}$ , $I_C = 1.65\text{mA}/\mu\text{m}^2$
Breakdown voltage, $BV_{CEO}$	3.3V	$I_C = 10\mu\text{A}$
Rated current density, $I_{rate}$	$4\text{mA}/\mu\text{m}^2$	$W_e = 0.24\mu\text{m}$ , single or dual

and dual emitter HBT configurations are available, the dual emitter stripe option is favoured in this thesis because its lower intrinsic and extrinsic base resistance minimises the base resistance-induced thermal noise [6].

The  $f_t$  characteristics of Figure 2.16 have been used as an aid to determine HBT collector bias current for maximum frequency performance, relative to the effective emitter area. Optimal SiGe HBT device matching is achieved through symmetrical layout techniques with: devices



**Figure 2.16.** High- $f_t$  SiGe NPN  $f_t$  characteristic versus emitter area ( $V_{CB} = 1V$  and  $T = 25^\circ C$ ) [34]. The characteristic is used to determine transistor bias current for optimum frequency performance.

located as close as possible to each other, identical device size and orientation and similar wiring.

### Passive Devices

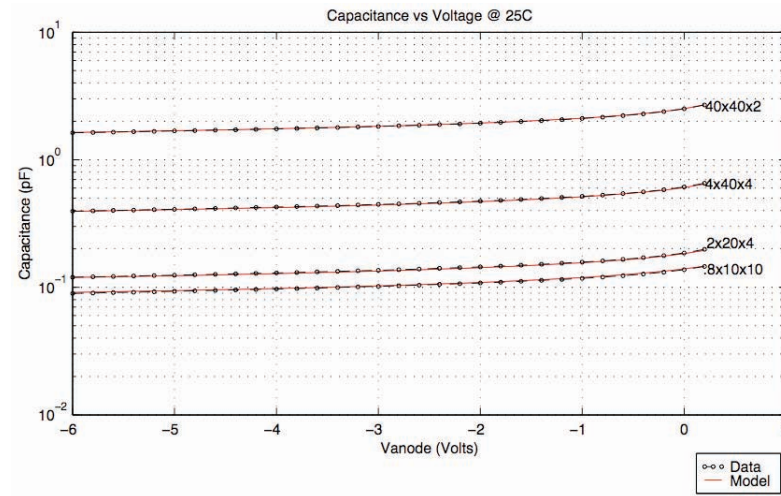
BiCMOS7WL has an extensive standard library of passive components, however only a small subset have been utilised in this thesis. Six resistor types are provided with a variety of specifications and applications. Resistor selection criteria include: sheet resistance, sensitivity or tolerance, mismatch sensitivity, parasitic capacitance and current carrying capacity. Deep trench isolation mesh underneath resistors has also been used where possible.

Single layer spiral inductors (asymmetrical and symmetrical) have been used and are formed in the thick copper top metal for high Q performance. The inductors have deep trench isolation mesh underneath to decrease spiral to substrate capacitance, lower coupling between turns and maximise self resonant frequency. Inductor reactive values are customised through the geometrical parameters of: outer diameter, number of turns, turn width and turn spacing.

The seven metal wiring layers also support Metal Insulator Metal (MIM) capacitor construction. Single MIM capacitors have a capacitance calculated according to the area capacitance of  $4.05\text{fF}/\mu\text{m}^2$  and perimeter capacitance of  $0.14\text{fF}/\mu\text{m}$ , as a guide.

The VCO tuning elements used in this thesis are constructed from the medium- $f_t$  NPN collector-base (C-B) varactor diode. Scalability is obtained through selection of anode size and the number of anodes. Parasitic series resistance is minimised by wrap-around cathodes surrounding each varactor anode. Example varactor capacitance versus voltage characteristics

are displayed in Figure 2.17, while the nominal varactor tunability is specified as  $C_{0V}/C_{3V} = 1.36$ .



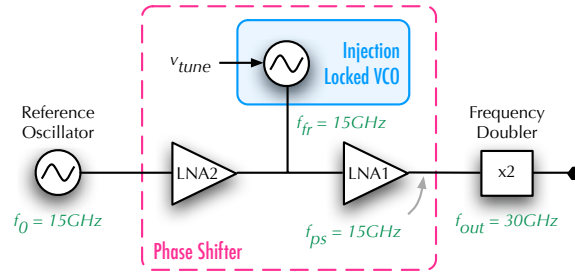
**Figure 2.17.** BiCMOS7WL C-B diode varactor capacitance versus voltage characteristic ( $T = 25^{\circ}\text{C}$ ), illustrating the tunable capacitance range of standard size varactors [34].



# Chapter 3

## 15GHz Oscillator Implementations

This chapter documents the design, simulation and layout of four 15GHz single-ended VCOs in a  $0.18\mu\text{m}$  SiGe BiCMOS technology. The VCO is intended for implementation in the 30GHz continually tunable phase shifter and active antenna beam-forming network as described in Section 1.2.1 and identified in the block diagram of Figure 3.1. The basic requirements of the circuit revision include: injection locking capability, accurate frequency synthesis, improved linear tuning range, improved insensitivity to circuit loading (i.e. better output matching) and sufficient output voltage amplitude.



**Figure 3.1.** Phase shifter block diagram highlighting the injection locked 15GHz VCO designed in this chapter.

### 3.1 Single-Ended VCO Topologies

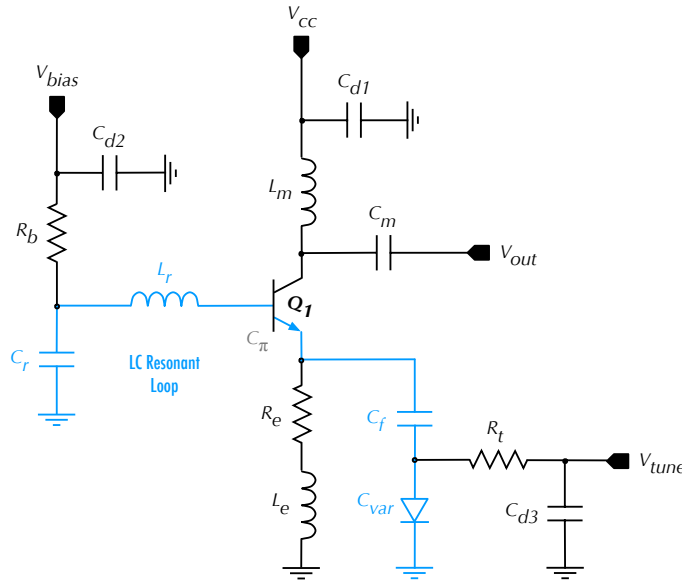
There are two single-ended VCO topologies presented in this thesis – the emitter-tuned topology and the base-tuned topology. As the naming suggests, the differentiating feature of these VCOs is the physical location of the tuning mechanism with respect to transistor

### 3.1 Single-Ended VCO Topologies

terminals. Both topologies facilitate injection locking by injecting a high quality reference oscillator signal into the output port of the VCO, as described in Section 1.2.1. The following subsections discuss each topology in detail.

#### 3.1.1 Emitter-Tuned VCO Topology

Figure 3.2 shows the Colpitts based circuit topology used in three versions of the E-tuned VCO and is based on the original work [4]. The single-ended Colpitts topology is favoured for its good phase noise performance [6]. Note that in this topology the tuning element



**Figure 3.2.** Schematic view of the single-ended Colpitts based VCO topology with varactor tuning element connected to the emitter of the transistor.

$C_{var}$  is connected via the feedback capacitor  $C_f$  to the emitter of the transistor.  $C_f$  acts to destabilise the transistor and creates negative resistance at the input port of the transistor. This negative resistance then cancels the resistance of the resonant tank comprising  $C_r$ ,  $L_r$ ,  $C_f$ ,  $C_{var}$  and the input capacitance  $C_\pi$  of the transistor  $Q_1$ , allowing sustained oscillation to occur. The amount of negative resistance generated can be derived by evaluating the real part of the input impedance ( $Z_a$ ) looking into the base of the transistor expressed as,

$$Z_a = \frac{r_\pi}{(1 + w^2 r_\pi^2 C_\pi^2)} \left( 1 - \frac{g_m r_\pi C_\pi}{C_e} \right) \quad (3.1)$$

where  $g_m$  is the transconductance of the transistor,  $r_\pi$  is the transistor input resistance,  $C_e$  is the series combination of  $C_f$  and  $C_{var}$ ,

$$C_e = \frac{C_f C_{var}}{C_f + C_{var}} \quad (3.2)$$

and the angular frequency  $\omega = 2\pi f$ . From Eq. (3.1) it can be seen that negative resistance is indeed created if,

$$\frac{g_m r_\pi C_\pi}{C_e} > 1 \quad (3.3)$$

which implies,

$$C_e < g_m r_\pi C_\pi. \quad (3.4)$$

Therefore, by simulating the amount of negative resistance at the desired transistor bias point, it is theoretically possible to determine a value for  $C_e$  to satisfy the rule of thumb for achieving an optimum power impedance match in eventual large signal steady state oscillations,

$$Z_a \approx -3 Z_r \quad (3.5)$$

where  $Z_a$  is the real transistor input impedance and  $Z_r$  is the real tank loss resistance. Unfortunately, one side effect of  $C_{var}$  connected in series with  $C_f$  is that varying the effective varactor capacitance via the tuning voltage changes the destabilising effect at the emitter node and hence the negative resistance generated. Changes in the amount of negative resistance may inadvertently effect the large signal operating point of the active device.

Assuming that the emitter inductance,  $L_e$  is a high impedance at the oscillation frequency and can therefore be treated as an open circuit, an equation can be derived for the predicted oscillation frequency as,

$$f_{osc} = \frac{1}{2\pi \cdot \sqrt{L_r \left( \frac{1}{C_r} + \frac{1}{C_\pi} + \frac{1}{C_f} + \frac{1}{C_{var}} \right)^{-1}}}. \quad (3.6)$$

Thus, the following relationship can be used to estimate the theoretical tuning range capability of the VCO,

$$f_\Delta = \frac{1}{2\pi \cdot \sqrt{L_r \left( \frac{1}{C_r} + \frac{1}{C_\pi} + \frac{1}{C_f} + \frac{1}{C_{var_{min}}} \right)^{-1}}} - \frac{1}{2\pi \cdot \sqrt{L_r \left( \frac{1}{C_r} + \frac{1}{C_\pi} + \frac{1}{C_f} + \frac{1}{C_{var_{max}}} \right)^{-1}}} \quad (3.7)$$

where  $C_{var_{max}}$  and  $C_{var_{min}}$  are the maximum and minimum varactor capacitance bounds.

The relatively large capacitances  $C_{d1}$ ,  $C_{d2}$  and  $C_{d3}$  are decoupling or bypass capacitors to shunt unwanted power supply noise to ground. Supply impurities can cause oscillator pushing where by voltage fluctuations alter the bias point of the transistor and subsequently the frequency of oscillation. The effects of supply noise are particularly evident in a single-ended topology where common mode noise sources are not eliminated compared to a differential design.

### 3.1 Single-Ended VCO Topologies

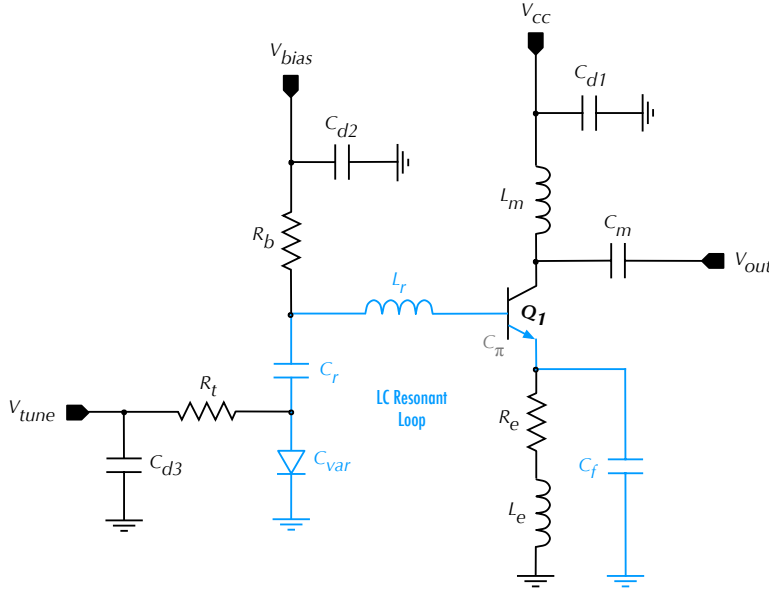
The inductance  $L_m$  and capacitance  $C_m$  form an output matching network optimised for maximum transfer of RF power to the load.  $L_m$  also acts as a DC feed of  $V_{cc}$  to  $Q_1$ , whilst  $C_m$  couples RF signals only to the output port.

The transistor base bias voltage  $V_{bias}$  and varactor tuning voltage are applied to the circuit through resistors  $R_b$  and  $R_t$  respectively. The varactor is orientated with the cathode connected to ground to maximise Q due to the subcollector to substrate capacitance [35].

The emitter degradation resistance  $R_e$  provides DC feedback to compensate for temperature fluctuations and threshold voltage process variation. This improves the stability of the transistor DC operating point. The series inductance  $L_e$  simply acts as an AC open circuit to direct RF signals through the tuning capacitance path when under oscillating conditions.

#### 3.1.2 Base-Tuned VCO Topology

Figure 3.3 shows the B-tuned single-ended VCO topology as presented in [36, 6, 37] and introduced to provide a possible alternative to the E-tuned design. In this configuration



**Figure 3.3.** Schematic view of the single-ended Colpitts based VCO topology with varactor tuning element alternatively located at the base of the transistor.

the tuning capacitance  $C_{var}$  is connected to the base of the transistor via the resonant tank inductor,  $L_r$ . As such, it does not change the amount of capacitive feedback destabilisation at the emitter or the associated generation of negative resistance. The negative resistance generated by the base-tuned topology can again be derived by evaluating the real part of the



transistor input impedance at the base of the transistor expressed as,

$$Z_a = \frac{r_\pi}{(1 + w^2 r_\pi^2 C_\pi^2)} \left( 1 - \frac{g_m r_\pi C_\pi}{C_f} \right) \quad (3.8)$$

where  $g_m$  is the transconductance of the transistor,  $r_\pi$  is the transistor input resistance,  $C_\pi$  is the transistor input capacitance,  $C_f$  is the feedback capacitance and the angular frequency  $w = 2\pi f$ . Therefore, according to Eq. (3.8) negative resistance is achieved if,

$$\frac{g_m r_\pi C_\pi}{C_f} > 1 \quad (3.9)$$

which implies,

$$C_f < g_m r_\pi C_\pi. \quad (3.10)$$

Expressions for the oscillation frequency and tuning range defined in Eq. (3.6) and Eq. (3.7) respectively are directly applicable to the base-tuned topology because the resonant loop consists of the same series reactive elements as the E-tuned structure, despite the relocation of  $C_{var}$ .

The remaining circuit elements perform identical functions to those described for the E-tuned topology in Section 3.1.1.

## 3.2 Biasing and Device Selection

Although the original intent of this research task was to simply port the existing VCO design and its parameters to the new technology, simulation identified certain key performance deficiencies, particularly with respect to frequency tuning capability. The tuning range proved insufficient to cover centre frequency variation from process variation. In an attempt to mitigate these deficiencies, four 15GHz VCOs were designed and prepared for fabrication. Three are parametric variations of the E-tuned topology and identified by the abbreviations: ET15G, ET15G\_V2 and ET15G\_V3 (where  $Vn$  represents the version number). The fourth VCO design is based on the B-tuned topology and is abbreviated to BT15G. The schematic device parameters of each VCO are recorded in Table 3.1 while Section 3.4 evaluates their simulated pre and post-layout performance. The focus of initial device selection was to produce oscillations at approximately 16–17GHz to allow 1–2GHz margin for the detuning effects of layout parasitics.

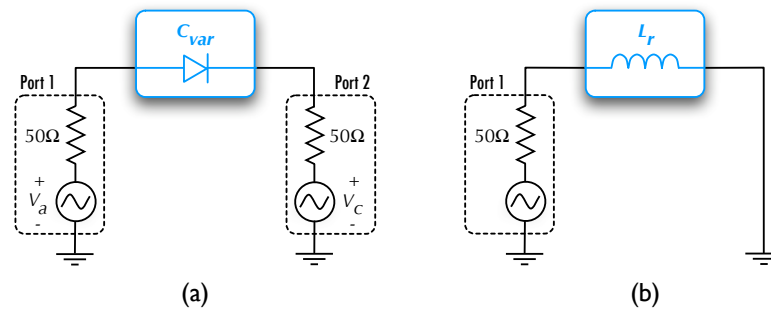
**Table 3.1.** Schematic parameters of the 15GHz singled-ended VCO implementations: ET15G, ET15G\_V2, ET15G\_V3 and BT15G.  $C_{var}$  and  $L_r$  reactance values are determined at the oscillation frequency.  $W_e$  = emitter width,  $L_e$  = emitter length and  $N_e$  = number of emitter stripes.

Device	Properties	ET15G	ET15G_V2	ET15G_V3	BT15G
$Q_1$	High- $f_t$ NPN HBT: $W_e \times L_e, N_e$	$0.24\mu m \times 4\mu m, 2$	$0.24\mu m \times 2.5\mu m, 2$	$0.24\mu m \times 2.5\mu m, 2$	$0.24\mu m \times 2.5\mu m, 2$
$C_{d1}$	$V_{cc}$ supply decoupling	8.64pF	8.64pF	7.36pF	7.36pF
$C_{d2}$	$V_{bias}$ supply decoupling	3.26pF	3.26pF	3.26pF	3.26pF
$C_{d3}$	$V_{tune}$ supply decoupling	2.09pF	2.09pF	3.26pF	3.26pF
$C_r$	$V_{bias}$ DC block + RF ground	10.90pF	7.36pF	3.26pF	1.83pF
$C_f$	Instability feedback for $-R$	2.22pF	812.3fF	812.3fF	455.5fF
$C_m$	Output coupling + matching	128.1fF	518.7fF	5.11pF	5.11pF
$C_{var}$	Tuning varactor capacitance	$143fF \rightarrow 221fF$	$458fF \rightarrow 706fF$	$858fF \rightarrow 1.323pF$	$229fF \rightarrow 353fF$
$R_b$	Base bias voltage feed	126 $\Omega$	132 $\Omega$	5k $\Omega$	5k $\Omega$
$R_e$	Temperature stabilisation	106 $\Omega$	106 $\Omega$	16k $\Omega$	16k $\Omega$
$R_t$	Tuning voltage feed	5k $\Omega$	5k $\Omega$	5k $\Omega$	5k $\Omega$
$L_r$	Resonant tank inductance	1.076nH	910pH	704pH	910pH
$L_m$	$V_{cc}$ feed + output matching	882pH	1.07nH	4.99nH	4.99nH
$L_e$	RF high impedance choke	1.027nH	1.027nH	4.99nH	4.99nH
$V_{bias}$	Base bias voltage	+1V	+1.1V	+1V	+1V
$V_{cc}$	Supply rail voltage	+1.8V	+1.8V	+1.8V	+1.8V
$V_{tune}$	$C_{var}$ tuning voltage	$-3V \rightarrow 0V$	$-3 \rightarrow 0V$	$-3V \rightarrow 0V$	$-3V \rightarrow 0V$

Two variants of the high- $f_t$  SiGe NPN HBT were selected from the technology device library for  $Q_1$ , with emitter dimensions as shown in the schematic parameters Table 3.1. The smaller transistor should have a reduced capacitive contribution to the resonant loop. The subsequent collector bias currents for maximum  $f_t$  performance were determined with reference to the  $f_t$  characteristics presented in the technology design manual and shown in Figure 2.16. The voltages  $V_{cc}$  and  $V_{bias}$  are used to achieve the desired bias point of the core transistor. Given a supply voltage of 1.8V and transistor  $V_{BE} \approx 0.737V$ ,  $V_{bias}$  is set in the order of 1V to provide adequate headroom under large signal oscillation without driving  $Q_1$  into the non-linear saturation region. Saturation of the active device in a single-ended topology may result in sinusoidal asymmetries in the output waveform and hence spectral impurity. A base-collector varactor diode forms the tuning element,  $C_{var}$  in both VCO topologies. The varactor cathode is at AC ground potential to maximise Q. The emitter-base junction breakdown voltage limits the varactor tuning voltage to the range,  $-3V \leq V_{tune} \leq 0V$ .

### 3.2.1 $C_{var}$ and $L_r$ Characterisation

Characterisation of varactor and inductor properties was undertaken to determine the capacitive tuning range of varactor configurations as a function of reverse bias potential and the inductance, Q and series loss resistance of resonant tank inductor configurations as a function of frequency. Figure 3.4(a) shows the two-port schematic used to perform Scattering parameter (S-parameter) simulation on varactor configurations, where the reverse bias tuning voltage is the difference between anode and cathode DC potentials ( $V_a$  and  $V_c$ ) defined in the port properties. Individual parametric analysis on the reverse bias voltage and input



**Figure 3.4.** S-parameter schematics used to characterise the reactance, Q and series resistance of varactor and inductor configurations.

### 3.2 Biasing and Device Selection

signal frequency produce capacitance and Q characteristics according to the expressions,

$$C(V_{ac}) = \frac{Y_{11}}{2\pi f} \quad (3.11)$$

$$Q(V_{ac}) = \frac{Y_{11}}{Y_{11}} \quad (3.12)$$

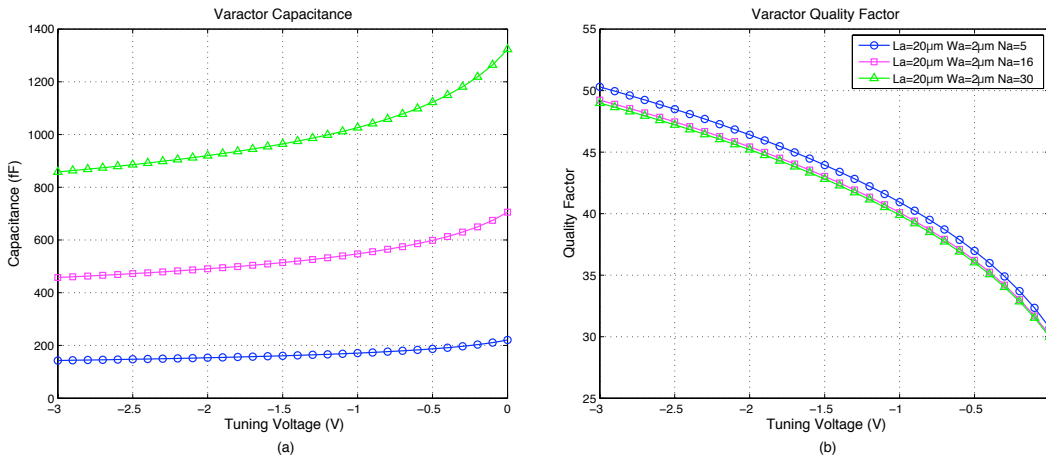
where  $Y_{11}$  and  $Y_{11}$  are the real and imaginary parts of the Y-parameter,  $Y_{11}$  of Port 1 respectively. Parametric simulation of the inductor circuit shown in Figure 3.4(b) with respect to input signal frequency produces inductance, loss resistance and Q characteristics according to the expressions,

$$L = \frac{Z_{11}}{2\pi f} \quad (3.13)$$

$$Q = \frac{Z_{11}}{Z_{11}} \quad (3.14)$$

$$R = Z_{11} \quad (3.15)$$

where  $Z_{11}$  and  $Z_{11}$  are the real and imaginary parts of the Z-parameter,  $Z_{11}$  of Port 1 respectively. The chosen varactors have standard anode size  $L_a \times W_a = 20\mu\text{m} \times 2\mu\text{m}$  and operate in reverse bias mode. The number of varactor anodes,  $N_a$  is selected in conjunction with the tank inductance  $L_r$  through a process of iterative simulation, to achieve the 15GHz oscillation frequency requirement.  $N_a$  in the four VCO designs ranges from 5 to 30 and their simulated capacitance and quality factor characteristic graphs are shown in Figure 3.5. The characteristics indicate that irrespective of the varactor size, the capacitive tuning ratio

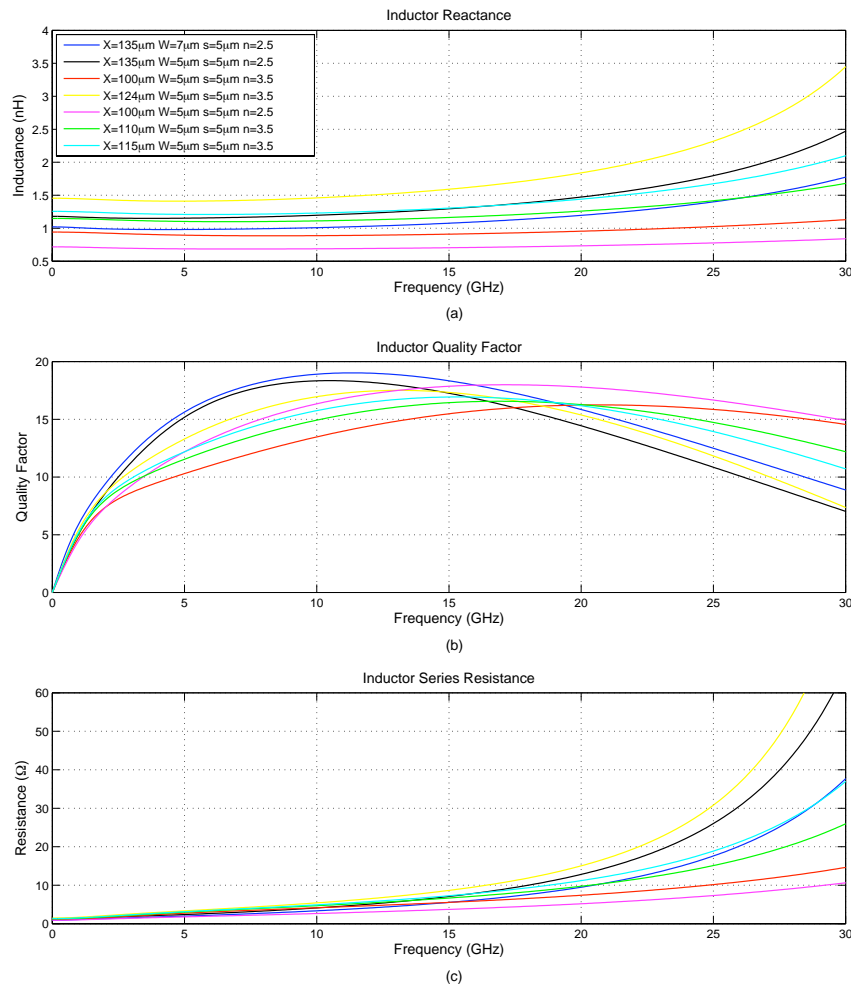


**Figure 3.5.** S-parameter simulation of varactor: (a) capacitance and (b) quality factor at 15GHz as a function of applied reverse bias potential,  $V_{ac}$ .  $L_a$  = varactor anode length,  $W_a$  = anode width and  $N_a$  = number of anodes.

remains constant at  $C_{V_{ac}=-3V} : C_{V_{ac}=0V} = 1 : 1.54$ . Therefore, increasing varactor size

alone is not an effective means of increasing VCO frequency tuning capability, instead only the median capacitance is increased. The varactor quality factor characteristic illustrates a significant roll-off as  $V_{tune}$  approaches zero volts. This ultimately indicates a large variation of the energy restoration capability of the resonant loop during tuning.

$L_r$  is a standard top metal spiral inductor over a crosshatch pattern of deep trench isolation, which creates a barrier of insulator material, effectively cutting up the conductivity of the substrate near the surface [33]. Figure 3.6 shows the inductance, quality factor and series resistance characteristics of the devices used in each of the single-ended 15GHz VCO designs as a function of frequency. It is worth noting that inductor Q ranges from 15 to 18 at



**Figure 3.6.** S-parameter simulation of 15GHz VCO resonant tank inductor: (a) inductance, (b) Q and (c) series loss resistance, as a function of frequency.  $X$  = spiral outer diameter,  $W$  = spiral width,  $s$  = turn separation and  $n$  = number of turns.

15GHz and peaks in the vicinity of the operational frequency. Series resistance increases

### 3.3 Circuit Layout

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exponentially as frequency increases, however it is generally less than  $9\Omega$  at 15GHz. A high Q resonant tank is typically more difficult to tune with the necessary precision, however it leads to better selectivity. In the phase shifter application, a low VCO Q is desirable because it promotes a wide locking range to the external injected reference signal [38]. Although the low VCO Q results in poor phase noise, during lock the oscillator will adopt the phase noise characteristic of the injected high purity reference oscillator.

Sufficiently large values are selected for the decoupling capacitors  $C_{d1}$ ,  $C_{d2}$  and  $C_{d3}$  to provide adequate isolation of unwanted AC noise superimposed on the DC power supply lines.

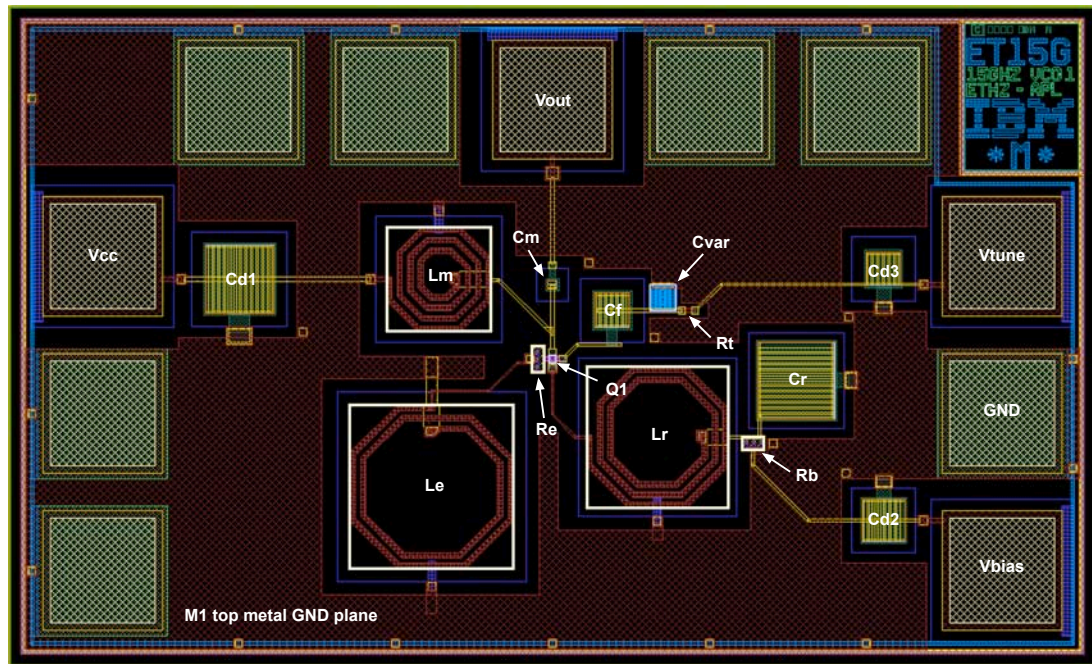
While the remaining passive components of ET15G are an adaptation of the original work, ET15G\_V2 is a minor optimisation of these components focussing on improving frequency tunability by reducing the feedback capacitor,  $C_f$  to allow for increased varactor size. BT15G and ET15G\_V3 however, are more extensive redesigns. Whilst still concerned with maximising tuning range, they attempt to improve bias voltage isolation, temperature stability and RF blocking in the emitter degradation path via increasing the values of components  $R_b$ ,  $R_e$  and  $L_e$  respectively. Impedance matching analysis was performed to improve the output match of  $L_m$  and  $C_m$  for maximum linearity and signal transmission. However, interdependencies between the matching network and centre oscillation frequency make this difficult. The redesigned circuits exhibited sufficient negative resistance to sustain oscillation at above 40GHz, albeit with small output amplitude.

### 3.3 Circuit Layout

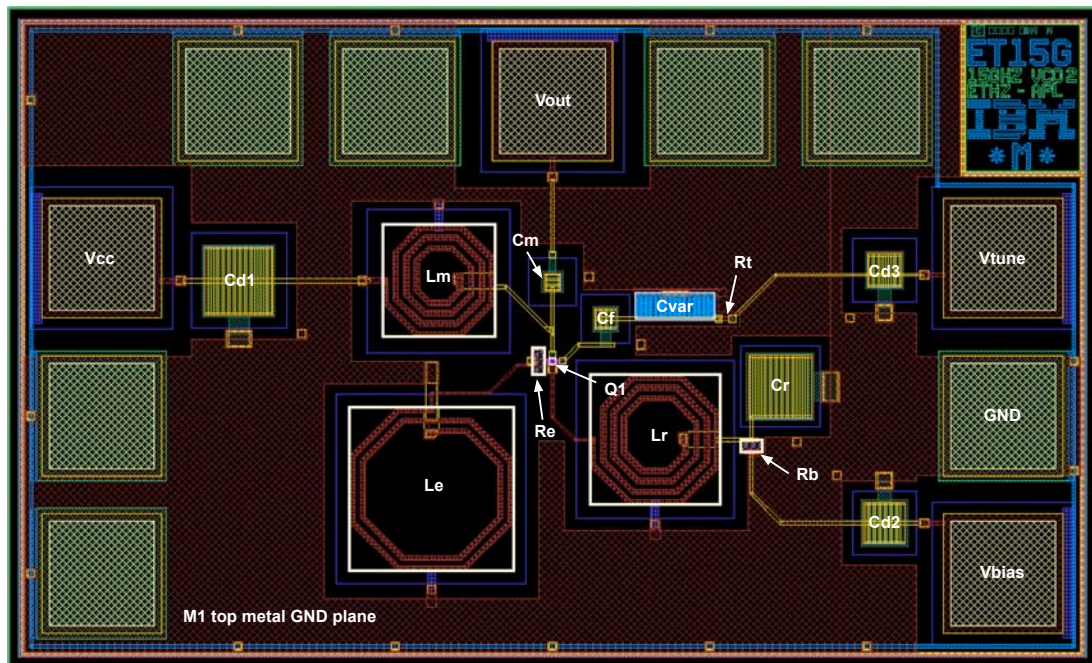
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Industry standard RF layout techniques were employed in the generation of the four 15GHz single-ended VCO layouts shown in Figures 3.7, 3.8, 3.9 and 3.10. Compact device placement and minimisation of parasitics were of particular focus. A top metal ground plane is incorporated in each layout to ensure a low resistance, common ground path, reduced metal layer to substrate parasitic effects and to shield against RF signal cross-coupling. All inductors and bond pads utilise deep trench isolation to break up the conductivity in the substrate surface and reduce coupled noise in the VCO output. Bond pads are placed at minimum pitch around the perimeter of each VCO core, the size of which is dominated by the passive inductive and capacitive components. The size and pitch of bond pads is dictated by the mechanical constraints of the wafer measurement probes. Encompassing chip rings and the necessary metal density fill for fabrication, complete the layout process. ET15G and ET15G\_V2 have a total chip area of  $1038\mu\text{m} \times 630\mu\text{m}$ , while ET15G\_V3 and BT15G are slightly larger at  $1038\mu\text{m} \times 780\mu\text{m}$  to accommodate increased  $L_m$  and  $L_e$  inductor size.





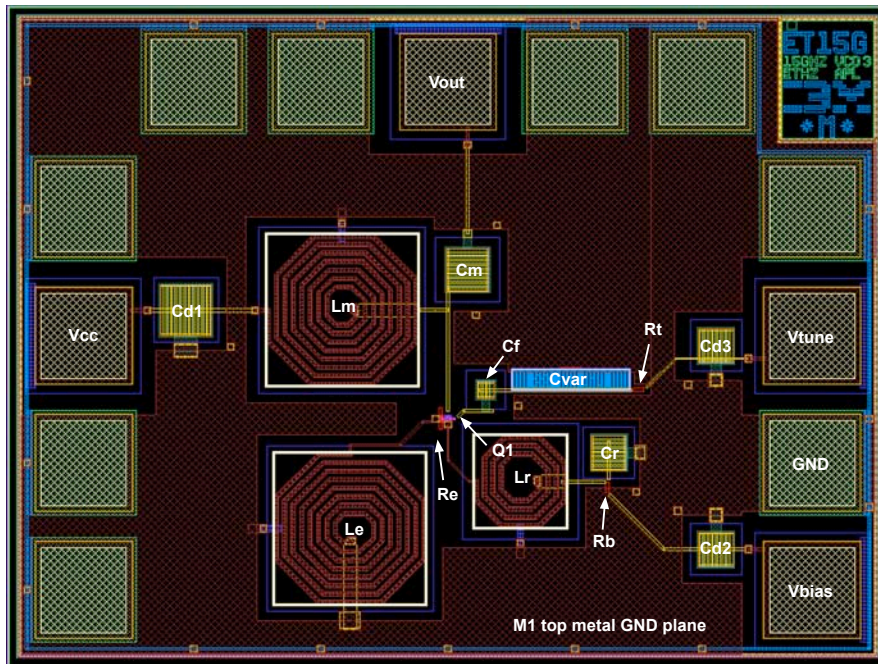
**Figure 3.7.** ET15G 15GHz single-ended E-tuned VCO layout cell view with annotated device labels – chip size  $1038\mu\text{m} \times 630\mu\text{m}$ .



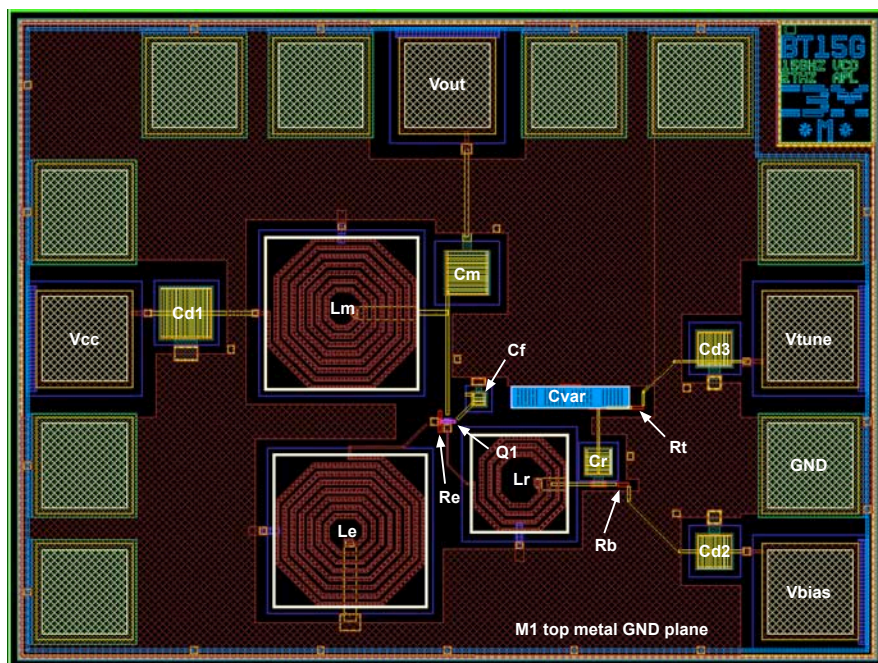
**Figure 3.8.** ET15G.V2 15GHz single-ended E-tuned VCO layout cell view with annotated device labels – chip size  $1038\mu\text{m} \times 630\mu\text{m}$ .



### 3.3 Circuit Layout



**Figure 3.9.** ET15G\_V3 15GHz single-ended E-tuned VCO layout cell view with annotated device labels – chip size  $1038\mu\text{m} \times 780\mu\text{m}$ .



**Figure 3.10.** BT15G 15GHz single-ended B-tuned VCO layout cell view with annotated device labels – chip size  $1038\mu\text{m} \times 780\mu\text{m}$ .



### 3.3.1 Layout Parasitic Extraction

Analog parasitic resistance and capacitance were extracted from the VCO layouts (including metal density fill) using the design tools, with the values back-annotated into the circuit schematics. Unfortunately, the design kit did not allow extraction of parasitic inductance, therefore, some discrepancy is expected between simulated and measured performance. Post-layout simulations were performed on the extracted schematics and appear in Section 3.4 in conjunction with pre-layout simulation results for comparison.

The results triggered minor schematic modifications with respect to resonant tank inductor ( $L_r$ ) properties, to fine tune the expected oscillation frequencies. Table 3.2 summarises the modifications while the inductance, quality factor and series resistance characteristics of the new devices are included in Figure 3.6. All pre and post-layout simulated VCO results reported in this chapter incorporate these  $L_r$  instance changes.

**Table 3.2.**  $L_r$  schematic modifications resulting from post-layout simulations, to fine tune each VCO fundamental frequency. The original and updated device attributes are included.

<i>MMIC</i>	<i>Version</i>	<i>Dimensions</i>	$L_r$ (nH)	$R$ ( $\Omega$ )	$Q$	$f_{peak\ Q}$ (GHz)
ET15G	Original	$135\mu m \times 7\mu m \times 2.5$	1.076	5.53	18.33	9.85
	Updated	$135\mu m \times 5\mu m \times 2.5$	1.295	7.15	17.26	9.58
ET15G_V2	Original	$100\mu m \times 5\mu m \times 3.5$	0.9101	5.54	15.48	11.83
	Updated	$124\mu m \times 5\mu m \times 3.5$	1.591	8.65	17.33	8.42
ET15G_V3	Original	$100\mu m \times 5\mu m \times 2.5$	0.7044	3.72	17.86	14.17
	Updated	$110\mu m \times 5\mu m \times 3.5$	1.164	6.671	16.44	10.13
BT15G	Original	$100\mu m \times 5\mu m \times 3.5$	0.9101	5.54	15.48	11.83
	Updated	$115\mu m \times 5\mu m \times 3.5$	1.305	7.27	16.93	9.44

## 3.4 Simulation Results

Simulation of the single-ended VCO implementations was carried out in accordance with the large and small signal oscillator analysis as described in [39]. The basic premise of this procedure is that small signal simulation quickly identifies a satisfactory circuit topology in the early design phase, while large signal analysis focuses on accurate design of the oscillator and its associated parameters for reliable performance. Using S-parameter analysis to obtain the reflection coefficients and resulting impedances at the interface between the active device and the resonator (the plane between  $L_r$  and  $Q_1$  in Figure 3.2 and Figure 3.3), the simulation

### 3.4 Simulation Results

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tools can be set up to directly plot the real ( ) and imaginary ( ) impedance relationships,

$$\frac{Z_a(A, \omega)}{Z_r(\omega)} \quad (3.16)$$

$$Z_a(A, \omega) + Z_r(\omega) \quad (3.17)$$

where  $Z_a$  is the frequency ( $\omega$ ) and oscillation amplitude ( $A$ ) dependent impedance looking into the active circuit network and  $Z_r$  is the frequency dependent input impedance looking into the resonant circuit network. The predicted small signal oscillation frequency can be read from the graph at the point where the conditions for stable oscillation are met for negative resistance oscillators, in accordance with Eq. (2.5) and Eq. (3.5). Whilst these conditions are mandatory to achieve oscillation, [40] derives an equation representing the correlation between a differential change in the circuit impedance and variations in the operating point amplitude as,

$$\left[ \frac{\partial R_a(A)}{\partial A} \right]_{A=A_0} \cdot \left[ \frac{\partial X_r(\omega)}{\partial \omega} \right]_{\omega=\omega_{LO}} - \left[ \frac{\partial R_r(\omega)}{\partial \omega} \right]_{\omega=\omega_{LO}} \cdot \left[ \frac{\partial X_a(A)}{\partial A} \right]_{A=A_0} > 0. \quad (3.18)$$

Properties of the active and passive loads allow simplification of Eq. (3.18) to the following form,

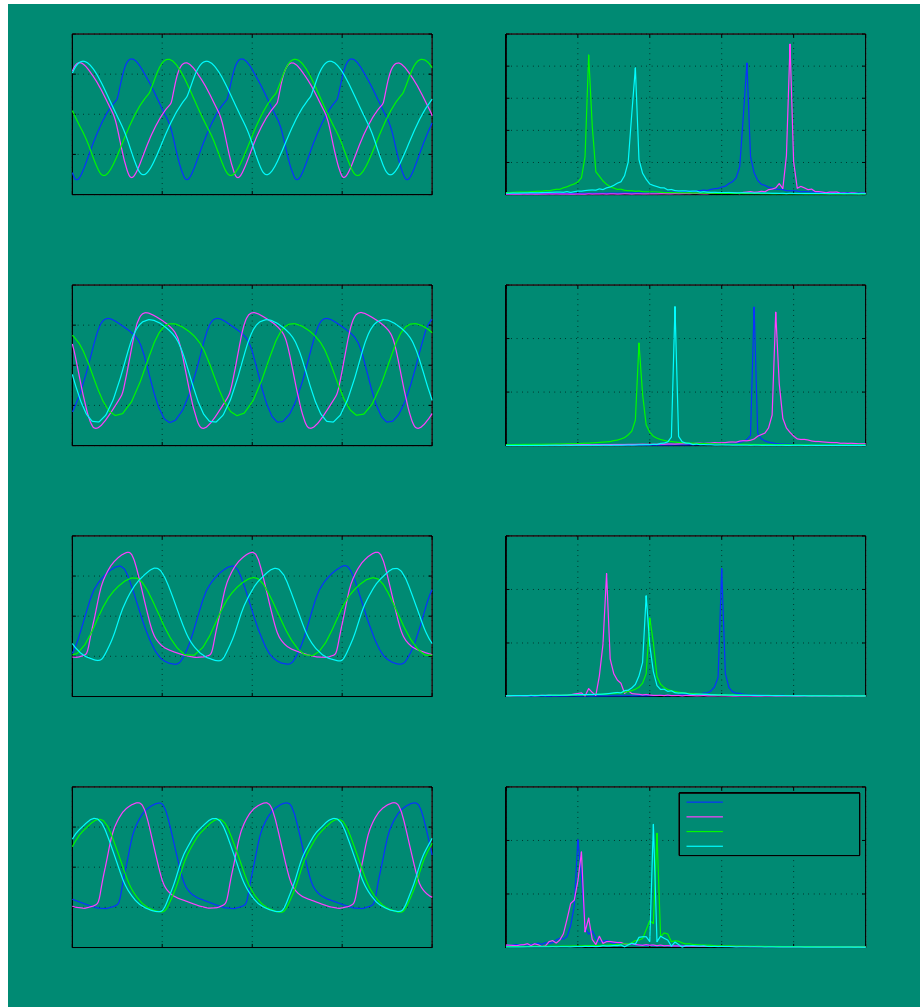
$$\left[ \frac{\partial X_r(\omega)}{\partial \omega} \right]_{\omega=\omega_{LO}} > 0 \quad (3.19)$$

stipulating that to guarantee stable oscillation, the reactive component of the  $Z_r$  impedance must also be increasing with frequency about the operating point. Simulation verified that this condition is automatically satisfied by the passive resonant networks of each VCO.

Transient and periodic steady-state (PSS) simulation techniques were utilised to accurately model VCO output and tuning characteristics under large signal operating conditions, after start-up. A component of the PSS simulation was also used to evaluate single-sided VCO phase noise characteristics relative to the fundamental oscillation frequency.

#### 3.4.1 VCO Output and Phase Noise

Time domain waveforms of each VCO output were obtained using transient simulation of the single-ended output voltage signals at the tuning voltage limits,  $V_{tune} = -3V$  and  $0V$ . A load impedance of  $50\Omega$  is assumed and represents the input impedance of a matched succeeding circuit connection. The results are shown in Figure 3.11, and represent constant amplitude sinusoids. Post-layout waveforms closely follow the shape of the pre-layout predictions, while ET15G\_V3 and BT15G appear to suffer more voltage amplitude degradation. ET15G demonstrates approximately double the amplitude compared to the other VCOs. This can be attributed to the increased current capacity of the larger transistor used in its design.



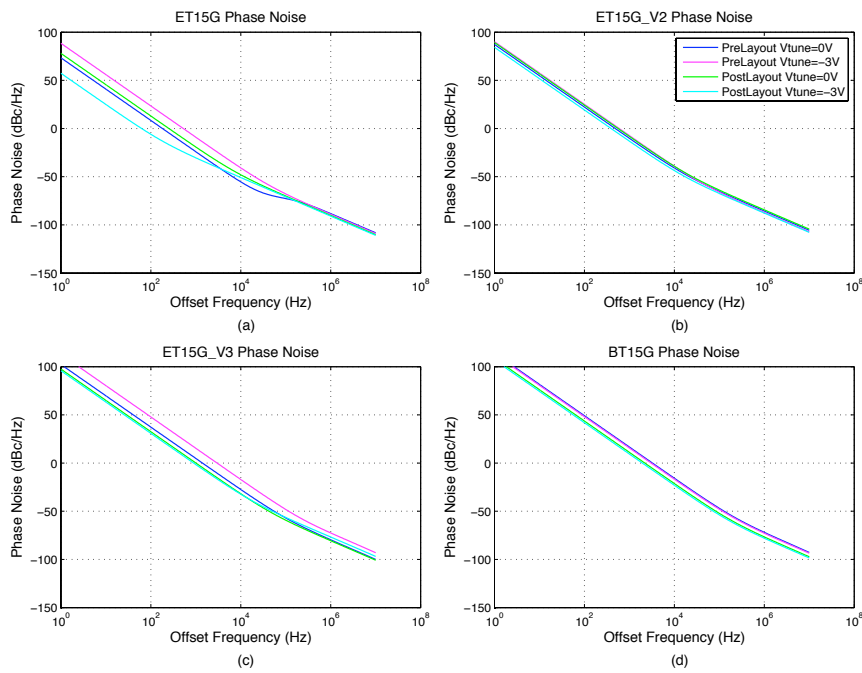
**Figure 3.11.** Simulated pre-layout schematic and post-layout analog extracted 15GHz VCO output signals at the tuning voltage limits,  $V_{tune} = -3V$  and  $0V$ , in the time and frequency domain: (a) & (b) ET15G, (c) & (d) ET15G.V2, (e) & (f) ET15G.V3, and (g) & (h) BT15G.

The frequency domain plots shown in Figure 3.11 were generated using a windowed Fast Fourier Transform (FFT) function on each output voltage signal and reveal upper and lower oscillation frequency bounds. The frequency spectrum are also extremely useful in demonstrating the sensitivity of VCO resonant frequency to layout parasitics. Although the frequency tuning range of ET15G is relatively unaffected by circuit layout, the centre frequency has shifted down by approximately 2GHz. ET15G.V2 suffers a similar downward shift of the centre frequency by approximately 1.5GHz after layout, however the tuning range has actually slightly increased according to the simulations. ET15G.V3 is somewhat of an anomaly. While pre-layout results predict that it has the largest tuning range of all the VCO designs, post-layout results show that only roughly a third of the range centred around 15GHz is

### 3.4 Simulation Results

realised. The pre-layout lower frequency bound has therefore moved upward in frequency after layout. It is unclear whether such a severe reduction in tunability is the result of simulation errors or an accurate indication of layout influences. BT15G shows the least promising results in terms of tunability, however it also appears to be the least effected by layout parasitics in terms of the centre oscillation frequency. Output voltage amplitude and fundamental oscillation frequency are recorded in Table 3.3.

Simulated VCO phase noise characteristics are shown in Figure 3.12 as a function of offset frequency from the fundamental. Phase noise values at 1MHz offset are extracted from the



**Figure 3.12.** Simulated pre-layout schematic and post-layout analog extracted 15GHz VCO phase noise characteristics at the tuning voltage limits,  $V_{tune} = -3V$  and  $0V$ , relative to the fundamental frequency: (a) ET15G, (b) ET15G\_V2, (c) ET15G\_V3, and (d) BT15G.

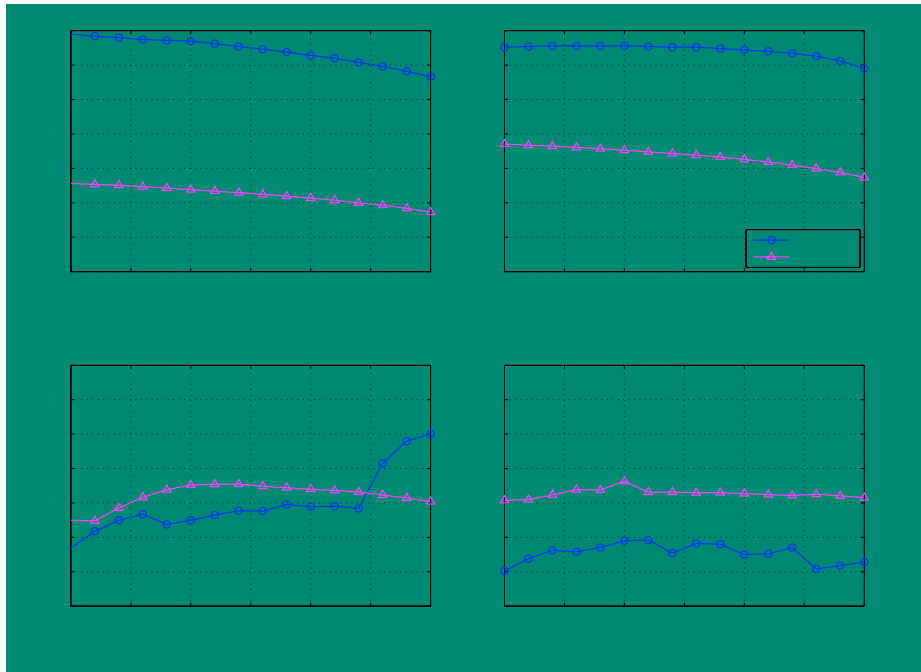
graphs and recorded in Table 3.3. The values range between  $-71.93\text{dBc/Hz}$  and  $-90.92\text{dBc/Hz}$  and in general the post-layout phase noise is better than pre-layout simulations predict. Aside from ET15G\_V3, VCO phase noise also improves as  $V_{tune}$  approaches the negative tuning voltage limit. This may be a direct effect of the varactor Q characteristic investigated in Section 3.2.1.

**Table 3.3.** Simulated 15GHz VCO pre-layout schematic and post-layout analog extracted output characteristics at the tuning voltage limits,  $V_{tune} = -3V$  and  $0V$ , assuming an output load,  $R_{load} = 50\Omega$ . Phase noise is measured at  $\Delta\omega = 1MHz$  offset from the carrier.

<i>MMIC</i>	<i>Cell View</i>	$V_{tune}$ (V)	$v_{out}$ (mV)	$f_{osc}$ (GHz)	$\mathcal{L}(\Delta\omega)$ (dBc/Hz)
ET15G	Pre-layout Schematic	-3	286.93	16.95	-89.00
		0	301.19	16.35	-88.33
	Post-layout Extracted	-3	283.27	14.80	-90.92
		0	289.79	14.15	-90.23
ET15G_V2	Pre-layout Schematic	-3	144.47	16.75	-87.10
		0	129.71	16.45	-85.65
	Post-layout Extracted	-3	127.60	15.35	-87.78
		0	114.62	14.85	-84.42
ET15G_V3	Pre-layout Schematic	-3	131.29	14.40	-72.53
		0	122.98	16.00	-79.64
	Post-layout Extracted	-3	115.77	14.95	-76.79
		0	97.39	15.00	-80.63
BT15G	Pre-layout Schematic	-3	131.70	14.05	-71.93
		0	131.77	14.00	-72.83
	Post-layout Extracted	-3	116.54	15.05	-78.01
		0	115.88	15.10	-76.66

### 3.4.2 VCO Tuning Characteristics

Parametric simulation is used to obtain VCO tuning characteristics by varying  $V_{tune}$  from  $-3V$  to  $0V$  in  $+0.2V$  increments and recording oscillation frequency, output voltage amplitude, RF output power, power consumption and power conversion efficiency. Frequency tuning data is plotted in Figure 3.13 for all four VCOs. ET15G and ET15G\_V2 display relatively linear transition from maximum to minimum oscillation frequency. However the severity of parasitic detuning effects are again illustrated but the downward shift of the post-layout characteristics. ET15G\_V3 pre-layout results indicate a tuning range in the order of  $1.6GHz$ , however the behaviour is quite nonlinear. Most of the tuning capability is only available in the increased slope region where  $-0.6V \leq V_{tune} \leq 0V$ . The rest of the characteristic has a shallow slope and contains frequency fluctuations. Contradictorily, ET15G\_V3 post-layout results show a smooth tuning function with only  $533MHz$  range and irregular negative curvature about  $V_{tune} = -1.8V$ . BT15G pre and post-layout tuning characteristics both demonstrate relatively flat response over the  $V_{tune}$  range and any variation in the oscillation frequency does not appear to be in a controllable fashion. The characteristics of



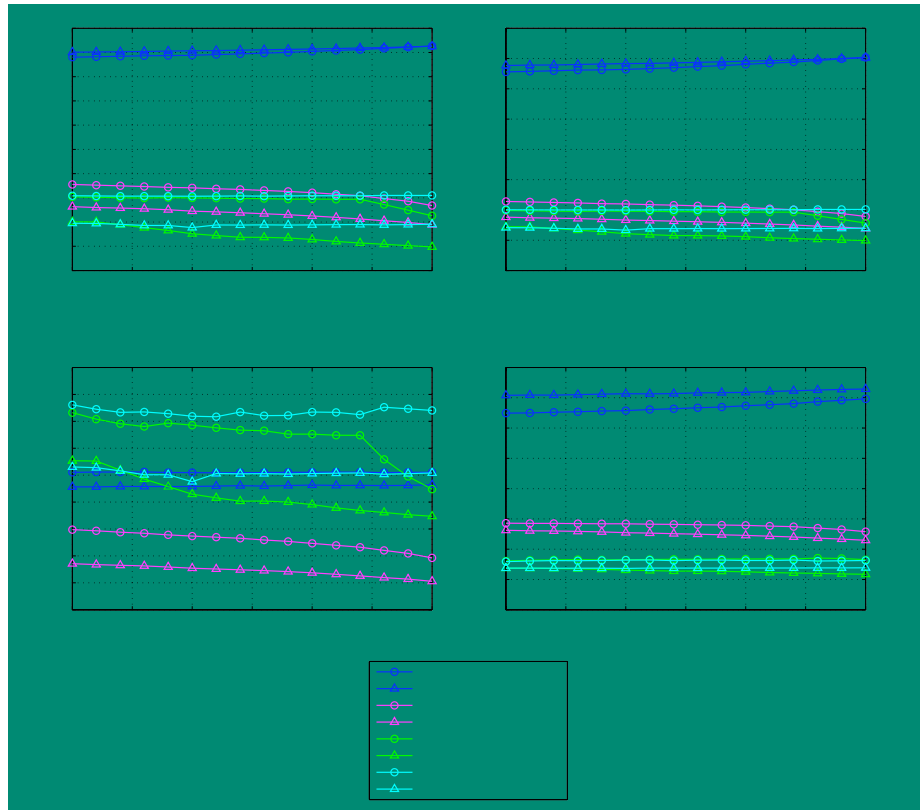
**Figure 3.13.** Simulated 15GHz VCO pre-layout schematic and post-layout analog extracted frequency tuning characteristics: (a) ET15G, (b) ET15\_V2, (c) ET15G\_3 and (d) BT15G.  $V_{tune} = -3 \text{ V}$  to  $0 \text{ V}$  in  $+0.2 \text{ V}$  increments.

ET15G\_V3 and BT15G suggest that tuning of these VCOs with any precision would be very difficult. The exact centre frequency and tuning range of each VCO design is recorded in Table 3.4.

Output signal voltage and RF power characteristics are shown in Figure 3.14, along with DC power consumption and power conversion efficiency over the tuning voltage range. As alluded to in the time domain waveforms, ET15G exhibits approximately double the output voltage and hence quadruple the output power compared to the other VCO circuits. Relatively constant voltage amplitude, greater than  $100 \text{ mV}$ , is observed over the tuning range in all cases and is deemed sufficient for the phase shifter application. DC power consumption ranges from  $3 \text{ mW}$  to  $6.3 \text{ mW}$ , while the efficiency plots reveal that ET15G and ET15\_V2 are more effective at converting DC power into RF output signal power. VCO voltage and power metrics averaged over the tuning range are included in Table 3.4.

#### 3.4.3 Summary

In summary, of the four single-ended 15GHz VCOs presented in this chapter, ET15G and ET15G\_V2 have superior performance in terms of accurate frequency synthesis, linear tuning



**Figure 3.14.** Simulated 15GHz VCO pre-layout schematic and post-layout analog extracted voltage and power characteristics: (a) output voltage amplitude, (b) RF power output, (c) DC power consumption, and (d) power conversion efficiency.

**Table 3.4.** Simulated 15GHz VCO pre and post-layout performance metrics over the tuning range,  $V_{tune} = -3 \text{ } 0V$  including: centre oscillation frequency ( $f_{osc}$ ), frequency tuning range ( $f_{\Delta}$ ) and averaged values of output voltage ( $v_{out}$ ), RF power ( $P_{out}$ ), DC power consumption ( $P_{DC}$ ) and power conversion efficiency ( $\eta$ ).

MMIC	Cell View	$f_{osc}$ (GHz)	$f_{\Delta}$ (MHz)	$v_{out}$ (mV)	$P_{out}$ (dBm)	$P_{DC}$ (mW)	$\eta$ (%)
ET15G	Pre-layout Schematic	16.640	620.0	259.76	-1.71	5.05	13.36
	Post-layout Extracted	14.571	417.8	262.25	-1.63	4.80	14.33
ET15G_V2	Pre-layout Schematic	16.615	330.0	145.15	-6.77	3.78	5.57
	Post-layout Extracted	15.110	486.5	126.60	-7.96	3.22	4.98
ET15G_V3	Pre-layout Schematic	15.174	1657.7	137.81	-7.22	5.72	3.33
	Post-layout Extracted	15.006	533.2	108.85	-9.28	4.63	2.56
BT15G	Pre-layout Schematic	14.235	450.0	141.61	-6.98	6.17	3.25
	Post-layout Extracted	15.175	280.0	117.72	-8.58	5.04	2.75

### 3.4 Simulation Results

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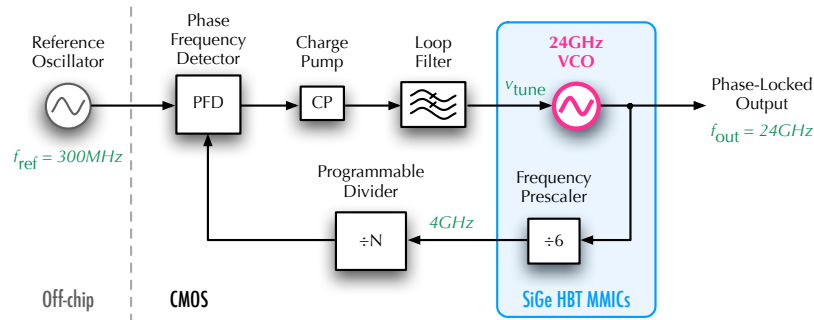
range, phase noise and power conversion efficiency. Their physical layout implementations are also more compact, reducing manufacturing costs and making them the best options for phase shifter integration. In general, layout parasitics adversely reduce centre frequency and output amplitude of the VCOs, yet positively effect phase noise and DC power consumption metrics, according to the simulation data. There remains open questions regarding the frequency tuning characteristics of ET15G\_V3 and the severe lack of tuning capability of the base-tuned VCO topology in BT15G. The results show that reducing the transistor's capacitive contribution to the resonant loop by reducing emitter size, and increasing the number of varactor anodes does not improve the tuning range as first thought.



# Chapter 4

## 24GHz Oscillator Implementation

This chapter documents the design, simulation and layout of a 24GHz differential cross-coupled VCO in a  $0.18\mu\text{m}$  SiGe BiCMOS technology. The VCO is a sub-circuit of the PLL system for 24GHz UWB automotive SRR as described in Section 1.2.2 and identified in the block diagram of Figure 4.1. Desired VCO attributes include accurate frequency synthesis, maximised tuning range, low phase noise and sufficient output voltage amplitude to drive the 1/6 frequency prescaler.

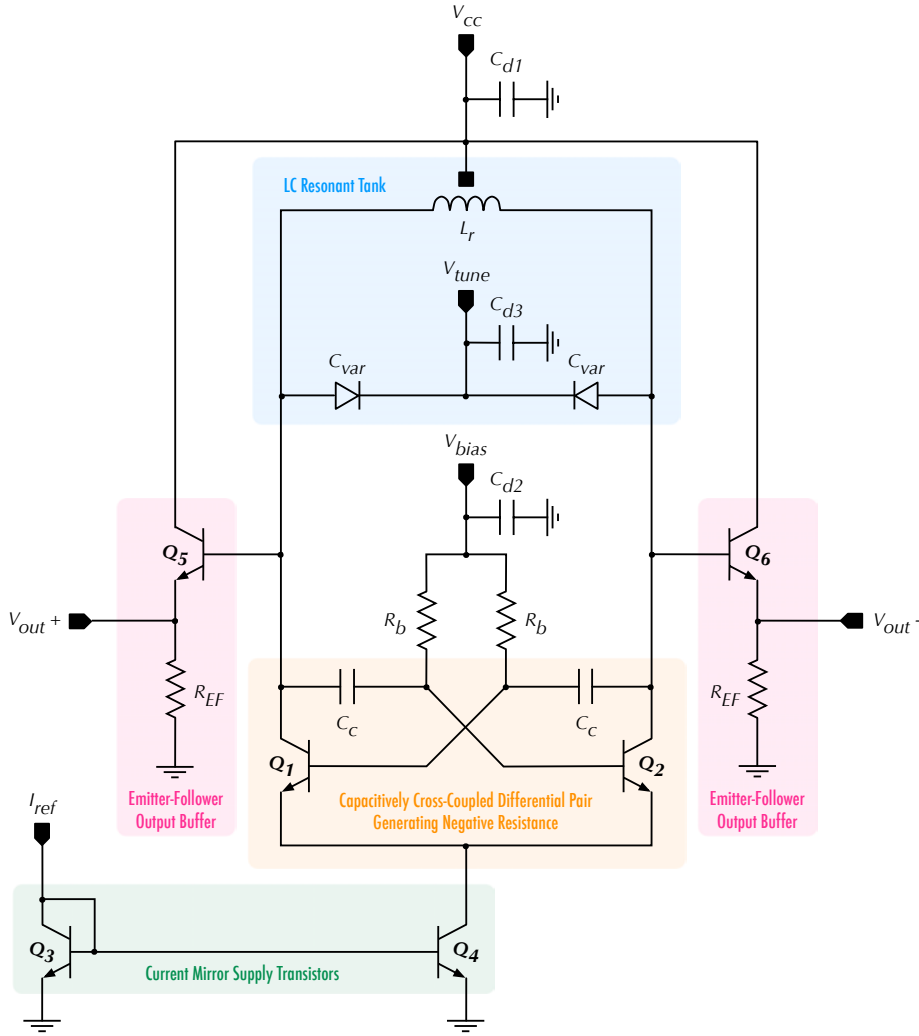


**Figure 4.1.** System diagram of the 24GHz PLL suitable for UWB automotive SRR applications, highlighting the 24GHz VCO designed in this chapter.

### 4.1 Differential VCO Topology

The differential cross-coupled bipolar VCO topology of Figure 4.2 is selected to provide the 24GHz local oscillator source within the PLL system. This fundamental VCO topology is

## 4.1 Differential VCO Topology



**Figure 4.2.** Schematic view of the 24GHz differential cross-coupled VCO core, emitter-follower output buffer design and active current mirror bias structure. C-B varactor diodes facilitate resonant tank tuning.

an industry proven monolithic topology with the benefit of compact layout implementation and high output power, however it heavily relies on the fabrication technology in terms of transistor gain and inductor quality factor at the oscillation frequency. The fully symmetric circuit exploits the advantages of reduced signal interference from the substrate and superior coupling of RF power to differential latch based frequency dividers. Initial schematic investigations revealed that an oscillation frequency of 24GHz is realisable in the available IBM BiCMOS7WL technology using a fundamental VCO topology and standard library active and passive devices without the need for custom designed and modelled elements such as transmission line. Generating 24GHz directly eliminates the need for frequency multipliers

which are expensive in terms of chip area due to the large number of inductors required, generate subharmonics in the output and have high power consumption.

The implemented VCO design consists of two core transistors  $Q_1$  and  $Q_2$  capacitively cross-coupled via  $C_c$  to create negative resistance looking into the collectors of the transistor pair as discussed in Section 2.2.2.  $C_c$  forms a capacitive divider in the feedback path to avoid heavy saturation of the transistors by isolating the base inputs, enabling greater swings and higher common-mode levels at the collector nodes [11]. The bias structure comprising  $V_{bias}$  and  $R_b$  sets the DC operating point of the core transistors relative to the supply voltage  $V_{cc}$  and  $V_{CE}$  of  $Q_4$ .  $V_{bias}$  must be sufficiently large such that transistors  $Q_1$  and  $Q_2$  operate in the forward active region, even under large signal oscillatory conditions.  $R_b$  must be large enough to isolate  $V_{bias}$  from potential RF feedback signals.

VCO oscillation frequency is governed by the parallel LC resonant tank comprising a single symmetric inductor,  $L_r$  with centre metal tap to the supply voltage and two C-B varactor diodes,  $C_{var}$  enabling frequency tuning. The symmetric inductor helps to eliminate device mismatch which would otherwise be present in two separate inductors. It also has a favourable higher Q characteristic and the centre tap reduces metal wiring and the number of vias required for layout interconnections, hence reducing parasitic effects. The single turn symmetric inductor also consumes far less chip surface area in comparison to two individually placed inductors. VCO symmetry facilitates small signal half-circuit analysis using virtual AC nodes created between the two varactor cathodes and at the centre tap of the inductor, to determine an expression for estimating the oscillation frequency,

$$\omega = \frac{1}{\sqrt{\frac{L_r}{2} \cdot C_r}}. \quad (4.1)$$

$C_r$  is the total tank capacitance including tunable varactors, cross-coupling capacitors and intrinsic transistor input capacitance expressed for the left-hand half circuit as (neglecting the effect of Miller capacitance  $C_\mu$  between collector and base),

$$C_r = C_{var} + C_{\pi 5} + \frac{C_c \cdot C_{\pi 1}}{C_c + C_{\pi 1}} \quad (4.2)$$

where  $C_{\pi 1}$  and  $C_{\pi 5}$  are the core and EF buffer transistor input capacitance respectively. It follows that the tuning range can be estimated using the equation,

$$f_\Delta = \frac{1}{2\pi \sqrt{\frac{L_r}{2} \cdot (C_{var_{min}} + C_{\pi 5} + \frac{C_c \cdot C_{\pi 1}}{C_c + C_{\pi 1}})}} - \frac{1}{2\pi \sqrt{\frac{L_r}{2} \cdot (C_{var_{max}} + C_{\pi 5} + \frac{C_c \cdot C_{\pi 1}}{C_c + C_{\pi 1}})}} \quad (4.3)$$

## 4.1 Differential VCO Topology

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where  $C_{var_{max}}$  and  $C_{var_{min}}$  are the maximum and minimum varactor capacitance bounds. Assuming that  $C_{var} \gg C_{\pi 5}$  and  $\frac{C_c \cdot C_{\pi 1}}{C_c + C_{\pi 1}}$ , a simplification of  $f_{\Delta}$  can yield useful theoretical estimations of the necessary device values, with further optimisation via simulation.

The current mirror composed of transistors  $Q_3$  and  $Q_4$  provides the VCO core tail current by replicating or multiplying the reference current  $I_{ref}$  depending on the size multiplicity of  $Q_4$  relative to  $Q_3$ . The tail current is used to set the optimum transistor DC operating point for maximum  $f_t$  and is split evenly between the two branches under DC conditions. Incorporating an emitter degradation resistor,  $R_E$  improves current matching between  $I_{ref}$  and  $I_{Q_4}$  and boosts small-signal output impedance of the current source, according to  $R_o \approx r_o(1 + g_m R_E)$  [41]. However, emitter degradation is not implemented due to its reduction of output voltage headroom. Current supply stability under large-signal operation further stipulates that  $V_{bias}$  must be sufficient to correctly bias both the core differential pair and current mirror while the reference current is supplied externally to the chip.

Identical EF output buffers constructed from  $Q_5$ ,  $Q_6$  and  $R_{EF}$  are added to provide a low output impedance to the following frequency divider circuitry or measurement equipment while minimising VCO core loading. Although EF amplifier gain is less than unity, their favourable high input impedance mitigates possible oscillation frequency shifts due to load pulling<sup>7</sup>. The emitter resistor  $R_{EF}$  must be optimised for maximum RF power transfer to the assumed  $50\Omega$  load and is most conveniently performed using parametric simulation techniques. Thoughtful emitter follower transistor sizing must be exercised since the input capacitance appears connected to the VCO resonant tank, thereby directly effecting the oscillation frequency.

Capacitors  $C_{d1}$ ,  $C_{d2}$  and  $C_{d3}$  serve as bypass capacitors to shunt unwanted AC noise superimposed on the voltage supply rails to ground. Supply rail impurities may manifest themselves as frequency spurs in the output spectrum and/or increased VCO phase noise, both of which detriment PLL low noise performance.

### 4.1.1 Biasing and Device Selection

Theoretical VCO biasing and device selection was first carried out, followed by verification and optimisation through schematic simulation. The optimised circuit, abbreviated by XC24G, has the device values as shown in Table 4.1.

High- $f_t$  SiGe NPN HBTs with emitter width  $W_e = 0.24\mu\text{m}$ , length  $L_e = 10\mu\text{m}$  and number of stripes  $N_e = 2$  were selected for transistors  $Q_{1-4}$  from the technology device library.

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<sup>7</sup>A phenomenon where VCO output load variation causes the input impedance to change. Thus  $f_{osc}$  must change to satisfy the varying conditions for oscillation in the negative-resistance model [42].

**Table 4.1.** Optimised 24GHz differential VCO device values and bias conditions.

<i>Device</i>	<i>Properties</i>	<i>Value</i>
$Q_{1-4}$	High- $f_t$ NPN HBT: $W_e \times L_e, N_e$	$0.24\mu m \times 10\mu m, 2$
$Q_{5-6}$	High- $f_t$ NPN HBT: $W_e \times L_e, N_e$	$0.24\mu m \times 20\mu m, 2$
$C_{d1}$	$V_{cc}$ supply decoupling	$3.26pF$
$C_{d2}$	$V_{bias}$ supply decoupling	$3.26pF$
$C_{d3}$	$V_{tune}$ supply decoupling	$3.26pF$
$C_c$	C-B feedback + DC decoupling	$201fF$
$C_{var}$	Tuning varactor capacitance	$564 \rightarrow 366fF$
$R_b$	Base bias voltage feed	$1k\Omega$
$R_{EF}$	Emitter-follower load	$300\Omega$
$L_r$	Resonant tank inductance	$139.5pH$
$V_{bias}$	Base bias voltage	$+1.4V$
$V_{cc}$	Supply rail voltage	$+1.8V$
$V_{tune}$	$C_{var}$ tuning voltage	$1.8 \rightarrow 4.8V$
$I_{ref}$	Current mirror reference	$4mA$

Specific emitter size and subsequent collector bias current for maximum  $f_t$  performance were determined with reference to the  $f_t$  characteristics presented in the technology design manual and shown in Figure 2.16. Transistors  $Q_1$  and  $Q_2$  are biased with a collector current equal to 4mA – half of the tail current of the differential pair under DC conditions.  $Q_4$  has a multiplicity of two, providing a current multiplication of the reference current  $I_{ref} = 4mA$ , generating 8mA as the tail current. The emitter-follower output buffer transistors  $Q_5$  and  $Q_6$  are also high- $f_t$  NPN HBTs with  $W_e = 0.24\mu m$  and  $L_e = 10\mu m$  to reduce distortion components evident in the output.

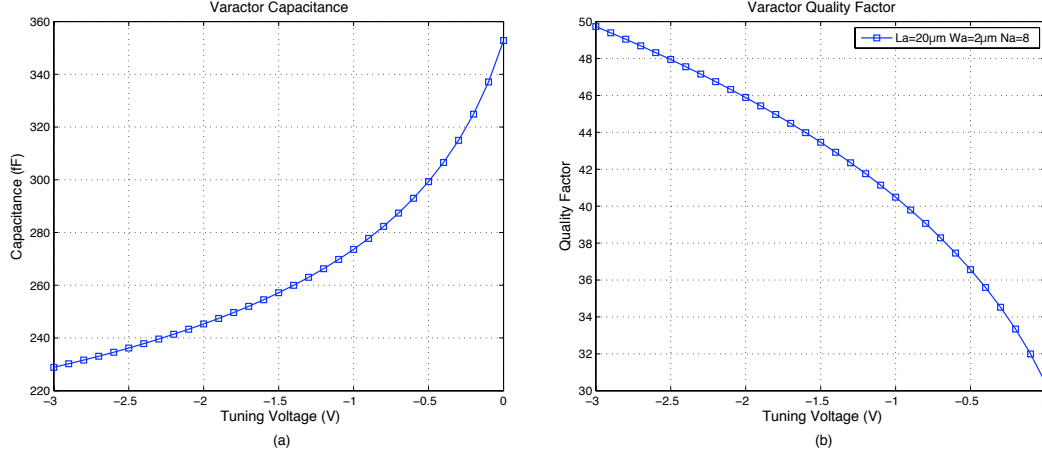
Given a supply rail voltage of  $V_{cc} = 1.8V$ , the core bias voltage  $V_{bias}$  is set to  $1.4V \approx 2 \times V_{BE}$  to ensure  $Q_{1-2}$  and  $Q_4$  are on while maintaining approximately 400mV of differential oscillation headroom. Under DC conditions, the varactor anodes are at  $V_{cc}$  potential and since the medium performance NPN emitter-base breakdown voltage is 3V, this leads to a voltage tuning range  $1.8V \leq V_{tune} \leq 4.8V$ .

MIM decoupling capacitor values,  $C_{d1}$ ,  $C_{d2}$  and  $C_{d3}$  were selected in the order of 3pF to provide a compromise between low RF impedance and layout area.

The cross-coupled feedback capacitance,  $C_c$  is determined by simulation such that it adequately DC decouples the base of each transistor from the collector of the other while minimally impacting the accumulated resonant tank reactance.

## 4.1 Differential VCO Topology

The varactors have standard anode size of  $L_a \times W_a = 20\mu\text{m} \times 2\mu\text{m}$  with anode count  $N_a = 8$  and operated in reverse bias mode. Varactor capacitance range and Q characteristics were obtained using the technique described in Section 3.2.1 and appear in Figure 4.3. The



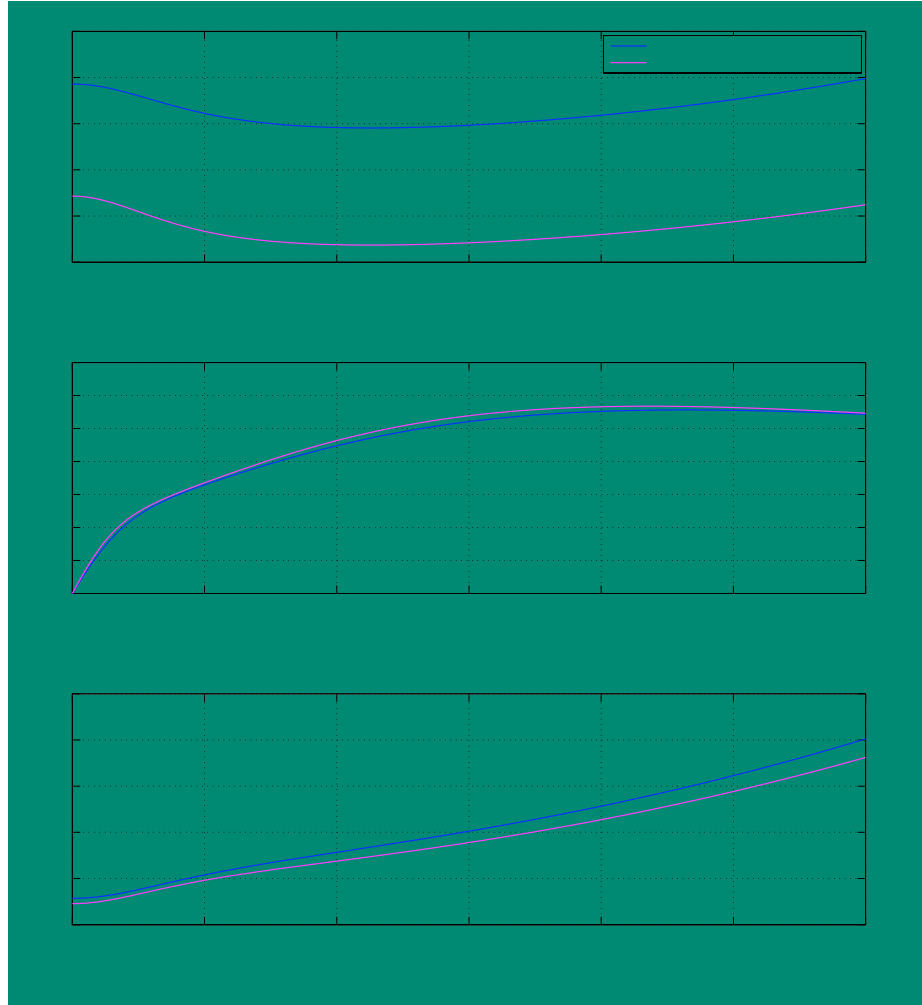
**Figure 4.3.** S-parameter simulation of varactor: (a) capacitance and (b) quality factor at 24GHz as a function of applied reverse bias potential,  $V_{ac}$ .  $L_a$  = varactor anode length,  $W_a$  = anode width and  $N_a$  = number of anodes.

resultant capacitance tuning ratio is  $C_{V_{ac}=0V} : C_{V_{ac}=-3V} = 1.54 : 1$  with Q ranging from  $Q_{V_{ac}=0V} = 19$  to  $Q_{V_{ac}=-3V} = 31$  at 24GHz. Simulation of the VCO oscillation frequency was used to determine the number of varactor anodes required given the value of  $L_r$  in the resonant tank. By orientating each varactor such that its cathode is connected to virtual AC ground, the Q of the device is maximised due to the subcollector to substrate capacitance [35].

$L_r$  is a symmetric single turn inductor over a crosshatch pattern of deep trench isolation, selected in conjunction with  $C_{var}$  to yield an oscillation frequency as close as possible to 24GHz. S-parameter simulation was used to generate the inductance, Q and series resistance characteristics shown Figure 4.4. The plots indicate an inductance of 139.5pH, a Q of 24 and series loss resistance of 872m $\Omega$  at 24GHz. The geometry of this inductor is approaching the minimum realisable inductance of the available library devices. If a significantly smaller inductance were required, custom transmission line would need to be designed and modelled accordingly.

Parametric analysis on the emitter-follower resistance  $R_{EF}$  from 100 $\Omega$  to 1k $\Omega$  indicates an optimum value of 300 $\Omega$  with respect to output voltage swing and RF output power.

The multitude of simulations carried out in the optimisation process identified the following device and performance interdependencies, which require compromise in the VCO design.



**Figure 4.4.** S-parameter simulation of the 24GHz VCO resonant tank inductor: (a) inductance, (b) Q and (c) series loss resistance, as a function of frequency.  $X$  = spiral outer diameter,  $W$  = spiral width,  $s$  = turn separation and  $n$  = number of turns.

- Larger  $L_r$  greatly increases the VCO output voltage swing, however to obtain a frequency of 24GHz the varactors have to be minimum size. Therefore a compromise between tuning range and output power exists.
- The size of the EF transistors influences the level of distortion in the output signal. Of course, increasing transistor size also increases the fixed capacitance contribution of the output buffers to the resonant tank capacitance. Hence detuning the oscillation frequency and reducing achievable tuning range.
- Increasing the output buffer transistor size increases the differential output swing and improves the VCO phase noise performance.

## 4.2 Circuit Layout

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- Doubling EF transistor emitter length ( $L_e$ ) appears to have less effect on de-tuning the VCO than increasing the multiplicity of the transistors. Therefore, there must be more capacitance associated with multiple device instantiations rather than increasing emitter area.
- Optimising  $R_{EF}$  with respect to RF output power does not give the best simulated phase noise performance. Increasing  $R_{EF}$  from the value at maximum  $P_{out}$  improves the phase noise by approximately  $-1\text{dBc/Hz}$  per  $100\Omega$ . However, since the phase noise simulation techniques appear to be dubious at times, the value of  $R_{EF}$  was selected for maximum output voltage swing and hence output power.

## 4.2 Circuit Layout

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Layout of the 24GHz differential cross-coupled VCO was generated with strict adherence to industry standard RF layout techniques. Aside from the bias structures, the differential nature of the VCO core was exploited in a fully symmetric layout as shown in Figure 4.5. Symmetry fosters improved device matching, optimally balanced loading of the active devices, equal output amplitude and hence accurate  $180^\circ$  phase relation between differential outputs.

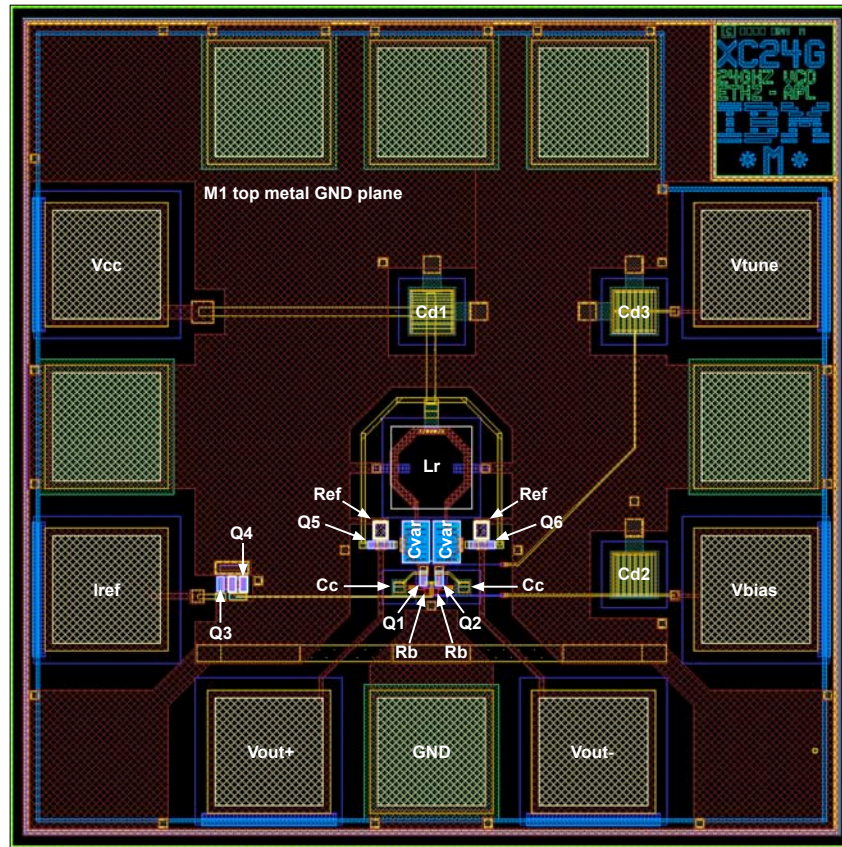
Current analysis at all circuit nodes facilitated accurate metal sizing and the design of via interconnections to comply with the process current density requirements. Failure to provide the necessary current carrying capacity could lead to performance degradation, overheating, open circuits as a result of wire burn out and in the severe case, chip breakdown.

The compact layout minimises wiring parasitics on both VCO core branches which would otherwise alter the total tank reactance. Close parallel routing of high frequency signals was strictly avoided. Where absolutely necessary, wires cross on different metal layers at right angles so as to minimise cross-coupled interference which could be manifested as additional VCO noise sources.

A top metal ground plane was incorporated to provide the best possible common ground node for measurement, proper substrate connection to ground, shielding against RF signal cross-coupling and reduce inter-layer parasitic capacitance.

Bond pads over deep trench isolation were placed at minimum pitch around the core perimeter and in accordance with the mechanical constraints of the wafer measurement apparatus. Although the top three bond pads are all connected to the ground plane, they are necessary to satisfy metal density rules and offer additional grounding options for chip bonding. The orientation of RF input and output pads was carefully considered with respect to linear





**Figure 4.5.** XC24G 24GHz differential cross-coupled VCO layout cell view with annotated device labels – chip area  $776\mu\text{m} \times 776\mu\text{m}$ .

signal flow through the chip, minimising corruption from noisy DC power supply wires. The VCO core is orientated to minimise the length of RF wires to the bond pads. At microwave frequencies, signal degradation over long wire lengths can be significant due to transmission line effects such as electromagnetic (EM) radiation, reflection and matching. The symmetrical centre tapped inductor,  $L_r$  greatly reduces the area occupied by the VCO core, resulting in a pad limited total chip area of  $776\mu\text{m} \times 776\mu\text{m}$ .

#### 4.2.1 Layout Parasitic Extraction

Analog parasitic resistance and capacitance were extracted from the VCO layout (including metal density fill) and back-annotated into the circuit schematic. Unfortunately, the design kit did not allow extraction of parasitic inductance, therefore, some discrepancy is expected between post-layout simulated and measured performance. Post-layout simulations were performed on the extracted schematic and appear in Section 4.3 in conjunction with pre-layout simulation results for comparison.

### 4.3 Simulation Results

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Post-layout simulations resulted in a minor schematic modification with respect to the spiral width of the resonant tank inductor  $L_r$ , to increase the oscillation frequency and centre the tunable range around 24GHz. Table 4.2 summarises the modifications while the inductance, quality factor and series resistance characteristics of the new device are included in Figure 4.4. All pre and post-layout simulated VCO results reported in this chapter incorporate this  $L_r$  instance change.

**Table 4.2.**  $L_r$  schematic modifications resulting from post-layout simulations, to fine tune the XC24G fundamental frequency. The original and updated device attributes are included.

<i>Dimensions</i>	<i>Version</i>	$L_r$ (nH)	$R$ ( $\Omega$ )	$Q$	$f_{peak\ Q}$ (GHz)
$75\mu m \times 5.52\mu m \times 1$	Original	139.5	872.1	24.13	61.95
$75\mu m \times 6.8\mu m \times 1$	Updated	126.9	764.7	25.02	66.97

### 4.3 Simulation Results

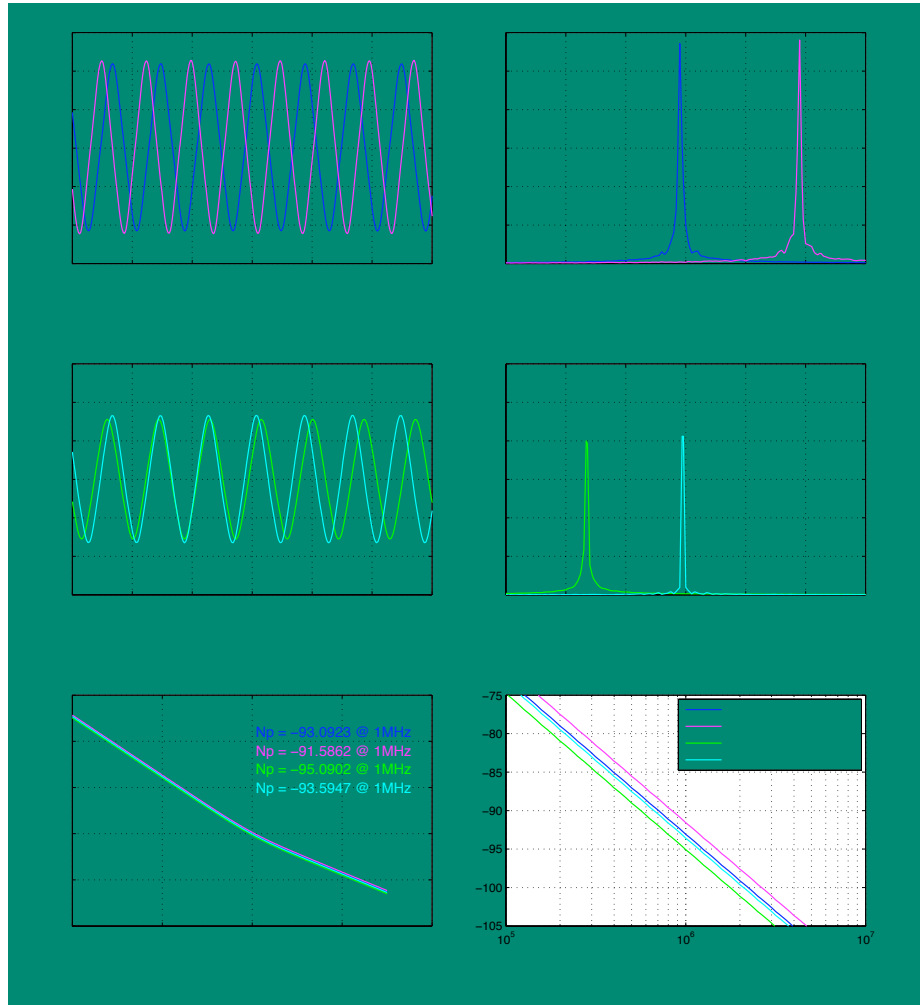
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Transient, PSS and Monte Carlo simulation methods were used to investigate VCO output and tuning performance. A component of the PSS simulation was also used to evaluate single-sided VCO phase noise characteristics relative the the fundamental oscillation frequency.

#### 4.3.1 VCO Output and Phase Noise

Time domain waveforms of the optimised 24GHz VCO schematic were obtained using transient simulation of the differential output voltage signal at the tuning voltage limits,  $V_{tune} = 1.8V$  and  $4.8V$ . The results are displayed in Figure 4.6(a) and (c) and represent constant amplitude sinusoids. A windowed FFT function was used to generate the frequency domain plots of each waveform shown in Figure 4.6(b) and (d), revealing upper and lower oscillation frequency bounds. Comparing FFT plots gives useful insight into the detuning effects of layout parasitics on the VCO resonant frequency and the reduction in output signal magnitude.

Simulated VCO phase noise characteristics are shown in Figure 4.6(e) and (f), as a function of carrier offset frequency. At the commonly quoted 1MHz offset frequency the graphs reveal an approximate 2dBc/Hz improvement post-layout. Notably, phase noise is better than 91.5dBc/Hz for all simulations and layout has not drastically effected this performance measure. A summary of simulated output amplitude, oscillation frequency and phase noise metrics is presented in Table 4.3.



**Figure 4.6.** Simulated XC24G output time domain waveforms, frequency spectrum and phase noise at the tuning voltage limits,  $V_{tune} = 1.8V$  and  $4.8V$ : (a) & (b) pre-layout schematic, (c) & (d) post-layout analog extracted and (e) & (f) pre and post-layout phase noise relative to the 24GHz fundamental.

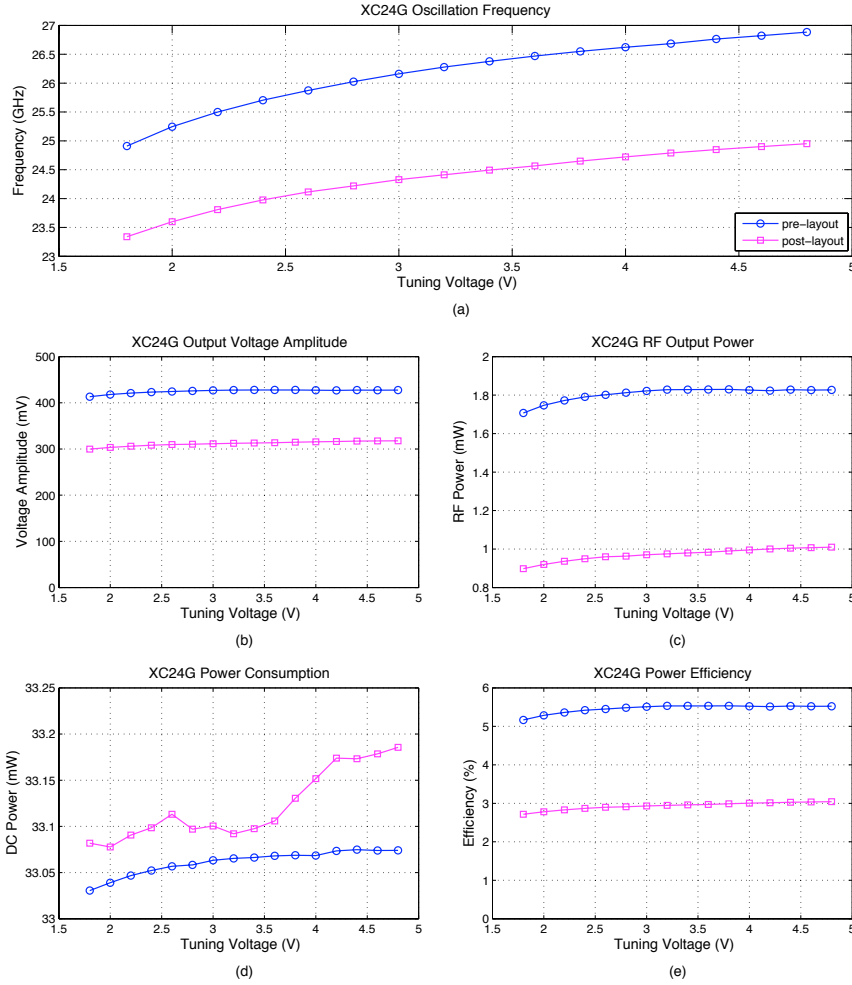
**Table 4.3.** Simulated XC24G pre-layout schematic and post-layout analog extracted output characteristics at the tuning voltage limits,  $V_{tune} = 1.8V$  and  $4.8V$  assuming an output load,  $R_{load} = 50\Omega$ . Phase noise is measured at  $\Delta\omega = 1MHz$  offset from the carrier.

<i>MMIC</i>	<i>Cell View</i>	$V_{tune}$ (V)	$v_{out}$ (mV)	$f_{osc}$ (GHz)	$\mathcal{L}(\Delta\omega)$ (dBc/Hz)
XC24G	Pre-layout Schematic	1.8	435.108	24.9	-93.09
		4.8	451.643	26.9	-91.59
	Post-layout Extracted	1.8	311.636	23.34	-95.09
		4.8	332.092	24.96	-93.59

## 4.3 Simulation Results

### 4.3.2 VCO Tuning Characteristics

VCO tuning characteristics were obtained using a parametric simulation technique which involved increasing  $V_{tune} = 1.8V$  to  $4.8V$  in  $+0.2V$  increments and recording oscillation frequency, output voltage amplitude, RF output power, power consumption and power conversion efficiency. The resultant data is plotted against the tuning voltage in Figure 4.7.



**Figure 4.7.** Simulated XC24G pre-layout schematic and post-layout analog extracted performance characteristics over the tuning voltage: (a) frequency tuning range, (b) output amplitude, (c) RF power output, (d) DC power consumption and (e) power conversion efficiency.

It can be seen from the simulations that the VCO possesses a continuous and relatively linear frequency tuning range that importantly encompasses 24GHz after circuit layout. Post-layout results demonstrate a downward shift of the VCO centre frequency by approximately 1.75GHz

such that 24GHz is in the centre of the predicted tuning range. Differential output voltage amplitude and RF power output remain relatively constant over the tuning range with a slight increase in both as  $V_{tune}$  increases. VCO output amplitude is greater than 300mV with a maximum DC power consumption of 33.19mW at  $V_{tune} = 4.8V$ . All characteristics suffer notable degradation when accounting for layout non-idealities. In particular the RF output power is practically halved, while the DC power consumption slightly increases, leading to the significant reduction in conversion efficiency. A summary of VCO performance metrics averaged over the tuning range appear in Table 4.4.

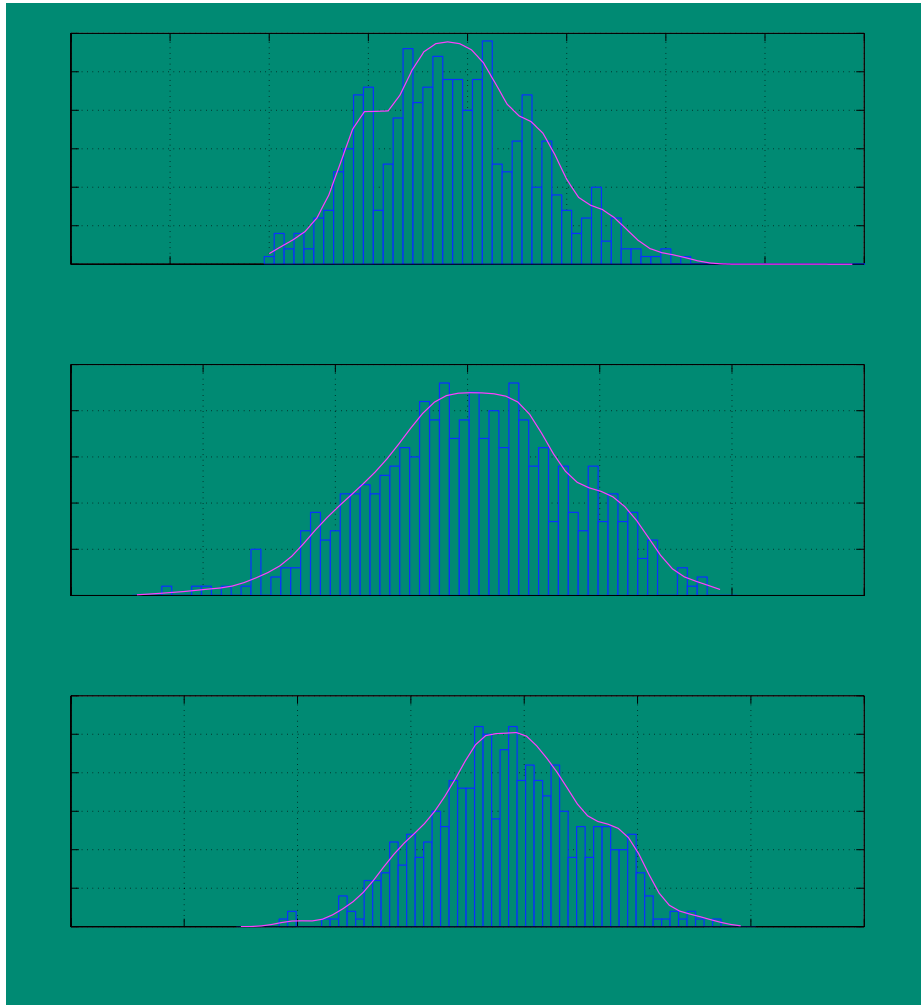
**Table 4.4.** Simulated XC24G pre-layout schematic and post-layout analog extracted performance metrics over the tuning range,  $V_{tune} = 1.8 \quad 4.8V$  including: centre oscillation frequency ( $f_{osc}$ ), frequency tuning range ( $f_{\Delta}$ ) and averaged values of output voltage ( $v_{out}$ ), RF power ( $P_{out}$ ), DC power consumption ( $P_{DC}$ ) and power conversion efficiency ( $\eta$ ).

<i>MMIC</i>	<i>Cell View</i>	$f_{osc}$ (GHz)	$f_{\Delta}$ (GHz)	$v_{out}$ (mV)	$P_{out}$ (dBm)	$P_{DC}$ (mW)	$\eta$ (%)
XC24G	Pre-layout Schematic	25.896	1.9754	424.97	2.5668	33.061	5.463
	Post-layout Extracted	24.145	1.611	311.62	-0.1285	33.122	2.933

### 4.3.3 Monte Carlo Analysis

Monte Carlo simulation is a tool used to verify the functionality of integrated circuits. It generally involves performing multiple simulations of a circuit for different combinations of temperature, process and device matching variation. Circuit attributes of interest can be plotted to determine statistical characteristics such as mean, standard deviation, etc. This simulation technique is essential for integrated circuits intended for large scale production where chip performance must meet the design specifications governed by strict environmental and regulatory conditions and to maximise chip yield across wafer runs. High yield leads to high utilisation of manufacturing expenses, lower cost per chip and ultimately greater potential for economic success. Due to the large number of simulations involved, the analysis is by nature very time consuming and often not feasible to perform on post-layout schematics including extracted parasitics.

Monte Carlo statistical analysis was performed on the final VCO schematic under normal DC bias conditions and  $V_{tune} = 1.8V$ , with 500 iterations of process and device matching variation at 27°C nominal temperature. Figure 4.8 displays the frequency of occurrence distributions for VCO oscillation frequency, differential output voltage amplitude and output



**Figure 4.8.** XC24G process and matching Monte Carlo simulations (500 iterations at 27°C nominal temperature) of: (a) oscillation frequency, (b) differential output voltage and (c) output power.

power. Assuming the metrics approximate Normal or Gaussian distribution, the mean, standard deviation and three-sigma confidence intervals can be calculated and appear in Table 4.5.

Unfortunately due to the time consuming nature of Monte Carlo simulations the analysis was only performed on the pre-layout schematic and at a single value of  $V_{tune} = 1.8V$ . Ideally, the analysis should be performed at both VCO control voltage extremes and the oscillation frequency evaluated to always lie below 24GHz for one extreme and always above for the other. Therefore, the VCO tuning range requirement can be defined by the desired tuning range plus tuning margin to cover process variation.

**Table 4.5.** XC24G Monte Carlo analysis statistics including mean ( $\mu$ ), standard deviation ( $\sigma$ ) and three-sigma confidence intervals ( $\mu \pm 3\sigma$ ) for oscillation frequency ( $f_{osc}$ ), differential output voltage amplitude ( $v_{out}$ ) and output RF power ( $P_{RF}$ ).

<i>Metric</i>	$\mu$	$\sigma$	$\mu \pm 3\sigma$
$f_{osc}$	24.948GHz	400.61MHz	23.746GHz : 26.150GHz
$v_{out}$	440.986mV	14.660mV	397.008mV : 484.965mV
$P_{RF}$	2.178mW	135.669 $\mu$ W	1.771mW : 2.585mW

The three-sigma rule or 68-95-99.7 rule states that for a normal distribution, 99.7% of the values lie within three standard deviations of the mean value ( $\mu \pm 3\sigma$ ), 95% lie within two standard deviations of the mean ( $\mu \pm 2\sigma$ ) and 68% lie within one standard deviation of the mean ( $\mu \pm \sigma$ ). Considering that the post-layout simulated VCO tuning range is  $f_{\Delta} = 1.611\text{GHz}$  and the three-sigma variation in output frequency is 2.4GHz, Monte Carlo analysis suggests that there may be a significant number of VCOs that can not be tuned to 24GHz.

Without performing Monte Carlo analysis on the parasitic extracted VCO and at the other tuning voltage extreme  $V_{tune} = 4.8\text{V}$ , it is difficult to accurately calculate chip yield. However, utilising the available data for  $V_{tune} = 1.8\text{V}$ , the output frequency condition that still allows VCO tuning to 24GHz is defined by,

$$24\text{GHz} - f_{\Delta} \leq f_{osc} \leq 24\text{GHz} \quad (4.4)$$

where  $f_{\Delta} = 1.611\text{GHz}$  is the post-layout simulated total tuning capability from Table 4.4. The condition then equates to,

$$22.389\text{GHz} \leq f_{osc} \leq 24\text{GHz}. \quad (4.5)$$

Assuming that the pre-layout simulated Monte Carlo mean statistic suffers an equivalent 1.75GHz of frequency detuning as the VCO centre frequency,  $f_{osc}$  in Table 4.4, then an estimate of the post-layout mean would be,  $\mu^* = \mu - 1.75\text{GHz} = 23.198\text{GHz}$ . Thus, the condition defined in Eq. (4.5) falls almost exactly in the region,

$$f_{osc} = \mu^* \pm 2\sigma \quad (4.6)$$

$$= 23.397\text{GHz} \quad 23.999\text{GHz} \quad (4.7)$$

assuming the standard deviation ( $\sigma$ ) for pre and post-layout Monte Carlo  $f_{osc}$  distributions are equal. Therefore, the estimated yield of VCOs that can be tuned to 24GHz is 95%. Based on this analysis, the majority of fabricated VCOs should achieve 24GHz operation.

### 4.3 Simulation Results

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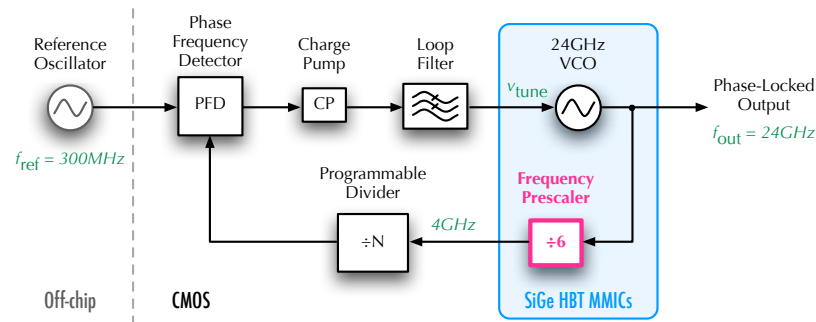
The output voltage distribution and three-sigma confidence interval predict that 100% of the VCOs should produce a differential output voltage greater than the specified minimum of 200mV to drive the frequency prescaler.



# Chapter 5

## Frequency Prescaler Implementation

This chapter documents the design, simulation and layout of a 1/6 synchronous static frequency prescaler in a 0.18 $\mu\text{m}$  SiGe BiCMOS technology operating at 24GHz. The prescaler is a sub-circuit of the PLL system as described in Section 1.2.2 and identified in the system block diagram of Figure 5.1. Desired prescaler attributes include broad band frequency operation, high input level sensitivity at 24GHz, low noise performance and sufficient output voltage to drive the following programmable divider.



**Figure 5.1.** System diagram of the 24GHz PLL suitable for UWB automotive SRR applications, highlighting the frequency prescaler designed in this chapter.

### 5.1 1/6 Synchronous Static Frequency Prescaler

There are two prominent frequency prescaler (or divider) topologies presently used in the microwave frequency realm – namely static and dynamic. Refer to Section 2.4 for a detailed

## 5.1 1/6 Synchronous Static Frequency Prescaler

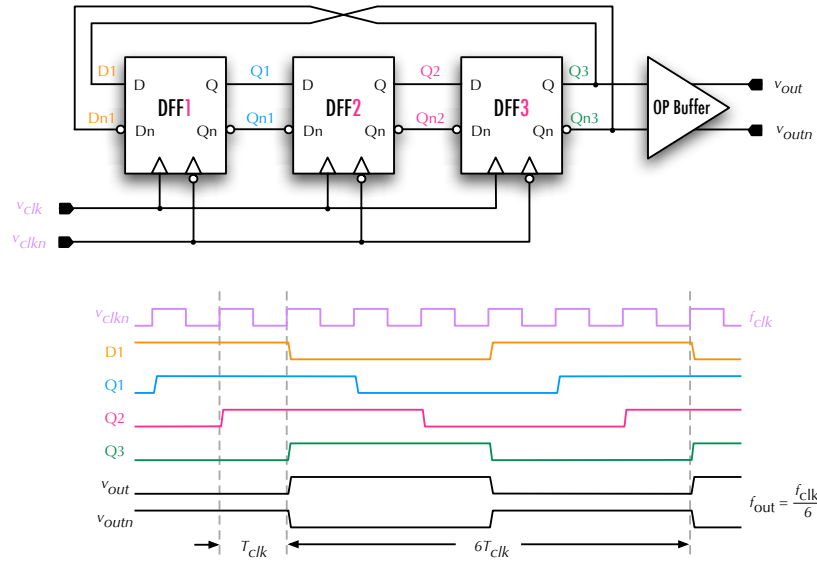
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treatment of the theory of operation of the two divider types. The following discussion will concentrate on the implemented design and summarise the foreseen advantages and disadvantages.

Static frequency dividers typically have a greater operational bandwidth compared to dynamic designs. Bandwidth is closely linked to the ability of the PLL to achieve the locked state after frequency perturbation. Dynamic dividers however, can generally operate at higher frequencies. As such, very high frequency divider designs often incorporate a dynamic first stage succeeded by multiple static stages. This approach helps to mitigate the high power consumption of fully static ECL latch based dividers at the expense of increased jitter (phase noise) accumulation.

The implemented frequency divider topology for this PLL application is the synchronous static divider architecture as illustrated in Figure 5.2. The divider core consists of three ( $n = 3$ ) series connected negative edge triggered DFFs, therefore generating a division ratio 6:1 ( $2n:1$ ). An EF based Darlington output buffer amplifier is incorporated to provide a high input impedance to the final DFF output and a low output impedance. The voltage gain of the buffer is less than one, however it aids in the transfer of power to the load via improved matching and reduces the influence of external loading (bond wires, AC coupling capacitors or the input impedance of the following circuitry) on prescaler operation and speed. The timing diagram in Figure 5.2 demonstrates DFF switching within the divider core and generation of the output frequency,  $f_{out} = f_{clk}/6$ .

A fully synchronous static divider core was preferred over an asynchronous approach since each DFF output is simply a shifted version of the same 1/6 divided output waveform. As such, the input frequency is simultaneously applied to the clock inputs of each flip-flop such that the stage delay and jitter do not accumulate through each succeeding stage. Assuming that signal wiring delays are minimised through careful layout planning, the output waveform should theoretically only suffer from the delay of a single DFF element and exhibit jitter performance corresponding to the input clock – the VCO output. This in turn minimises the amount of phase noise contributed by the frequency divider to the overall system phase noise and jitter. A static DFF divider is also easily increased to higher order division ratios by adding additional DFFs in the chain, provided that the propagation delay through each DFF including input and output wiring is less than the input clock period. As the DFF count increases so too does the feedback wiring length from the final stage output to the input. This can add significant signal delays and is highly dependent on how compact the circuit can be laid out and the number of metal layers available for wiring.



**Figure 5.2.** 1/6 synchronous static frequency prescaler structure composed of three series connected DFF stages with the output inverted and fed back to the first stage. The input frequency is simultaneously applied to the clock inputs of each DFF such that stage delay and jitter do not accumulate with each additional division stage. The waveform diagram illustrates generation of the output signal with a period of  $6T_{clk}$ , and hence frequency  $f_{out} = f_{clk}/6$ .

Static dividers developed using bipolar technologies generally achieve faster switching speeds, however their constant leakage current leads to higher current consumption compared to equivalent CMOS implementations, regardless of the operational state. On the other hand, this relatively constant current draw means lower switching noise induced on chip than CMOS designs where on-off states (and hence transitions from zero to maximum current consumption) fluctuate at the clock frequency.

A synchronous divider topology is also expected to exhibit high power consumption since all constituent D-latch circuits are switching at the input clock frequency of 24GHz. This is opposed to an asynchronous topology where following division stages would operate at divided down versions of the input signal frequency ( $f_{clk}/2$ ,  $f_{clk}/4$ , etc.).

A disadvantage of the synchronous divider structure is that the input signal, which is essentially the VCO output, is connected in parallel to three DFF stages. Therefore the effective loading placed on the VCO is three times that of an equivalent asynchronous divider topology. Therefore the VCO must be capable of providing sufficient output voltage swing to drive this heavy, predominantly capacitive load without load-pulling taking effect. Designing for maximum prescaler sensitivity around 24GHz will relax the driving capability requirements on the VCO.

## 5.1 1/6 Synchronous Static Frequency Prescaler

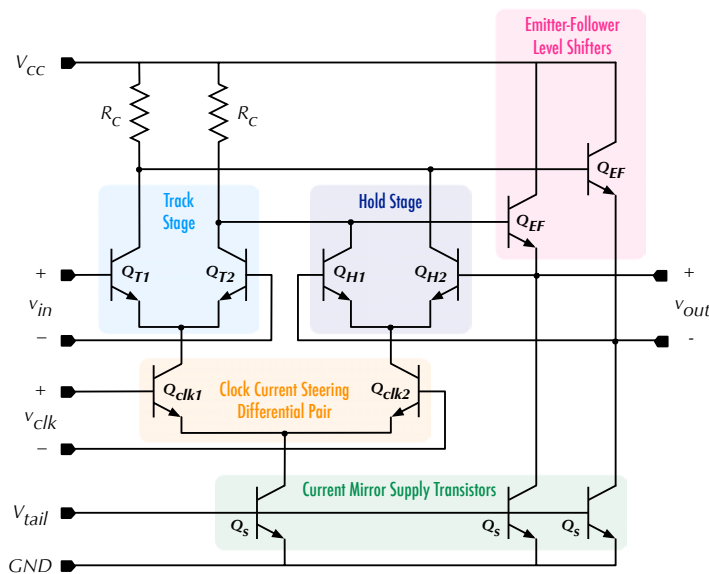
The following sub-sections describe the cellular design of the prescaler building blocks: the D-latch, DFF, output buffer amplifier and bias networks.

### 5.1.1 ECL D-latch Construction

The static divider core, with the exception of its output buffer, can be thought of as being constructed from a single elementary subcircuit - the ECL<sup>8</sup> D-latch.

ECL is the term given to a family of circuits composed of bipolar transistors and designed to perform logic functions via current steering. The transistors are arranged in differential pair configuration and biased such that they are always in the active region. Thus the transistors and resultant ECL based circuits can operate at very high speeds. A disadvantage of the ECL D-latch is that it is continuously drawing current which leads to high power consumption.

The D-latch circuit implemented in the static prescaler design is shown in Figure 5.3. The



**Figure 5.3.** ECL D-latch circuit schematic indicating sample and hold differential pair stages, current mirror supply transistors and emitter-follower level shifters.

schematic consists of two differential pair stages (track and hold) that are switched between active and inactive modes via the clock current steering differential pair. The exact output voltage swing is determined by the choice of load resistance  $R_C$  and the supply current provided by the lower current mirror transistors. Two transistors in EF configuration increase the speed of the switching pair transitions by reducing possible transistor saturation,

<sup>8</sup>Also known as Current Mode Logic (CML).

to achieve the highest possible operating frequency. The EFs also perform voltage level shifting of the output signals to ensure that following cascaded D-latches are all driven at the same input voltage point, whilst decreasing the output impedance and increasing the driving capability, or fan-out. Unfortunately, EFs adversely increase the overall power consumption of the latch and add to the differential inverter gate delay.

Inductive peaking can be exploited by inserting inductors in series with the  $R_c$  resistors of the track differential pair to increase D-latch speed, however this would significantly increase circuit area and hence inter-latch wiring lengths. Signal delays associated with the additional wiring and layout parasitics would therefore negate the benefits of this technique for multi-stage designs.

### D-latch Operation

The ECL D-latch circuit described above functions as a temporary bit-storage element and can be regarded as a clocked 1-bit memory. Basically, the output port  $v_{out}$  tracks the data signal level presented at the input port  $v_{in}$  during the positive clock half period via the track differential stage. In the negative half period the cross-coupled hold differential stage utilises positive feedback to hold  $v_{out}$  at the value of  $v_{in}$  present just before the negative clock transition. These two modes of operation are referred to as track and hold phases. Figure 5.4 graphically illustrates ECL D-latch operation while the text below explains the mechanism in detail.

1. Figures 5.4 (a) and (c) represent the track mode of operation where the clock signal is logic level high,  $v_{clk} > 0$ , turning on transistor  $Q_{clk1}$  and activating the left differential stage. The supply current  $I_s$  is switched through the left D-latch branch creating a voltage potential  $v_T$  which follows the input signal  $v_{in}$  after the inherent gate delay. The output  $v_{out}$  is simply the value of  $v_T$  shifted down by the base-emitter voltage of the EFs. In this mode the latch acts transparently since the output follows the input.
2. Figures 5.4 (b) and (d) represent the hold or latch mode of operation where the clock signal is logic level low,  $v_{clk} < 0$ , turning on transistor  $Q_{clk2}$  and activating the right differential stage. The left differential stage is inactive, decoupling the input signal from the latch. The value of  $v_T$  just before the negative clock transition is temporarily stored on the base-collector capacitance of the left differential stage. A positive feedback loop connection of the right differential stage creates a bistable memory circuit continuously storing the state of  $v_T$  before the negative clock edge. The output  $v_{out}$  is therefore held or latched at the input level of the previous clock phase, shifted down by the base-emitter voltage of the EFs.

## 5.1 1/6 Synchronous Static Frequency Prescaler

3. Figure 5.4 (e) gives an example of D-latch operation, showing the circuit mode in each clock half-cycle and clearly illustrates latch transparency during track mode.

Maximisation of D-latch switching speed is key in the design of a synchronous static divider at 24GHz. Any delays generated by the latch and associated wiring parasitics cause an increase in the overall signal propagation delay, potentially making the desired division ration unobtainable. It is also critical that the latching of the hold differential stage is fast enough to capture the input from the track stage before it returns to zero.

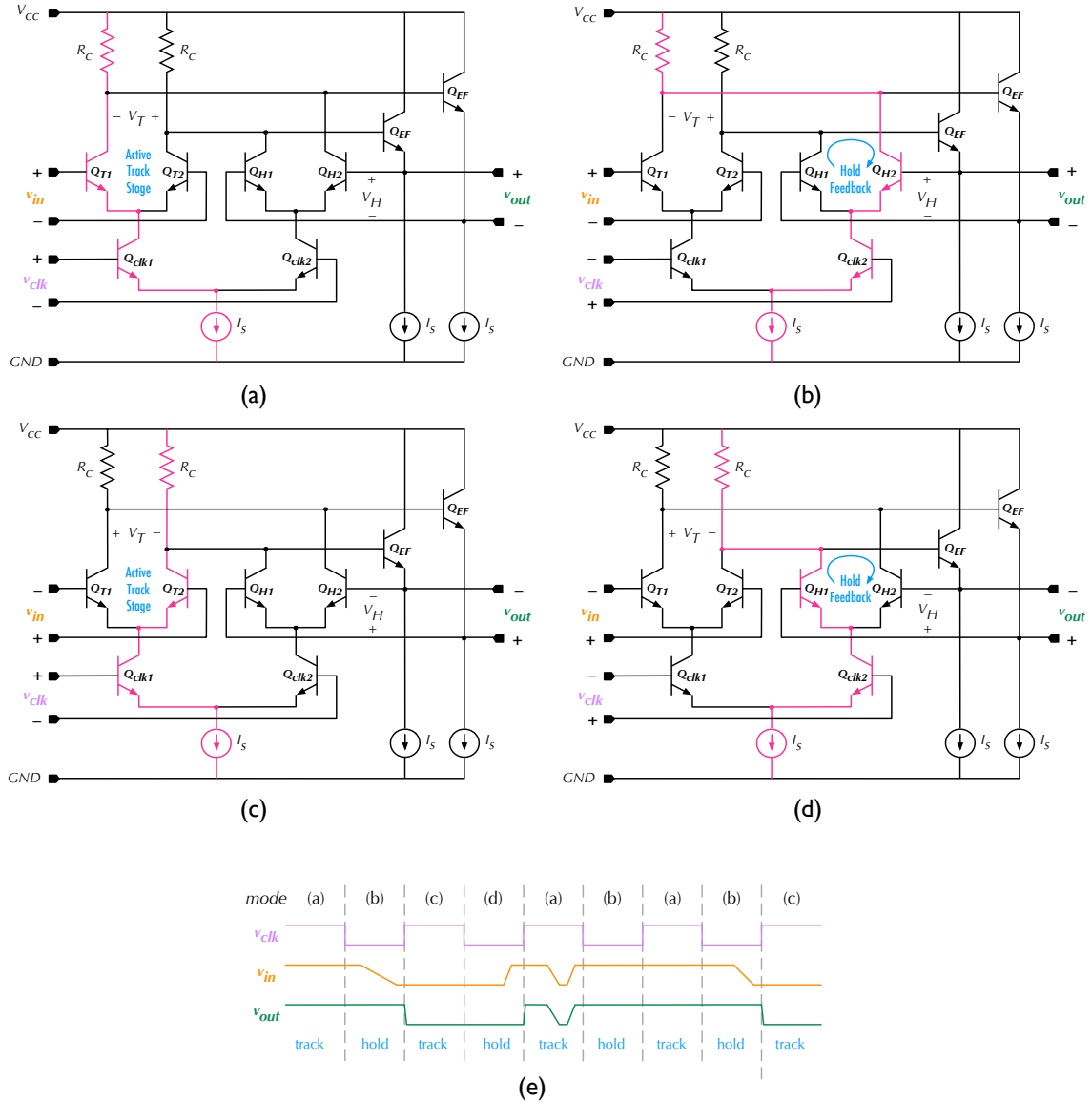
### D-latch Component Selection and Biasing

With the prescaler topology defined, the design focus is on achieving maximum speed and sensitivity over a broad frequency range also amidst process and matching variation. This relies on the optimisation of the D-latch design in terms of switching speed, biasing and propagation delay. The process of D-latch device selection and biasing is as follows, with reference to the schematic in Figure 5.3 and Table 5.1.

**Table 5.1.** Prescaler device values and bias conditions.

<i>Device</i>	<i>Properties</i>	<i>Value</i>
$Q_{clk1}, Q_{clk2}$	Current steering high- $f_t$ NPN HBTs: $W_e \times L_e, N_e$	$0.24\mu m \times 2.5\mu m, 2$
$Q_{T1}, Q_{T2}$	Track stage high- $f_t$ NPN HBTs: $W_e \times L_e, N_e$	$0.24\mu m \times 2.5\mu m, 2$
$Q_{H1}, Q_{H2}$	Hold stage high- $f_t$ NPN HBTs: $W_e \times L_e, N_e$	$0.24\mu m \times 2.5\mu m, 2$
$Q_{EF}$	Emitter-follower high- $f_t$ NPN HBTs: $W_e \times L_e, N_e$	$0.24\mu m \times 5\mu m, 2$
$Q_S$	Tail current mirror high- $f_t$ NPN HBTs: $W_e \times L_e, N_e$	$0.24\mu m \times 5\mu m, 2$
$R_c$	Collector resistors	$100\Omega$
$R_{ref}$	Current mirror reference resistor	$400\Omega$
$R_{ref\_clk}$	Input clock bias reference resistor	$1k\Omega$
$C_{clk}$	Input clock coupling capacitor	$3.26fF$
$V_{cc}$	Supply rail voltage	$4.2V$
$V_{ref}$	Current mirror supply voltage	$2.8V$
$V_{ref\_clk}$	Input clock bias voltage	$2V$

High- $f_t$  SiGe NPN HBTs with emitter width  $W_e = 0.24\mu m$ , length  $L_e = 2.5\mu m$  and number of stripes  $N_e = 2$  were selected for  $Q_{T1-T2}$ ,  $Q_{H1-H2}$  and  $Q_{clk1-clk2}$  from the technology device library. It is critical that the clock transistors are biased at maximum  $f_t$ , according to their dimensions, since they operate at the high input frequency. All other transistors in the D-latch operate at the divided down output frequency. Given the  $f_t$  characteristics presented in Figure 2.16, it can be deduced that for optimum gain at high frequency,  $Q_{clk1}$  and  $Q_{clk2}$  must be biased at  $I_c = 2mA$ . The EF and tail current transistors,  $Q_{EF}$  and  $Q_s$  are double the



**Figure 5.4.** ECL D-latch track and hold modes of operation. (a) & (c) show the latch in track mode where  $v_{clk}$  is logic high ( $v_{clk} > 0$ ) and  $v_{out}$  follows  $v_{in}$ . The current flow path through the active left differential stage is determined by the input signal level  $v_{in}$  and indicated in pink. (b) & (d) show the latch in hold mode where  $v_{clk}$  is logic low ( $v_{clk} < 0$ ) and positive feedback in the right differential stage holds  $v_{out}$  at the value of  $v_{in}$  present just before the negative clock transition. The principle of D-latch operation is illustrated in example (e).

## 5.1 1/6 Synchronous Static Frequency Prescaler

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emitter area with  $W_e = 0.24\mu\text{m}$ ,  $L_e = 5\mu\text{m}$  and  $N_e = 2$ , exhibiting higher current carrying capacity and more accurate mirroring of the supply reference current,  $I_{ref} = 4\text{mA}$ . The bias voltage  $V_{tail}$  is not externally supplied to the chip but connects to the current mirror circuit described in Section 5.1.4.

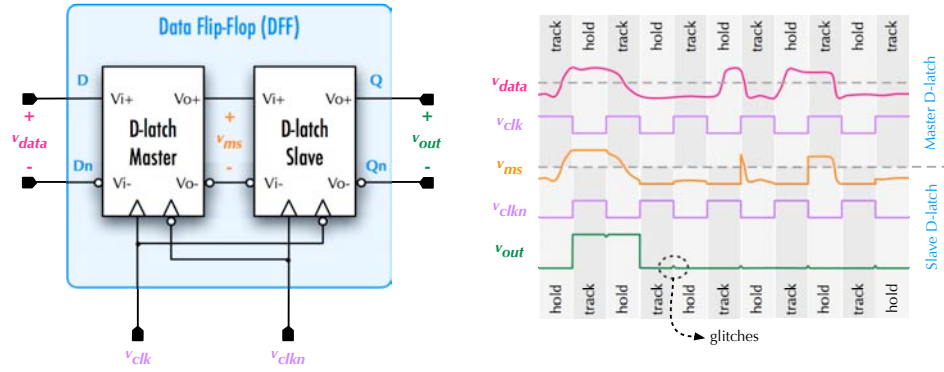
The differential stages must be driven by large signals such that they behave as inverters with fast state transitions. The differential input logic swing ( $V_{R_c} = I_s \cdot R_c$ ) must therefore be larger than  $3V_T$ , where the thermal voltage  $V_T = kt/q \approx 26\text{mV}$  at  $300^\circ\text{K}$ , pushing the transistors strongly out of linear amplifier operation and into nonlinear operation. A common rule of thumb for good noise margins and operation over increased temperature is input swing  $8\text{--}12V_T$  or  $208\text{--}312\text{mV}$  [1]. The D-latch output signal dictates the prescaler output since the output buffer has a gain of less than one. A prescaler output amplitude of  $200\text{mV}$  is considered sufficient for the following programmable divider, therefore the D-latches themselves must produce at least this output swing. Assuming that the entire bias tail current switches through the collector resistors,  $R_c$  then a resistance value of  $100\Omega$  theoretically realises a differential output voltage of  $\pm 400\text{mV}$ . Thus, achieving the design goal with additional margin for layout effects, whilst minimising the D-latch time constant,  $\tau = R_c \cdot C$  and generating the necessary amplitude for following D-latch stages. Transistor depletion and diffusion capacitances along with wiring and fan-out parasitics make up the capacitive component of the D-latch time constant. Reduced transistor area, high current density and minimised parasitic capacitance particularly between the collector-base also aid in minimising gate delay.

The nominal base-emitter voltage,  $V_{BE}$  of the high- $f_t$  HBTs operating in the active region is defined as  $0.737\text{V}$ , however DC simulations indicate  $V_{BE}$  approaching  $0.9\text{V}$ . Since the desired voltage across  $R_c$  is  $200\text{mV}$ , then  $V_{cc}$  must be at least  $2.9\text{V}$ . To avoid transistor saturation during operation, a  $4.2\text{V}$  supply rail was chosen to provide sufficient biasing headroom given the three levels of stacked transistors and to ensure that collector-base junctions do not become forward biased ( $V_{cb} > V_{sat}$ ) under all operating conditions.

### 5.1.2 Master-Slave Data Flip-Flop

The transparency of D-latch operation during the positive input clock phase is rectified by connecting two D-latch circuits in a master-slave configuration clocked in anti-phase. Thus forming the negative edge triggered DFF as shown in Figure 5.5. An example of DFF functionality is also shown including internal and external voltage waveforms and the mode of master-slave D-latches. Basically, the master D-latch tracks the input waveform while  $v_{clk} > 0$  and restores the logic level corresponding to the input data level  $v_{data}$  on the negative clock transition. This value is held at  $v_{ms}$  during the negative clock phase,  $v_{clk} < 0$ .





**Figure 5.5.** Negative edge triggered DFF constructed from two ECL D-latches in master–slave configuration. Glitches in the output waveform are due to finite transitions of the clock signal.

The slave D-latch is driven by the inverse clock signal and therefore tracks the restored logic value of the previous negative clock phase  $v_{clkn} > 0$  and samples  $v_{ms}$  at its negative clock transition. This value is then held at  $v_{out}$  until the end of the negative phase of  $v_{clkn}$ . Finite rise and fall clock transitions result in glitches in the output signal as indicated.

The maximum speed of the synchronous static divide-by-2 topology is limited by the propagation delay,  $t_p$  and setup time,  $t_s$  of the D-latches implemented within each DFF. Therefore the following expression must be satisfied for each latch to ensure accurate division:

$$\frac{T_{clk}}{2} < t_p + t_s \quad (5.1)$$

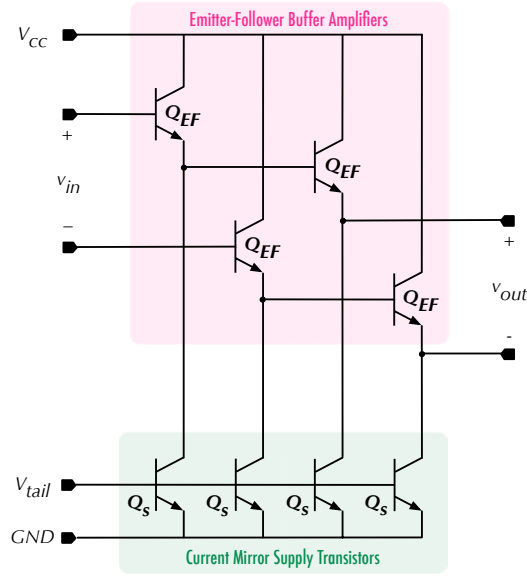
where  $T_{clk}$  is the input clock signal period.

### 5.1.3 Divider Core Output Buffer

The EF based output buffer amplifier as shown in Figure 5.6 connects directly to the last DFF stage as indicated in Figure 5.2. It consists of two EFs for each differential signal in a Darlington pair configuration with device parameters as shown in Table 5.1. Although this amplifier gives a voltage gain slightly less than one, it exhibits high current gain and extremely high input impedance into the base of the first EF. The Darlington pair also has very low output impedance and is therefore helpful in translating the higher DFF output impedance to a lower value to improve matching and hence power transmission. The phase of the input and output signals is also maintained, assuming minimal device mismatching. Isolation between the prescaler and measurement equipment or following circuitry is also improved.

High- $f_t$  SiGe NPN HBTs with emitter width  $W_e = 0.24\mu\text{m}$ , length  $L_e = 5\mu\text{m}$  and number of stripes  $N_e = 2$  were selected for  $Q_{EF}$  to operate at optimum frequency utilising the same

## 5.1 1/6 Synchronous Static Frequency Prescaler



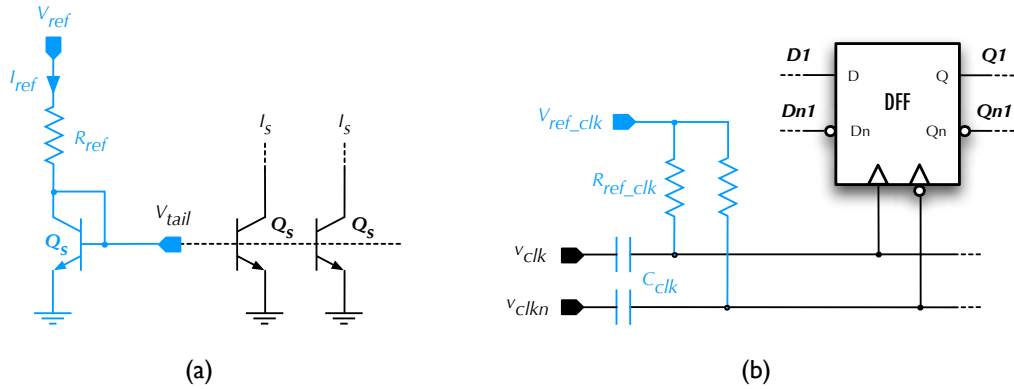
**Figure 5.6.** Prescaler output buffer schematic consisting of double EF amplifiers in each differential signal path.

tail current supply as the DFF chain. Maximum  $f_t$  of these transistors occurs at  $I_c = 4\text{mA}$ , enabling reuse of the divider chain bias current supply. This avoids the need for additional biasing networks, reducing device count and hence circuit area. The tail current transistors,  $Q_S$  have the same properties as  $Q_{EF}$ , therefore accurately replicating the supply current  $I_{ref}$  in each EF to maintain output signal symmetry.

### 5.1.4 Prescaler Biasing

To complete the prescaler design, the tail current supply and input clock signal biasing is defined. The tail current,  $I_s = 4\text{mA}$  is generated using the current mirror structure of Figure 5.7(a), replicating into all D-latch current steering logic and EF circuits within the divider core and output buffer. Identical high- $f_t$  SiGe NPN HBTs are implemented with  $W_e = 0.24\mu\text{m}$ ,  $L_e = 5\mu\text{m}$  and  $N_e = 2$ . Since the high frequency switching capability of the current mirror transistor is not critical, a larger emitter area is used to increase the current capacity of the transistor. The bias voltage  $V_{ref}$  is externally supplied and used in conjunction with  $R_{ref}$  to set the reference current  $I_{ref} = 4\text{mA}$ .

The input clock signal  $v_{clk}$  simultaneously switches six D-latches within the divider core and must provide the DC bias point for the clock current steering differential pair of each latch. This is achieved using the externally supplied bias voltage  $V_{ref\_clk}$  and on chip resistance,



**Figure 5.7.** Prescaler biasing circuits: (a) tail current mirror and (b) input clock steering differential pair.

$R_{ref\_clk}$  as shown in Figure 5.7(b). The clock bias logic is optimised as part of the D-latch speed optimisation.

The full top level chip schematic including bondpads, substrate ties, supply decoupling capacitors, bias networks, divider core and output buffer is shown in Figure A.17 of Annex A.

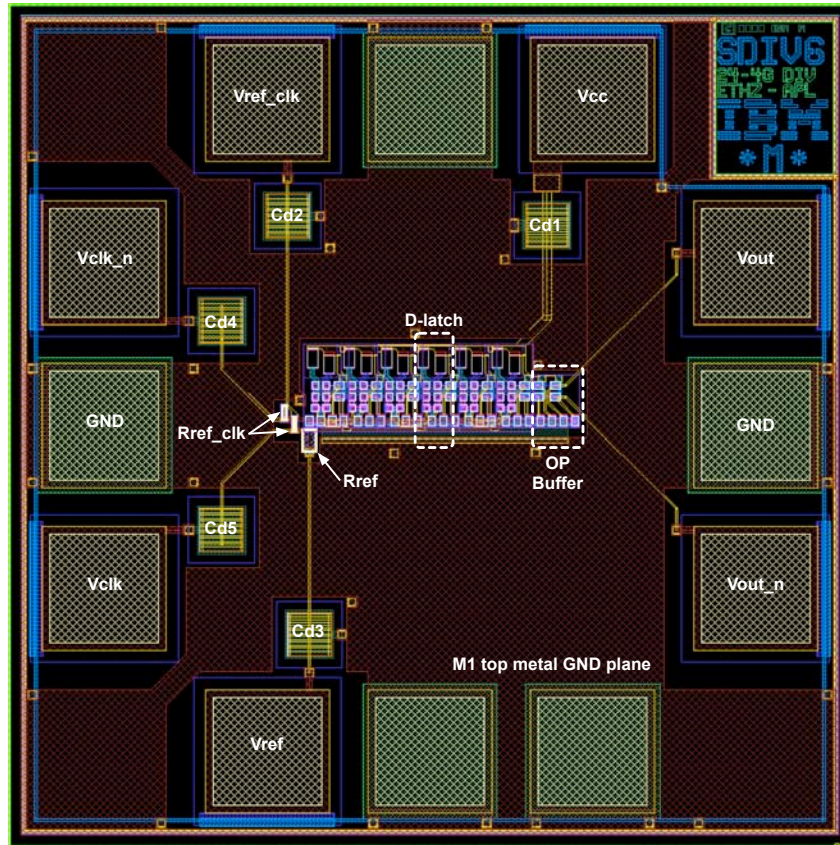
## 5.2 Circuit Layout

Full chip layout (abbreviated by SDIV6) was undertaken using a hierarchical approach with the D-latch, DFF and output buffer laid out and verified individually, as shown in Appendix B. Three DFFs were abutted to form the divider core with only the clock, bias and inter-stage wire connections required. The output buffer was then abutted to the final DFF stage and connected to the current reference and supply voltages. A maximally compact divider core was the primary focus, to ensure that performance-affecting lines between each D-latch (DFF master and slave) and in the feedback path were as short as possible to minimise the propagation delay [23]. Multi-finger HBTs of the same size were located as close as possible to each other to reduce the effects of device mismatch, which cause unbalanced amplitude and phase errors.

Bond pads were placed at minimum spacing around the chip perimeter with the divider core located centrally. Assignment of RF signal pads is such that the necessary wiring is completely symmetrical for both differential signal paths. Each path should therefore suffer equivalent wiring losses and maintain accurate phase orientation. The chip size is pad limited, providing more than sufficient space for supply decoupling capacitors and top metal ground plane. Figure 5.8 shows a snapshot of the final verified prescaler layout before metal density

## 5.2 Circuit Layout

fill, representing a total chip area of  $776\mu\text{m} \times 776\mu\text{m}$ . The diagram has been annotated with device and signal labels for identification against the constituent circuit schematics.



**Figure 5.8.** SDIV6 1/6 synchronous static frequency prescaler layout cell view with annotated device labels – chip size  $776\mu\text{m} \times 776\mu\text{m}$ .

### 5.2.1 Layout Parasitic Extraction

Analog parasitic resistance and capacitance were extracted from the prescaler layout (including metal density fill) and back-annotated into the circuit schematic. Unfortunately, the design kit did not allow extraction of parasitic inductance, therefore, some discrepancy is expected between simulated and measured performance. Post-layout simulations were performed on the extracted schematic and appear in Section 5.3 in conjunction with pre-layout simulation results for comparison.

## 5.3 Simulation Results

Transient and Monte Carlo simulation methods were used to investigate prescaler division accuracy, input sensitivity and robustness to process and matching variation.

### 5.3.1 Prescaler Output

The prescaler was simulated with a differential  $50\Omega$  resistive load representing the impedance of measurement equipment as well as a differential  $100\text{fF}$  capacitive load representing the input impedance of the following circuit in the PLL – the programmable divider. Output waveforms in the time and frequency domain are shown in Figure 5.9 when supplied with a  $200\text{mV}$  differential input clock signal at  $24\text{GHz}$ . The plots demonstrate accurate  $1/6$  frequency division and output amplitudes of greater than  $200\text{mV}$  at the  $4\text{GHz}$  fundamental output frequency. The purely capacitive load produces a slightly higher output voltage however the harmonic fluctuations at maximum and minimum voltage swing are more prominent. Harmonic components at  $1/2f_{clk}$  and  $f_{clk}$  are evident in the time domain waveforms at high and low logic levels, however the following conditions are maintained:

$$v_{out} > 200\text{mV} \text{ for logic level "1" or "high",} \quad (5.2)$$

$$v_{out} < -200\text{mV} \text{ for logic level "0" or "low",} \quad (5.3)$$

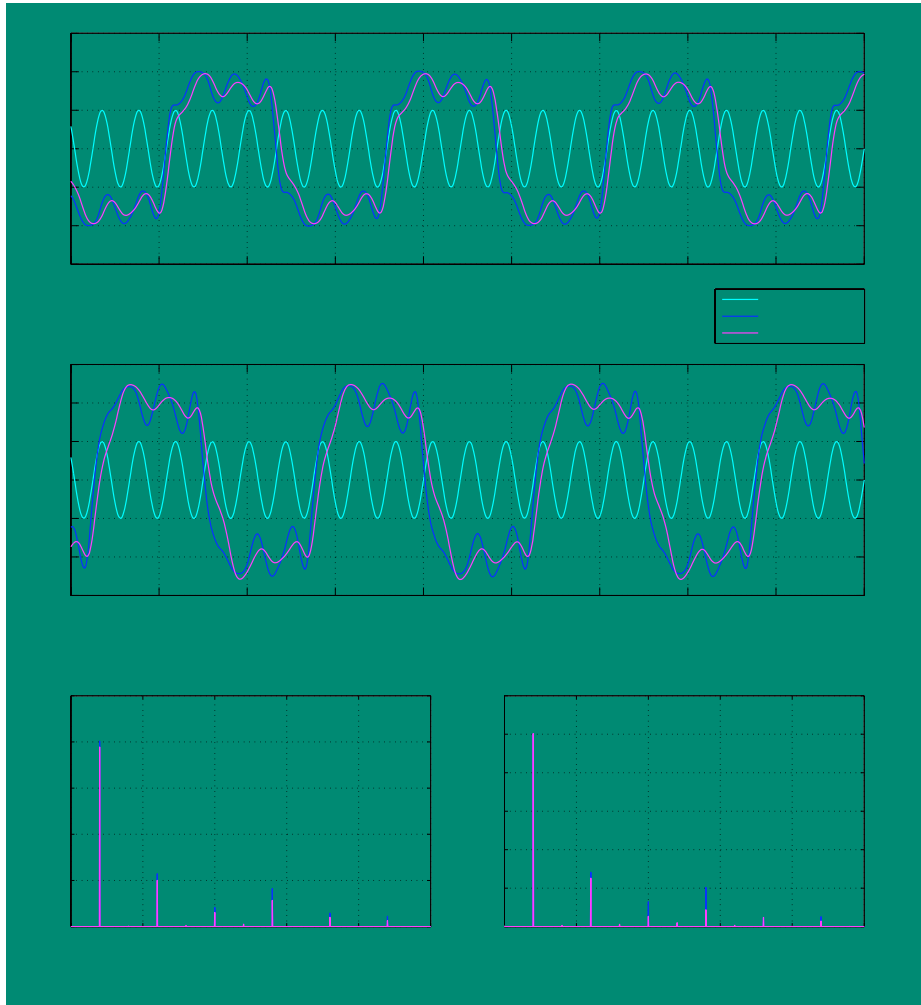
where the duration of high and low logic states, ignoring transition time, is approximately  $t_{out}/2 = t_{clk}/12$ . Frequency components of the output are also illustrated in the FFT of the time domain waveforms. Simulated prescaler output voltage amplitude and calculated RF power metrics are displayed in Table 5.2 for the  $50\Omega$  load only.

**Table 5.2.** Simulated SDIV6 pre-layout schematic and post-layout analog extracted output voltage amplitude and calculated RF power metrics for  $Z_{load} = 50\Omega$ .

<i>MMIC</i>	<i>Cell View</i>	$v_{out}$ (mV)	$P_{out}$ (mW)	$P_{out}$ (dBm)
SDIV6	Pre-layout Schematic	402.62	1.621	2.10
	Post-layout Extracted	390.24	1.523	1.83

DC analysis was performed on the prescaler to evaluate the power consumption characteristics. Table 5.3 displays the simulated total DC current and power consumption figures as well as the break-down into circuit sub-blocks: the DFF, D-latch and output buffer.

### 5.3 Simulation Results



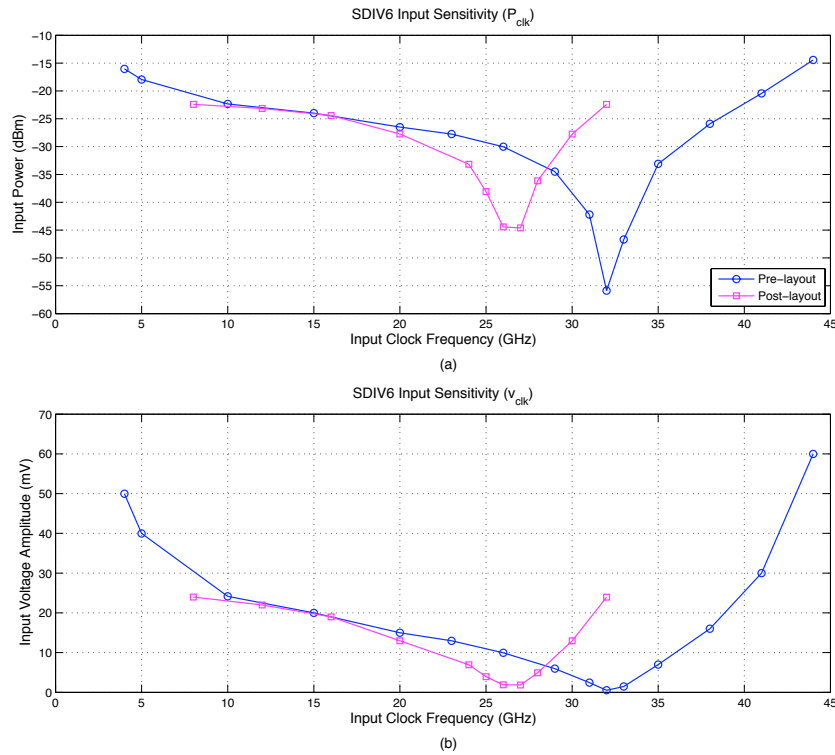
**Figure 5.9.** Simulated SDIV6 pre-layout schematic and post-layout analog extracted time domain waveforms and frequency spectrum, for a (a) & (c)  $50\Omega$ , and (b) & (d)  $100\text{fF}$  load, given an input clock signal at  $24\text{GHz}$ .

**Table 5.3.** Simulated SDIV6 DC current and power consumption metrics, assuming  $V_{ref\_clk} = 2\text{V}$ ,  $V_{ref} = 2.8\text{V}$ , and  $V_{cc} = 4.2\text{V}$  (which supplies the D-latch, DFF and output buffer).

<i>Data</i>	$V_{ref\_clk}$	$V_{ref}$	<i>D-latch</i>	<i>DFF</i>	<i>OP Buffer</i>	<i>Total</i>
$I_{DC}$ (mA)	0.190	4.804	15.071	30.142	17.552	112.972
$P_{DC}$ (mW)	0.380	13.451	63.398	126.596	73.718	467.340

### 5.3.2 Input Sensitivity

Prescaler input sensitivity was investigated by parametric simulation of the pre and post-layout circuit schematics.  $v_{in}$  and  $f_{clk}$  were varied parametrically and the division factor plotted for each value of  $f_{clk}$ .  $v_{clk}$  is typically increased until a 1/6 division factor is achieved, thus identifying the minimum voltage required to drive the prescaler at each particular input frequency setting. The recorded data points are converted to dBm and plotted against  $f_{clk}$  in Figure 5.10.



**Figure 5.10.** Simulated SDIV6 pre-layout schematic and post-layout analog extracted input sensitivity over 4–44GHz: (a) in dBm and (b) in mV.

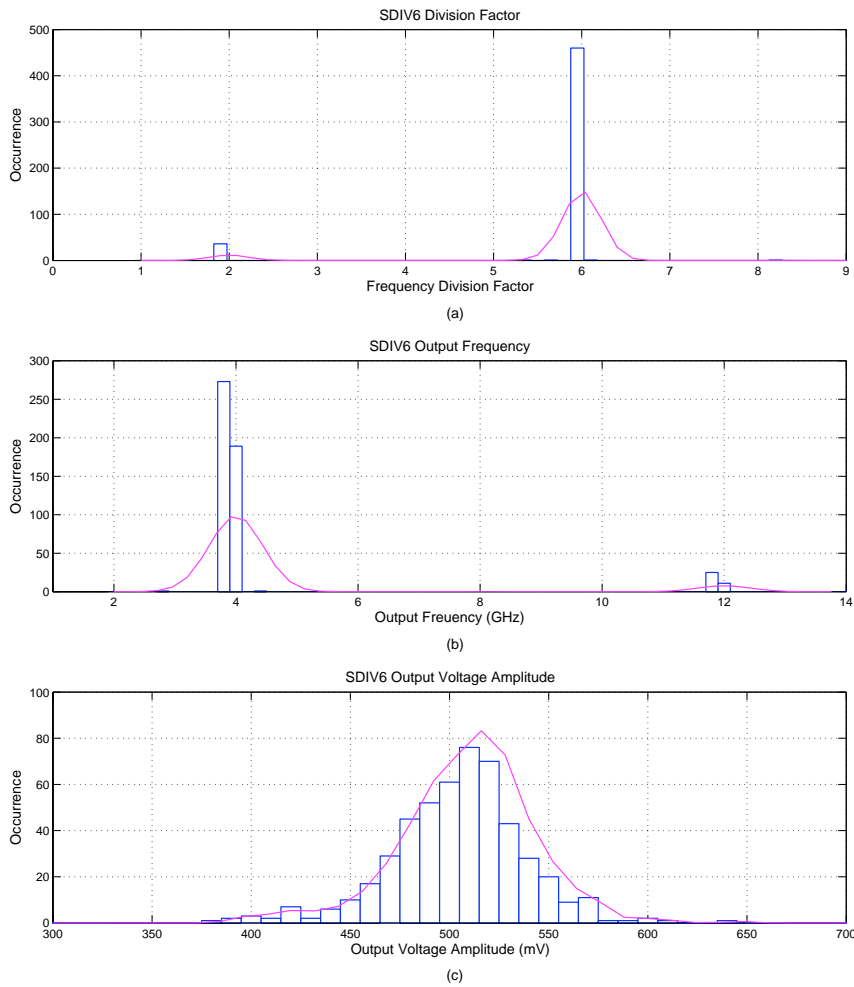
The input sensitivity graphs reveal a pre-layout simulated minimum of -55.87dBm (508.6 $\mu$ V) at 32GHz and a post-layout simulated minimum of -44.61dBm (1.859mV) at 27GHz. The point of maximum sensitivity has therefore shifted down 5GHz as a result of layout parasitic effects. Apart from this frequency shift, pre and post-layout input sensitivity characteristics are almost identical in shape. Accurate prescaler operation can be confidently predicted over the post-layout simulated input frequency range of 8–32GHz and potentially beyond.



## 5.3 Simulation Results

### 5.3.3 Monte Carlo Analysis

Monte Carlo statistical analysis was performed on the top-level prescaler schematic under normal DC bias conditions, with 500 iterations and focusing on process and device matching variation at 27°C nominal temperature. The time consuming nature of the analysis limited simulation to pre-layout schematics only. Figure 5.11 plots prescaler division ratio, output frequency and differential output voltage amplitude given a 24GHz input clock signal. The



**Figure 5.11.** SDIV6 process and matching Monte Carlo simulations (500 iterations at 27°C nominal temperature) of: (a) frequency division factor, (b) divided output frequency and (c) output voltage amplitude, given a 24GHz input.

division ratio and output frequency graphs show that for the majority of iterations, exactly 1/6 division factor and 4GHz output frequency are observed. The output voltage exhibits an approximate normal distribution with mean, standard deviation and three-sigma confidence



interval as calculated in Table 5.4. In summary, Monte Carlo analysis confirms that the

**Table 5.4.** SDIV6 Monte Carlo analysis statistics including mean ( $\mu$ ), standard deviation ( $\sigma$ ) and three sigma confidence intervals ( $\mu \pm 3\sigma$ ) for differential output voltage amplitude ( $v_{out}$ ).

Metric	$\mu$	$\sigma$	$\mu \pm 3\sigma$
$v_{out}$	509.084mV	33.892mV	407.408mV : 610.760mV

fabricated prescaler IC should perform to the design specifications within a very high degree of confidence.

## 5.4 Combined 24GHz VCO and Prescaler Simulation

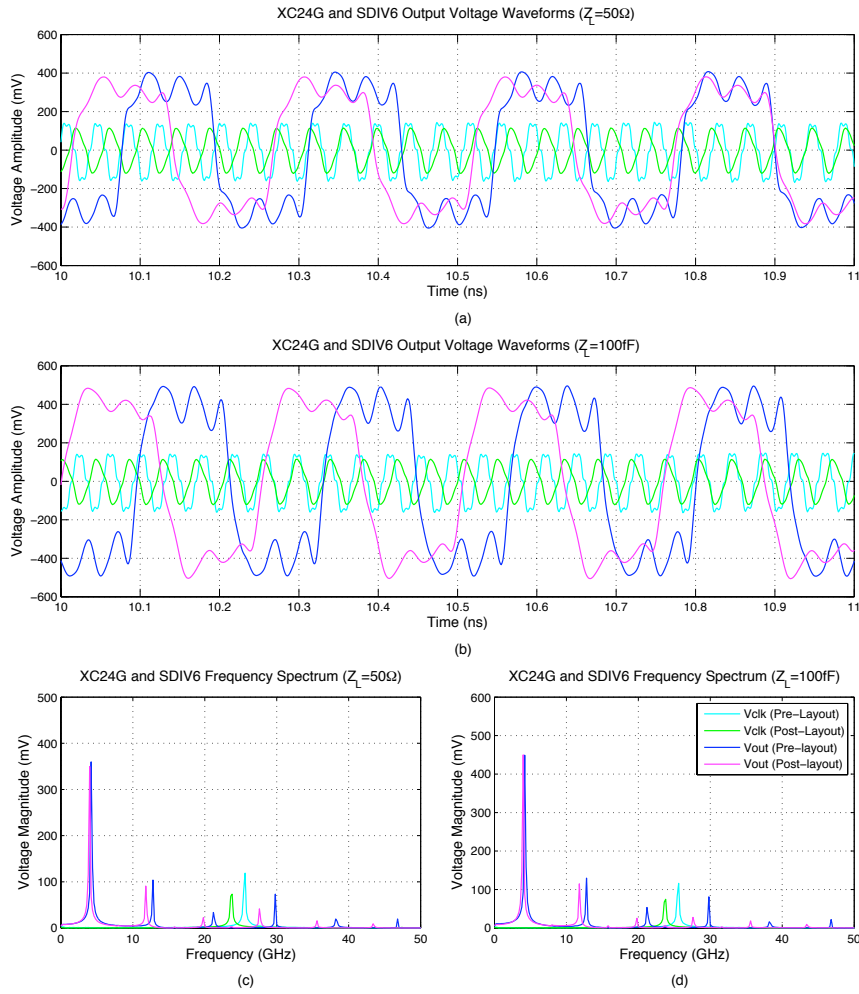
To this point, the individual functionality of both the 24GHz differential VCO and the 1/6 frequency prescaler have been proven. Basic VCO and prescaler interoperability was investigated using the test bench schematic shown in Figure A.22, representing a wire bonded test scenario (assuming ideal bond wires). Simulations were carried out on pre and post-layout cell views for a  $50\Omega$  resistive and a 100fF capacitive differential load termination. Table 5.5 summarises the output voltage, frequency and power metrics at both tuning voltage extremes,  $V_{tune} = 1.8V$  and 4.8V.

**Table 5.5.** Simulated pre-layout schematic and post-layout analog extracted XC24G and SDIV6 output performance metrics for load impedances,  $50\Omega$  and 100fF.

Load	Cell View	$V_{tune}$ (V)	$v_{clk}$ (mV)	$f_{clk}$ (GHz)	$f_{\Delta clk}$ (GHz)	$v_{out}$ (mV)	$f_{out}$ (GHz)
$Z_L = 50\Omega$	Pre-layout Schematic	1.8	175.342	23.7146	1.8030	404.289	3.9528
		4.8	159.318	25.5176		407.466	4.2536
	Post-layout Extracted	1.8	112.594	22.1475	1.5542	377.075	3.6913
		4.8	115.725	23.7017		382.451	3.9505
$Z_L = 100fF$	Pre-layout Schematic	1.8	175.141	23.7138	1.8002	509.778	3.9527
		4.8	163.174	25.5140		494.630	4.2534
	Post-layout Extracted	1.8	112.614	22.1465	1.5574	479.004	3.6911
		4.8	116.685	23.7039		497.288	3.9508

Figure 5.12 shows an example of the simulated time and frequency domain VCO output signal  $v_{clk}$ , and resultant divided prescaler output signal  $v_{out}$  for a single VCO control voltage setting,  $V_{tune} = 4.8V$ . Again, the VCO centre frequency experiences a drop of approximately

## 5.4 Combined 24GHz VCO and Prescaler Simulation



**Figure 5.12.** Combined XC24G and SDIV6 simulated output signals given  $V_{tune} = 4.8V$ . (a) & (c) Pre-layout schematic and post-layout analog extracted time domain waveforms and frequency spectrum for a 50Ω load respectively. (b) & (d) Pre-layout schematic and post-layout analog extracted time domain waveforms and frequency spectrum for a 100fF load respectively.

1.7GHz and a 240MHz reduction in tuning range when accounting for extracted parasitics, however it does maintain an amplitude of at least 112mV. Comparing VCO performance in the combined system with results obtained in Section 4.3, reveals that the large, predominantly capacitive load presented by the prescaler causes a detuning of the centre frequency by approximately 1.2GHz. Output amplitude is also impacted, with approximately half of the individually simulated voltage appearing at the prescaler input in the combined simulation.

The prescaler accurately divides the VCO frequency presented to it by 1/6, producing an output amplitude greater than 240mV.