GaN-based SEPIC DC-DC Converters; Design and Performance Comparisons

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Originality Statement

The work published in this thesis is original and has not been submitted in whole or as part of any thesis before. Work by other researchers referred to in this thesis is acknowledged in text and references.

Viqar Ahmad__ _18/11/2015_____

Name and signature Date

Acknowledgements

To begin with, all praise to the Creator who owns my soul. I owe this work to my supervisor, Professor Graham Town, who showed faith in me throughout my research period and helped me not only academically but in all possible ways to achieve the intended research targets. Special thanks to my wife for being patient while I spent long hours studying and her constant support. I would also like to thank my parents for all their prayers and for making me who I am today.

Abstract

The need for more efficient and compact DC-DC converter design has directed recent research to the use of Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs), capable of achieving higher switching speeds, in place of Silicon (Si) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) which are nearing their theoretical maximum performance limit. The Single-ended Primary Inductor Converter (SEPIC) is one of the simplest designs of DC-DC converter with a relatively low component count, yet is capable of both buck and boost operation. A GaN-based current-regulated SEPIC, is therefore attractive for applications such as in solid state lighting; which is the prime focus of this research. This thesis reports work conducted to evaluate GaN HEMT's performance against a Si FET with matching specifications. This comparison was carried out over a range of frequencies and duty cycles. The results of this work show a marked improvement in performance efficiency of GaN in comparison to Si over MHz frequency range. Moreover, a GaN-based SEPIC using discrete components having current regulation was developed. The underlying idea for building this circuit is to develop a regulated simple and efficient power supply, capable of being integrated for solid state lighting applications in the future.

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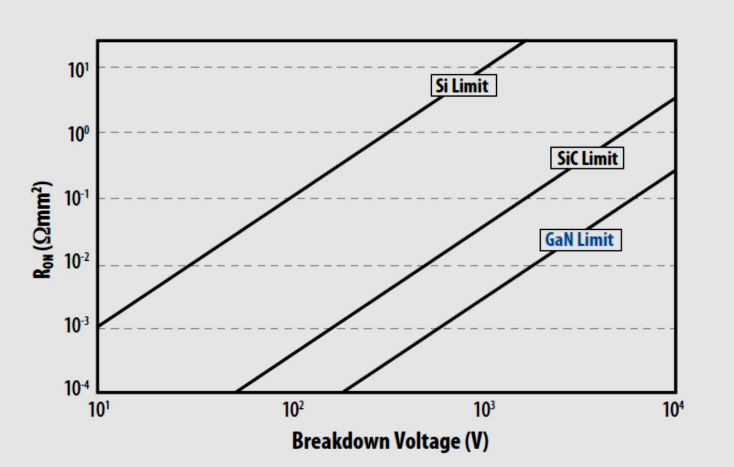
Chapter 1

Introduction

1.1 Introduction to GaN Transistors

Bipolar transistors were widely used in power circuits before Si MOSFETs surfaced in 1976. Since their arrival, advancements in power MOSFET design caused major improvements in FETs' performance for a period of almost three decades. However, there is a theoretical limit to Si performance, based on its figure of merit, as shown in the Figure 1 which limits any further improvement in Si's showing. It must be mentioned, however, that introduction of super-junction MOSFETs and improvement in Insulated Gate Bipolar Transistor (IGBT) performance has been able to push the efficiencies of Si MOSFETs even beyond theoretical limits which is now believed to be the maximum that can be squeezed out of Si MOSFETs.



Wide bandgap devices have been focus of researchers for the past few years as they allow devices to run at higher frequencies and power densities. Wide bandgap devices are also able to withstand higher voltages and temperatures. These devices acquire their name due to the fact that electrons within them require higher energy to go from valance band to conduction band. For example, Si requires 1.1 electron-volt (eV) of energy. Generally, materials needing above 2 eV of energy are regarded as wide bandgap devices. Silicon Carbide (SiC) and GaN are common examples of wide bandgap devices. Table 1 lists some properties of Si compared to SiC and GaN.

Table 1 Comparison of material properties [2]

Property	**Si**	**SiC-4H**	**GaN**
Band Gap (eV)	1.1	3.2	3.4
Critical Field (10^6V/cm)	0.3	3	3.5
Electron Mobility (cm^2/V-s)	1450	900	2000
Electron Saturation Velocity (10^6cm/s)	10	22	25
Thermal Conductivity (W/cm^2K)	1.5	5	1.3

SiC leads the pack in thermal conductivity which means it is capable of working at highest energy densities. Both GaN and SiC possess higher value of critical field, with GaN being the highest, which makes high voltage operation possible. Higher switching frequencies can be achieved in GaN transistor due to superior electron mobility. Figure 1 also shows GaN and SiC to be well off Si in terms of highest theoretical performance limit. Apart from thermal conductivity, GaN can be seen as the material with the most potential as seen in Table 1.

GaN transistors were first officially introduced in 2004, being depletion mode high electron mobility transistors (HEMTs) [1]. They were essentially GaN on SiC substrates recorded to possess very high electron mobility. Figure 2 shows GaN on a substrate layer (Si or SiC). The high mobility achieved is due to a phenomenon called 2 dimensional electron gas (2DEG) which exists between GaN and AlGaN junction. These HEMTs were initially used in RF designs. Efficient Power Conversion (EPC), in 2009, was the first company to announce a GaN on Si FET suited to fulfil needs of power electronics design market.

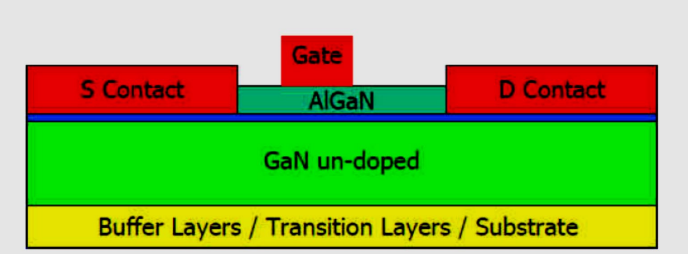


Figure 2 GaN MOSFET on Si/SiC [2]

1.2 DC – DC Converter Circuits

A DC-DC converter performs the same function for DC signals as a step-up or step-down transformer does in case of AC signals, i.e. of increasing or decreasing voltage level at the output relative the input. Converters which have capability to output voltage lower than input are called Buck converters. Converters that give a higher voltage at output relative to the input are called Boost converters. Flyback, Buck-boost and SEPIC are names of some converters that can either give a higher or lower output signal compared to the input. DC-DC conversion can be achieved by linear and switching regulators. Linear regulators make use of resistive networks to provide output signal which causes power loss.

Switching regulators on the other hand make use of inductors to store and release energy in switching cycles and is more efficient than linear regulators. Switching regulator circuit contains a transistor for switching, a diode and an inductor. A variation in position of these three components forms a Buck, Boost or Buck-boost as shown in Figures 3, 4 and 5.

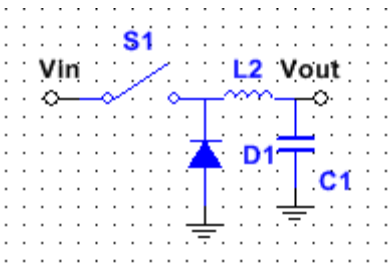


Figure 3 Buck converter

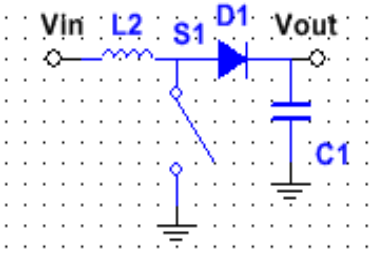


Figure 4 Boost converter

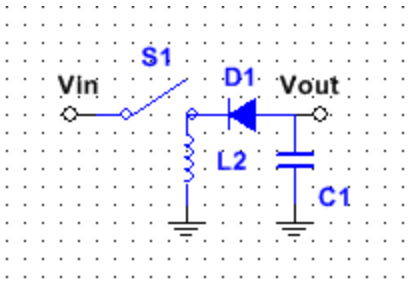


Figure 5 Buck-boost converter

1.3 Introduction to SEPIC Circuit

SEPIC is generally preferred over Flyback and Buck-boost topology due to lack of inversion issue and lower component count. A generic SEPIC circuit is shown in Figure 6.

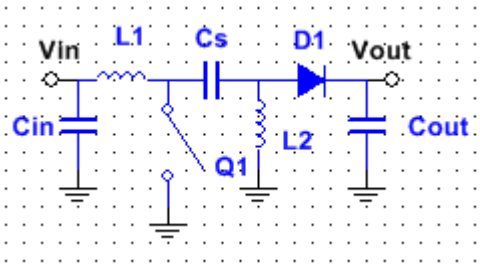


Figure 6 SEPIC circuit

where C_{in} and C_{out} are input and output capacitances respectively. Q1 and D1 are the switch and diode whereas C_s is the coupling capacitor. L1 and L2 are two inductors involved. The voltage across L2 is V_{out}. When the switch Q1 is on, as shown in Figure 7, energy gets stored in L1 via the supply and L2 gains energy from C_s. When the switch goes off, as shown in Figure 8, the energy stored in L1 gets transferred to the diode onto the output via C_s. The capacitor C_s charges to input level and voltage across L2 is negative of input as C_s becomes parallel to L2.

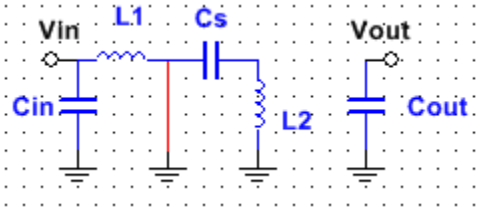


Figure 7 SEPIC with switch on

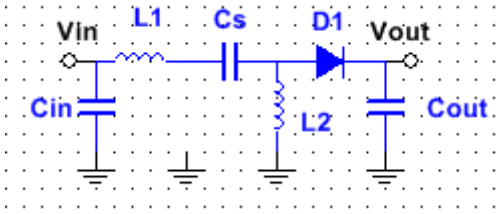


Figure 8 SEPIC with switch off

To lower component count, coupled inductors are often used in place of two separate inductors which give an added advantage of halving inductor size and improved efficiency. SEPIC voltage and current waveforms are shown in Figure 9.

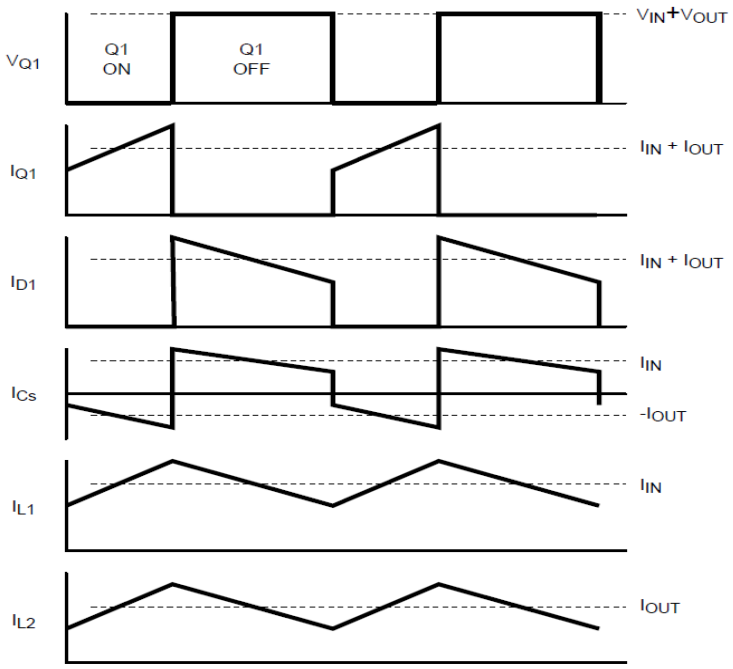


Figure 9 SEPIC waveforms [3]

1.4 Current Regulation in Converter Circuits

For applications of DC-DC converters in solid-state lighting, current control is of primary importance in case of change in load or change in input. There are many commercially available ICs as driver circuits with Si MOSFETs at the heart of operation of most of them. These driver ICs have built-in current regulation circuit and vary based on current regulation limit and frequency of operation.

Feedback is necessary for regulation to occur with two types of regulation methods based on pulse width modulation (PWM) control namely current-mode and voltage-mode control. Both modes are used in this thesis (Chapter 4) with current-mode implemented in simulation and voltage-mode implemented in practical design. Current-mode requires two feedback paths, one from output and the other from sense resistor at the source of the transistor.

Due to two feedback paths, it is difficult to implement control systems of the circuit. Voltage-mode control on the other hand uses one feedback path from the output. This feedback signal is a small portion of the output and is compared with a reference voltage. The difference is compared with a sawtooth generated waveform and its output is fed to the gate of the transistor to achieve regulation.

1.5 Brief Thesis Overview

This thesis is divided into five chapters with introduction being the first followed by literature review. Chapter 3 and 4 consist of body of the thesis with Chapter 3 discussing GaN-based SEPIC design and performance evaluation on Transphorm board and comparison with Si. [4] and [5] have been written as outcome of this research. [4] was rated as one of the best papers in the conference and thus was invited to be published in IEEE Transactions on Industry Applications. [5] is due to be submitted to the mentioned journal at the end of Nov 2015.

Chapter 4 describes simulation, design and implementation of a GaN-based current regulated SEPIC circuit design using discrete components with an aim to integrate them in the future. Conclusion and future work is presented in Chapter 5 followed by type-3 compensator design for feedback circuit in Appendix. Appendix-I consists of to-be submitted paper [5]. References conclude the thesis.

Chapter 2

Review of GaN-based Converter/ Inverter Designs

This chapter documents the most recent advancements in DC-DC converter design using GaN devices. Being relatively new entrant in DC-DC converter designs and showing encouraging results, GaN transistors are a very popular area of research in the field of power electronics. Various ways and means are being investigated to improve the performance of GaN transistors. Models are also being developed to understand how GaN performs in various circuits and the losses associated with it. This year, the world's first GaN-based PWM control IC has also been developed [33] and intensity of research worldwide suggests there are many more to come.

2.1 Application -Specific GaN Designs

GaN converters are being tested for applications like in photovoltaic (PV) systems, wireless power transfer, for an energy storage device in DC microgrids, microwave designs and more.

In case of photovoltaic systems, [6] has shown the use of a GaN gate injection transistor (GIT) to design a three level inverter and claimed to achieve an efficiency of 99.2% at 16kHz with an output power of 1.2kW. The research also claims to reduce size of filter at output and sink size significantly too by using GaN and SiC MOSFETs instead of Si devices. The design includes a bidirectional half bridge inverter without a transformer with four switches. Another application of GaN in PV systems where integrated converters are designed to achieve distributed maximum power point tracking is presented in [7]. Three submodule integrated converters (subMICs) using GaN are developed. SubMICs are designed to perform maximum power point tracking and are attached to PV panels to eliminate mismatch between connected PV panels. The peak recorded efficiency for this design is claimed to be 99% at 400kHz frequency with a tracking precision of 99%.

A PV micro-inverter design is detailed in [8] based on GaN HEMT. The design consists of a 250W flyback converter (for buck or boost) and works in continuous conduction mode. The paper also compares performance efficiency of GaN and Si-based flyback design for varying load power as shown in Figure 10.

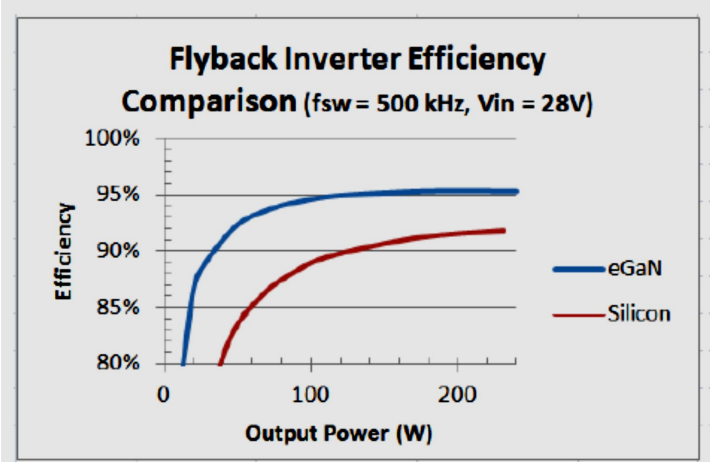


Figure 10 Flyback efficiency curve [8]

Recent research is also focussed on use of GaN-based converters for energy storage devices in electrical distribution systems. [9] is a good example of such a device where a bi-directional DC-DC converter is used in stationary energy storage device for 400V DC microgrid. The use of GaN in this research has been deemed to be responsible for two improvements. First of which is efficiency increase due to lower on resistance and switching loss. Secondly, in Si-based design, a snubber inductor is required which is not needed in the GaN version. The half-bridge converter was built with Si and GaN is shown in Figure 11 (the lack of inductor in GaN design can be seen).

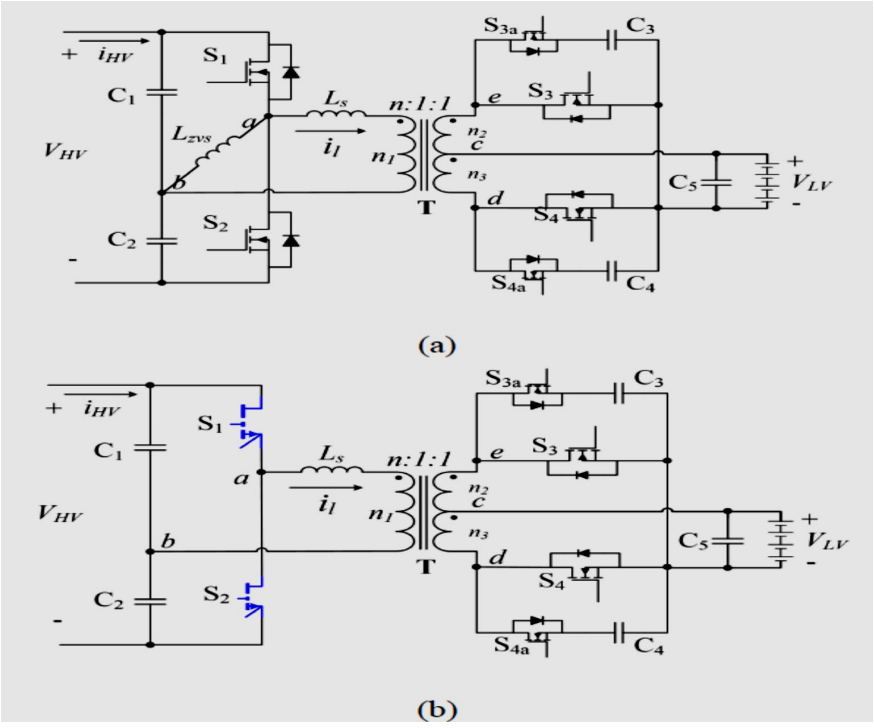


Figure 11 Half-bridge center-tapped converter a) Si MOSFET design, b) GaN design [9]

The same authors have presented a similar distributed energy storage device capable of being connected to a 380V DC grid [10]. Researchers from Japan have come up with a current-fed GaN-based converter for high power density DC distribution systems [11]. The design contains both buck and boost converters at the front-end with a peak efficiency of 95.5% for a 1kW load.

GaN converters are also being investigated in the microwave frequency range e.g. [12] deals with with design of class-E power amplifiers. The prototype includes a 1.2GHz class-E power amplifier and is claimed to reach a peak efficiency of 72% for a power of 4.2W. The same authors, very recently, built a class E amplifier using GaN with a self-synchronous rectifier [13]. The efficiency achieved is claimed to be 75%. The design is targeted for a 1.2GHz frequency range. eGaN HEMTs are used for simulating a Class E converter designed to operate at 10MHz by [14] with an improvement in switching times. A group in Stanford has proposed a 1.3kW resonant converter using GaN for wireless power transfer at a frequency of 13.56MHz [15]. It is a class Φ_2 inverter with zero voltage switching.

2.2 General GaN Designs

In [16], an extremely high efficiency buck converter design with a peak of 99.5% is proposed. The design uses GaN HEMTs switching at 400kHz frequency and a rated power of 2kW with an input of 400V and a 370V output. PCB layout for any circuit can prove to be critical in determining performance of the circuit especially if it is switching at high frequency as in case of GaN converter circuit. This fact has been experimentally verified by [17] in a buck converter design built with GaN HEMTs. The focus of this paper is to optimize the layout so as to reduce power loop and driver loop inductance. Improvements are shown in terms of reduction in overshoot and ringing period of transistor voltage waveforms.

A power factor correction boost design is proposed in [18] with a comparative analysis between Si, SiC and GaN performances. A very detailed analysis of power loss in various diodes and transistors is presented with a conclusion of GaN being 0.5% to 1% more efficient as compared to Si device tested. One of the graphs from the paper showing efficiency comparison is shown in Figure 12.

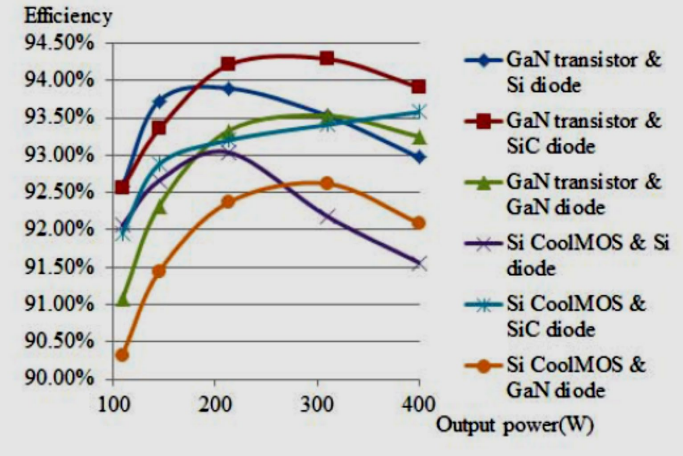


Figure 12 Efficiency vs power for various devices [18]

[19] presents the design of a phase shifted full bridge DC-DC converter built with GaN FET for 600W load. It also compares performance of GaN circuit with a Si MOSFET based circuit. The improvement in efficiency of GaN circuit is claimed to be 1.43% at 260W. Phase shifted full bridge circuit is shown in Figure 13.

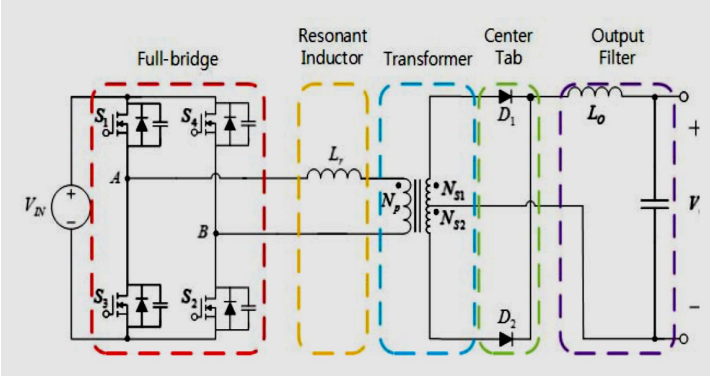


Figure 13 Phase shifted full bridge converter [19]

2.3 GaN Loss Analysis, Models and Comparison with Si

[20] introduces zero voltage resonant transition switching to minimize switching losses, in a synchronous buck converter, with an improvement of 7% efficiency at 3MHz. A detailed analysis of capacitive, turn-on and turn-off losses is performed in [21] which proposes a 1.7kW full bridge converter design. Two EPC devices are used and a peak efficiency of 98.6% is recorded. Interesting results about dead time behaviour of GaN transistor in a buck converter are posted by [22] where it is claimed that source to drain voltage is not a constant quantity during dead time.

To overcome the problem identified in [22], [23] presents an analytical model to select optimal dead time to minimize losses caused by GaN HEMT converters based on operating conditions and GaN switching times. A comprehensive model for GaN HEMTs is proposed by [24] for loss calculations. Turn-on and turn-off switching processes are represented in the form of equations to realise the model. Experimental results are also performed to verify the results. Model also caters for non-linear effects of capacitances and inductances within the circuit.

EMI modelling for a GaN-based half-bridge converter is performed in [25] to identify interference impacts. The outcome firstly identifies EMI effects and then suggests an experimental layout to minimize EMI effects. [26] puts forth a model to test conduction and switching losses for GaN device. Similar model is also suggested by [27] to analyse switching behaviour of GaN HEMT. Capacitive losses in a full bridge DC-DC converter are investigated in [28].

There are many recent researches focussed on proving GaN to be superior in performance to Si and SiC transistors. [28] also presents one such comparison. More such comparisons for various DC-DC converter designs can be found in [29-32].

2.4 GaN Integration and Paralleling

[33] claims to have made the world's first GaN PWM IC with a 5V supply and operational frequency of 1MHz. The complete architecture of a PWM controlled DC-DC boost converter is shown in Figure 14.

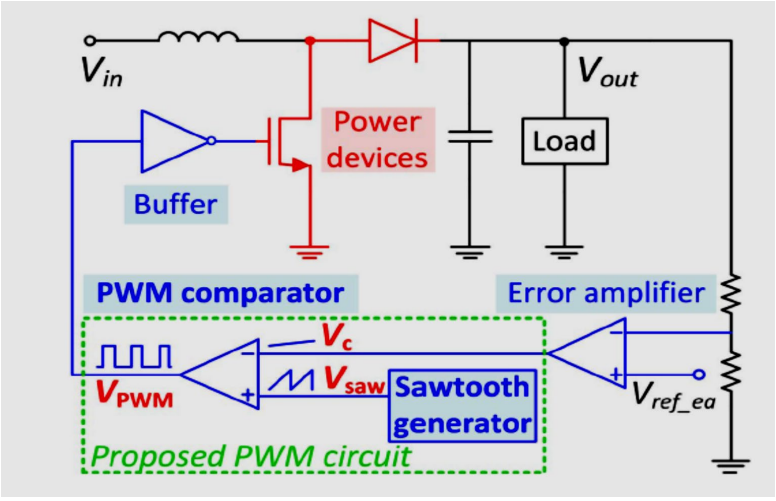


Figure 14 Voltage-mode PWM boost converter [33]

The first integration of depletion and enhancements GaNs has been presented in [34] for applications of mixed signals. Integrated voltage reference generator circuits are also implemented in [35, 36]. Cascoding of GaN transistors is successfully achieved by [37] for use in high voltage applications. [38] is also an example of successful monolithic integration of GaN to achieve better efficiency.

[39,40] describe paralleling of GaN transistors to achieve high current values in high frequency applications. Both designs use 4 GaN devices in parallel to achieve higher power output.

It can be seen from latest research trends that GaN transistors are being tested in a number of possible application areas and results so far are very encouraging. However, there is not a lot of research conducted over using GaN-based converters for solid state lighting purposes having a regulation circuit. There are a number of ICs available commercially for driving LEDs, driven by Si MOSFETs, but GaN-based driver ICs are not common yet. This very fact provides motivation for my research as the aim is to build a GaN-based converter with regulation capability with the ability to act as solid state lighting driver. Moreover, this research also conducts comparison of Si and GaN devices having same on-resistance and threshold voltage, in a SEPIC circuit, to compare performance efficiencies of both devices.

Chapter 3

GaN-based SEPIC Design Using Transphorm Board

As explained earlier in Chapter 1, SEPIC circuits are useful for buck or boost utilities due to their low component count and because they output a non-inverted signal. To build a SEPIC circuit from scratch, a driver circuit needs to be built to drive the switching device. Transphorm board, TDPS501E0A, provides a built in driver IC and can easily be converted to a SEPIC by an addition of coupled inductor and coupling capacitor. This chapter explains design process of SEPIC on Transphorm device.

There were two main targets for development of SEPIC circuit on Transphorm board. The first aim was to build a SEPIC circuit by making some changes to the built-in circuit and judge its efficiency. The second goal was to build a platform for comparison of GaN HEMT and Si MOSFET without any other alteration in the circuit. Transphorm board served as an effective platform for achieving both the objectives as it possesses a compact design and has the ability to run both Si and built-in GaN device with the same on-board driver. This chapter has 3 sections in which the first section introduces Transphorm board followed by implementation of our first SEPIC circuit and concludes by implementation of improved SEPIC circuit.

3.1 Introduction to Transphorm Board

The TDPS501E0A board [41] is a pre-assembled boost converter with GaN as switching device. It is a very compact circuit with optimal layout and gives improved efficiency performance as compared to Si-driven converters. The board uses a TPH3006PS GaN HEMT which is a 600V, 17A (at 25°C) device having a low R_{ds} of 150mΩ. It has a very low reverse recovery charge of 54nC allowing it to be used at higher frequencies without causing high switching losses. Figure 15 shows circuit diagram of the converter.

The GaN HEMT is driven by a FAN3100CSX which provides a 12V peak to peak gate signal to the transistor. The IC is run by a 5V peak square pulse. This platform was ideal

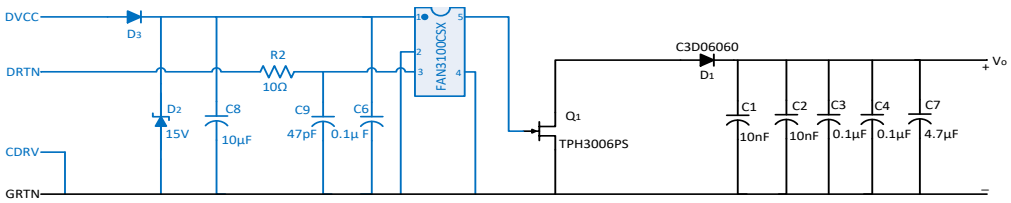


Figure 15 Transphorm board layout [41]

for the experiment as it enabled running both GaN and Si devices using the same on-board driver. TPH3006PS being a hybrid GaN on Si device allows it to be driven by FAN3100CSX. The board further has a CREE Schottky diode for rectification with 600V rating and multiple ceramic capacitors at input and output for filtering purposes with a 4.7µF electrolytic capacitor at the output. The board is limited in its frequency performance due to driver IC being limited to a maximum of 2MHz frequency of operation.

3.2 SEPIC Design

Minor changes were made to the actual circuit board to implement SEPIC design. SEPIC circuit has the ability to either buck or boost and has very low component count. The SEPIC was designed for the following specifications:

Table 2 SEPIC parameters

Parameter	Value
Input Voltage, V_{in}	30V-40V
Output Voltage, V_{out}	50V
Output Current, I_{out}	2A
Output Power, P_{out}	100W
Frequency of Operation, f_s	1.5MHz

3.2.1 Design Calculations

For the specifications mentioned above, the first step towards designing the SEPIC was to determine the duty cycle which can be calculated from the following formula:

$$Duty\ Cycle\ (min) = \frac{V_{out} + V_d}{V_{in(max)} + V_{out} + V_d} \qquad (3.1)$$

$$Duty\ Cycle\ (max) = \frac{V_{out} + V_d}{V_{in(min)} + V_{out} + V_d} \qquad (3.2)$$

Where V_d is the diode voltage drop and was assumed to be 0.5V. The duty cycle range was calculated to be 55.8% to 62.7%. Inductance was calculated in the next step using the following equation.

$$Lc = 0.5 * \frac{V_{inmax} * dt}{\Delta I_{ripple}} \qquad (3.3)$$

RMS current through the inductor was calculated using the following equation.

$$I_{Lrms} = \frac{V_{out} * I_{out}}{V_{in(min)} * efficiency} \quad (3.4)$$

The current ripple, ΔI_{ripple} was assumed to be 40%. There is no consensus among researchers to 40% ripple rule but is generally followed and thus used here.. The peak current to flow through the circuit was calculated to be 5.6A from the following equation.

$$I_{peak} = I_{Lrms} + I_{out} + 0.5\Delta I_{ripple} \quad (3.5)$$

It is important to choose diode and transistor with a current rating of approximately 20% more rated current than 5.6A, as found in (3.5). Moreover, the transistor and diode must be able to withstand peak voltage of 90V (V_{inmax} + V_{out}) for this circuit. The RMS current through coupling capacitor and its ripple voltage were found using the following set of equations.

$$I_{Ccrms} = I_{out}\sqrt{\frac{V_{out} + V_d}{V_{in}}} \quad (3.6)$$

$$\Delta V_{Cc} = \frac{I_{out} + D_{max}}{C_c * f_s} \quad (3.7)$$

RMS current and ripple voltage for this design was found to be 2.59A and 0.177V respectively. Keeping in view the parameters found using above equations; components were carefully chosen to satisfy peak voltage and current requirements. A 4.7µF, 450V rated film capacitor was added to the input to minimize ripple effects. Furthermore, a 20µH coupled inductor (MSD1583-103MEB) [42], with a saturation current of 11A, from Coilcraft, was used instead of two separate inductors to lower component count. Coupled inductor circuits benefit from the fact that using a coupled inductor instead of two uncoupled inductors cuts down the value of inductance to be used in the circuit and improves efficiency. 1:1 ratio is chosen for the inductor as same voltage needs to appear at both ends of the

Figure 16 SEPIC built on Transphorm board (red lines show additions to the circuit) [4,41]

lm capacitor was used as a coupling capacitor connected between drain of the transistor and coupled inductor. Table 3 shows component ratings as used in the designed circuit.

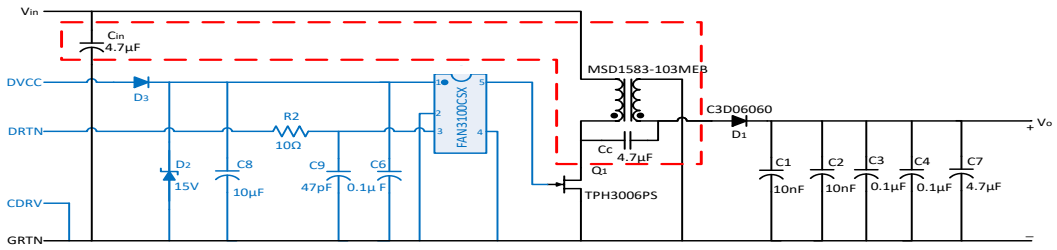


Table 3 Component description

Components	Description	Values
Input Capacitor, C_{in}	Panasonic Film Capacitor	4.7µF
Coupling Capacitor, Cc	Panasonic Film Capacitor	4µF
Coupled Inductor, Lc	Coilcraft	20µH, 11A
GaN HEMT, Q1	TPH3006PS	600V, 11A
SiC Schottky	CREE C3D06060	600V, 20A

The modified circuit board is shown in Figure 16. The dashed lines in red indicate the three components added to the built-in circuit.

3.2.2 Simulation

Simulation for this circuit was carried out in NL5. Instead of the driver FAN IC, a pulse generator was used to generate square wave at a frequency of 1.5MHz with 12V peak to peak voltage. Several iterations with various load powers, frequencies and duty cycles were carried out to estimate behaviour of the circuit. Figure 17 shows one such iteration of parameters for the simulated circuit. Equivalent series resistance was added with all capacitors and inductor to have a realistic estimate of circuit's performance.

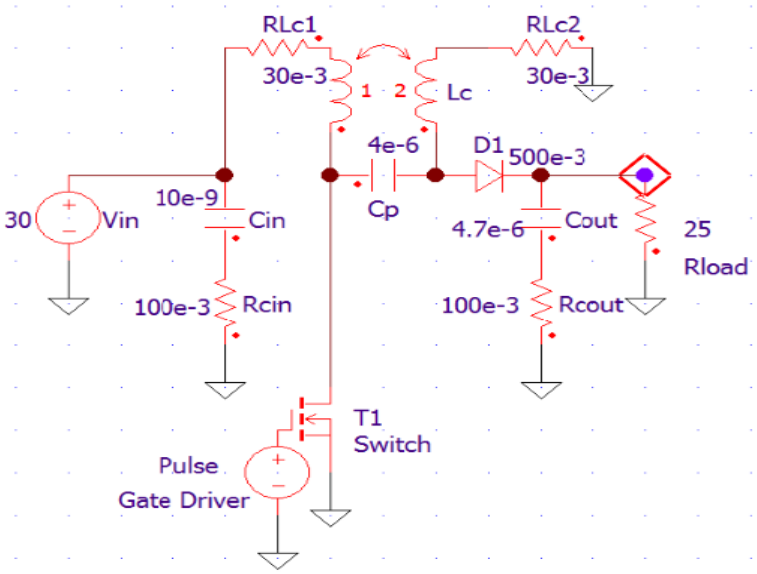
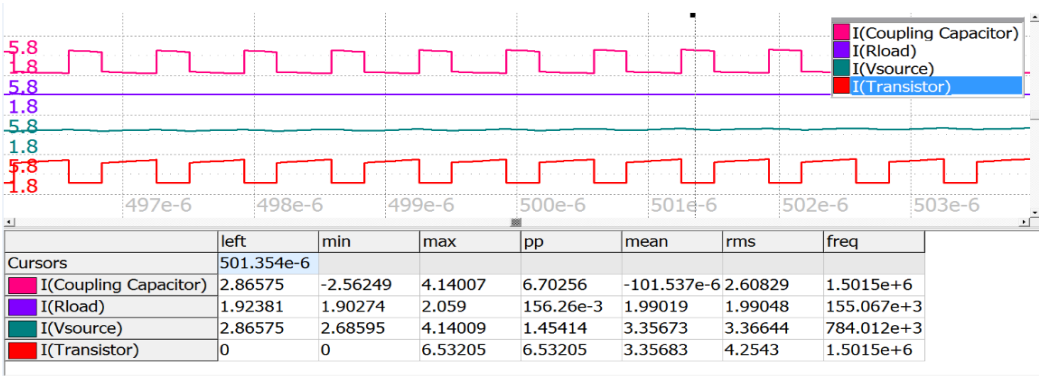


Figure 17 SEPIC simulated in NL5

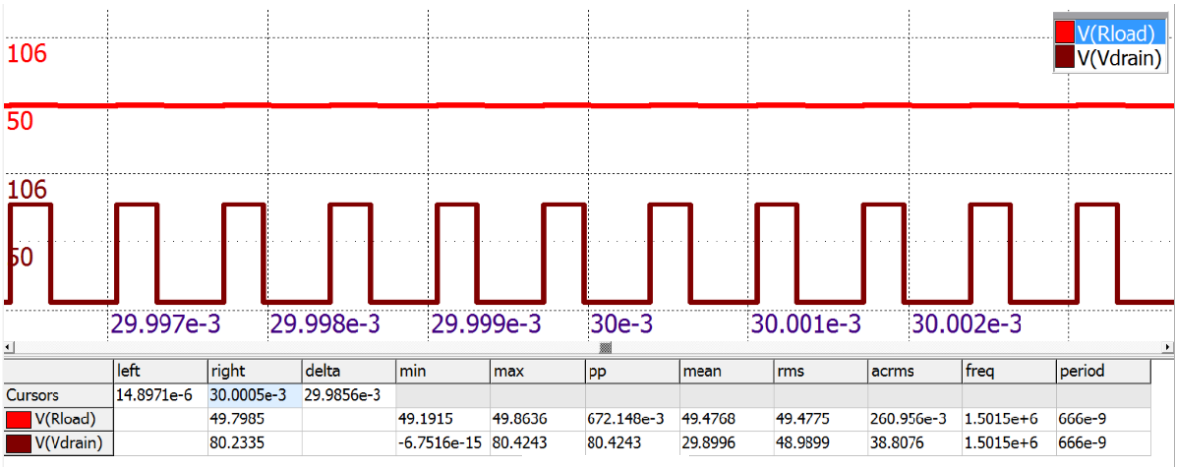
Transient and steady state waveforms were analysed to make sure selected components had voltage and current stresses under acceptable limits. Figure 18 shows some of simulated waveforms of current passing through coupling capacitor, load, voltage source and transistor. It can be seen from the legend below the graph that values of peak current conform to the calculated values in section 3.2.1.



	left	min	max	pp	mean	rms	freq
Cursors	501.354e-6						
I(Coupling Capacitor)	2.86575	-2.56249	4.14007	6.70256	-101.537e-6	2.60829	1.5015e+6
I(Rload)	1.92381	1.90274	2.059	156.26e-3	1.99019	1.99048	155.067e+3
I(Vsource)	2.86575	2.68595	4.14009	1.45414	3.35673	3.36644	784.012e+3
I(Transistor)	0	0	6.53205	6.53205	3.35683	4.2543	1.5015e+6

Figure 18 SEPIC simulation of current waveforms in NL5 [4]

Simulations showed a peak efficiency of 98.93% at a duty cycle of 62.7% and an input voltage of 30V. It can be seen from the Figure 18 that a steady current of 2A passed through the load resistance with a ripple of 156mA. Peak currents through coupling capacitor and transistor were found to be in the range of 6A approximately. The output voltage of 50V and a peak stress of 80V (30V for input and 50V for output) on the transistor can be seen from Figure 19.



	left	right	delta	min	max	pp	mean	rms	acrms	freq	period
Cursors	14.8971e-6	30.0005e-3	29.9856e-3								
V(Rload)		49.7985		49.1915	49.8636	672.148e-3	49.4768	49.4775	260.956e-3	1.5015e+6	666e-9
V(Vdrain)		80.2335		-6.7516e-15	80.4243	80.4243	29.8996	48.9899	38.8076	1.5015e+6	666e-9

Figure 19 SEPIC simulation of voltage waveforms in NL5 [4]

The circuit was designed for a 100W load power and Figure 20 shows a comparison of input and output power waveforms and a subsequent calculation of efficiency for the simulated circuit.

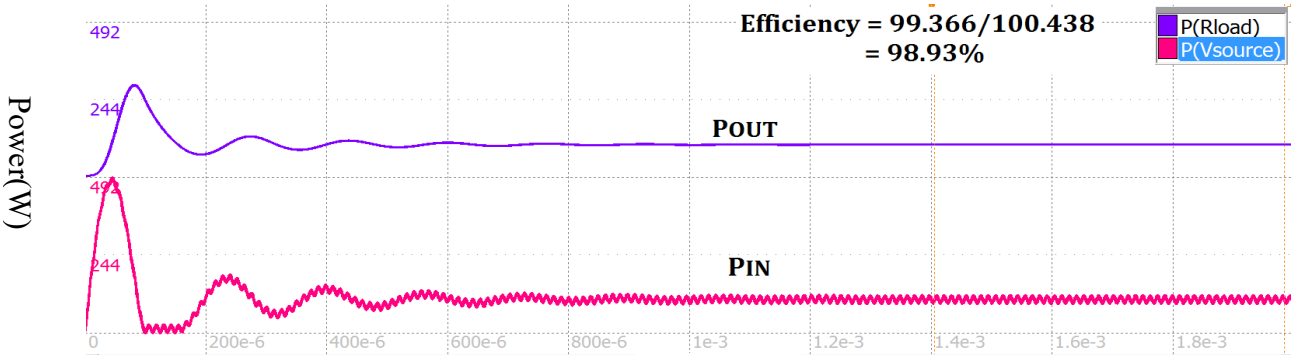


Figure 20 SEPIC input and output power waveform in NL5 [4]

3.2.3 Implementation

The implementation was performed on Transphorm board with the addition of two capacitors and a coupled inductor as mentioned previously. Figure 21 shows the implemented circuit.

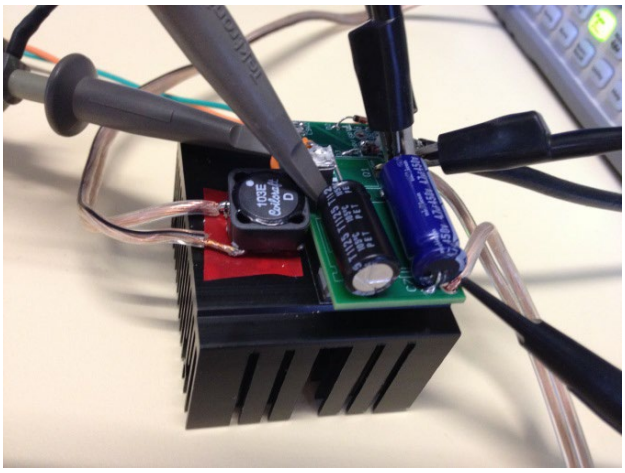


Figure 21 Implemented SEPIC circuit on Transphorm board [4]

The TDPS501E0A driver has the capacity to drive Si MOSFETs and for comparison purpose an IRF520 [43] Si MOSFET from Vishay was chosen. It is a 100V, 9.2A device and compatible with FAN driver IC. Both transistor and diode, built-in on the board, are 600V devices having 11A and 20A ratings respectively.

The input voltage was provided by a 42V, 6A DC power supply. FAN IC required a 12V signal and a 5V peak square pulse provided by 30 MHz Hewlett Packard function generator. The driver IC extracted a 36mA current from 12V supply. FAN IC has a Miller-drive architecture which helps in reducing switching loss. Signals at the input and output were observed using a 100MHz Tectronix digital oscilloscope. A 300W electronic load from Array Electronic was used as an active load. Digital multimeters were used at input and output to measure voltage and current values. A Rogowski coil was used to observe current waveforms at coupling capacitor and coupled inductor operating at 0.5MHz to 1.9MHz range. Current flowing through coupling capacitor is shown in Figure 22.

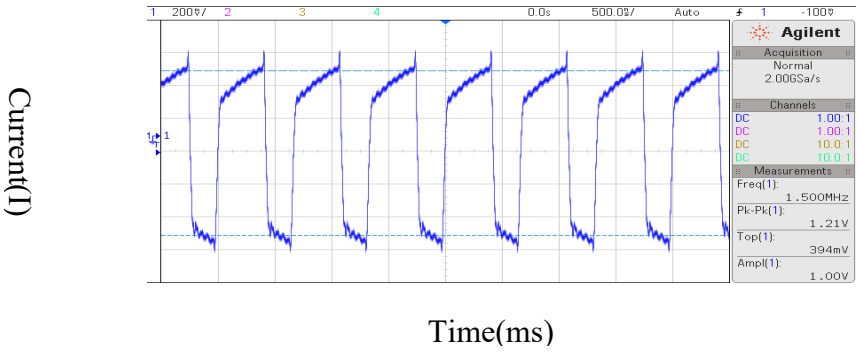


Figure 22 Coupling capacitor current waveform from implemented circuit [4]

3.2.4 Results

The SEPIC was tested over a range of frequencies, duty cycles and load power to observe its performance and measure the peak efficiency. The highest efficiency was recorded to be 98.2% at 1.5MHz operating frequency for an 80W load at a 1A load current. The justification for peak at 1A lies in the fact that as the converter was designed initially for 2A loads, halving the current reduced resistive power losses by a factor of 4 (I^2R). Results of efficiency measured against frequency and load power are shown in Figures 23 and 24.

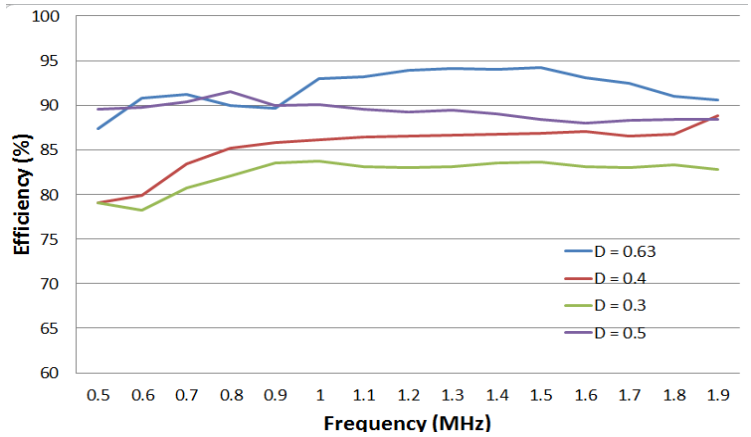


Figure 23 Efficiency vs frequency of SEPIC on Transphorm board [4]

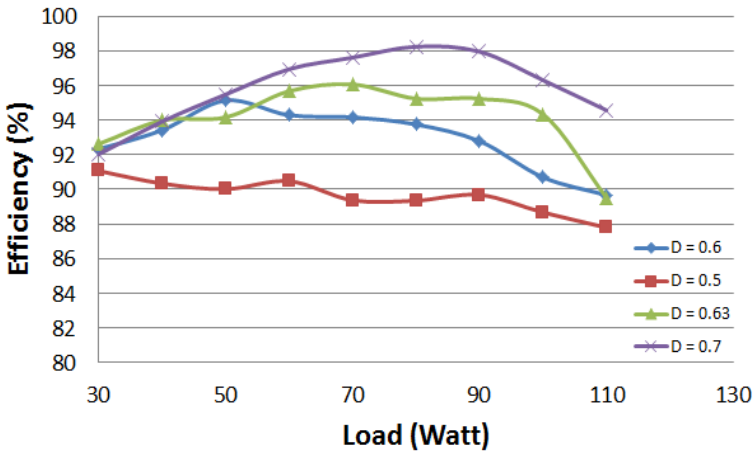


Figure 24 Efficiency vs load power of SEPIC on Transphorm board [4]

The following two graphs capture the comparison between efficiencies of Si and GaN devices. Figure 25 represents efficiency performance for a 50% duty cycle and Figure 26 shows efficiency performance for a 63% duty cycle. It can be seen from both graphs that as frequency increases, switching losses in Si MOSFET play a dominant role and cause the SEPIC to be less efficient as compared to GaN-based circuit.

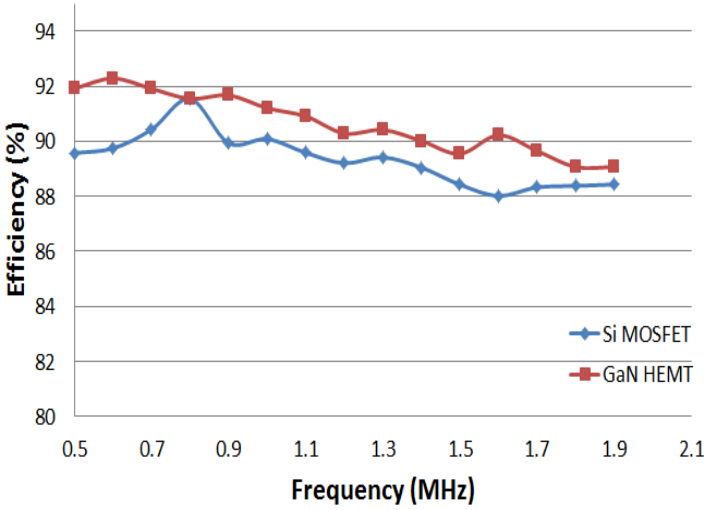


Figure 25 Efficiency vs frequency comparison of GaN and Si on Transphorm at 50%dutycycle [4]

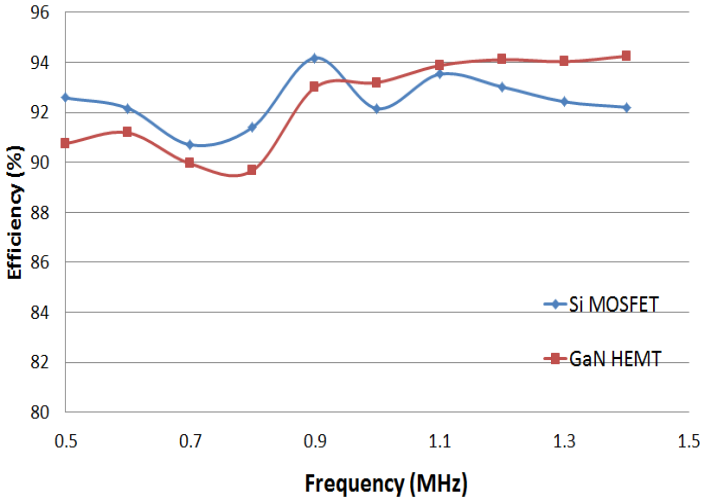


Figure 26 Efficiency vs frequency comparison of GaN and Si on Transphorm at 63% dutycycle [4]

3.3 Improved SEPIC Design

3.3.1 The Need for Improvement

The design detailed in section 3.2 was able to meet first of the two targets set out at the start of the previous section with the development of an efficient and compact SEPIC circuit on Transphorm board. However, the second target, to compare GaN and Si devices, couldn't be performed thoroughly as IRF 520 is a 100V device with almost twice the on-resistance of 600V GaN device which favours GaN HEMT in efficiency comparison. A 600V Si MOSFET with same on resistance as GaN (150mΩ) would have made the comparison more balanced. Furthermore, the design presented in previous section had some shortcomings like being designed for boost only (due to duty cycle range of 55.7% to 63%). The input voltage range could have been kept in line with a DC bus voltage like 24V or 48V

to make it more practical. Moreover, the 20µH coupled inductance was formed by joining two 10µH inductors in series which does not exactly result in a 20µH inductance value due to mutual inductance.

All of the above mentioned shortcomings were catered for in the new design with an input voltage range of 24V to 48V. A single 10µH inductor was used instead of joining two together. For judging performance of Si and GaN devices, a 600V Si device (SiHP22N60E) [44], with same on resistance as GaN, was chosen to give a better estimate of extent of efficiency improvement in GaN. Table 4 shows a comparison of improved design specification with the previous design.

Table 4 Previous vs improved design

Parameter	**Previous Design**	**Improved Design**
Input Voltage Range	30V – 40V	24V – 48V
Output Voltage	50V (boost possible only)	36V (both buck and boost possible)
Si Device	IRF520 (100V, 270mΩ)	SiHP22N60E (600V, 150mΩ)
GaN Device	TPH3006PS (600V, 150mΩ)	TPH3006PS (600V, 150mΩ)
Inductor Used	10µH + 10µH (in series)	10µH only
Current Rating	2A	2.5A
Power Rating	100W	90W

Duty cycle range (42% to 60%), inductance (10µH), inductor RMS current (3.94A) and peak current (7.2A) were calculated using (3.1) till (3.5). The voltage and current stresses were well within limits for devices used.

3.3.2 SEPIC Loss Calculations

To get a better insight into performance of both GaN and Si devices, loss calculations were carried out individually for circuits operating with GaN and Si MOSFET, before implementing the design, at a range of frequencies so as to be in a better position to comprehend performance comparison once design had been realized. Power lost in each component of the circuit is found below.

3.3.2a Power Lost in the Inductor

The 10µH, MEB1583-103MEB has a rated DC resistance of 26mΩ. For an inductor RMS current of 3.94A as calculated before, power consumed by the inductor was estimated using the equation:

$$P_{DCR} = I_{Lrms}^2 * DCR \quad (3.7)$$

The resulting power loss was found to be 400mW. Another factor that contributes in overall power loss of the inductor is core loss. Core loss was found using Coilcraft's online resource by inputting current and frequency values. The estimated core loss came out to be 6mW. Loss is contributed by AC resistance of the inductor as well but was neglected in this case due to its very low value. Thus overall power lost by the inductor was estimated to be 406mW.

$$P_{inductor} = P_{DCR} + P_{core} \quad (3.8)$$

3.3.2b Power Lost in the Diode

To find power expended by the diode, it is necessary to find its internal resistance. The diode internal resistance is given by the following equation.

$$R_T = 0.09 + (T_j * 0.51 * 10^{-3}) \quad (3.9)$$

where R_T refers to internal resistance, T_j is temperature of diode junction. Assuming a 40°C junction temperature, internal resistance of the diode comes out to be 115mΩ. Having found internal resistance, power loss in diode was calculated by the following equation.

$$P_{diode} = I_{out}^2 * R_T \quad (3.10)$$

where I_{out} is output current of the diode which is the same as load current (2.5A). Using the above equation, predicted diode power loss stood at 719mW.

3.3.2c Power Lost by Driver IC

FAN3100 consumes power to drive gate of the transistor. The loss equation for driver is given as

$$P_{driver} = I_{dynamic} * V_{DD} \quad (3.11)$$

where $I_{dynamic}$ is the current flowing through driver and V_{DD} is voltage fed to the driver (12V) with resulting power loss amounting to 432mW.

3.3.2d Power Lost in GaN HEMT/ Si MOSFET

This was the most interesting part of power loss calculations where power lost in GaN HEMT and Si MOSFET was found and compared as these results provided a deeper insight into why GaN outperformed Si in the previous section.

There are two types of losses associated with switching devices; conduction and switching losses [32]. Conduction loss is given by the following equation.

$$P_{cond} = R_{DSon} * I_{rms}^2 \quad (3.12)$$

where R_{DSon} is on resistance between drain and source and I^2_{rms} is rms current passing through the transistor. As both GaN and Si were deliberately chosen with same on resistances, conduction loss for both devices was assumed to be the same and had a value of 375mW from the above formula.

There are many components of switching losses which add together to form overall switching loss of the device. One contributor of switching loss is the switching transition loss. This loss occurs during switching transition from on to off and vice versa as during transition, voltage and current are non-zero for a very small period of time, causing power loss given by the following equation.

$$P_{switch-transition} = V_{in} * I_{out} * f_s * t_s \quad (3.13)$$

where V_{in} is input voltage, I_{out} is output current through the transistor, f_s is switching frequency and t_s is switching time. Switching time for GaN is 4ns whereas Si has a switching time of 24ns. Using the above formula for a switching frequency of 1.5MHz, power lost via switching transition in GaN was found to be 75mW whereas Si power loss was estimated to be 450mW.

Switching loss also occurs due to reverse recovery. The problem with Si MOSFET is that it suffers from a large reverse recovery, one of the major contributors of Si switching loss. Reverse recovery charge, Q_{rr}, for Si device under consideration stands at 250nC whereas Q_{rr} for GaN device is only 1nC. Such a massive difference in reverse recovery

charge values resulted in predicted loss results to be 9.3mW for GaN and 1.875W for Si, at 1.5MHz, by use of the following equation.

$$P_{rr} = f_s * Q_{rr} * V_{in} \qquad (3.14)$$

Switching loss is further swelled due to non-zero output capacitance of switching devices. Q_{oss}, the output charge of transistor has a value of 7nC for Si and 0.65nC only for GaN which resulted in loss estimate to be 52mW and 5mW, at 1.5MHz, for Si and GaN device respectively by use of the given equation.

$$P_{ocap} = f_s * Q_{oss} * V_{in} \qquad (3.15)$$

The final major contributor of switching loss in a transistor is the body diode. Equation for lost power in body diode is given as

$$P_{bdiode} = f_s * V_{SD} * I_{out} * t_{rr} \qquad (3.16)$$

where V_{SD} is forward voltage drop of the diode which stands at 1.2V for Si and 1.9Vfor GaN. t_{rr} is reverse recovery time which is 462ns for Si and 30ns for GaN which resulted in a power loss estimate of 213mW for GaN and 2W for Si at 1.5MHz frequency. Table 5 presents a comparison of power loss estimates for both transistors.

Table 5 Estimated loss comparison of GaN HEMT and Si MOSFET [5]

Loss Component	GaN Loss (mW)	Si Loss (mW)
Conduction	375	375
Switch-Transition	75	450
Reverse Recovery	9.3	1875
Output Capacitor	5	52
Body Diode	213	2000
Total Loss	**677.3**	**4752**

Table 5 was calculated only for a frequency of 1.5MHz. As the range of frequencies at which SEPIC circuit was run were from 0.5MHz to 1.9MHz, an estimate of losses occurring in both Si and GaN device for the whole range was carried out resulting in Figure 27.

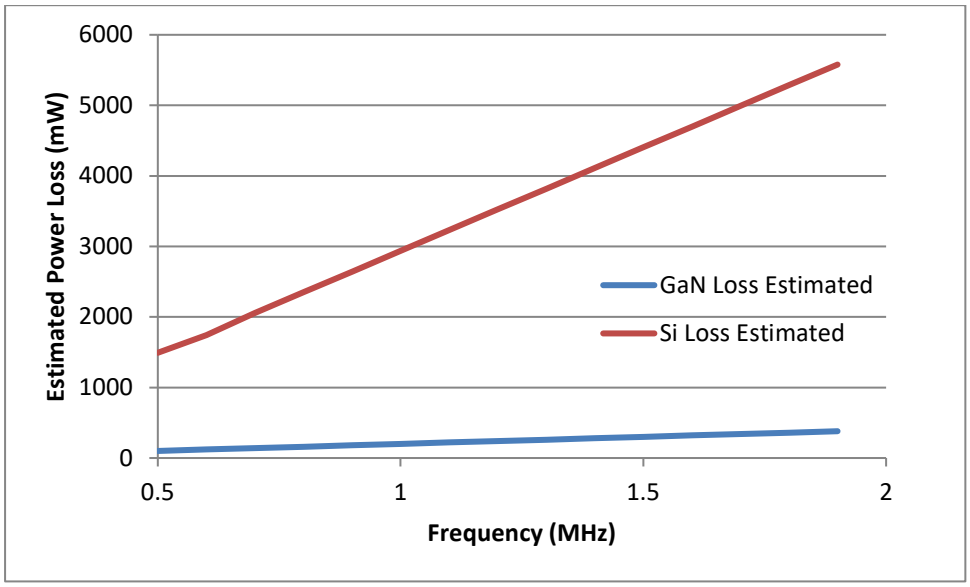


Figure 27 Estimated power loss vs frequency comparison for GaN and Si transistors [5]

3.3.3 Implementation and Results

Implementation of the improved SEPIC was exactly in the same way as done in previous design with only a few parameter changes as mentioned in Table 4. Experiments were conducted on both GaN-run and Si-run SEPIC circuits over inputs, 24V and 48V. Moreover, operating frequency was varied from 0.5MHz to 1.9MHz and duty cycle from 42% to 60%. Keeping in view LED driver design needing constant current at the output, current was fixed at 2.5A for all variations in voltage, frequency and duty cycle. Figures 28-31 were extracted from measurements taken during the experiment.

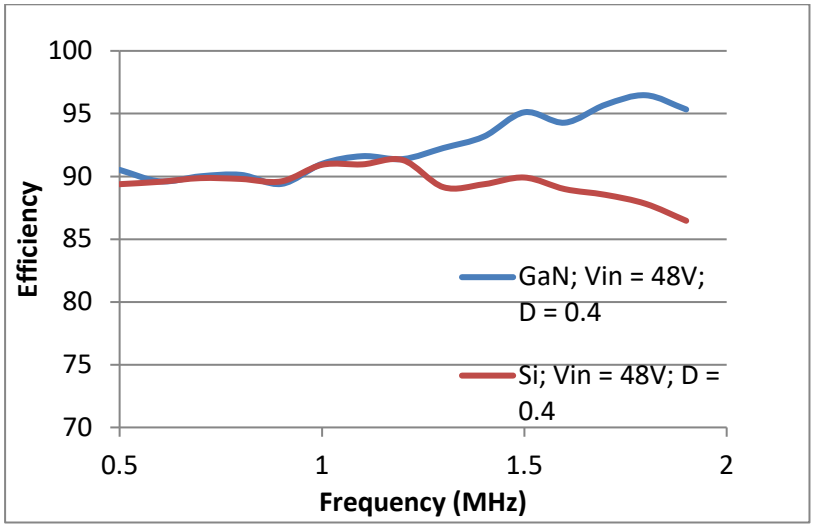


Figure 28 Efficiency vs frequency comparison for GaN and Si based SEPIC at 48V input [5]

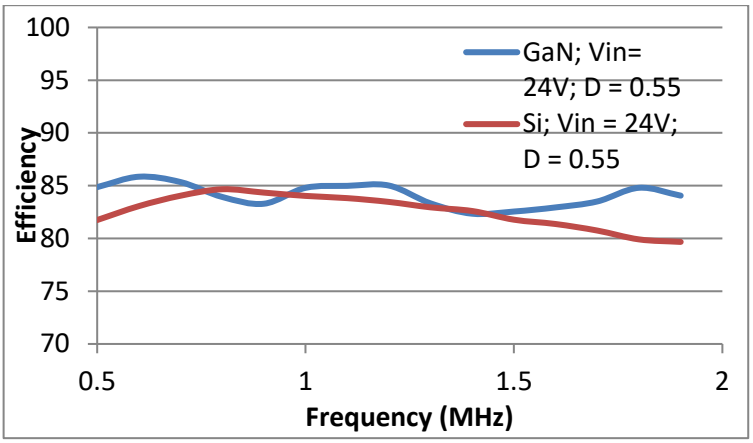


Figure 29 Efficiency vs frequency comparison for GaN and Si based SEPIC at 24V input [5]

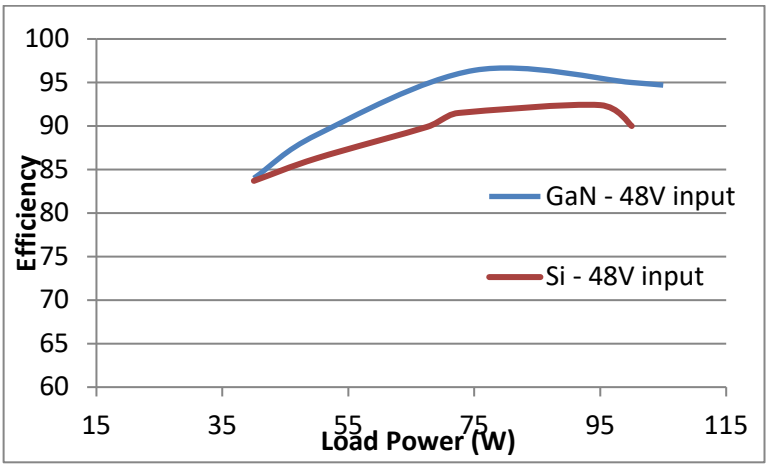


Figure 30 Efficiency vs load power comparison for GaN and Si based SEPIC at 48V input [5]

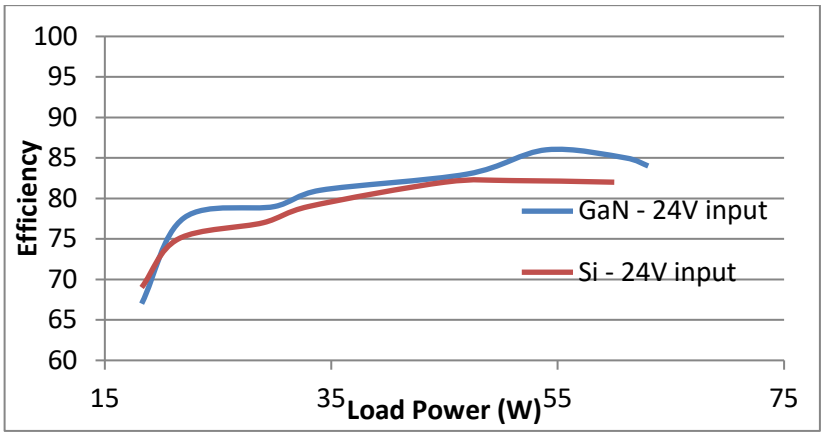


Figure 31 Efficiency vs load power comparison for GaN and Si based SEPIC at 24V input [5]

3.3.4 Analysis

Figure 28 depicts efficiency comparison with frequency of GaN and Si for an input voltage of 48V and a 42% duty cycle. It can be seen from the graph that at frequencies beyond 1.2MHz range, there is a significant improvement in efficiency of GaN in relation

to Si. The primary reason for a decrease in efficiency of Si device is due to increasing switching losses due to frequency increase. It is also evident that losses contributed by passive devices are dominant at lower frequencies in case of GaN as seen in Figure 28 and 29.

It was also interesting to verify power loss in both transistors estimated in section 3.3.2d. At 48V input and 1.5MHz frequency, power loss suffered by Si-based SEPIC was 8.1W whereas GaN-based SEPIC lost 4W only. With rest of the circuit exactly the same, it can be seen that Si introduces a loss of approximately 4W more than GaN as accurately predicted in Table 5. Table 6 compares analytical and experimental loss of GaN and Si devices. The experimental difference is evaluated from the subtraction of power loss of GaN-based SEPIC from Si-based SEPIC. It is assumed that power loss for all other devices remain the same for both circuits.

Table 6 Si and GaN analytical and experimental loss comparison

Frequencies (MHz)	Si and GaN Loss Comparison (mW)			
	GaN Analytical Loss	Si Analytical Loss	Analytical Difference	Experimental Difference
0.5	100	1492	1392	900
0.6	120	1741	1621	2400
0.7	140	2055	1915	3000
0.8	160	2350	2190	2100
0.9	180	2643	2487	1850
1.0	200	2937	2737	2100
1.1	220	3230	3010	2480
1.2	240	3524	3286	3000
1.3	260	3818	3552	4540
1.4	280	4112	3832	5103
1.5	300	4405	4105	5207
1.6	320	4698	4378	5522
1.7	340	4992	4652	5124
1.8	360	5285	4925	4287
1.9	380	5578	5198	5725

Figure 29 shows performance comparison of both transistors for 24V input, 55% duty cycle. There is a marked difference in efficiency of the converter between buck and boost mode with buck being more efficient than boost.

The GaN-based SEPIC circuit topped at an efficiency of 96.47% at 48V input and 40% duty cycle while Si-based SEPIC showed its best performance of 92.4% efficiency at 48V input and 50% duty cycle.

Analysis was also carried out on evaluating efficiency in relation to load power. Figures 30 and 31 compare efficiencies of both transistors at inputs of 48V and 24V respectively. It can be seen from these graphs that almost over the entire range of load power, GaN outperforms Si, especially in powers close to 90W mark; the original design power rating. For powers higher or lower than optimum power rating, the efficiency of converter decreased.

Chapter 4

Modelling, Design and Analysis of GaN-based Current-Regulated SEPIC

Chapter 3 described the development and performance of GaN-run SEPIC circuit developed on Transphorm board foundations. It provided a stepping stone towards realization of a SEPIC converter built entirely from scratch. Moreover, as the driving force behind building a SEPIC was to design driver circuits for LEDs, which need current regulation to maintain a steady output current, it was decided to introduce current regulation in our new design. Discrete components were used in design of this regulated SEPIC so that the circuit can be integrated in a single chip at the next stage of this research (beyond scope of this thesis). This chapter explains in detail the modelling, design methodology and implementation of current regulated SEPIC built with discrete components. This chapter is divided mainly into three parts in which first part refers to simulation of regulated SEPIC model and the second part will detail implementation and testing phase. This chapter caps off with description and analyses of results. Figure 32 shows flow chart of design process.

Figure 32 Flow chart of design process

4.1 Simulation

Simulation for modelling the performance of current regulated SEPIC was performed in National Instruments (NI) Multisim 14.0. The simulation was divided into two stages. First stage involved the use of generic PWM controller in-built in the software to control duty cycle for regulation purpose. Current-mode control was implemented in this stage. In the second stage of simulation, PWM control was designed to be achieved by the use of error amplifier and comparator in feedback path. This stage utilized voltage-mode control. More text about current regulation by PWM control can be found in Chapter 1.

4.1.1 Simulation- Stage 1

As a first step towards simulation of current regulated SEPIC, input and output parameters were decided. Table 7 gives a summary of parameters chosen for this model.

Table 7 SEPIC simulation specifications - Stage 1

Specifications	Values
Input Voltage, V_{in}	30V-60V
Output Voltage, V_{out}	50V
Output Current, I_{out}	2A
Switching Frequency f_s	1.5MHz

Values for duty cycle (45.4% to 62.7%), inductance (20µH), peak (4.8A) and RMS current (3.6A) were found using equations (3.1) to (3.5) as mentioned in previous chapter. Figure 33 shows the complete regulated SEPIC model.

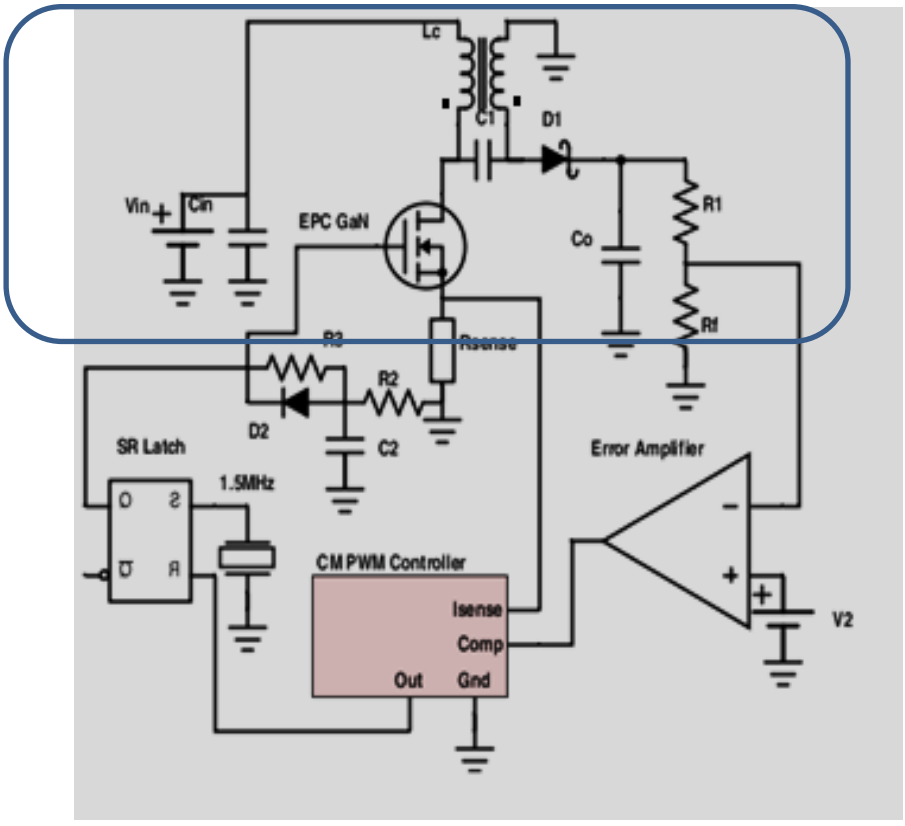


Figure 33 Simulation of regulated SEPIC with generic PWM controller- Stage 1

4.1.1a Working Principle

The highlighted part of the circuit presents the same SEPIC circuit that has been discussed in previous chapter. To achieve regulation a small portion of the signal is fed back to an error amplifier which compares the output signal with a reference provided externally. As this model used current-mode control, there were two feedback paths. One signal is fed back from the output as just mentioned, whereas, the other feedback signal is taken from source of GaN device using a very low valued sense resistor. Both fed back signals were input into generic PWM controller which modified duty cycle by investigating both fed back signals. The signal coming out of PWM controller was given to SR latch which served as driver for GaN device. A 1.5MHz oscillator acted as clock for the SR latch.

The circuit made use of capacitors in the nF range, to avoid large sized/ valued electrolytics, with a 20µH inductor. Choosing 20µH enabled high voltage, high frequency converter design coupled with the benefit of small size. A 150V, 12A EPC 2018 GaN transistor [45] model was used along with a 5A, 650V Infineon Schottky diode model as the maximum voltage stress across both devices was 110V (sum of maximum input and output voltage). Table 8 summarizes component models used in the simulation.

Table 8 Simulation parameters for regulated SEPIC - Stage 1

Component	Description	Value
Cin	Input Capacitor	400nF
C1	Coupling Capacitor	400nF
Co	Output Capacitor	500nF
Lc	1:1 transformer	20µH
Q1	GaN, EPC2018	150V, 12A
D1	Infineon, IDH05G65C5, SiC Schottky	650V, 5A
PWMCM2	Generic Current-mode PWM Controller	N/A

Current mode control requires slope compensation to avoid system oscillation, especially for designs with an operational duty cycle of near or over 50%. The combination of R_2, R_3, D_2 and C_2, as can be seen in Figure 32, formed the slope compensation circuit

working independently of the clock frequency. This circuit included an RC network to provide the desired compensation ramp.

4.1.1b Simulation Efficiency Results and Analyses

Figure 34 shows output voltage and current waveform for 30V input signal at 62.7% duty cycle. The output holds at 1.93A by fixing the output voltage to 48.5V after initial transients. A 3.39A input current results in an efficiency of 92.04% with a less than 8% ripple in output current.

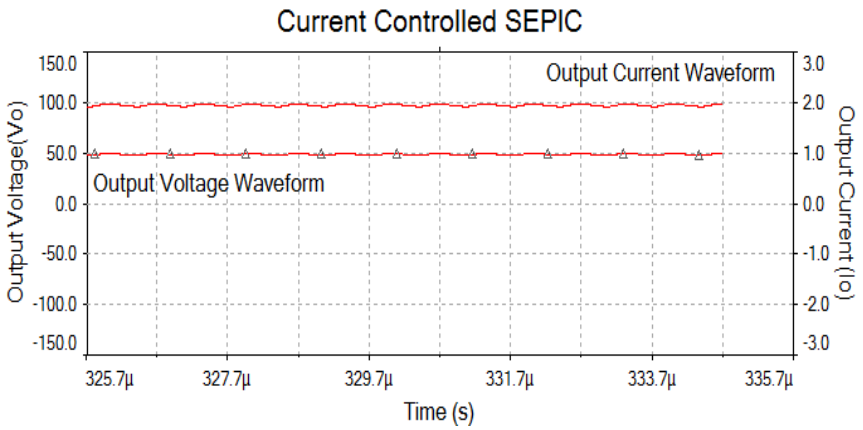


Figure 34 Output voltage and current waveform for regulated SEPIC at 30V input - Stage 1

Figure 35 shows output voltage and current waveform for a 40V input at 55.8% duty cycle. An efficiency of 92.6% was achieved at this input with input current of 2.61A and output voltage and current equal to 49.3V and 1.96A respectively with a less than 6% output current ripple.

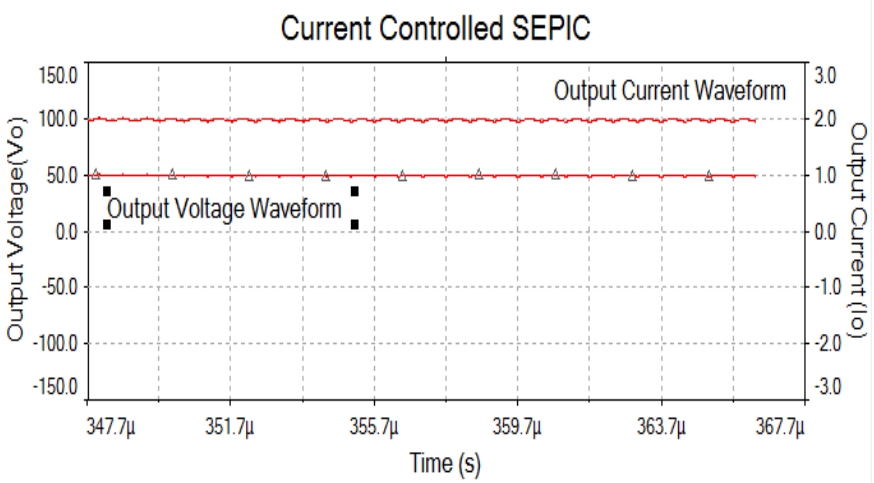


Figure 35 Output voltage and current waveform for regulated SEPIC at 40V input - Stage 1

Figure 36 shows output voltage and current waveform for a 50V input at 50% duty cycle. A 50% duty cycle input signal with an input current of 2.08A yielded maximum

efficiency of 94.2% with a 49.5V output voltage and 1.98A current with less than 5% output current ripple.

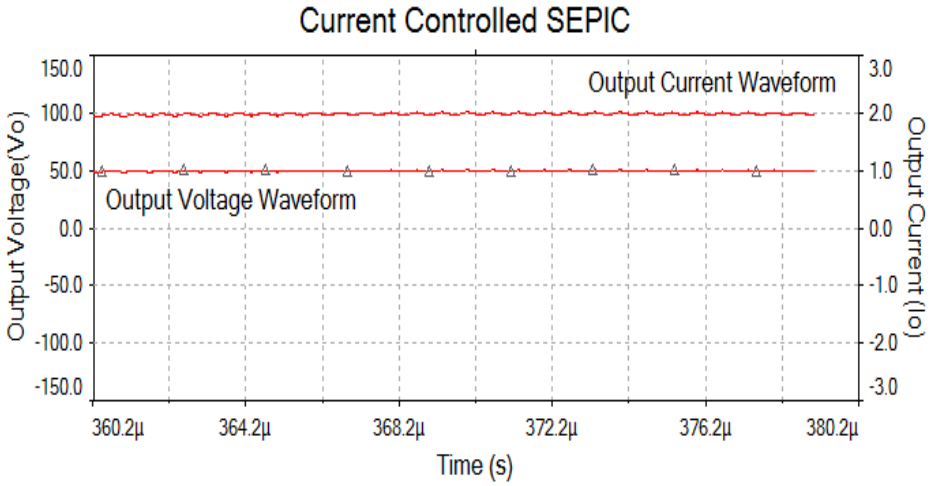


Figure 36 Output voltage and current waveform for regulated SEPIC at 50V input - Stage 1

An input of 60V with 1.63A current produced an output waveform with a voltage and current reading of 48V and 1.9A respectively resulting in an efficiency of 93.2% and output current ripple of less than 6% as represented in Figure 37.

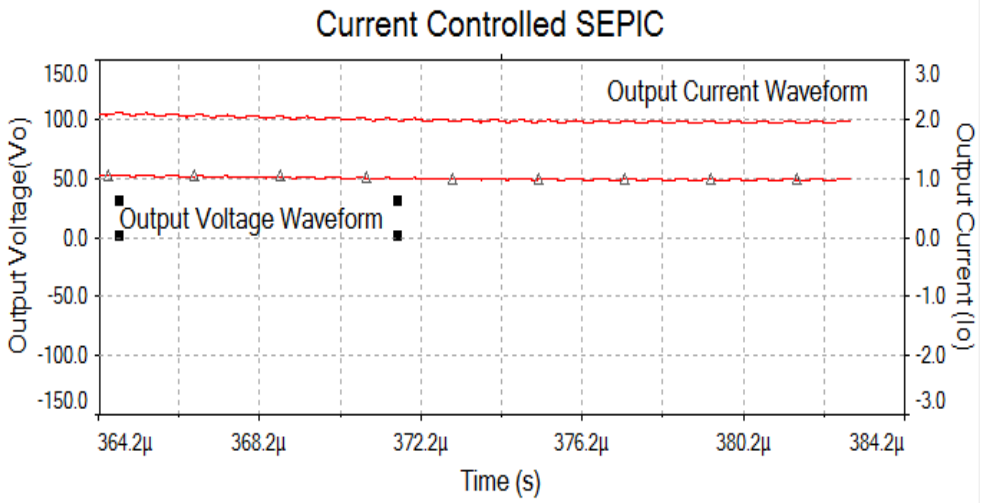


Figure 37 Output voltage and current waveform for regulated SEPIC at 60V input - Stage 1

A comparison of efficiency versus duty cycle can be seen in graph on Figure 38 showing highest efficiency at 50% duty cycle with a decline as duty cycle is increased.

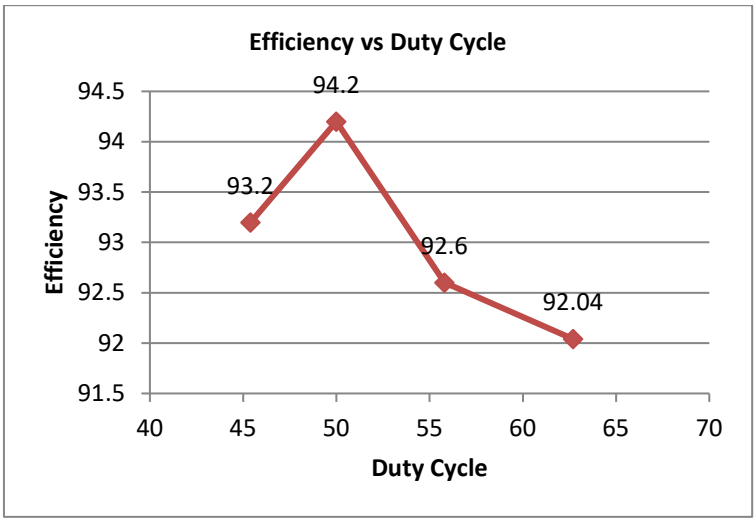


Figure 38 Simulated efficiency vs duty cycle - Stage 1

4.1.1c Simulation Regulation Results and Analyses

30V input (62.7% duty cycle) showed worst case efficiency results. Thus line and load regulation was calculated for this input to measure worst case regulation outcome.

Line Regulation

To test line regulation, a 10% change in input voltage was made (30V+3V). Figure 39 shows the output voltage and current for change in input voltage. The current settled in at 1.98A with an output voltage of 49.6V with a 10% output current ripple. Thus line regulation is given as

$$\text{Line regulation} = \frac{\Delta Iout}{\Delta Vin} = \frac{50mA}{3V} = 16.6mA/V$$

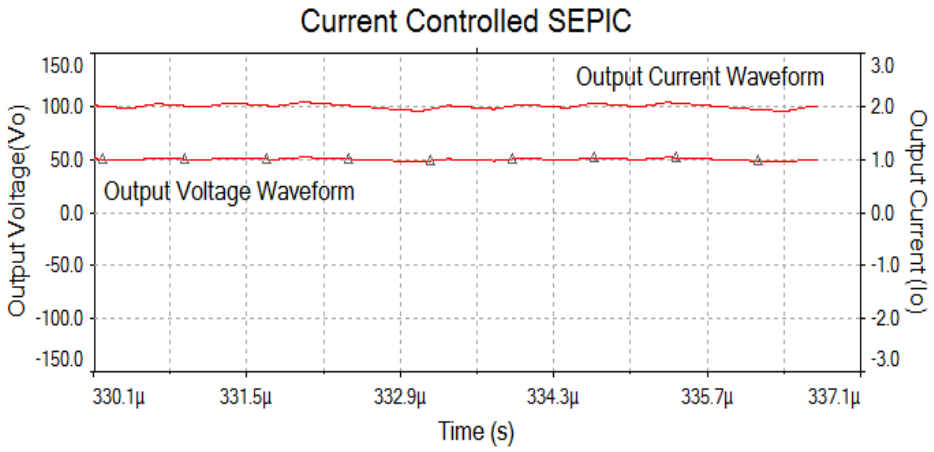


Figure 39 Simulated line regulation - Stage 1

Load Regulation

A 10% change in load resistance (25Ω - 2.5Ω) caused the output current to increase by 40mA with a 7% output current ripple. Output voltage and current waveform for increased load resistance is shown in Figure 40. Load regulation is thus given as:

$$\text{Load regulation} = \frac{\Delta Iout}{\Delta Rload} = \frac{40mA}{2.5\Omega} = 16\text{mA}/\Omega$$

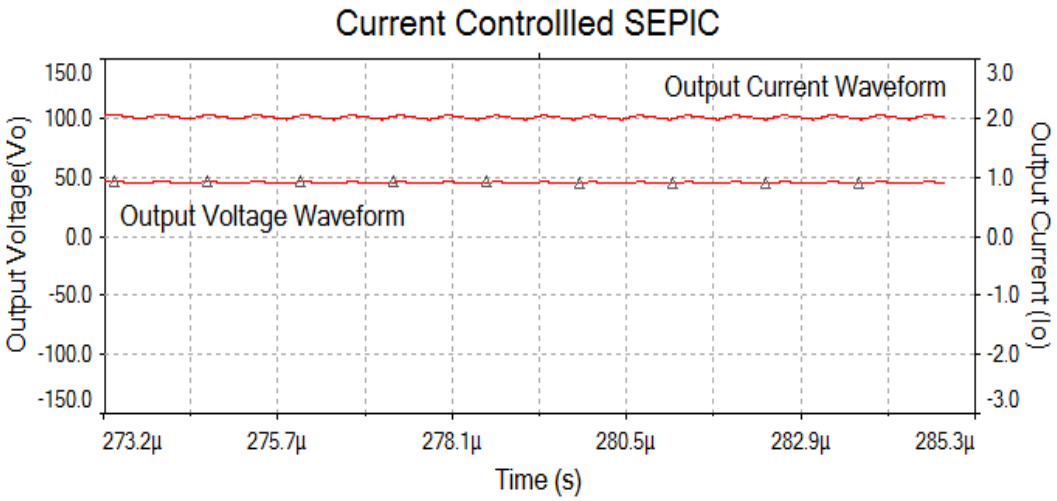


Figure 40 Simulated load regulation - Stage 1

4.1.2 Simulation- Stage 2

Insightful results were achieved by simulating first stage of regulated circuit but the use of generic PWM controller in the design hindered practical implementation. Moreover, due to the use of current-mode control, dual feedback caused problems of stability for the circuit.

To overcome both problems mentioned above, an error amplifier and comparator chip was used in the feedback path instead of generic controller. Voltage-mode regulation was preferred over current-mode due to ease of compensation circuit design. To keep consonance between previous simulation and the current, the same EPC device, EPC 2018, was used.

This stage of simulation was carried out keeping in mind the development of a PCB implementation of the simulated design. Thus, all capacitors used were multi-layer ceramic capacitors (MLCCs) as they possess low equivalent series resistance (ESR) and equivalent series inductance (ESL). Moreover, resistors used were rated according to estimated current

passing through them. Simulation sampling time is 0.1µs. Figure 41 shows simulation circuit followed by Table 9 summarizing circuit design parameters.

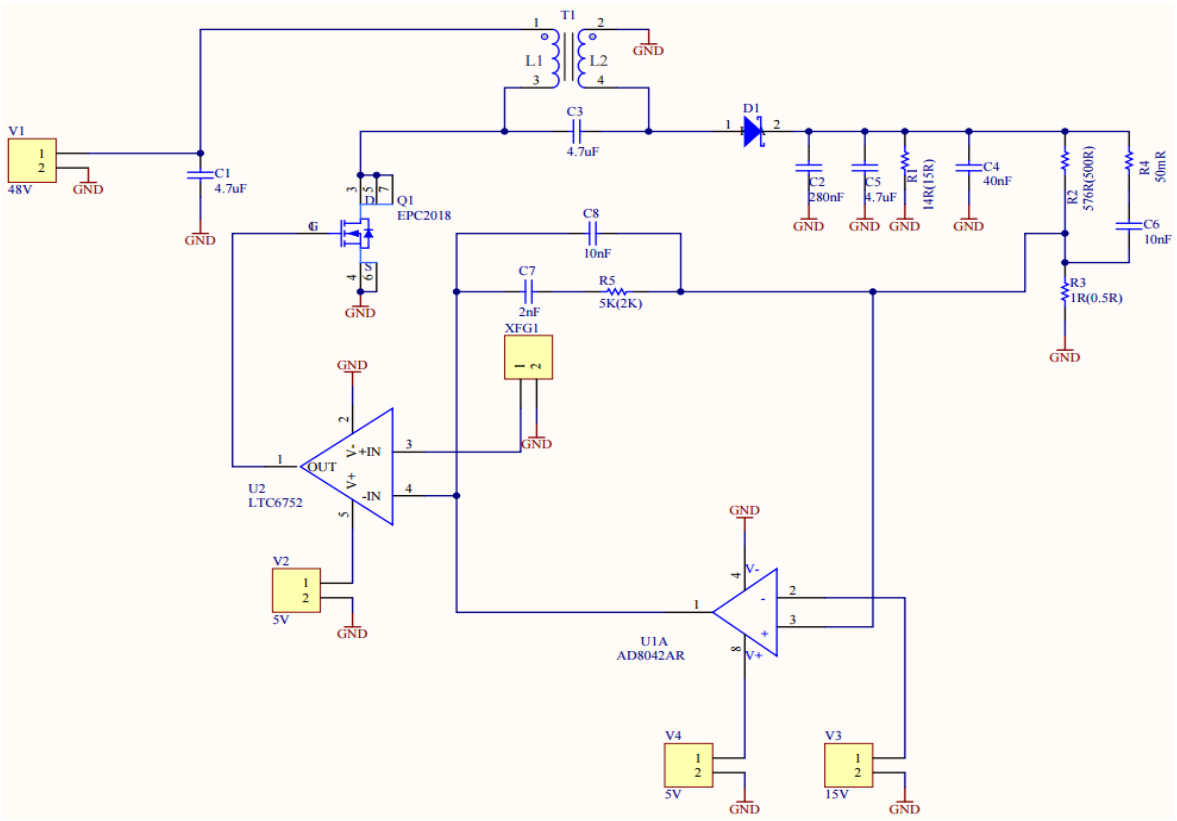


Figure 41 Schematic of current regulated SEPIC- Stage 2

Table 9 Design Components

Components	Description	Values
Input Capacitor, C_{in}	MLCC	4.7µF
Coupling Capacitor, C_c	MLCC	4.7µF
Output Capacitor, C_{out}	MLCC	4.7µF, 280nF, 40nF
Coupled Inductor, Lc	Coilcraft	20µH, 11A
GaN HEMT, Q1	EPC2018	150V, 12A
Schottky	MBRB20200CTG	200V, 20A
Error Amplifier	AD8042AR	160MHz Amplifier
Comparator	LT6752	280MHz Toggle Frequency

4.1.2a Working Principle

Feedback introduces stability problem and to handle that, a Type 3 compensator was designed in the feedback path. In Figure 40, resistors R_2, R_3, R_4, R_5 and capacitors C_6, C_7 and C_8 constitute the compensator. There were two more components apart from compensator in feedback path namely error amplifier and comparator. Error amplifier compares output from the load to a reference voltage and feeds the amplified error to the comparator. Comparator compares this error signal to a sawtooth waveform, given from a function generator in this case, and generates a pulse width modulated signal that drives gate of the EPC device.

Sawtooth signal generated by function generator was a 12V, 1.5MHz signal with 80% duty cycle to output a 42% duty cycle signal at the gate of EPC device under unregulated conditions. AD8042AR [46] was used as error amplifier as it constituted a high gain bandwidth product (160MHz) sufficient for our high frequency design. LT6752 [47] was used as the comparator as it is currently one of the fastest switching comparators available in the market with a toggle frequency of 280MHz. Details on role of error amplifier and comparator are mentioned in Chapter 1 whereas details on Type 3 compensator design can be found in Appendix with all calculations involved. Figure 42 shows simulation results of output voltage, power and current of regulated circuit.

4.2.1b Simulation Efficiency Results and Analyses

Frequency of the sawtooth generator was varied from 0.5MHz to 2.0 MHz to check for efficiency performance and Figure 42 was achieved.

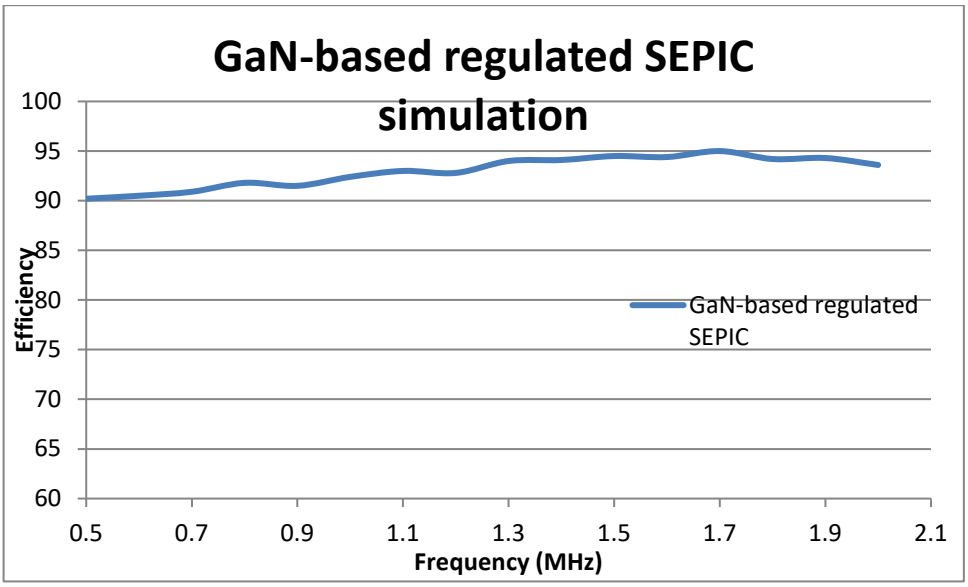


Figure 42 Simulation efficiency of regulated SEPIC-Stage 2

Simulation results showed a stable efficiency performance of the model with a peak of 95% at 1.7MHz frequency. It is pertinent to mention here that apart from inductor used in simulation, all components used were actual device models so as to accurately predict their behaviour in the circuit and estimate performance of actual design.

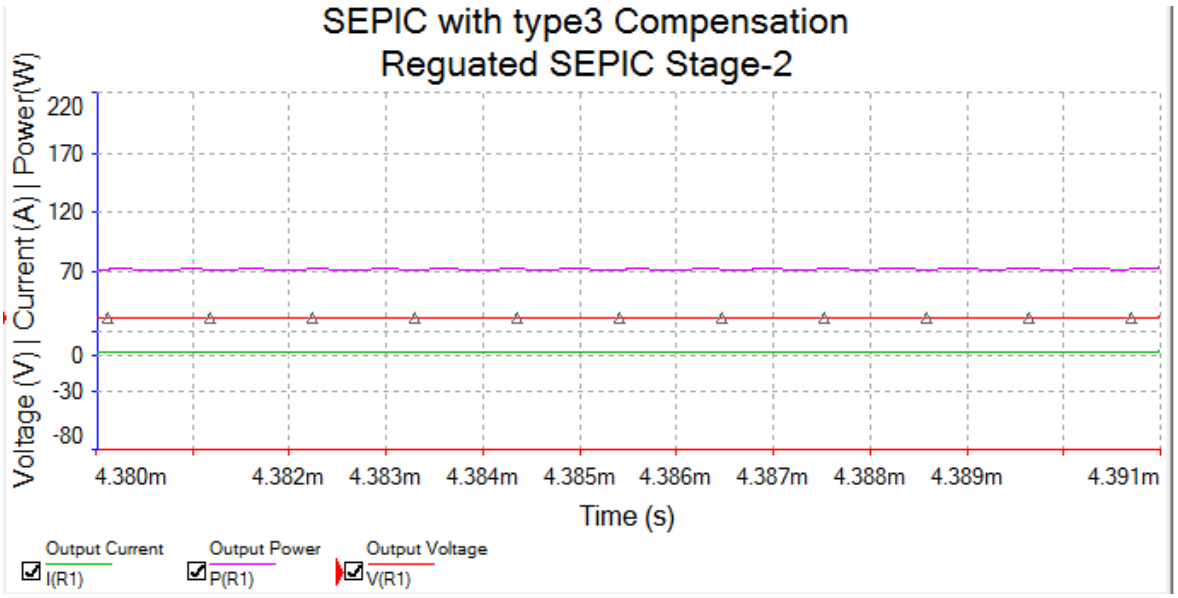


Figure 43 Regulation performance of simulated SEPIC-Stage 2

4.2.1c Simulation Regulation Results and Analyses

Line and load regulation were estimated by changing the input voltage and load resistance by 10% respectively. The circuit showed superior regulation performance.

Line Regulation

For a 10% rise in input signal (48V + 4.8V = 52.8V), the output current rose by 100mA. Thus line regulation is given by the following equation.

$$Line\ Regulation = \frac{Change\ in\ Output\ Current}{Chnage\ in\ Input\ Voltage} = \frac{100mA}{4.8V} = 20.8mA/V$$

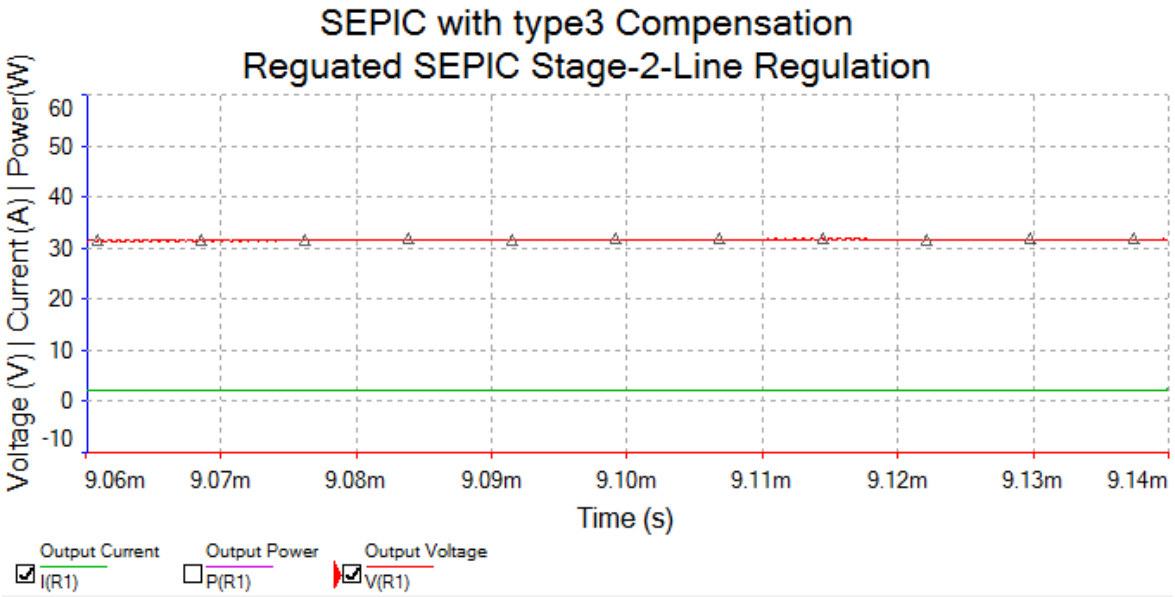


Figure 44 Line regulation performance of simulated SEPIC-Stage 2

Load Regulation

For a 10% rise in load resistance (15Ω + 1.5Ω = 16.5Ω), caused the output current to decrease by 50mA. Thus load regulation becomes.

$$Load\ Regulation = \frac{Change\ in\ Output\ Current}{Change\ in\ Output\ Resistance} = \frac{50mA}{1.5\Omega} = 33.3mA/\Omega$$

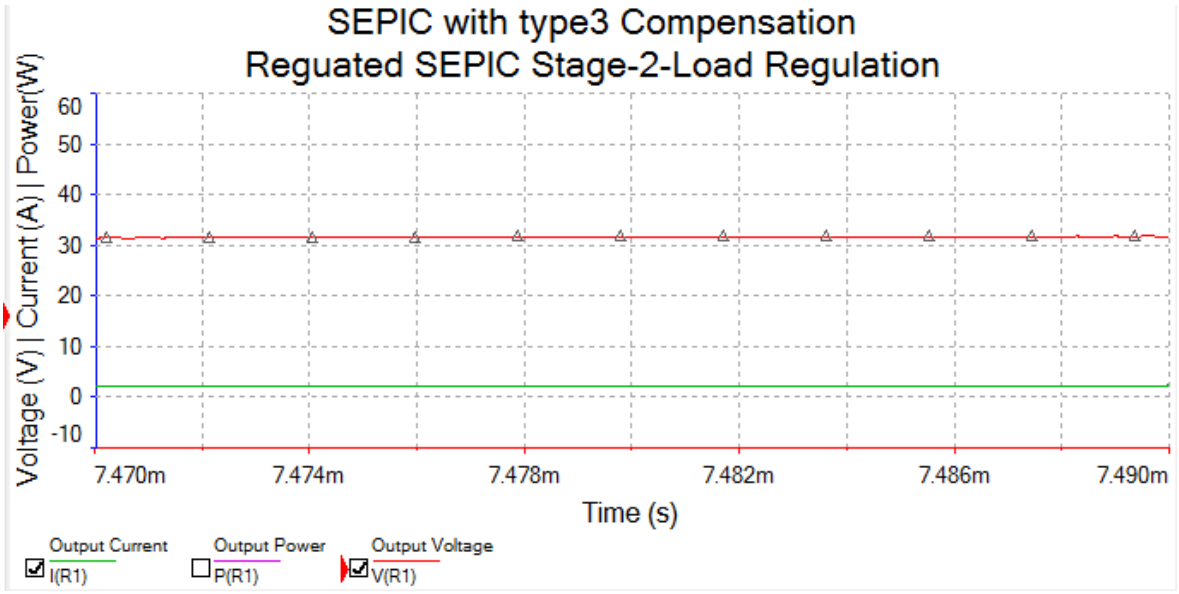


Figure 45 Load regulation performance of simulated SEPIC-Stage 2

4.2 Design and Implementation of Stage 2 Model

Three steps were involved during implementation of the simulated model; PCB layout, PCB fabrication and testing for results.

4.2.1 PCB Layout

After achieving successful results from simulation, the first phase of implementation involved PCB layout. The layout was made in NI Ultiboard14.0. The layout is 80mm * 80mm in area. Care was exercised to keep comparator close to gate of the transistor in order to keep the noise to low level as high rates of voltage change were involved. Moreover, the trace width had been chosen keeping in mind current expected to pass through the components. High continuous current traces were deliberately kept short to avoid current stress. Traces for pulsating current paths were also kept short so as to avoid radiating magnetic fields. Traces around diode and output capacitor had also been kept limited in length to avoid spikes in current. The final layout is given in Figure 45.

4.2.2 PCB Fabrication

The layout was given to a private PCB designer to manufacture the board. As some of the components were surface mount, especially with EPC device being very miniature in

design, it was difficult to solder the components in the university. So mounting job was also performed by the PCB manufacturer.

4.2.3 Testing and Results

The manufactured regulated SEPIC was tested in the laboratory for efficiency and regulation performance. Impressive results were achieved in regulation and efficiency both.

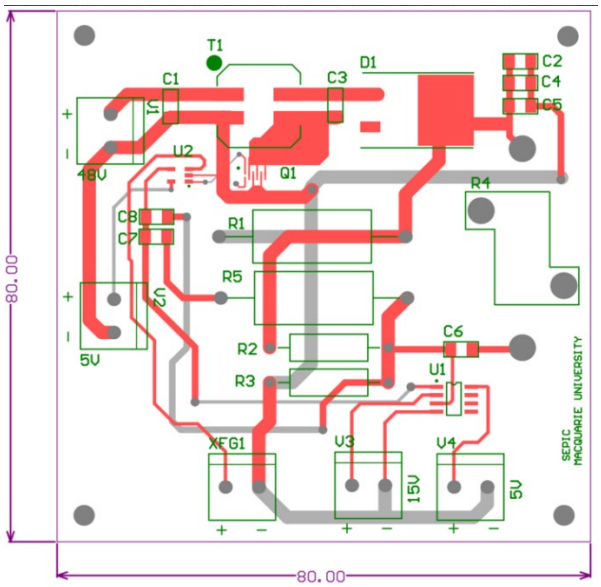


Figure 46 PCB layout of regulated SEPIC-Stage 2

The fabricated PCB with components soldered on it is shown in Figure 47.

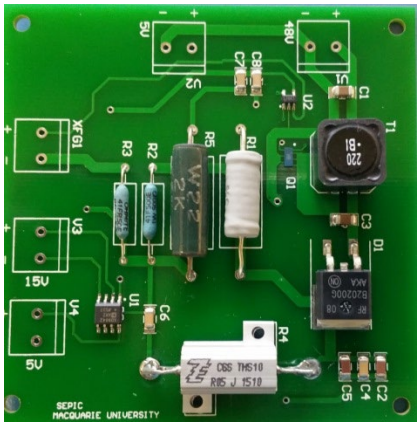


Figure 47 Fabricated PCB

4.2.3a Efficiency Performance

The circuit was designed for a frequency of 1.5MHz but was tested at 1MHz due to function generator limitation of sawtooth waveform with 0.1µs sampling time. Moreover, as

can be seen in circuit in Figure 46, the load resistor (R1) was removed and electronic load (300W, Array Electronic) was connected to measure currents and voltages. The results were verified using Keysight true-RMS digital multimeter. Waveforms were observed on a Tektronix digital oscilloscope. The circuit was tested at an input of 48V and gave an efficiency of 89%. Waveform generated at the gate is shown in Figure 48.

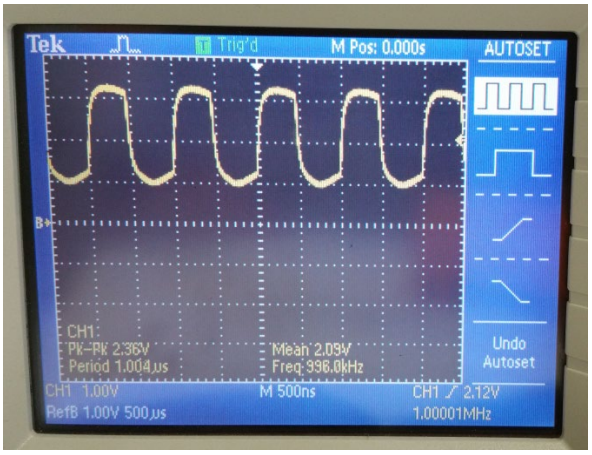


Figure 48 Output signal of comparator fed to the gate of EPC 2018

4.2.3b Regulation Performance

The line and load regulation results were 31mA/V and 48mA/Ω respectively. There was a 10% rise in line voltage induced (4.8V) to measure line regulation and 10% load resistance was increased (1.5Ω) to measure load regulation results.

The limited time to submit the thesis only allowed limited tests to be performed on this circuit. More results and consequent improvements are planned for this circuit in the near future in a bid to integrate all components on a single chip (future plan for PhD).

Chapter 5

Conclusions and Future Work

There were multiple tasks set out at the start of this research work including a) finding GaN HEMT performance efficiency in a SEPIC circuit, b) comparing GaN performance with an equivalent Si MOSFET SEPIC circuit (with all other components being the same) and c) building a current regulated GaN-based SEPIC circuit assembled with components capable of being integrated to act as an LED driver circuit. All three tasks mentioned above were successfully achieved with GaN showing promising results and outperforming Si MOSFETs especially at frequencies in MHz range.

The achieved results show an increased need for further research into the use of GaN transistors in converter circuits as they enable efficient and compact converter designs with efficiencies Si transistors fail to achieve. SEPIC built on the Transphorm board, discussed in Chapter 3, achieved highest efficiency of more than 98% for 30V to 40V input design and more than 96% for 24V to 48V input design. These efficiencies were sufficiently higher than what Si transistors achieved with a peak of just above 94% and 92% respectively in both designs.

The current regulated circuit, implemented in Chapter 4, showed impressive results in simulation as efficiency reached a peak of 95% for simulated circuit. The same design, when implemented on PCB gave satisfactory results by achieving peak performance of 89% efficiency at 1MHz frequency. Line and load regulation performance was equally satisfying with line regulation standing at 31mA/V and load regulation being 48mA/Ω.

Results summarized in previous paragraph present good performance for the circuit to be implemented as an LED driver. This research can be carried further by implementing an integrated circuit from design fabricated in Chapter 4. An LED driver IC with a GaN device at its heart will be one of the first of its kind, unlike available LED drivers in the market currently, driven mostly by Si MOSFETs. This research paves the way for future GaN-based LED drivers by first proving GaN to be better than Si in performance and then implementing a GaN-based current regulated SEPIC in Chapter 4.

With GaN devices providing superior efficiency at higher switching frequencies, more and more reduction in circuit size can be made possible by the use of smaller values of inductors and capacitors. There is still a limitation on high voltage and high frequency circuits due to multi-layer ceramic capacitors (ideal for high frequency circuits) in µF range being limited in their voltage ratings.

This research was solely focussed on modelling, design and implementation of SEPIC circuit. It would make an interesting investigation to build a flyback or buck-boost circuit from GaN device alongside SEPIC and compare them over a range of parameters to judge their performance.

High frequency design involves high switching speeds, which means currents and voltages have to rise and fall in nanoseconds which causes heating in components especially GaN. Further research can be targeted to find thermal changes occurring in GaN device during operation and finding means to effectively reduce heating problems in the circuit.

High frequency switching also causes Electromagnetic Interference (EMI) which can play havoc with voltages and currents being measured. Future work can be directed towards reducing EMI effects in the circuit. Furthermore, rise and fall times of GaN can be reduced to increase efficiency of the circuit overall.

Appendix - 1 Type 3 Compensator Design

There are 3 types of compensators for feedback designs namely type-1, type-2 and type-3 [48]. The accurate type to be used for a particular circuit depends on crossover frequencies. This section only discusses type-3 design which is mostly used when output capacitors have low ESL and ESR, like ceramic capacitors, as used in Chapter 4 design. A general type-3 compensator is shown in Figure 49.

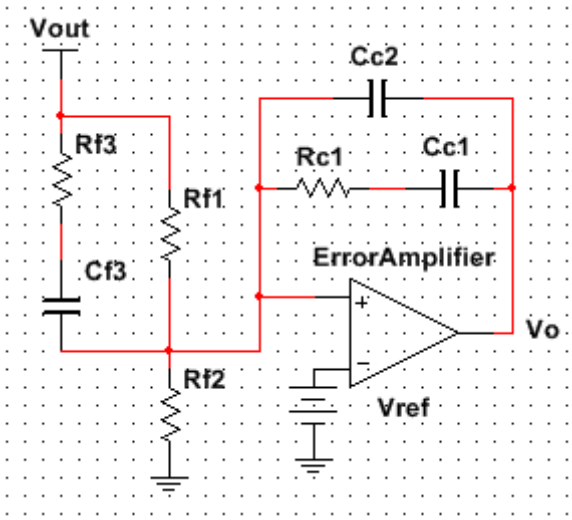


Figure 49 Type 3 compensator [48]

Let impedance Z_C denote the collective impedance of R_{C1}, C_{C1} and C_{C2} and let Z_f represent the collective impedance of R_{f1}, R_{f2}, R_{f3} and C_{f3}. The transfer function G(s) will thus be;

$$G(s) = -\frac{Z_C}{Z_f} \qquad (a)$$

By expanding impedances and resolving, the transfer function approximates to;

$$G(s) \approx -\frac{(1 + R_{C1} * C_{C1} * s) * [1 + s * C_{f3} * (R_{fi} + R_{f3})]}{s * R_{f1} * C_{C1} * (R_{C1} * C_{C2} * s + 1) * (1 + s * R_{f3} * C_{f3})} \qquad (b)$$

There are two zeros and three poles for the compensator. The following formulas give details of pole and zero equations:

$$F_{Z1} = \frac{1}{2\pi R_{C1} * C_{C1}} \qquad (c)$$

$$F_{Z2} = \frac{1}{2\pi C_{f3*}(R_{f1} + R_{f3})} \qquad (d)$$

$$F_{P1} = 0 \qquad (e)$$

$$F_{P2} = \frac{1}{2\pi R_{f3} * C_{f3}} \qquad (f)$$

$$F_{P3} = \frac{1}{2\pi R_{C1} * C_{C2}} \qquad (g)$$

For the case of MLCCs, F_{P3} is defined as half the switching frequency F_s. F_{Z2} and F_{P2} form lead compensators and are affected by lead angle (∅) desired for compensation.

$$F_{Z2} = F_O \sqrt{\frac{1 - \sin \emptyset}{1 + sin\emptyset}} \qquad (h)$$

$$F_{P2} = F_O \sqrt{\frac{1 + \sin \emptyset}{1 - sin\emptyset}} \qquad (i)$$

$$F_{P3} = \frac{F_s}{2} \qquad (j)$$

From equations (h), (i) and (j), values of pole and zero frequencies can be found which when put back in equations (c) through (g) result in values of resistors and capacitors forming type-3 compensator. Values of resistors and capacitors forming the compensator used in Chapter 4, using equations shown above, are given in Table 10.

Table 10 Calculated compensator parameters

Components	Values

R_{f1}	2kΩ
R_{f2}	500mΩ
R_{f3}	50mΩ
R_{C1}	5kΩ
C_{C1}	2nF
C_{C2}	10nF
C_{f3}	10nF

Appendix-2 To-be submitted paper [5]

Performance Comparison of GaN and Si-based FETs in a SEPIC Circuit

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***Abstract*—Improved performance parameters of Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs), such as low on resistance, high electron mobility, low gate and reverse recovery charge in comparison to silicon (Si) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), are motivating increased interest in the use of GaN devices in modern power converters. Recent research is focused on operating power converters at higher frequencies so as to help reduce converter size. The single-ended primary inductor converter (SEPIC), due to its low component count and lack of inversion problem, presents an attractive option for designs where compact buck or boost conversion is required. We compare the performance of SEPIC converter over a range of input voltage (24V to 48V), operating frequency (0.5MHz to 1.9MHz) and duty cycle (30% to 60%) using GaN HEMT and Si MOSFET. The peak measured efficiency of the circuit was found to be 96.47% at 48V input and 40% duty cycle (75W load, 1.8MHz). Whereas, the peak efficiency with Si device was measured to be 92.4% at 48V input and 50% duty cycle (100W load, 1MHz). The results support increased performance efficiency of GaN HEMTs over Si in MHz frequency range.**

***Index Terms*—DC-DC converter, GaN-Si comparison, high frequency SEPIC.**

I. Introduction

Silicon (Si) metal oxide semiconductor field effect transistors (MOSFETs) have been serving the field of power conversion for over three decades [1] and have reached the peak of their material performance capabilities [2]. The performance limitation coupled with the fact that GaN transistors have lower on resistance, higher voltage capabilities and increased power density as compared to Si can make way for increased use of GaN in high frequency power converters [1]. Higher frequencies result in minimizing size of the converter [3], whereas, an increase in power density enables the use of GaN in radio frequency range power supplies [4] and a lower on resistance helps to keep the power losses down making GaN an ideal candidate for efficient conversion circuits [5].

GaN devices have frequently been used in both buck and boost applications [6-9]. A SEPIC provides both functionalities of buck and boost without the problem of inversion like in a buck-boost converter. There have been a few designs of SEPIC based LED drivers making use of Si MOSFET to perform switching operations [10-13]. The problem with these designs is that they are tuned to work at low frequencies causing inductors to be large and thus incurring losses. A GaN-based SEPIC, however, can eliminate the low frequency issue thereby reducing size of the inductor, and thus the overall circuit size, significantly.

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II. Design

A SEPIC circuit was designed on Transphorm board for constant current applications such as LED drivers. The following table lists initial design parameters:

TABLE I
DESIGN PARAMETERS

Parameters	Values
Input Voltage Range, V_{in}	24V – 48V
Output Voltage, V_{out}	36V
Output Current, I_{out}	2.5A
Optimum Load Power	90W
Current Ripple	40%
Operating Frequency, f_s	1.5MHz

The input voltage range is targeted to suit a DC bus of either 24V or 48V. Output of 36V allowed both buck and boost operations to be tested. The circuit was designed for 40% current ripple as suggested by most texts. Moreover, the SEPIC was designed for 1.5MHz frequency but tested over a range of frequencies (0.5MHz – 1.9MHz) to observe its performance.

For the mentioned input range, the duty cycle was calculated by using the formula below:

$$Duty\ Cycle\ (min) = \frac{V_{out} + V_d}{V_{in(max)} + V_{out} + V_d} \quad (1)$$

$$Duty\ Cycle\ (max) = \frac{V_{out} + V_d}{V_{in(min)} + V_{out} + V_d} \quad (2)$$

(2)

V_d is the diode forward voltage drop whereas $V_{in(min)}$ and $V_{in(max)}$ are 24V and 48V respectively. Using (1) and (2), the

range of duty cycle was calculated to be 42% to 60%. Considering 40% ripple [14], the ripple current was found to be 1.5A peak using (3)

$$I_{ripple} = \frac{I_{out} * V_{out} * (\% \Delta I_{ripple})}{V_{in(min)}} \quad (3)$$

A 10µH Coilcraft coupling inductor was chosen to reduce input ripple. The RMS current through the inductor (3.94A) was calculated using the following equation, assuming a 95% efficient system:

$$I_{Lrms} = \frac{V_{out} * I_{out}}{V_{in(min)} * \eta} \quad (4)$$

The peak current through the circuit (7.25A) was calculated by using (5) and all circuit devices were chosen to accommodate this peak:

$$I_{peak} = I_{Lrms} + I_{out} + 0.5\, I_{ripple} \quad (5)$$

III. Implementation

The circuit was implemented on a Transphorm boost driver board, TDPS501E0A with some changes to make it a SEPIC. The board consists of a 600V GaN HEMT, TPH3006PS, with a current rating of 17A. The GaN is driven by FAN3100C which limits the board's performance to 2MHz operating frequency. The FAN IC is driven by a 5V square wave provided by a function generator. Rectification at the output was performed by a 600V Silicon Carbide (SiC) Schottky diode, CREE C3D06060. The driver board has a simple design and low component count. Also, the HEMT is a GaN on Si device thus FAN driver is able to drive both transistors which provides an efficient platform for GaN vs Si comparative analysis.

A 450V, 4.7µF film capacitor was added to the input to reduce supply voltage ripple. A 10µH coupled inductor, MSD1583, from Coilcraft was selected due to its low DC resistance and a saturation current rating of 11A. A 450V, 4.7µF film capacitor was used as a coupling capacitor connected between drain and coupling inductor. Fig. 1 shows circuit diagram of the SEPIC converter as implemented on Transphorm board. Red dotted lines indicate changes to the original circuit board. The changes made were very minor, maintaining compactness of the circuit.

Input and output signals were measured with the help of 100MHz Tektronix digital storage oscilloscope and multiple digital multimeters (DMMs). A Rogowski coil was used to determine current waveforms through capacitor and inductor. A 300W Electronic load from Array Electronic served as active load for the circuit drawing an output current of 2.5A as per design. FAN IC was driven by a 15MHz Hewlett Packard function generator. The design was tested over a wide range of frequencies (0.5MHz- 1.9MHz), duty cycles (30% - 60%) and input voltages (24V – 48V) to make a thorough comparison of both GaN and Si devices. Details of performance comparison results are presented in the next section. This SEPIC design was able to attain a maximum efficiency of 96.47% at 48V input and 40% duty cycle with switching device being GaN HEMT whereas Si MOSFET peaked at the same voltage input with 92.4% efficiency at 50% duty cycle.

IV. Results

Experiments were carried out on SEPIC circuit with Si MOSFET and GaN HEMT and GaN surpassed Si in efficiency as frequency was raised in MHz range over a range of duty cycle, input voltage and load power levels. The following graphs highlight performance of both devices in our experimental setup. Figure 2 shows efficiency measurements of both devices for 48V input at a duty cycle of 0.42. The efficiency comparison of both devices for an input of 24V is given is shown in Figure 3. Figure 4 and 5 represent efficiency in comparison to load power for 48V and 24V respectively.

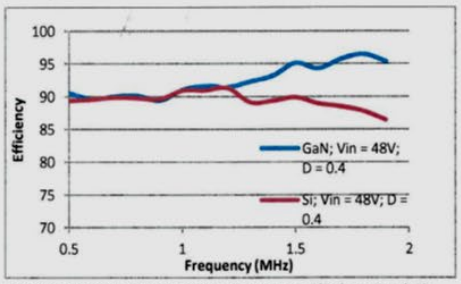

Fig. 2. Measured efficiency against frequency at 48V input D = 0.42

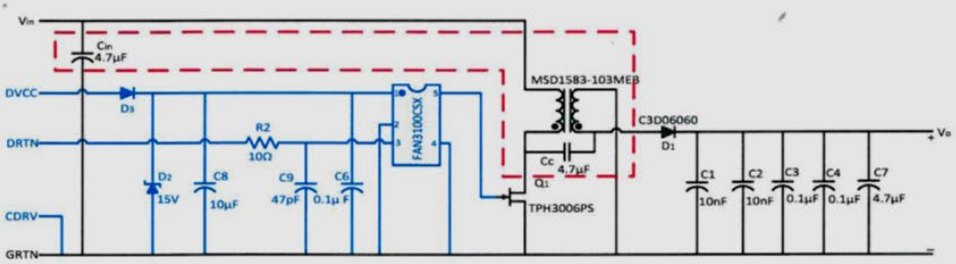

Fig. 1 SEPIC built on Transphorm board (red lines show additions to the built-in circuit) [15,16]

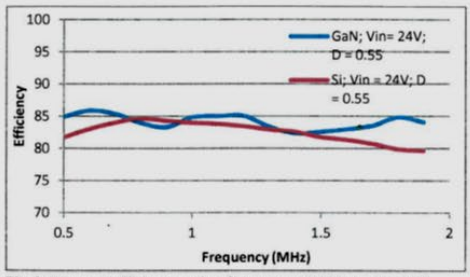

Fig. 3. Measured efficiency against frequency at 24V input, D = 0.55

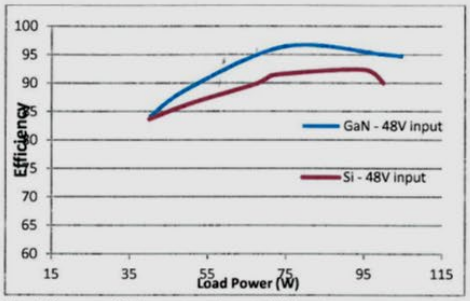

Fig. 4. Power vs efficiency comparison at 48V input

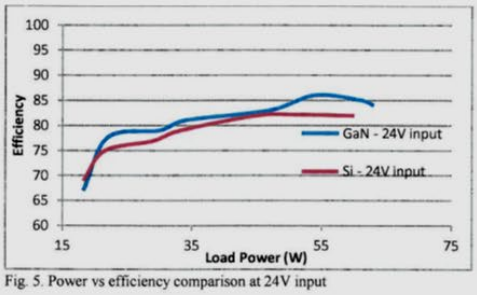

Fig. 5. Power vs efficiency comparison at 24V input

V. Comparative Analysis

The idea behind use of a Transphorm board was to have a platform in which Si can be replaced by a GaN HEMT with rest of the circuit design remaining the same. For a fair comparison, a 600V superjunction Si MOSFET, SiHP22N60S from Vishay, was selected with same R_{DSon} (150mΩ) as GaN HEMT. Moreover, the selected Si MOSFET was able to be driven by onboard FAN driver IC.

Both GaN and Si converter circuits were tested for their efficiency performance over a wide range of input parameters. The GaN HEMT was found to be more efficient at higher frequencies primarily because of high switching loss occurring in Si MOSFETs at those frequencies. The following loss calculations justify higher efficiency of GaN over Si at higher frequencies.

A. Loss Calculations

This section presents calculations for power loss in the design. It is pertinent to mention that both transistors and diode are 600V devices with capacitors rated at 450V giving more than enough voltage leverage for our design specifications with a peak voltage of 84V ($V_{inmax} + V_{out}$) only. An estimate of the power lost in the circuit was found by calculating transistor, gate drive, inductor and diode losses. Film capacitors used are very low in equivalent series resistance (ESR), thus their loss impact is neglected.

Power dissipated in the 10μH inductor due to DC resistance (400mW), P_{DCR}, is given by the following equation:

$$P_{DCR} = I_{Lrms}^2 * DCR \quad (6)$$

where DCR is the DC resistance of the coupled inductor (26mΩ). Core loss for the inductor is found using Coilcraft's online resource and comes out to 6mW only. AC resistance loss is neglected due to very low value of AC resistance.

Power lost in diode is found by first finding its internal resistance by the use of following equation:

$$R_T = 0.09 + (T_j * 0.51 * 10^{-3}) \quad (7)$$

where R_T is internal resistance of the diode and T_j is junction temperature. For a junction temperature of 40^0C, R_T comes out to be 115mΩ. Power loss for output current of 2.5A through the diode (719mW) can be found by:

$$P_{diode} = I_{out}^2 * R_T \quad (8)$$

Power consumed by FAN driver IC (432mW), at 1.5MHz, is found using the following formula:

$$P_{driver_p} = I_{dynamic} * V_{DD} \quad (9)$$

where $I_{dynamic}$ is current needed to drive the IC (36mA at 1.5MHz) and V_{DD} is 12V.

Losses in switching devices are broadly categorized as conduction and switching losses [17]:

$$P_{cond} = R_{DSon} * I_{rms}^2 \quad (10)$$

$$P_{switch-transition} = V_{in} * I_{out} * f_s * t_s \quad (11)$$

Due to the fact that both devices were specially chosen to have the same on-resistance, conduction loss for each is assumed to be same as the other (375mW). Switching loss as mentioned in (11) is due to overlap of current and voltage in the transistor. t_s, the switching time for Si is 24ns and 4ns for GaN. This makes switching loss for both devices stand at 75mW (GaN) and 450mW (Si).

Switching losses are also contributed by reverse recovery. Si being a minority carrier device suffers from relatively large reverse recovery loss (1.875W) in contrast to GaN (9.3mW) which can be calculated from the following equation:

$$P_{rr} = f_s * Q_{rr} * V_{in} \quad (12)$$

where Q_{rr} is MOSFET's reverse recovery charge which stands in this circuit at 250nC for Si as compared to 1nC for GaN HEMT at 1.5MHz; 250 times more. It is evident that as frequency increases, losses in Si MOSFET increase significantly relative to GaN HEMT as will be shown in the next section.

Energy dissipated in output capacitor (C_{oss}) of the MOSFET is another contributor of transistor power loss. Respective values of output charge (Q_{oss}) for Si MOSFET and GaN

HEMT are 7nC and 0.65nC respectively leading to output capacitance power loss that can be calculated from:

$$P_{ocap} = f_s * Q_{oss} * V_{in} \quad (13)$$

For 1.5MHz operation, Si MOSFET suffers an output capacitor loss of 52mW whereas GaN only loses 5mW at the output of HEMT. Power loss linked to body diode of the transistor can be calculated by:

$$P_{bdiode} = f_s * V_{SD} * I_{out} * t_{rr} \quad (14)$$

where V_{SD} is diode forward voltage having 1.2V value for Si and 1.9V in case of GaN. t_{rr} is the reverse recovery time. Si MOSFET has t_{rr} of 462ns and GaN HEMT possesses a 30ns recovery time. Power consumed in GaN HEMT body diode is evaluated to be 213mW whereas body diode of Si contributes a loss of 2W.

A table below provides a summary of estimated losses at 1.5MHz.

TABLE III
LOSS COMPARISON AT 1.5MHZ

Loss Component	GaN Loss (mW)	Si Loss (mW)
Conduction	375	375
Switch-Transition	75	450
Reverse Recovery	9.3	1875
Output Capacitor	5	52
Body Diode	213	2000
Total Loss	**677.3**	**4752**

As can be seen from the above table, Si MOSFET contributes a loss approximately 7 times more than GaN HEMT at 1.5MHz. The following graph provides an estimate of losses in both devices at various frequencies.

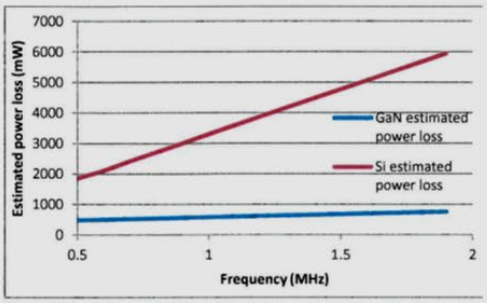

Fig. 6. Estimated power loss in each switch

VI. DISCUSSION

The results show efficiency of our SEPIC design to be better at 48V input as compared to 24V. The reason for low efficiency performance of 24V input is that the circuit is tested for constant output current for all iterations of frequency and duty cycle rather than constant voltage. For a constant voltage output, 24V input would have resulted in an output current of 1.5A approximately But as the circuit is forced to output 2.5A, the losses are higher. At 1.5MHz frequency, 40% duty cycle and 48V input, the power lost by SEPIC run on GaN HEMT is 4W whereas power consumed by Si-based SEPIC circuit is 8.1W. With all other circuit components being the same, Si loses approximately 4W more than GaN as predicted by mathematical calculations earlier in this section. At lower frequencies, losses incurred in passive components are more dominant in case of GaN than Si. It can be seen that there is a significant difference in efficiency of both devices generally at frequencies higher than 1.5MHz over input voltage and duty cycle range encouraging the use of GaN HEMT for high frequency power converters.

VII. CONCLUSION

The presented work gives an insight into performance comparison of GaN HEMT and Si MOSFET in a SEPIC design. The results advocate the use of GaN HEMTs in MHz frequency range due to low switching losses as compared to Si MOSFETs. The use of Transphorm board provided a compact platform for SEPIC design and the benefit of having driver circuit onboard.

Future work can be targeted towards self-exciting the circuit and building a SEPIC circuit capable of being integrated. Thermal measurements can be done to obtain better transistor loss understanding. Current regulation can also be accommodated with its necessity in LED driver designs.

ACKNOWLEDGMENT

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