PULSE WIDTH MODULATION TECHNIQUES TO SUPPRESS ELECTROMAGNETIC INTERFERENCE IN POWER CONVERTERS

by

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ABSTRACT

Rapid developments in power electronics and semiconductor manufacturing technology have increased the integration of power electronic converters in our everyday life. From biomedical services, utilities, electric cars up to satellite power systems, power electronics has been widely adopted to fulfil the power demands in the most efficient possible ways.

The modern power converter can be viewed as a combination of power switching devices, switched in a pattern to charge/discharge various passive elements to produce the required voltages and currents in a controlled manner. This switching pattern leads to a natural phenomenon of producing voltage and current transitions (dv/dt and di/dt respectively) which are the main cause of electromagnetic interference (EMI) noise from power converters. This noise may be conducted and/or radiated, leading to interference with neighboring electronic circuits and systems. Hence various electromagnetic compatibility (EMC) standards are introduced to keep the naturally occurring noise within a threshold limit.

Traditionally, EMI filters are used to suppress conducted EMI and hence are applicable to a narrow range of frequencies. On the other hand, EMI shielding is used for shielding the sources of EMI in an enclosed chamber to contain the radiated EMI. Both solutions have their limitations and increase the cost and weight of a power converter. Spread-spectrum techniques are utilized to spread the noise over a wider bandwidth, which leads to the suppression of the peaks of EMI, and which eventually suppresses the EMI.

The research work presented in this thesis is based on the generation and application of an aperiodic modulation methodology, which effectively spreads the spectrum of switching harmonics over a wide range of frequencies. It subsequently suppresses the peak EMI of a

power converter. A framework to generate such an aperiodic pulse-width modulated signal is presented which can readily be applied to different types of power converters to suppress the EMI. To support this proposition, the modulation methodology has been applied to a single-ended primary-inductor converter (SEPIC) converter, a quasi-Z-source (qZS) DC-DC and a novel transformerless common-ground DC-AC inverter. The suppression in EMI is presented for these converter topologies along with various simulation and experimental results in support of the proposed methodology. Since wide-bandgap (WBG)-based power semiconductor devices allow faster switching, with its associated transients, WBG-based power converters generate more EMI than their silicon-based counterparts. Therefore, WBG-based power converters here are considered for application to the proposed methodology. The hardware prototypes have been developed to integrate WBG power switches, which makes the results more thought-provoking and conclusive.

The presented aperiodic modulation methodology is generalized, which is applicable to a large variety of modern power converters. Various theoretical, analytical and empirical insights are presented in this thesis which develop a sound base for the understanding and suppression of EMI in power converters.

Keywords: Electromagnetic interference (EMI), electromagnetic compatibility (EMC), pulse width modulation (PWM), wide bandgap (WBG) semiconductors, spread-spectrum techniques.

STATEMENT OF CANDIDATE

I certify that the work in this dissertation titled "Pulse Width Modulation Techniques to suppress Electromagnetic Interference in Power Converters" has not previously been submitted for a degree nor has it been submitted as part of the requirements for a degree to any other university or institution other than Macquarie University. I also certify that the dissertation is an original piece of research and it has been written by me. In addition, I certify that all information sources and literature used are indicated in the dissertation.

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Saad Ul Hasan

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Dedicated to my awesome parents, siblings

&

all the people who are struggling

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"*All praise and thanks to the Almighty (swt)*"

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List of Publications

Patents

1. **S. U. Hasan** and G. E. Town, "Modulation method and apparatus to reduce EMI in a power converter," AU patent WO2017120644 A1, Jan. 15, 2016.

Refereed Journal Papers

2. **S. U. Hasan** and G. Town, "An Aperiodic Modulation Method to Mitigate Electromagnetic Interference in Impedance Source DC-DC Converters," in IEEE Transactions on Power Electronics, 2017 (early access). [Chapters 2 and 4]
3. **S. U. Hasan**, H. A. Hassan, M. J. Scott, Y. Siwakoti and G. E. Town, "Common-Ground Transformerless Inverter with virtual DC bus concept for Single-Phase PV Systems", Journal of Emerging and Selected Topics in Power Electronics (JESTPE), 2018 (under review), Manuscript ID: JESTPE-2018-04-0386. [Chapter 5]
4. **S. U. Hasan**, H. A. Hassan and G. E. Town, "An aperiodic modulation strategy to reduce peak EMI in a high frequency Coupled Inductor based SEPIC converter". (In draft, to be submitted to JESTPE). [Chapters 2 and 3]

Refereed Conference Papers

5. **S. U. Hasan** and G. E. Town, "A Quasi-periodic modulation strategy to mitigate EMI for a GaN-based Quasi-Z-Source DC-DC converter", IEEE Energy Conversion Congress and Expo (ECCE), USA, 2016. [Chapters 2 and 4]
6. **S. U. Hasan** and G. E. Town, "An FPGA-based aperiodic modulation strategy for EMI suppression in quasi-Z-source DC-DC converters", IEEE International Symposium on Circuits and Systems (ISCAS), USA, 2017. [Chapters 2 and 4]

7. **S. U. Hasan**, Y. R. Kafle and G. E. Town, "Aperiodic pulse-modulation technique to reduce peak EMI in impedance-source DC-DC converters", IEEE Energy Conversion Congress and Expo (ECCE), USA, 2017. [Chapters 2 and 4]
8. **S. U. Hasan**, Y. R. Kafle and G. E. Town, "Simple spread-spectrum pulse-modulation technique for EMI mitigation in power converters", Australasian Universities Power Engineering Conference (AUPEC), Australia, 2017. [Chapters 2 to 4]
9. **S. U. Hasan**, B. Shaffer, H. A. Hassan, M. J. Scott, Y. Siwakoti and G. E. Town, "Common-ground transformerless inverter for solar photovoltaic module", IEEE Applied Power Electronics Conference and Exposition (APEC), USA, 2018. [Chapter 5]

Other Co-authored Publications during PhD Candidature

10. Y. R. Kafle, **S. U. Hasan** and G. E. Town, "A new PWM shoot-through control technique to reduce switching losses in impedance source DC/DC converters", IEEE Energy Conversion Congress and Expo (ECCE), USA, 2017.
11. Y. R. Kafle, **S. U. Hasan**, M. Kashif, J. Hossain and G. E. Town, "A new PWM Shoot-through control for voltage-fed quasi-Z-source DC/DC converters", IEEE International Telecommunications Energy Conference (INTELEC), Australia, 2017.
12. B. Shaffer, H. A. Hassan, M. J. Scott, **S. U. Hasan**, G. E. Town and Y. Siwakoti, "A common-ground single-phase five-level transformerless boost inverter for photovoltaic applications", IEEE Applied Power Electronics Conference and Exposition (APEC), USA, 2018.
13. Y. R. Kafle, G. E. Town and **S. U. Hasan**, "Quasi-Z-source based Bidirectional DC-DC Converter and its Control strategy", Journal of Power Electronics (JPE), 2018 (under review), Manuscript ID: JPE-18-04-096 (0001).

Chapter 1

Introduction and Motivation

1.1. Overview and Significance of the Research Topic

Given that global energy demands are ever-increasing and fossil fuels are no longer 'infinite', the scientific community has started utilizing renewable energy sources as power generation sources. It is thus timely to develop and implement sophisticated, efficient and cost-effective energy generation, provision and utilization systems. Power Electronics provides the key enabling infrastructure which continues to develop and be able to integrate in electric power generation and utilization. It is believed that more than 30% of the generated electric power flows through the power electronics, and this number is expected to increase up to 80% by the year 2030 [1].

In the last seven decades, the integration of a wide range of power electronic converters has been rapidly increasing in our daily lives as well as in industries. Starting from consumer

products such as portable battery banks, laptop adapters, electric vehicles, and now public utilities, the power electronics field finds wide-ranging applications. Moreover, the semiconductor manufacturing industry has also boomed in recent decades and can now provide the most sophisticated products. This has undoubtedly increased our expectations regarding the size, efficiency, cost and compatibility of power converters.

Recent developments in the semiconductor manufacturing industry have pushed silicon-based semiconductor technology to its theoretical limits which is not enough for the modern power conversion applications and expectations. These requirements include lower on-state resistance ($R_{DS(ON)}$), higher reverse blocking voltage, better thermal performance and ability to be switched at relatively higher switching frequencies, in the MHz range [2]. Wide Bandgap (WBG)-based power semiconductor materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have been introduced to meet the aforementioned requirements. The advent of WBG semiconductor devices has triggered a new research stream leading to the utilization of planar magnetics, switched capacitors and resonance techniques to achieve soft-switching and optimized printed circuit board (PCB) design. It means utilizing this emerging technology in the best way possible.

Rapidly changing voltages and currents in a power converter lead to noise emissions and, as the integration of power converters keeps on increasing rapidly, we are now virtually surrounded by power electronics generated noise sources. This is in addition to some noise sources based on natural phenomena. Increased noise is a major concern associated with power converters and the presented research examines this aspect of power converters. Fig. 1.1 illustrates a typical noise environment.

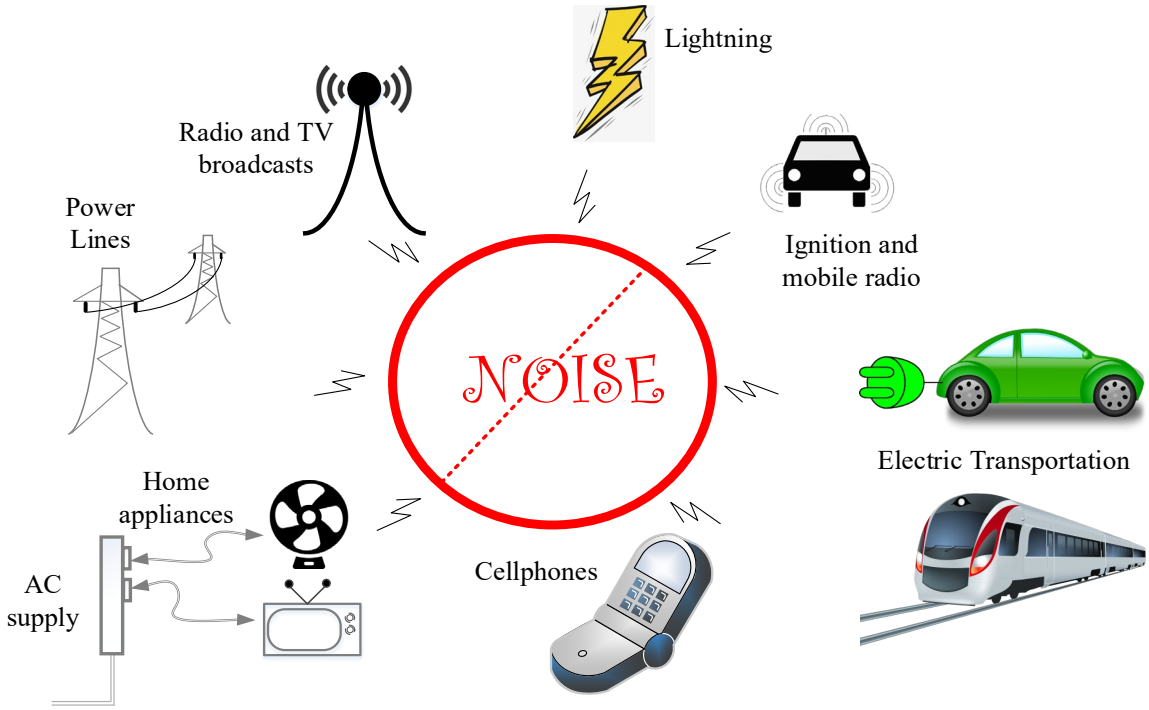


Figure 1.1. Natural/man-made common sources of EMI.

1.2. Problem Statement and Research Motivation

Semiconductor switches are considered to be the heart of a power converter. These switches are properly selected and operated along with various other passive components (such as inductors and/or capacitors) to ensure optimal operation for a given application. In power electronic conversion, switching is utilized to achieve the required voltage(s) and current(s) in accordance with particular applications. In steady-state operation, the duty cycle and switching frequency are kept constant, which leads to voltage and current transitions, resulting in electromagnetic interference (EMI). The harmonic powers of the input current and output voltage, hence can be seen as concentrated on multiples of the switching frequency at which it is operated [3]. WBG materials on one hand help to attain better performance in terms of efficiency, thermal stability and high power density, but on

the other hand, due to the higher switching speeds ($\sim ns$) as compared to their silicon counterparts, a broadband harmonic power distribution can be seen. Hence, WBG power devices can be seen as a double-edged sword which can realize the most sophisticated power conversion practices, but on the other hand, increase the spectral peaks and its bandwidth [4], [5]. With more power electronics research and development underway, various electromagnetic compatibility (EMC) standards [6] have been defined by the standardization agencies worldwide. These have sort to keep the noise levels under defined thresholds. Therefore, with the emergence of WBG power conversion technology, addressing the EMI matter has become more crucial.

1.3. Objectives and Scope of Dissertation

This dissertation proposes a new approach to implementing an aperiodic modulation technique for driving the switch(es) in a power converter, leading to the suppression of the spectral peaks of the associated harmonic power. The proposed methodology is implementable flexibly via both analog and digital practices. Moreover, the proposed framework is compliantly extended and applied to single-switch and multi-switch power converters. This dissertation also investigates the core performance parameters of power converters such as efficiency, voltage gain etc. in relation to the applied modulation methodology. It is pertinent to mention here that a more heuristic approach is adopted for this dissertation to explore the engineering aspects of power converters. Nevertheless, the basic analyses of the spread-spectrum modulation techniques have been added to familiarize the reader with the related generalizations. Moreover the EMI measurements have not been compared with the typical EMC standards due to the laboratory setup constraints.

1.4. Dissertation Outline

This dissertation is organized into six chapters including the Introduction and motivation (Chapter 1). The contents of Chapters 2-6 are briefly described here:

Chapter 2 provides the background context of this work. The reader can get a general idea about EMI in power converters, the traditional techniques to suppress EMI noise in power converters and an overview of the various EMI measurement techniques.

Chapter 3 presents a framework for implementing an aperiodically modulated switching signal which is then applied to a GaN high electron mobility transistor (HEMT)-based single-ended primary-inductor converter (SEPIC) to investigate the EMI suppression. The spectral analysis of the switching signal is also discussed to better understand the harmonics spreading phenomenon. Moreover, as the SEPIC converter is designed to be used as an LED driver and concur with a GaN switch, the converter is designed to be operated at high switching frequency, and hence various design guidelines/insights are also outlined in this chapter. Finally, experimental results such as efficiency and voltage-gain index are explained to justify the usefulness of the proposed technique.

Chapter 4 extends the proposed aperiodic modulation methodology to generate a coordinated set of hybrid pulse-modulation signals for application to a cascode GaN HEMT-based quasi-Z-source (qZS) DC-DC converter. The characteristic shoot-thorough states are specifically considered in this case to ensure a constant gain. Both quasi-periodic and aperiodic modulation techniques are applied to investigate the EMI suppression. The voltage gain and efficiency index are also presented to analyze the proposed technique's performance.

Chapter 5 introduces a novel common-ground, transformerless inverter topology for photovoltaic (PV) systems, and various switching states and design insights are discussed. The proposed topology employs a double-charging process to charge a virtual DC bus capacitor through an inductor, hence making a topological contribution to EMI suppression. Additionally, an aperiodic modulation is compliantly applied to furthermore suppress the EMI. Finally, a comparison in terms of efficiency index, total harmonic distortion (THD) and various key waveforms is presented for a 1 kW prototype.

Finally, **Chapter 6** concludes the dissertation and future work avenues are suggested.

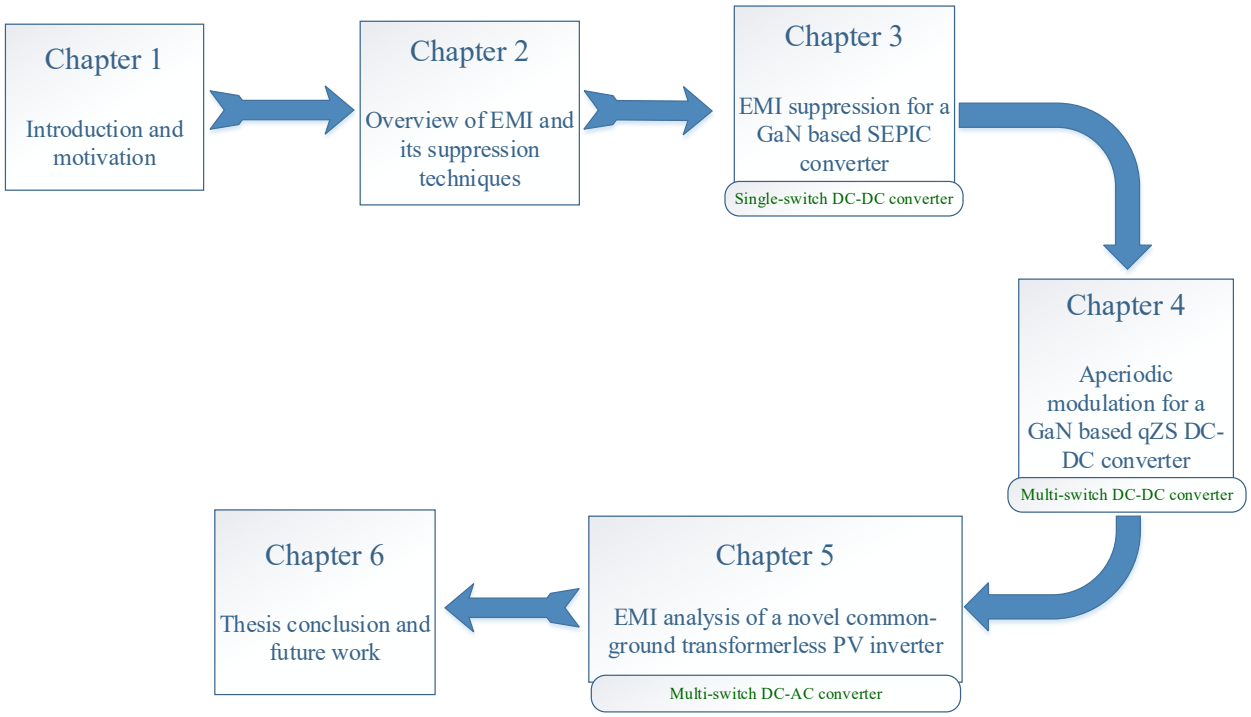


Figure 1.2. Thesis outline

Chapter 2

An Overview of EMI and Its Suppression Techniques

This chapter is dedicated to the preliminary knowledge associated with EMI in power converters. A general overview of EMI along with its different types is discussed. Various EMC standards are also listed which confine the noise produced by various sources below specified limits in accordance with different applications. Moreover, the EMI measurement methods and techniques are discussed. Finally, an overview of EMI suppression techniques is given.

2.1. EMI and EMC of Power Converters

All modern power converters can be viewed as a combination of reactive elements and power switches for energy storage and control respectively. The power switches are usually driven at a constant switching frequency with a constant or varying duty cycle, depending

on the control strategy. Eventually, in the steady-state operation of a power converter, the duty cycle and frequency remain fixed and, due to their switching mode, the power converters are also referred to as switching power converters. Switching often results in large voltage and current transitions (high dv/dt and di/dt respectively), which in turn generate broadband electromagnetic emissions. This phenomenon is the basis of the EMI generated in power converters. Since high efficiency and high power density are major driving forces for modern power converters, the di/dt and dv/dt increase even more, and hence cause severe EMI problems.

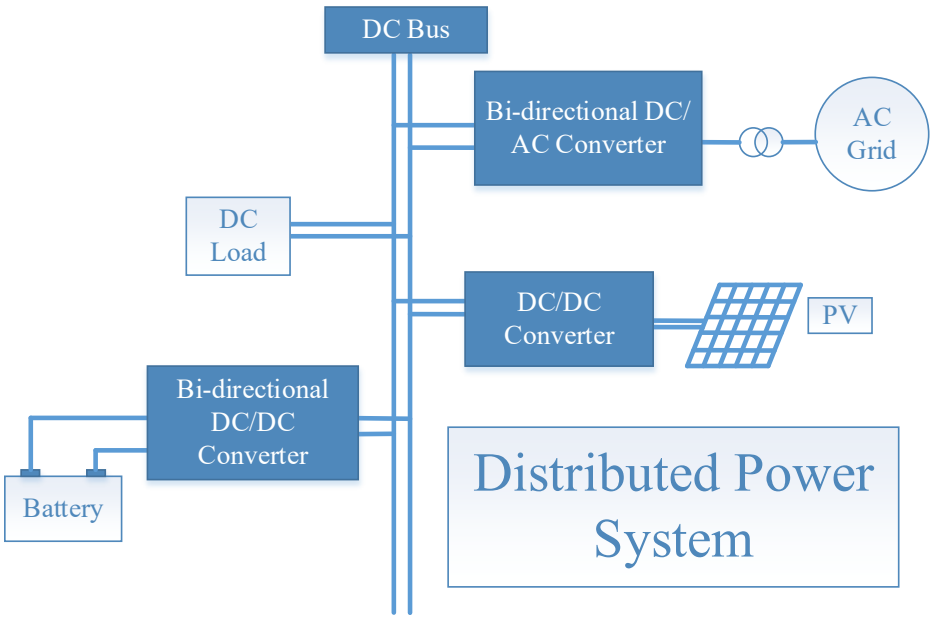


Figure 2.1. A typical example of a distributed power system (DPS) with DC bus.

EMI is an unwanted disturbance caused by electrical and electronic devices which carry rapidly changing electrical (voltage and/or current) signals. EMI caused by any kind of source can affect (obstruct, interrupt or degrade) the operation of electronic equipment working nearby. A typical example of a distributed power system (DPS) with a DC bus is shown in Fig. 2.1. This architecture greatly facilitates the integration of a number of DC

power sources and loads and so the system can have optimal operation. In such a DPS, since the various sources and loads are often connected in close proximity and each component can be regarded as an EMI source carrying voltage and current transitions, it is very important to minimize the interactions between the connected circuits. These can result from uncontrolled conducted or radiated EMI.

As more power electronic converters are being integrated and adopted in our daily lives, the emissions generated by any sort of source need to be kept under safe limits. This EMI consideration is not restricted to power converters, and various other issues have also been reported and researched. For example, the malfunctioning of an apnea monitor due to ambient EMI radiation [7]. A number of interesting and surprising issues have been reported in [8] including, military radios interfering with garage door openers, Russian satellite Geo-IK-2 possibly crashing due to external EMI and planes having inflight Wi-Fi facing more turbulence etc.

2.1.1. Types of EMI

EMI can be classified on the basis of the way in which the electromagnetic field (produced by high di/dt and dv/dt) propagates. It is classified as conducted EMI and radiated EMI. The possible coupling modes are shown in Fig. 2.2.

i. Conducted EMI:

With conducted EMI, the propagation occurs via the physical conductors. Empirically, the conducted EMI has a frequency range from 10 kHz to 30 MHz [9], and it is further classified as common-mode noise or differential-mode noise. These two sub-classifications are based on the direction of the propagation. In the case of common-mode noise, the

conduction occurs in the same direction through all the propagation paths. Common-mode (CM) noise always exists between the power line and the ground of a power electronic converter.

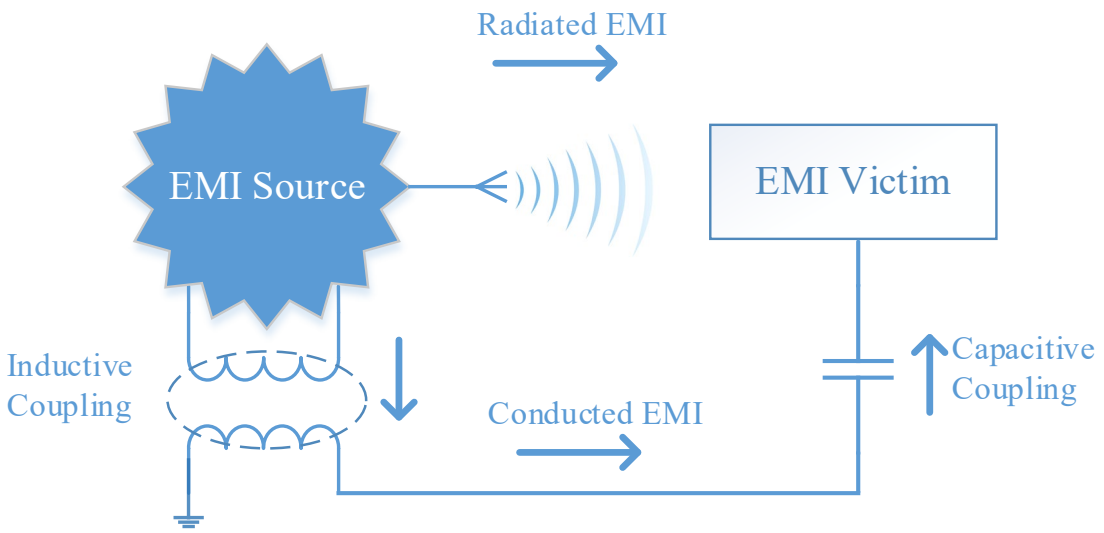


Figure 2.2. EMI coupling modes.

With differential-mode (DM) noise, the conduction is in different directions in two conduction lines. Differential-mode noise exists between the two power lines. The CM and DM noise are explained pictorially as follows:

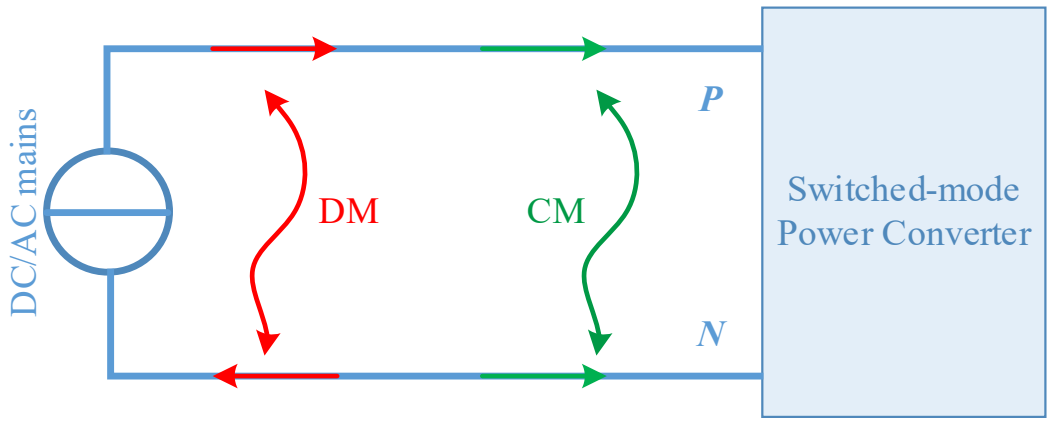


Figure 2.3. Types of conducted EMI.

ii. Radiated EMI:

Radiated EMI is propagated without physical conductors. Radiated EMI is usually significant for the cases when a power converter is switched at a high frequency (>30 MHz). This is the case when various parts of a PCB may radiate the EMI, acting as an antenna [10]. There can be several high-frequency current loops in a power converter which can lead to radiated emissions [11], [12]. These include the main switch power loop, the gate drive loop, the loop across inductive components (inductor, coupled-inductor or transformer), loops across the rectifier etc.

2.1.2. EMI in WBG-based Power Converters

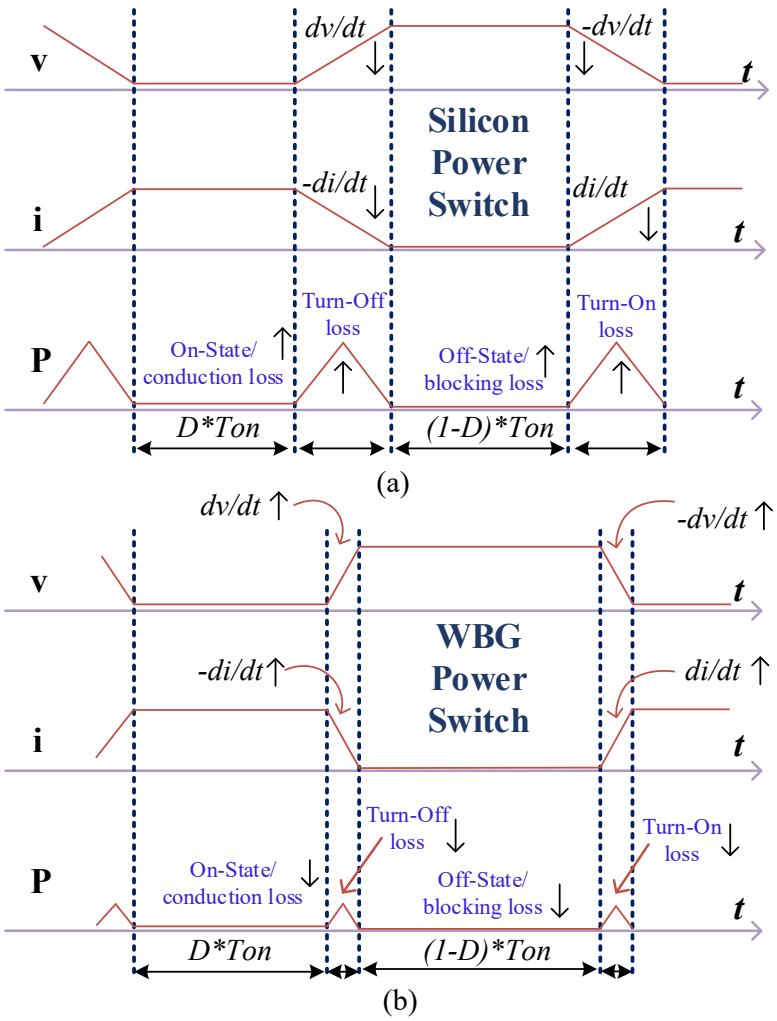


Figure 2.4. Comparative overview of switching transients between a) Silicon and b) wide-bandgap switching devices.

WBG power semiconductor devices, as compared to their silicon-based counterparts, with relatively low $R_{DS(on)}$ and high reverse blocking capabilities, offer high-switching-frequency operation along with sharp switching transitions (t_{ON} and t_{OFF}). These enable improved efficiency, lower conduction and switching losses, higher power density and small-sized passive filters. On the other hand, the sharp switching transients, though they reduce the switching losses, have larger di/dt and dv/dt as compared to ordinary silicon-based switches. Hence, the EMI issue becomes more severe in WBG-based power converters. Fig. 2.4 gives a pictorial view of how the switching transients are associated with the voltage and current alternations. A relative peak EMI behavior judgment can be made between a WBG-based power switch and a silicon power switch.

EMI is usually estimated with the power spectral density (PSD) of a signal (voltage and/or current) [13]. PSD gives the frequency distribution of the various constituent components of a signal. These components are also known as harmonics.

A Fourier-series expansion can be done to decompose a periodic signal into the sum of a set of sine and cosine functions. The general formula is given as:

$$f(t) = \frac{a_o}{2} + \sum_{m=1}^{\infty}(a_m \cos(m\omega t) + b_m \sin(m\omega t), \tag{2.1}$$

where

$$a_m = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t) * \cos(mwt)dt\,, m = 0, 1, 2, 3, \ldots \tag{2.2}$$

$$b_m = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t) * \sin(mwt)dt\,, m = 0, 1, 2, 3, \ldots \tag{2.3}$$

$\frac{a_o}{2}$ is the DC component and, other than this, the expression is a summation of sinusoidal functions. It is well known from the theory of Fourier analysis that, the more sinusoids are added up, the more exactly would their combination will add up to the original signal. In

the frequency domain, these sinusoids can be regarded as the harmonics. This implies that the more a signal has steep edges, the more broad its frequency band would be. Applying this concept to WBG-based power converters, the WBG switches make the voltage and current waveforms have steeper transitions, and hence a broadband spectrum is generated when high-speed WBG switches are used in a power converter. Moreover, as the switching frequency can be increased in WBG-based power converters, the spectral contents of the noise are also shifted to higher frequencies. Also, the noise magnitude depends on various additional factors such as operating power, the topology and type of applications etc. [4], [5].

2.1.3. EMI Measurement Methods

The EMC standards provide a set of attributes for the testing setup which may be difficult to replicate in a laboratory scale, therefore pre-compliance EMI testing is done for a product before it is sent for actual compliance testing. Since more than 50% of products fail EMC testing at the first time, the pre-compliance practice solves the hassle of re-sending a product for compliance testing and also saves money [14]. Depending on the EMI mode, i.e. conducted or radiated, various measurement procedures are followed. These are briefly described below:

2.1.3.1. Line Impedance Stabilization Network (LISN)

A LISN device and its basic functionality are shown in Fig. 2.5. It is basically a coupling device to measure the conducted EMI present on the supply lines of a power converter. LISN is typically a low-pass filter inserted into the supply line of the equipment under test

(EUT) and hence the conducted noise present at the terminals of the EUT can be displayed and analyzed on a spectrum analyzer [15].

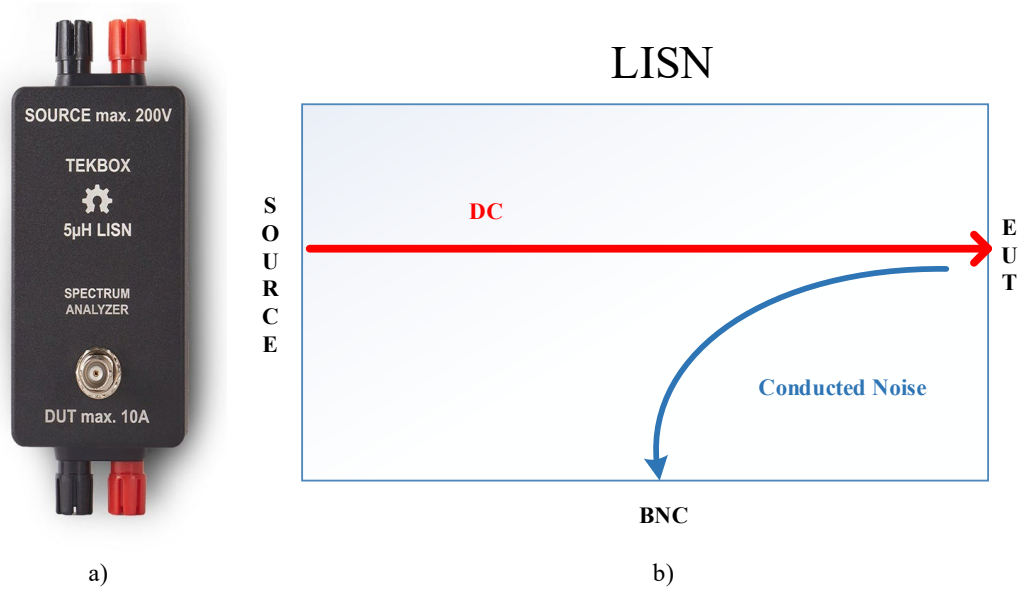


Figure 2.5. a) A LISN and b) its functionality [15].

A BNC connector output can be coupled to a spectrum analyzer with an appropriate attenuator (if required) to ensure safe operation of the spectrum analyzer. A typical setup for a conducted EMI measurement using a LISN as per the CISPR-25 standard is shown in Appendix A.1.

2.1.3.2. Transverse ElectroMagnetic (TEM)

An anechoic chamber is ideally used to analyze the radiated emissions of an EUT, and the standard compliance setup requires space, time, state-of-the-art equipment and similar resources. For this reason TEM cells are introduced to do the pre-compliance testing. A TEM cell is a stripline device which analyzes the radiated emissions of a EUT. It is not an ideal replacement for an anechoic chamber but, considering its feasible operation and comparatively low price, a TEM cell can be conveniently used to measure the radiated emission of a EUT for the pre-compliance testing. A setup for the radiated emission analysis

is shown in Appendix A.2, where the EUT is placed inside a TEM cell, one of whose two ports is connected to a 50 Ω termination. The other port is then coupled to the spectrum analyzer to analyze the radiated emissions. The EUT placement directions and a look-up table are provided by the manufacturer of a TEM cell; this gives an idea about the potential success or failure of compliance testing [16].

2.1.3.3. Close Field Probes

Close field probes are also known as near field probes, and are specifically used for locating the origin of a source of noise emissions. For this reason, sometimes these probes are also called "sniffing" probes. These probes are offered by various manufacturers and are available in various frequency ranges. Since the electromagnetic field is the combination of an electric field (E-field) and a magnetic field (H-field), which are produced by voltage and current, respectively. Thus the close field probes are classified as E-field probes and H-field probes.

Typical sources of H-field emissions are power or signal cables, chipset pins, PCB traces or improperly grounded metal enclosures, therefore, H-field probes work on the principle of an inductively coupled coil which becomes energized when it arrives in the vicinity of the H-field. On the other hand, E-field emissions are based on high-impedance logic, example of which are unterminated cables and wires etc. The E-field probe is basically a small antenna [17].

In brief, close field probes are a handy tool used for locating EMI sources in a device under test (DUT) or EUT. The probe can be moved around and aligned across different parts of a PCB to ensure that the EMI source is well located and can be shielded. Moreover,

these probes can be used in the opposite manner, i.e. utilizing these probes as a signal source to localize a section of a DUT or EUT susceptible to various types of signals. Such a testing setup is shown in Appendix A.3.

2.1.4. EMC Standards

All the above-mentioned EMI measurement/observing techniques help to detect, locate and measure the EMI noise of an EUT or DUT. The EMI can be suppressed/handled according to various EMC standards. According to the International Electrotechnical Commission (IEC), EMC is defined as "The ability of an apparatus or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment" [18]. In other words, an apparatus shall have enough "robustness" to work in an electromagnetic environment and keep its own emissions under the threshold limits as defined by various EMC standards.

With the widespread incorporation of power electronics worldwide, the relative EMI noise levels have increased to harmful levels. International standardization communities have agreed on various EMC standards which regulate/restrict the noise levels to continue the smooth operation of various equipment. In Europe, the organization designated to look after the EMC standards is the International Special Committee on Radio Interference, or CISPR. In the USA, it is the Federal Communications Commission (FCC), while in Australia the relevant organization is the Australian Communications and Media Authority (ACMA). Principally, EMC standards have the same goal, i.e. to ensure that a product complies with the defined noise levels. Eventually, there are different standards and requirements for different products, and these standards also vary in accordance with the geographical area like Australia, USA, Europe and Japan, etc. This also means that the

manufacturers of various products which are specifically designed to be exported to other regions have to pass the relevant EMC compliance tests to get approval from its importing country/region. Further information regarding noise threshold levels for various applications are reported in [19]–[21]. Several EMC standards are offered by the standardization organizations and are used in the industry based on type of applications, and for this reason some of these standards are briefly described as follows:

- **FCC Class A and Class B:** FCC divided digital electronic equipment into commercial and personal categories which are categorized as classes A and B, respectively. Of course, class B has relatively stricter limits for conducted and radiated EMI because such equipment (computers, calculators etc.) is more likely to be used in close proximity to other electronic devices.

- **CISPR 22:** Similar to FCC, CISPR 22 provides separate limits for class A and class B equipment. However, CISPR provides more detailed limits/classifications, e.g. further division to frequency ranges, specifying the detection mode such as 'quasi-peak' and 'peak'. Generally, the threshold levels offered by CISPR 22 are within a few dB of the FCC-specified limits (though for CISPR, the units are in $dB\mu V$ and μV for FCC, but appropriate conversion can be done). Using either of these will not compromise the accuracy of the measurement and EMC endorsement.

- **CISPR 16:** A series of 16 publications covering several appliances and apparatus, which specify the equipment and methods for measuring disturbances and also defining the immunity thresholds for frequencies > 9 kHz up to the GHz range.

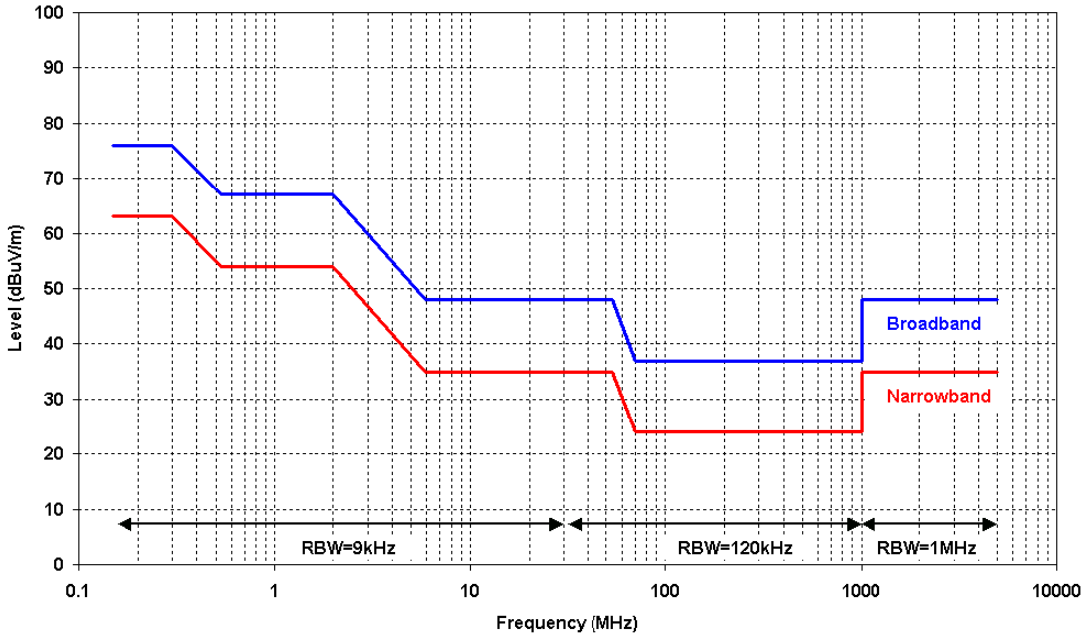


Figure 2.6. Generic limits based on CISPR-25 [22].

- **CISPR 25:** This has been designed to assure good performance for applications, for instance boats or vehicles, and provides limits for both conducted and radiated emissions. The procedures for measuring disturbances and limits ranging from 150 kHz to 1000 MHz frequency range are defined. An illustration of the threshold limits in shown in Fig. 2.6 [22].

- **CISPR 32:2015:** This is comparatively relevant and newer EMC standard. This standard covers a frequency range of 9 kHz to 400 GHz and it specifies the noise levels for the multimedia equipment which are powered by an AC or DC power supply up to 600 V (r.m.s or DC respectively) [23].

2.2. An Overview of EMI Suppression Techniques

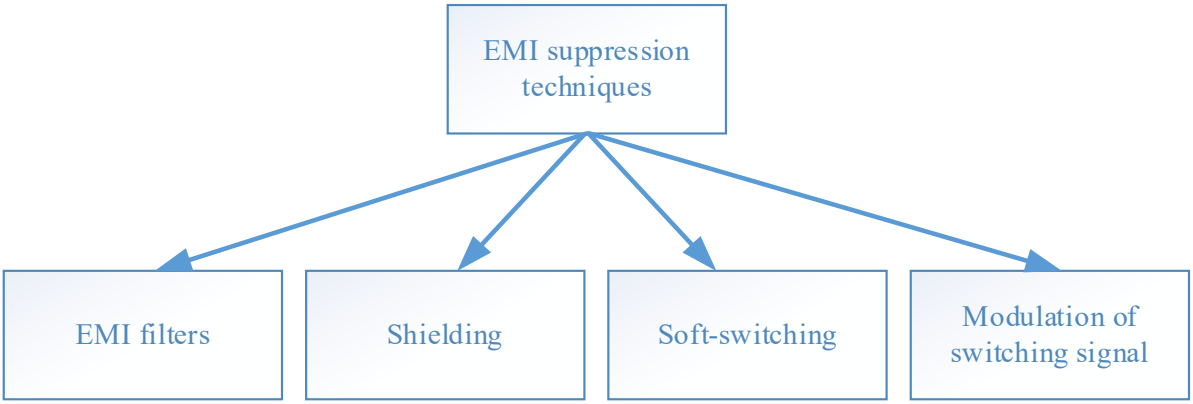


Figure 2.7. A broad classification of EMI suppression techniques.

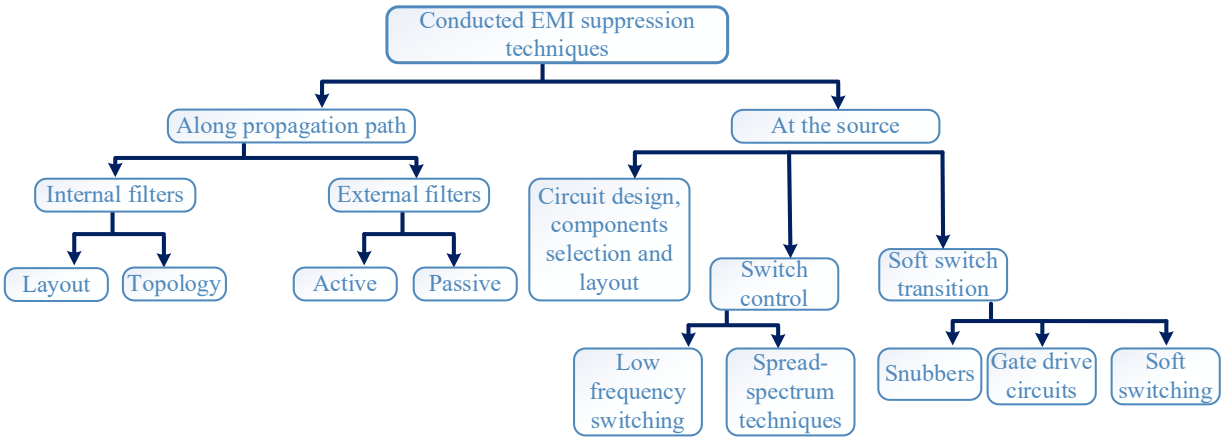


Figure 2.8. A classification of Conducted EMI suppression techniques.

A number of EMI mitigation techniques have been developed in order to keep EMI noise emissions (conducted and radiated) under the specified limits suggested by the EMC standards. These EMI techniques can be broadly classified into four categories, shown in Fig. 2.7 and explained later. Since this dissertation is focused on conducted EMI mitigation techniques, Fig. 2.8 gives a more detailed classification of conducted EMI mitigation techniques [24].

2.2.1. EMI Filters

Traditionally, a combination of passive electronic devices is used to suppress the conducted EMI of a power converter. Principally, an EMI filter is designed as a low-pass filter to impede the high-frequency noise, shorting it to ground [13]. Some insights into the design guidelines for EMI filters are reported in [25]–[27]. Although EMI filters are helpful to attenuate conducted EMI under the standardized thresholds, there are some major drawbacks that cannot be overlooked. The size and volume become a major concern in the case of portable products. As well, the narrow frequency range of filter limits the applicability of this solution. Various active/hybrid EMI filters have also been reported to partially overcome the limitations of passive EMI filters and to further suppress the EMI at lower component count but additional control complexity and limited frequency range [28], [29].

2.2.2. Electromagnetic Shielding

Electromagnetic shielding is one of the most effective, but expensive solution which keeps the noise emissions inside an enclosed chamber. Traditionally, metallic materials such as steel, aluminum and copper were shaped to enclose the EMI source but, since these materials are rigid, various flexible materials are used such as metal wires, foams and screens. More recently, particle-filled silicones [28] are used flexibly as an effective EMI shielding material. The conductive shield acts as a barrier to block the electromagnetic fields into “outer space”. Nevertheless, EMI shielding is an expensive solution and discouraged especially for portable products. Additionally, various leakages may occur at intakes, outlets and displays, etc., which undermine the performance.

2.2.3. Soft Switching

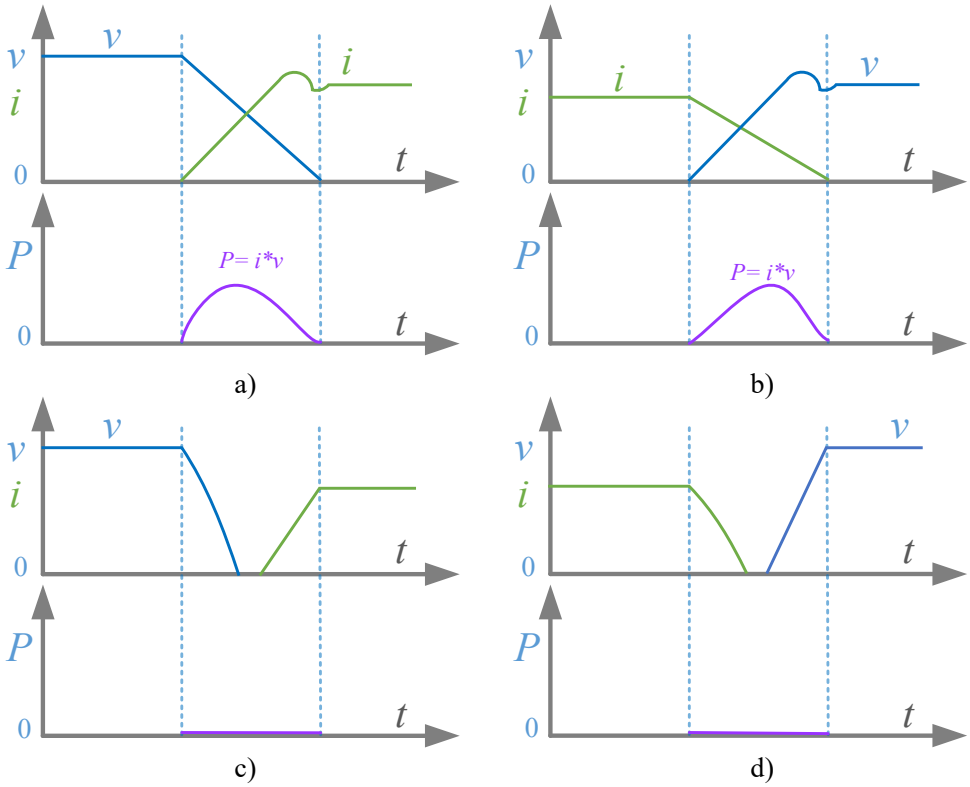


Figure 2.9. The switching process for hard switching (a and b), and soft switching (c and d).

The realization of high switching frequency operation of power converters enables to achieve many advantages such as compactness, easy filtering requirements and better waveforms. On the other hand, it adds to switching power losses and increased EMI due to the steeper edges offered by the power semiconductor devices. Soft-switching [30]–[32] is an indispensable solution for improving efficiency in power converters switched at high frequency. Primarily, zero-voltage and zero-current switching (ZVS and ZCS) are used to minimize the switching losses as shown in Fig. 2.9.

Soft-switched power converters have superior efficiency and EMI performance as compared to their hard-switched operation [33]. As hard-switched converters face higher dv/dt and di/dt, the EMI scenario becomes more crucial for the case of WBG-based hard-

switched power converters. Unlike this, soft-switching may require auxiliary circuitry and may add to complicating the control aspect.

2.2.4. Modulation of Switching Signal(s)

The modulation of one or more parameters of the switching signal(s) to spread the spectrum of the switching harmonics over a wide range of frequencies has been extensively researched, classified and reported with respect to different applications and implementations [5], [9], [13], [24], [34]–[36]. The foundation of this dissertation is based on achieving EMI suppression through the modulation of switching signals. A detailed relevant discussion is presented in more detail below:

2.2.4.1. The Switching Function

In a practical power converter, the required voltage and current are achieved using power switches. Ideally, these power switches have only two states, ON and OFF. This switching sequence/operation can be associated with binary function '$q(t)$' which is defined as follows:

$$q(t) = \begin{cases} 1, & when\ the\ switch\ is\ "on", \\ 0, & when\ the\ switch\ is\ "off" \end{cases} \tag{2.4}$$

$q(t)$ is defined for all values of time, and there are two discrete values associated with it. Therefore, $q(t)$ can also be called the switching function.

An example of a classic buck converter has been chosen to explore the switching function in more detail. It is noted that the basic operation a buck converter is controlled by the switching function $q(t)$, i.e. when $q(t) = 1$, the output voltage before the filter (u) is clamped to v_{in} and when $q(t) = 0$, 'u' may be equal to 'e' or 'u' depending on the current

conduction mode of the filter inductor. Moreover, the duty ratio comes into consideration which also has an impact on the value of the output voltage. The duty ratio may be defined as follows:

$$d = \frac{1}{T}\int_{t_o}^{t_o+Ts} q(t)dt \tag{2.5}$$

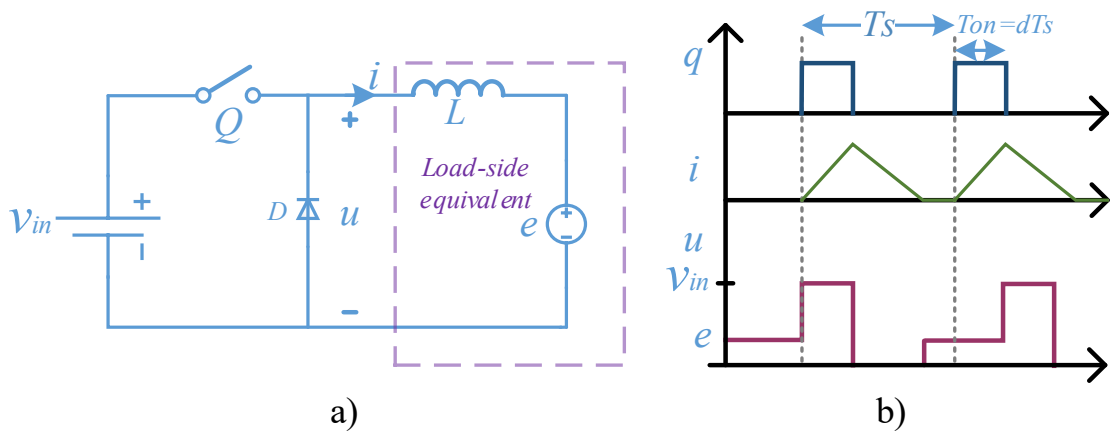


Figure 2.10. A classic buck converter and its associated waveforms.

In case of dc-dc converters, the duty cycle (d) and hence the output voltage is constant in steady-state operation. However, in case of dc-ac inverters, the duty cycle(s) varies periodically to synthesize the alternating output voltage. Furthermore, it can be noted that essentially, the voltage and current transitions are directed by the switching function $q(t)$. Yet in fact, many more parameters are involved in impacting on the way in which the voltage and current transitions (dv/dt and di/dt) occur. Such parameters are numerous and not limited to the conduction mode of the inductor ($CCM\ or\ DCM$), the parasitics of the PCB, the operating switching frequency, the power converter topology etc.

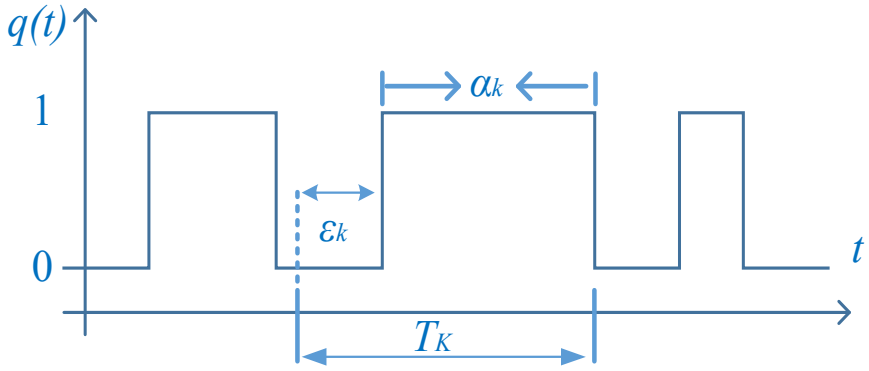


Figure 2.11. A generic switching signal used to drive the switches of a power converter.

Finally, since $q(t)$ is the fundamental driving force behind di/dt and dv/dt, spectral analysis of a variety of switching functions have been reported to analyze and predict the expected noise emissions of power electronic converters [3], [39]–[43].

In the following sub-sections, a broad classification of various modulation schemes is given. A discussion is presented so the reader can understand a variety of perspectives which can help achieve EMI reduction in power converters. A general switching signal $q(t)$ for the driving of the power switch(es) in a power converter is shown in Fig. 2.11. Such a signal consists of one pulse per switching cycle, each of which is defined by three parameters: ε_k is the delay from the start of the kth switching cycle to the switch turn-on time, α_k is the pulse duration in the kth switching cycle, and T_K is the total duration of the kth switching cycle [44]. In terms of these parameters the duty ratio of the kth switching cycle may be defined as $D_k = \frac{\alpha_k}{T_k}$.

Table 2.1. Classification of various Spread-spectrum modulation methods

Modulation Style	**Scheme**	**Sub-classification**	**Pulse modulation parameters**			**Duty ratio (α_K/T_K)**	**References**
			Switching cycle duration (T_K)	**Pulse width (α_K)**	**Pulse position (ε_K)**		
Periodic OR Aperiodic (pseudo-random, chaotic, determin-istic) OR Random*	PWM	--	Fixed	Variable	Fixed	Variable	Basic
	PPM	--	Fixed	Fixed	Variable	Fixed	[37]
	DRM + PPM + fixed carrier frequency	--	Fixed	Variable	Variable	Variable	Presented work, [36]*
	CFM	CFM with fixed duty cycle	Variable	Synchro-nized	Fixed	Fixed	[36], [38]*
		CFM with varying duty cycle	Variable	Fixed or Variable (not synched)	Fixed	Variable	[34], [36]*
	CFM + PPM + fixed duty ratio	--	Variable	Variable (synched)	Variable	Fixed (synched)	[36]*
	CFM + PPM + DRM	--	Variable	Variable	Variable	Variable	[36]*

PWM = Pulse Width Modulation, PPM = Pulse Position Modulation, DRM = Duty Ratio Modulation, CFM = Carrier Frequency Modulation

*All the techniques reported in [36] assumed random modulation of the pulse parameters.

Based on variation of the aforementioned parameters, many spread-spectrum pulse modulation techniques may be defined, as summarized in Table 2.1. The technique of spreading of harmonics through the modulation of one or more of the above-mentioned signal parameters is readily applied to single-switch converter topologies. However, there are very few reports concerning their application in converters with multiple switches, as the coordination of multiple switching signals can be difficult, especially if the switching cycle duration varies. The modulation of different parameters of the switching signal $q(t)$

also adds up to the suppression of EMI as well as the complexity of the implementation of such modulation schemes. The modulation styles can be sub-classified into periodic, aperiodic and random. These are explained below:

2.2.4.2. Periodic Modulation

The periodic modulation of one or more parameters of the switching signal $q(t)$ is classified as periodic modulation [45], [46]. A comparison of the frequency-domain spectrum for an unmodulated and a frequency-modulated signal is depicted in Fig. 2.12. Clearly, the spectrum envelope shows a reduction in the peaks, which is the basis of EMI suppression.

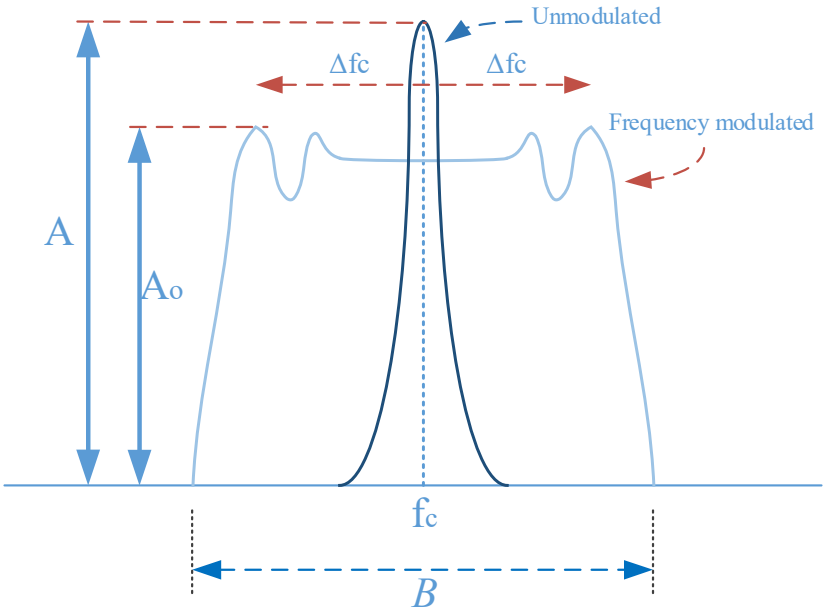


Figure 2.12. Spectrum of an unmodulated signal compared with a frequency-modulated sinusoidal signal [45].

It can be noted that the initial energy of the harmonic is spread and thus produces a wider spectrum of frequencies, 'B', with lower amplitudes. While Fig. 2.12 illustrates the spreading phenomenon of a single harmonic, in fact each individual harmonic is spread into a certain frequency band. Mathematically, a frequency-modulated signal may be represented as:

$$F(t) = A.\cos[2\pi f_c t + \theta(t)], \tag{2.6}$$

where A is the amplitude of the original (unmodulated signal) and f_c is the unmodulated carrier frequency. Moreover, $\theta(t)$ is the phase angle defined as

$$\theta(t) = \int_0^t k_w . v_m(\tau) d\tau, \tag{2.7}$$

where $v_m(\tau)$ can be regarded as a periodic function of frequency f_m and k_w is a factor designated to control the peak-frequency deviation. This gives a further insight into two more parameters, namely the 'modulation index', defined as $m_f = \frac{\Delta f_c}{f_m}$ and 'rate of modulation'$= \frac{\Delta f_c}{f_c}$, where Δf_c is the peak-frequency deviation and f_m defines the frequency of modulation. Different modulation styles can be produced [47], in this case a periodic frequency modulation is considered. Nevertheless the following conclusions can be made:

1. The energy of each fundamental component is spread into a wide band 'B', given as:

$$B = 2. f_m . \left(1 + m_f\right) = 2. (\Delta f_c + f_m). \tag{2.8}$$

2. The bandwidth (B_h) will eventually increase with an increase in the number of harmonic order (h) as per $B_h = 2. f_m . (1 + m_f h)$. In other words, at higher harmonic order, the spread harmonics might overlap and end up increasing the peak envelope. This is pictorially explained in Fig. 2.13.

3. Increasing Δf_c leads to an increase in spreading and subsequently suppression of spectral peaks, but on the other hand the fundamental operations (voltage gain, efficiency, current/voltage ripple etc.) of a power converter might be affected. There is always a trade-off in the amount of frequency deviation (leading to harmonic suppression) and the robustness of a power converter.

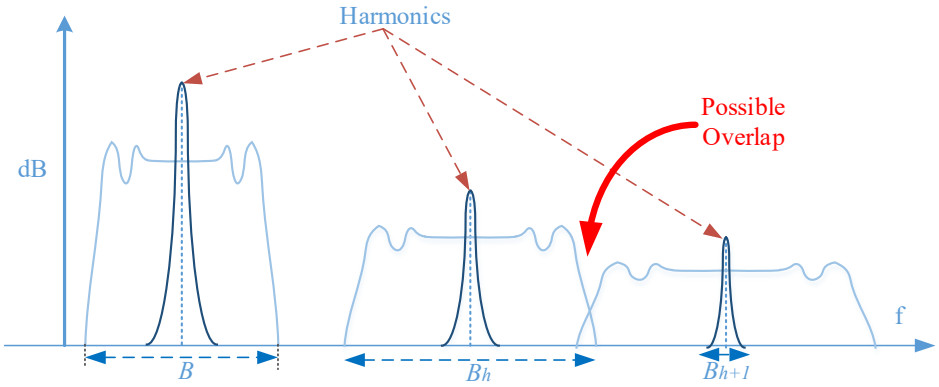


Figure 2.13. Spreading of harmonics leading to overlap.

Generally, this idea correlates with the frequency-modulation concept in telecommunications, in which two sidebands are generated when a signal is frequency modulated. This is also the reason for denoting the modulation techniques as spread-spectrum techniques which is a core concept in communications [48].

2.2.4.3. Aperiodic (Pseudo-random, Chaotic or Deterministic) Modulation

The term "aperiodic" refers to the opposite of periodic. Pseudo-random signals can be referred to as aperiodic signals. Though pseudo-random signals have a mathematical basis, they are not purely random and so cannot be categorized as periodic signals [44]. Another type of aperiodic signals are the "chaotic" signals. These signals carry the properties of a random signal, but since these signals have a mathematical basis, they cannot be categorized as random, so chaotic signals are categorized as aperiodic [9]. Chaotic signals can be implemented by both by analog and digital methods. A chaotic carrier generator or Chua's oscillator is reported in [49], [50] which can be utilized to implement chaotic characteristics in a signal. Nevertheless, chaotic signals are aperiodic in nature and strongly depend on the initial conditions, which makes long-term predictions of chaotic signals impossible, despite their deterministic nature [51]. Considering chaotic modulation from the prospect of the

operation of power converters, the control complexities increase due to the lack of any 'prediction' factor. Moreover, numerous parameters are to be considered for the practical implementation of the chaotic-based modulation [52]. Nevertheless, there is a need to come up with an aperiodic modulation methodology which is easy to implement via both analog and digital techniques in addition to owning the deterministic nature.

2.2.4.4. Random Modulation

Random modulation can be regarded as the superset of deterministic modulation and there can be numerous ways to implement randomness, i.e. there is no end to the ingenuity of the approaches by which 'randomness' can be achieved [42] . Random modulation refers to the technique of randomly modulating one or more parameters of the switching signal $q(t)$. There are various complications which are related with the usage of random signals to implement random modulation. Firstly, strictly speaking, an actual or purely random signal is difficult to generate and secondly, the parameter design and estimation of various other parameters becomes difficult when using random modulation [13]. For example, the duty ratio of a power converter is usually associated with the output voltage generated. If random modulation is implemented, it may cause complexities in terms of filter design, control loop characteristics and parameter design of the power converter etc.

Finally, an appropriate modulation style would have the properties of being "random" in addition to controllability. In this way there would be more choice of design parameters, implementation of a control loop and filter design in a power converter.

Table 2.2 highlights the similarities and difference between periodic, aperiodic and random signals. The focus of this thesis is on aperiodic pulse width modulation methods.

Table 2.2. Comparison of periodic, aperiodic and random signals

Modulation Style	**Controllability of parameters**	**Digital/Analog Implementation**	**Repetition ***	**Mathematical expression**	**Deterministic description (TD)**
Periodic	Yes	Yes	Yes	Yes	Yes
Quasi-periodic	Yes	Yes	No	Yes	Yes
Aperiodic	**Yes**	**Yes**	**No**	**Yes**	**Yes**
Chaotic	Yes	Yes	No	Yes	No
Random	No	No	No	Yes (FD only)	No

* Repeat in each switching cycle, FD= Frequency domain, TD= Time domain

2.3. Chapter Summary

This chapter provides preliminary information for obtaining insight into EMI produced by power converters. EMI behavior, being a natural phenomenon associated with power converters, can sometimes be difficult to predict accurately due to the number of noise sources (di/dt and dv/dt) present at various localities of a power converter. Active components such as power switches and diodes are the main noise sources which develop the voltage and current transitions. Nevertheless, a number of factors are also associated and cannot be overlooked. These include parasitic ringing voltages and currents, the power converter topology, modulation scheme, PCB design, load power and voltage/current values. Furthermore, not only is fairly accurate model needed to predict accurate ringing behavior, overshoots and rising/falling transients, but also an equivalent electrical circuit of the PCB is also needed. As this thesis is inclined to comment on the impact of modulation schemes to reduce the EMI in power converters, a basic discussion on spectral analysis of the modulated and unmodulated pulses is given in the next chapter. Furthermore, the proposed modulation strategy is applied to a single-switched power converter and the relevant results are discussed.

Chapter 3

EMI Suppression for a High-Frequency GaN-based SEPIC Converter

In this chapter, a high-frequency GaN-based SEPIC converter is presented and an aperiodic modulation is applied to analyze the EMI suppression behavior. The methodology to implement the aperiodic modulation is simple and implementable via both analog and digital techniques. The small rise and fall times (in the order of nanoseconds), offered by the GaN switch allow sharper voltage and current transitions (dv/dt and di/dt respectively), so a broadband EMI emissions can be expected. It is interesting to note that the WBG devices such as GaN and SiC on one hand help to attain low weight, high efficiency and better thermal stability. However, on the other hand, these devices have the potential to produce higher EMI levels [4], [44]. Therefore GaN power switches are used in the hardware prototype.

Firstly, the procedure to generate an aperiodic carrier signal is introduced which is further utilized to generate an aperiodically modulated pulse-position switching signal. This PPM signal is used to drive the GaN switch in a SEPIC converter. An introduction to the SEPIC converter is given in relation to the related applications, and the motivation to choose various parameters. Moreover, the design steps for the high-frequency layout of the PCB are presented and include high-frequency design insights. To support the proposed modulation, various experimental results such as voltage gain and efficiency vs load index of the SEPIC converter are presented along with EMI suppression outcomes.

3.1 Aperiodic Switching Function

A simple methodology for generating an aperiodic version of the switching signal $q(t)$ is presented in this section. The proposed methodology is believed to be generically adopted for the generation of aperiodic switching signals to realize the essential operation of power converters along with the achievement of EMI reduction. Specifically, in this chapter, the application is focused on a single-switched power converter, and a SEPIC converter is built and tested as a prototype.

3.1.1 Framework for the Implementation of an Aperiodic Switching Signal

A switching signal is usually realized by comparing a modulation signal and a carrier signal. The carrier signal can be a train of sawtooth or triangular pulses, which define the switching frequency of $q(t)$. There are numerous methods by which the aperiodic switching function can be generated, but in the proposed methodology an aperiodic carrier is generated using two anharmonically-related periodic signals, a sawtooth pulse train and a sinusoid

with a dc offset. The proposed aperiodic carrier generation methodology is shown pictorially in Fig. 3.1.

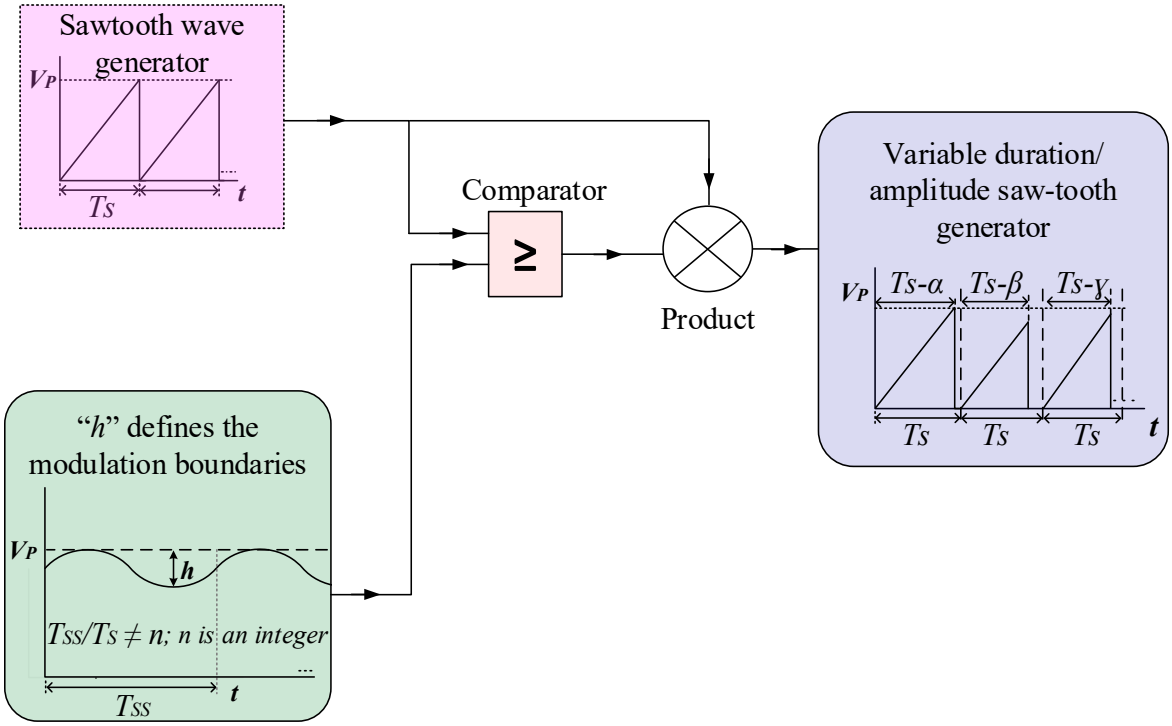


Figure 3.1. Scheme showing generation of the aperiodic carrier signal.

As shown, a sawtooth signal simply goes through a comparator and a multiplier block to generate a sawtooth carrier in which each consecutive ramp linearly varies aperiodically in amplitude and duration, whilst the switching cycle is kept constant [53]. The frequencies of the sawtooth signal and of the sinusoidal signal (with offset) are not integral multiples of each other, and this adds to the aperiodicity. The case of 'T_S' and 'T_{SS}' being an integral multiple been discussed in [54] and is called as quasi-periodic modulation. It offers less suppression when compared to aperiodic modulation [55].

This aperiodic signal, when compared with a dc constant, generates an aperiodic switching function, whose pulse position varies aperiodically. The amount of variation of the pulse position can be controlled by the peak-peak amplitude 'h' of the sinusoid, whereas,

'α', 'β' and 'γ' are used to pictorially represent that the width and height of the ramp signal varies for each cycle.

The spread-spectrum techniques reported in the literature may have some implementation limitations, but it is noted in our proposed methodology that the aperiodic carrier signal can easily be implemented with both analog and digital techniques. Another important property associated with the proposed technique is that it is deterministic in nature from periodic signals. The benefit of the deterministic nature of the proposed aperiodic signal is further explored and applied to a quasi-Z-source DC-DC converter in Chapter 4.

3.1.2. Functional Analysis of the Proposed Methodology

Various studies associate probabilistic characteristics with the parameters of the switching function. Here, the theory of functional analysis is utilized to represent the proposed methodology.

Let the sawtooth train be represented by $s(t)$ and the sinusoidal signal with the offset by $c(t)$. where

$$s(t) = \begin{cases} t & t \geq 0 \\ 0 & t < 0 \end{cases}; \tag{3.1}$$

and,

$$c(t) = \sin(2\pi f t + \phi)\,; \tag{3.2}$$

where f is the frequency of the modulation signal $c(t)$ and ϕ is the phase angle. Therefore, the initial step (shown in Fig. 3.1) for comparing $s(t)$ with $c(t)$ can be represented as

$$x(t) = \mathbf{1}(P_r(c(t) > s(t))), \tag{3.3}$$

where $\mathbf{1}$ is the indicator function represented as:

$$\mathbf{1}(.)\begin{cases} 1 & (.)is\ true \\ 0 & elsewhere \end{cases}, \tag{3.4}$$

and P_r represents the probability function.

Furthermore, the sawtooth function $s(t)$ is multiplied by the new function $x(t)$ to generate an aperiodic version $y(t)$ of $x(t)$, written as follows:

$$y(t) = x(t) * s(t). \tag{3.5}$$

Finally, when this aperiodic version of $s(t)$ is compared with a dc constant c, the resulting switching function can be described in the following way:

$$z(t) = \mathbf{1}(P_r(y(t) > c). \tag{3.6}$$

3.1.3. Spectral Analysis of a Pulse-position Modulated Signal

Traditionally PPM finds its application in the field of communications systems. The example of pulse positon modulation (PPM) is discussed in this section to give an insight about its associated spectral characteristics, how the sidebands are spread resulting in the suppression of harmonic peaks, and to get an idea of how the 'relative' suppression of conducted EMI is associated with the peak pulse deviation (associated with 'h' in Fig. 3.1) of PPM when it is employed in a power converter. The comparison of a dc signal with the proposed aperiodic carrier signal allows implementation the PPM. The spectral analysis of PPM signals has been reported elsewhere [56]–[58].

To justify how PPM leads to peak EMI suppression, the frequency-domain analysis of two switching sequences (with and without PPM) is presented in Fig. 3.2 (a and b, respectively). The switching frequency for both PPM signals is kept at 1 MHz and the peak pulse deviation is kept at 4%. Based on the numerical analysis, implemented in MATLAB, it can be noticed that the PPM leads to the spreading of harmonics and hence the suppression of the peak EMI spectrum. It can also be noted that the number of harmonics increases with the modulation of one or more parameters, yet overall peaks of the harmonics are relatively reduced. This phenomenon is the basis of EMI suppression in power converters.

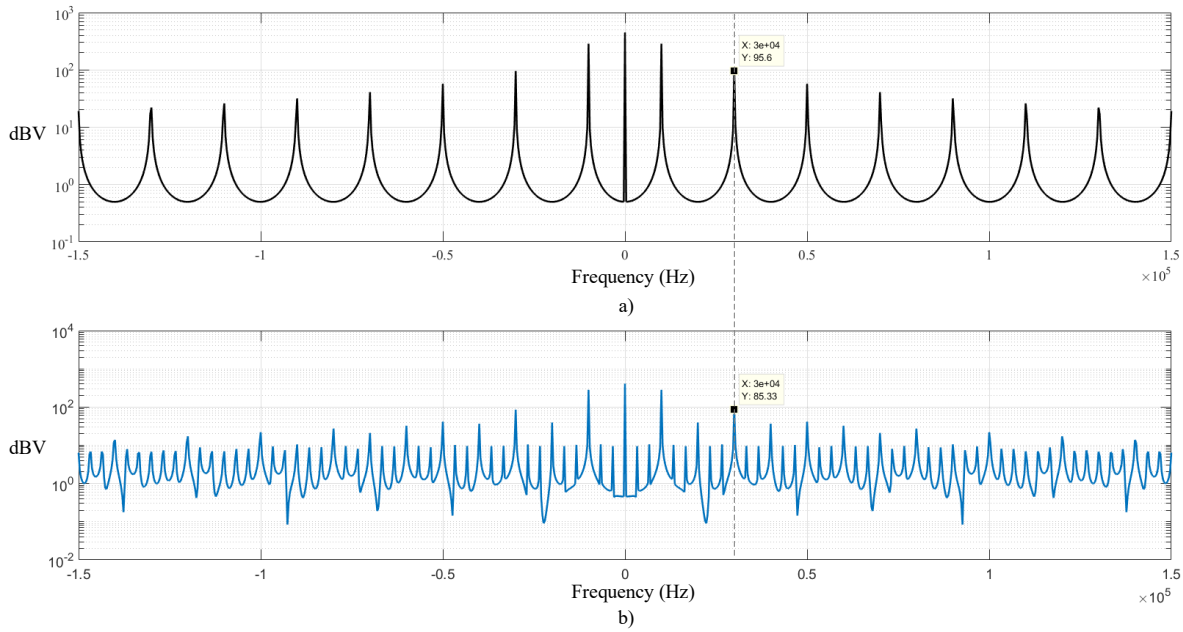


Figure 3.2. Frequency spectrum of a) simple $q(t)$ and b) aperiodic $q(t)$.

PPM with constant width has been discussed in [57], and its Fourier series is given by:

$$f(t) = \frac{A}{\pi}\left[\begin{array}{c} \omega_c h + \phi \sin\omega_m h \cos\omega_m t + \\ 2\sum_{n=-\infty}^{\infty}\sum_{k=1}^{\infty} J_n(k\Phi)\left(\frac{\sin(k\omega_c + n\omega_m)h}{k}\right)\cos(k\omega_c + n\omega_m)t \end{array}\right] \tag{3.7}$$

where,

A = Amplitude of the pulse,

h = width of the pulse,

ϕ = Maximum phase excursion = $2\pi h_d f_c$; h_d is the peak pulse deviation,

J_n = Bessel function of the first kind of order n,

ω_m = frequency of the modulation signal (sinusoidal signal with a dc offset),

ω_c = Carrier frequency, i.e the frequency of the sawtooth.

It can be noticed that the first term is simply a dc component of the unmodulated carrier signal, whereas the second term indicates the baseband components. Moreover, the third term is a continuum of harmonics which eventually fade away in the pattern of a Bessel function. The baseband component, defined as

$$\frac{A\phi}{\pi}\{(\sin\omega_m h)(\cos\omega_m t)\} \tag{3.8}$$

can be written in terms of the modulation index 'M' as

$$AM\sin\omega_m h\cos\omega_m h \tag{3.9}$$

Fig. 3.3 presents the energy associated with different harmonics for different values of M. It is clear that the spectral energy associated with the harmonics increases with increasing 'h', which eventually leads to the reduction of the spectral peaks along the frequency spectrum. It can also be observed that the baseband signal (which makes up a significant part of the spectrum) in the PPM is dependent on various parameters such as the modulation signal frequency, M and ϕ. Therefore, when the pulse position is not varied, i.e. 'h' is zero, then the spectrum of the baseband signal vanishes to the noise floor.

The aforementioned preliminary information is presented to contribute to an understanding of harmonic spreading, based on PPM as it is applied on a SEPIC converter, to analyze its EMI behavior, presented in the following subsections.

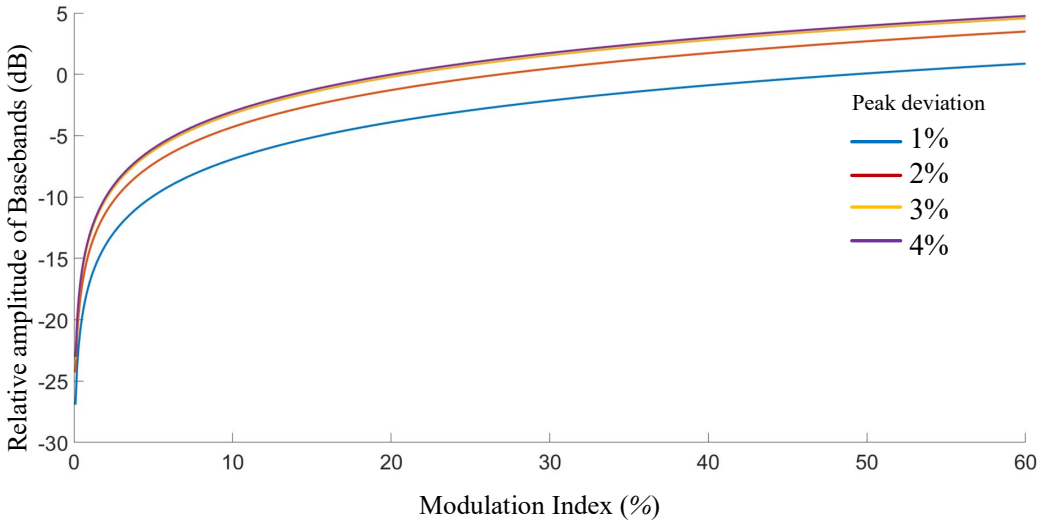


Figure 3.3. Relative amplitude of basebands vs modulation index (%).

3.2. Introduction to the GaN-based SEPIC Converter

With the focus on energy efficiency, the trend in using the light-emitting diodes (LED) for lighting can be seen. Although the LED lights are comparatively efficient, the cost of the light itself and its power supply (a power converter) are still a hindrance in its adoption. Therefore, there is a need to reduce the manufacturing cost of LEDs along with developing efficient, compact and cheaper power supplies. As a rule of thumb, the power density of a power converter is directly related to its switching frequency, which also leads to smaller passive components and reductions in weight. Moreover, a high switching frequency is being adopted throughout power electronic converters to achieve various advantages [59]. Of course this also enables a number of innovative streams, such as planar magnetics and resonance techniques, to achieve soft-switching, multi-layer PCB design and optimized PCB layouts for minimized parasitics etc.

A single-ended primary-inductor converter (SEPIC) is a well-known classic topology which can provide a buck-boost operation. In addition to the buck-boost operation, the SEPIC also offers a minimal component count. Often, a SEPIC converter is implemented with a coupled inductor, i.e. both of its constituent inductors are wound on a single core. This enables high power density, better integration, and a lower inductance requirement in comparison to two separate inductors. Nevertheless, the limited off-the-shelf coupled inductors may be challenging for power electronics designers [60].

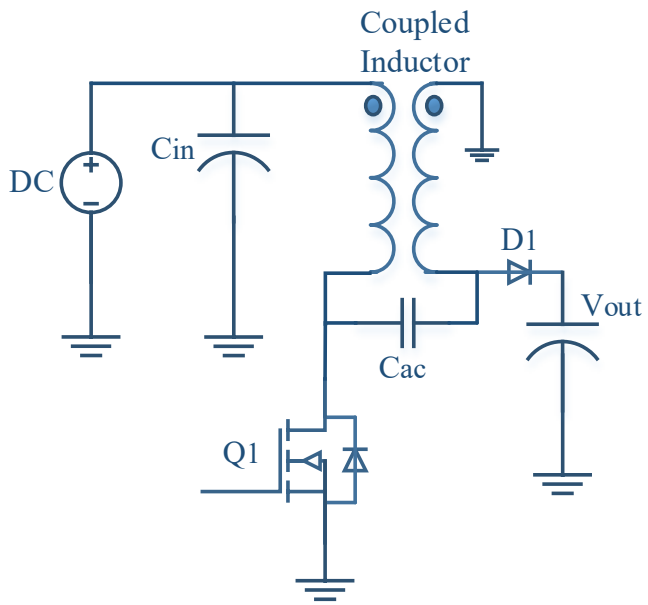


Figure 3.4. Coupled-Inductor-based SEPIC converter for LED driver application.

Considering the benefits of a coupled-inductor-based SEPIC converter to be used as an LED driver and its implementation with a GaN power switch, a prototype was built to observe its EMI behavior. A schematic diagram is shown in Fig. 3.4. The proposed aperiodic modulation approach was applied to demonstrate the suppression of the peak EMI with no impact on the normal operation of the SEPIC converter. The results such as voltage gain and efficiency are discussed in the following subsections.

3.3. Design Considerations

A coupled-inductor-based SEPIC converter was built and the proposed aperiodic modulation scheme was applied. There are major attributes associated with this design. Firstly, it is implemented with a GaN switch. An enhancement-mode GaN-on-silicon power transistor GS61008P by GaN Systems [61] was used as a power switch. This allows high-switching-frequency operation, low on-state resistance of 7 mΩ, voltage rating of 100 V and drain current of 90 A. The second major attribute of the prototype is that it was designed to be a hard-switched power converter. Despite the benefits of GaN able to be better achieved if the soft-switching is also realized in a power converter [62], the platform was built to analyze the EMI behavior (the basis of which is rapidly changing voltage and current transitions). For this reason a high-frequency hard-switched power converter prototype was built.

A pictorial comparison between a traditional silicon switch and a WBG switch such as GaN has already been depicted in Fig. 2.4. GaN-based power converters make an interesting setup to specifically analyze the EMI behavior, and hence apply the proposed EMI suppression technique.

3.3.1. Design Parameters

The SEPIC converter discussed in this chapter has been designed specifically for driving a 20 watts LED light. The parameters used for the prototype are listed in Table 3.1. These design steps are based on [63] to calculate the component parameters for a 20 watts rated prototype described as follows:

Table 3.1. Design Parameters for SEPIC converter

Parameter	**Value, Description**
Rated Power	20 watts
Input voltage (V_{in})	20 ~ 30 volts
Output voltage (V_o)	24 volts
Duty ratio (D_{SEPIC})	0.45 ~ 0.55
Coupled Inductor (CL)	Coilcraft, MSD7342-183ML
Switching frequency (f_{SW})	500 kHz ~ 1 MHz
Coupling Capacitor (C_{AC})	4 μF
Output capacitor (C_{out})	4.5 μF
Power switch	GS61008P, GaN Systems
Forward Diode	V30D60C

$$\text{Duty cycle} = D_{SEPIC} = \frac{V_o + V_d}{V_{in} + V_o + V_d} = 0.45 \sim 0.55, \tag{3.10}$$

where $\boldsymbol{V_d}$ is the forward diode voltage.

Allowed ripple across the inductor = ΔI_L

$$\Delta I_L = \frac{I_{in(max)}}{\eta} \text{ x } 30\% = \Delta I_L * I_{in}' * 30\% = 1.022 \text{ Amp}, \tag{3.11}$$

where $I_{in(max)}$ is the maximum input current required by the DC source and η is the efficiency of the SEPIC converter.

$$L_{1a} = L_{1b} = \frac{V_{in(min)} * D_{max}}{\Delta I_L * f_{sw\,(\min)}} = 16.28 \text{ μH} \tag{3.12}$$

where L_{1a} and L_{1b} are the inductance values of the coupled inductor and $f_{sw\,(\min)}$ is the minimum switching frequency.

$$I_{L1a(peak)} = I_{in}' + \frac{\Delta I_L}{2} = 1.3 \text{ amps} \tag{3.13}$$

where $I_{L1a(peak)}$ is the peak current flowing through the primary winding of the coupled inductor.

The output capacitance (C_{out}) value is calculated as

$$C_{out} \geq \frac{I_{out} * D_{max}}{\Delta V_{Ripple} * f_{sw\,(\min)}} = 4.5\ \mu\text{F}, \tag{3.14}$$

where ΔV_{Ripple} is the allowed output voltage ripple, set at 0.1 V.

3.3.2. High-Frequency PCB Design

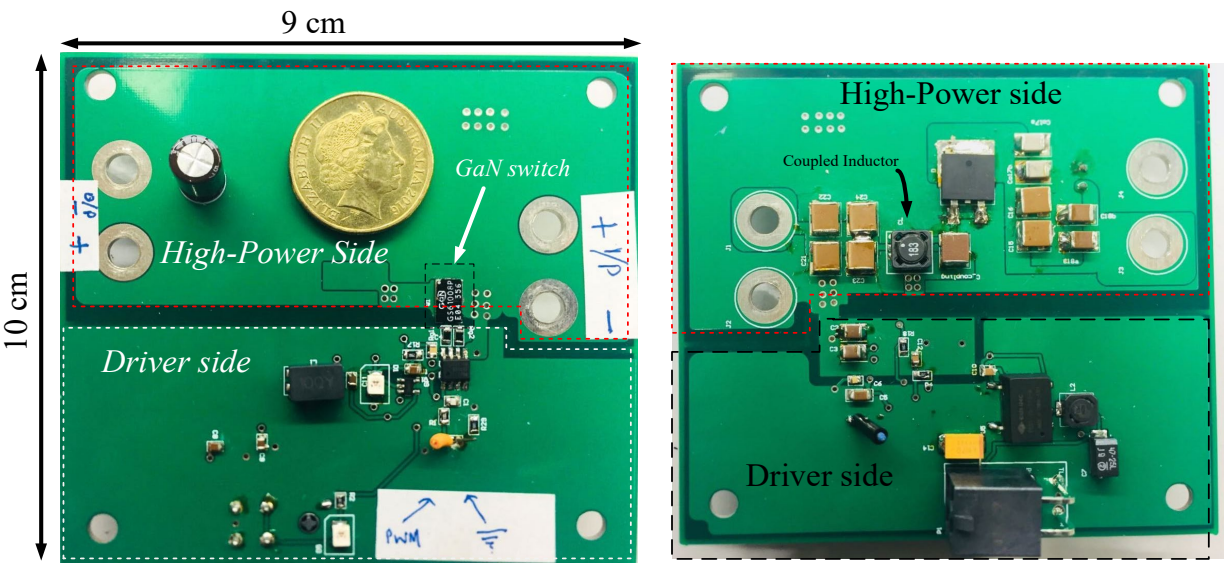


Figure 3.5. 4-layer PCB layout showing isolated driver and power circuitry.

High-frequency operation of power converters requires an optimal PCB layout to keep the parasitics minimal. Various studies have reported [64], [65] design insights which help to reduce the layout parasitics, especially for the GaN-based high-frequency operation of power converters. An optimized layout design for the PCB is presented to minimize the parasitic capacitors and inductive loops. A 9X10 cm^2, 4-layer PCB was designed for the SEPIC converter which has clearly isolated boundaries for the driving circuitry and the

power circuitry. Both sides of the PCB layout are shown in Fig. 3.5 and the boundaries are marked clearly.

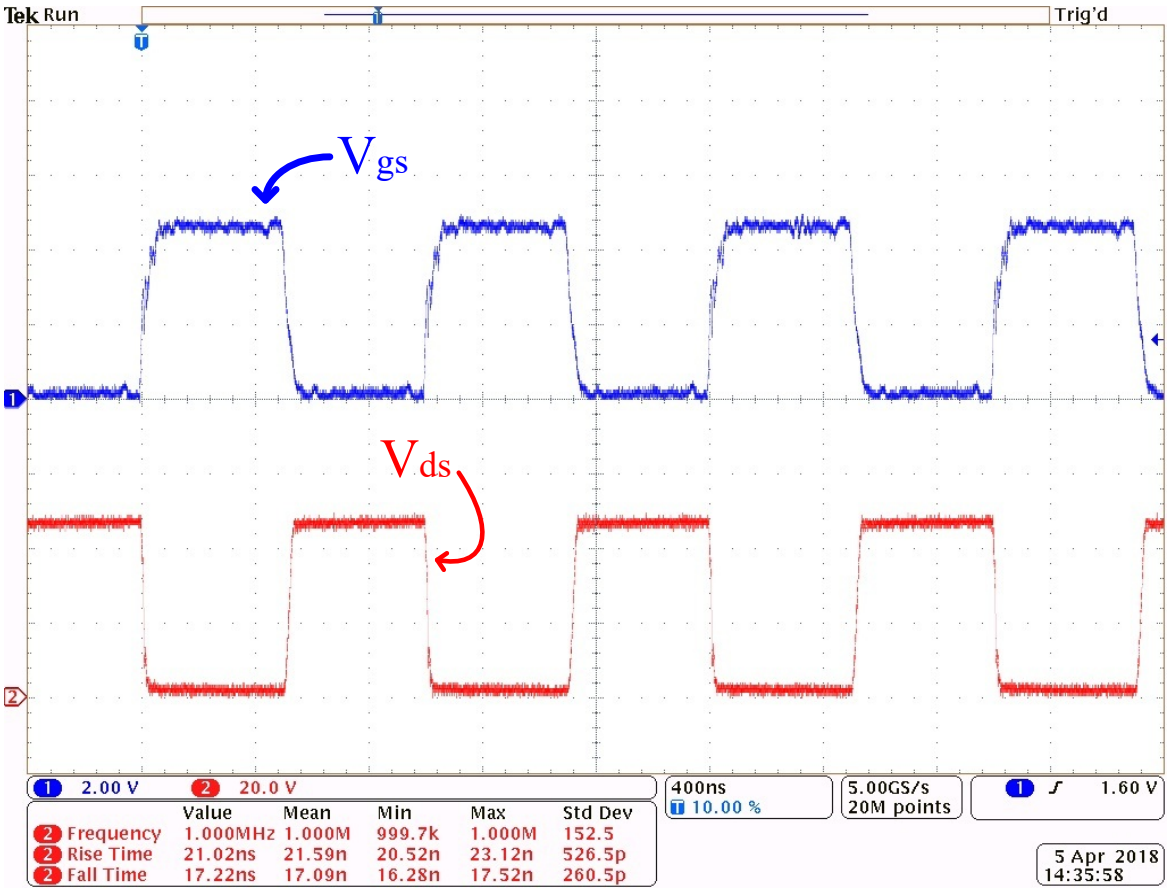


Figure 3.6. Comparative preview of the gate driving signal with the drain-source voltage of GS61008P.

Since the GaN switches are very vulnerable to overshoot gate-drive voltages, and the overshooting usually occurs because of inductive loops, therefore a minimal distance of 1.6 mm between the gate resistor (R_g) and the gate terminal of the GaN switch is selected to prevent any kind of overshoots. Another important aspect of a good PCB is to reduce the high-frequency current loop(s) in the power stage of the PCB. High-frequency loops are important to be considered because the naturally occurring current transitions may lead to surge currents when the area/traces, in which it occurs, is large. In the SEPIC converter, such a high-frequency loop exists around the coupled inductor, so the layout has been chosen to keep it compact. Fig. 3.6 shows a comparative preview of the fidelity between the gate

driving signal and the drain-source voltage of the GaN switch. A clean waveform without any ringing effect even at frequencies > 1 MHz can be seen.

A zoomed version of the switching behavior comparing the gate-source voltage to the drain-source voltage is shown in Fig. 3.7 in which both the turn-on and turn-off switching transitions are shown. This explains why the discrete components are soldered very carefully in the closest possible vicinity of each other.

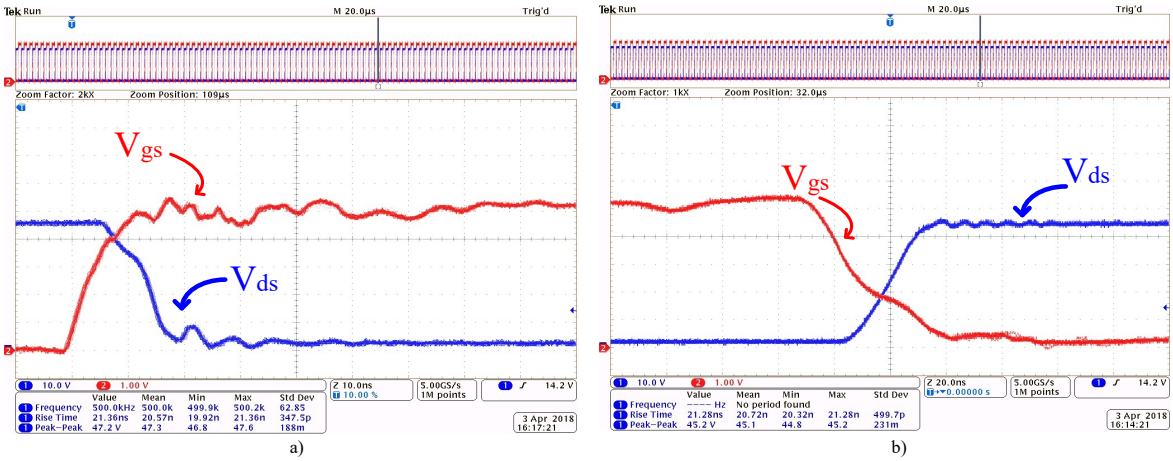


Figure 3.7. Vds and Vgs for a) turn-on and b) turn-off transient.

3.4. Aperiodic Gate-drive Signal for EMI Suppression

An aperiodically modulated PWM signal was served to drive the SEPIC converter. The aperiodic modulation methodology is shown in Fig. 3.8. The carrier and modulation signals (triangular and sinusoidal with a dc offset, respectively) can be generated using either analog or digital sources, and from them the aperiodic switching signal can be generated. Another important feature in the modulation methodology is the utilization of a triangular carrier, which allows the modulation of both the rising and the falling edges, facilitating better spreading of harmonics [58]. The modulation signal is simply a sinusoidal signal with a DC offset; the peak-peak value of the modulation signal 'h' defines the modulation range. For

example, considering two different modulation signals, a DC signal of amplitude $0.5\,V_P$ and another modulation signal being a sinusoid with a DC offset with $h = 0.1\,V_P$, the former gives a fixed duty cycle of 50%. However, regarding the latter modulation signal, the peak-peak value varies between $0.49\,V_P$ and $0.51\,V_P$. This implies a duty cycle variation from 49 ~ 51 % and the anharmonic relationship between the carrier and modulation signal is the basis of aperiodic modulation.

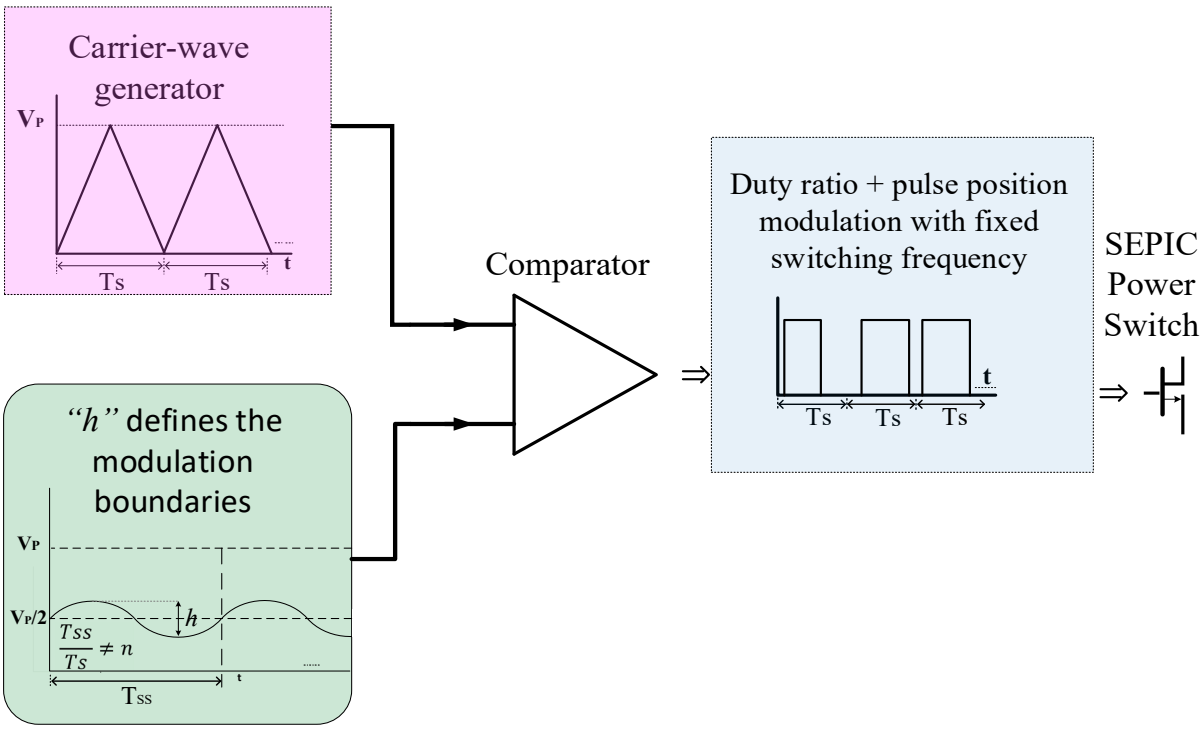


Figure 3.8. Aperiodic PWM signal generation framework for SEPIC converter.

Fourier analysis can be the first step in understanding the spreading due to the aperiodic modulation methodology. Therefore, the FFT analysis of a reference PWM signal (fixed pulse position and duty cycle) and an aperiodic PWM signal (aperiodically varying pulse position and duty cycle), has been done in the MATLAB Simulink environment. The Fourier spectra of both the reference signal and its aperiodic version are shown in Fig. 3.9, and the suppression of peaks along with the spreading of harmonics are noted. Compared to the spectral analysis given in Section 3.1.3, the harmonics are spread more effectively

when the carrier signal is a triangular pulse train in contrast to a sawtooth pulse train. This phenomenon tracks back to the dual-edge modulation in which both the rising and falling edges of the PWM signal are being modulated independently, giving greater harmonic spreading and leading to EMI suppression.

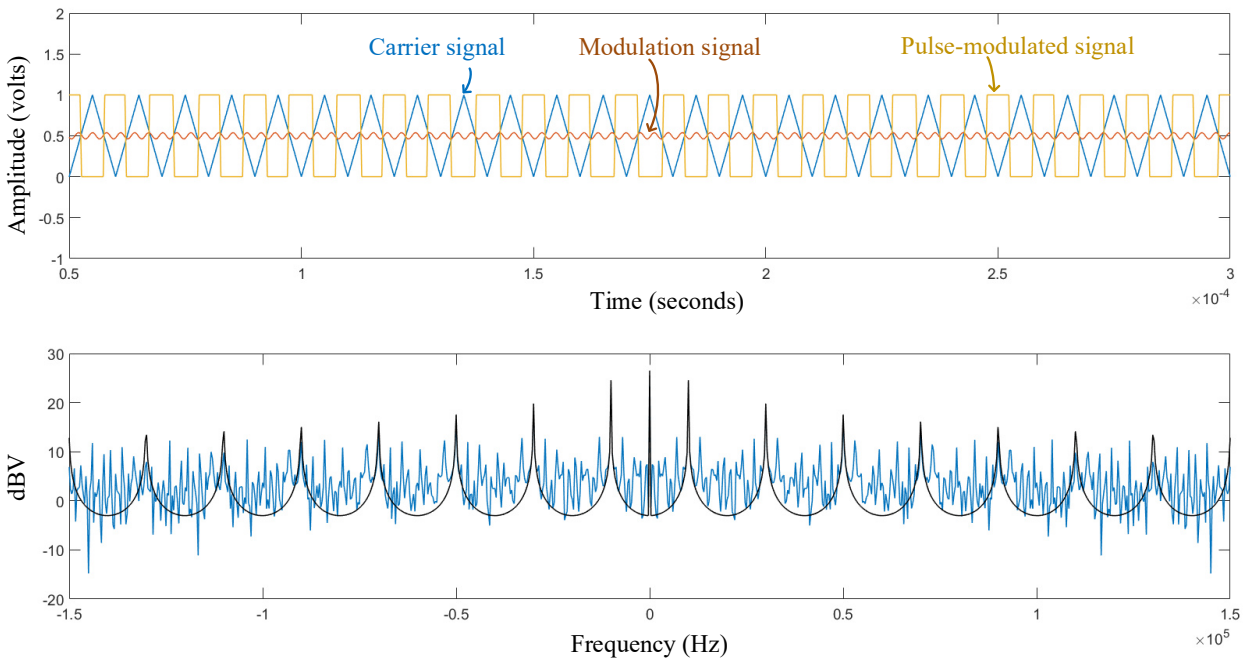


Figure 3.9. Fourier transform comparing the spectra of the periodic and aperiodic pulse modulations generated by a triangular carrier.

As a rule of thumb, the voltage regulation of a DC-DC converter depends on the duty cycle of the PWM signal, therefore varying the duty cycle could impact on the output voltage and current. This has been dealt with in the selection of the frequency of the modulation signal. As the carrier switching frequency defines the switching period and the frequency of the modulation signal is less than the carrier frequency, the duty cycle of consecutive switching cycles doesn't vary so much as to have impact on the voltage ratio. On the other hand, the pattern of switching transients (turn-on and turn-off) in each

switching cycle is aperiodic due to the proposed methodology. This leads to the spreading of harmonics as reported for various spread-spectrum modulation schemes [34], [36], [66].

3.5. Experimental Results and Discussion

3.5.1. EMI Suppression, Voltage Gain and Efficiency Analysis

The implementation of the modulation signal has been implemented via a sawtooth carrier signal as well as a triangular carrier signal. Of course, the implementation via a sawtooth carrier will produce a modulation/variation of one of the edges (leading or trailing), thus resulting in less spreading of the harmonics than with modulating of both edges.

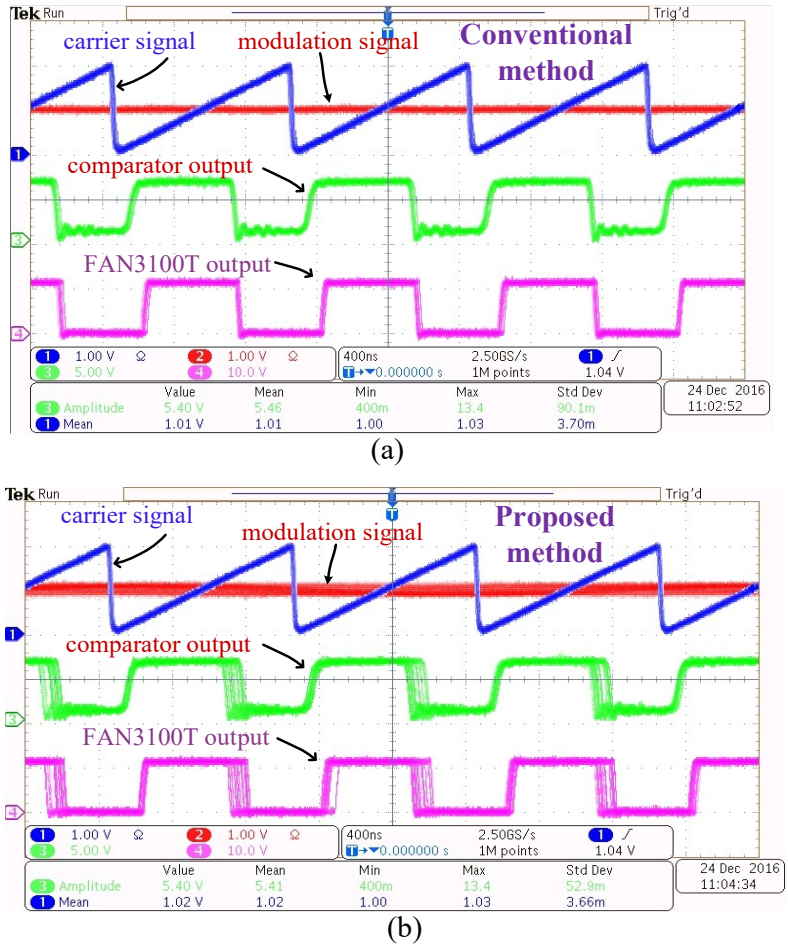


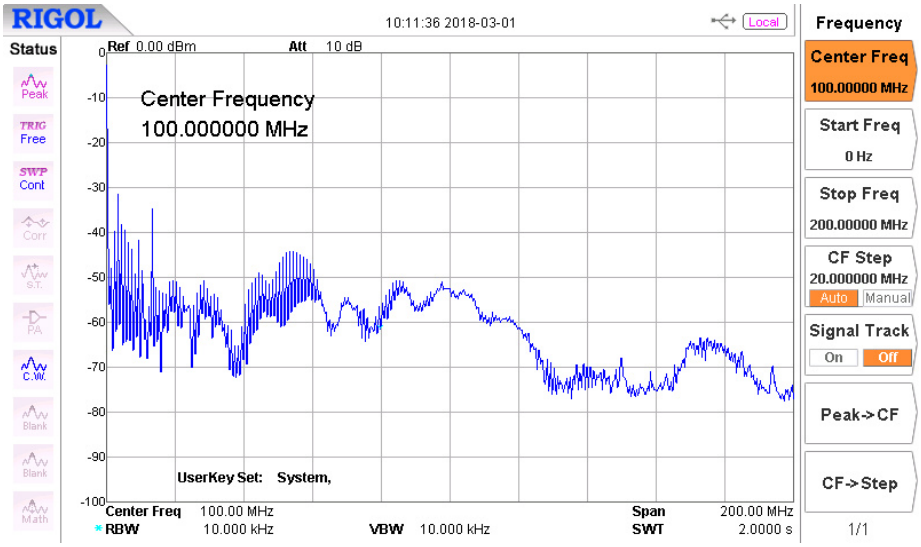
Figure 3.10. Key waveforms illustrating generation of switching patterns using (a) conventional and (b) sawtooth carrier-based proposed method.

The PWM generated with $\frac{T_S}{T_{SS}} = 1$ and $h = 10\%$ of V_P gives a PWM with a fixed duty cycle and pulse position, whereas the PWM generated with $\frac{T_S}{T_{SS}} = n$ with the same 'h' gives a varying pulse and its position. For a sawtooth carrier, the key waveforms of both the reference and the proposed modulation schemes are shown in Fig. 3.10 [67]. The blurred edges in the gate-drive signal in Fig. 3.10 (b) are an indication of the aperiodicity in the proposed pulse modulation scheme, which is the basis of the EMI suppression. The carrier and modulation signals were generated with the help of a laboratory function generator, whereas a comparator IC LM319N was used to compare and generate the resulting PWM. FAN3100T served as an isolated gate driver suitable for high-speed switching of WBG devices. Using triangular carrier, the logical implementation was done in PSIM software and realized on a TI peripheral explorer kit TMS320F28335 [68] by using the SimCoder block. The SEPIC converter was tested for both the reference and proposed modulation signal.

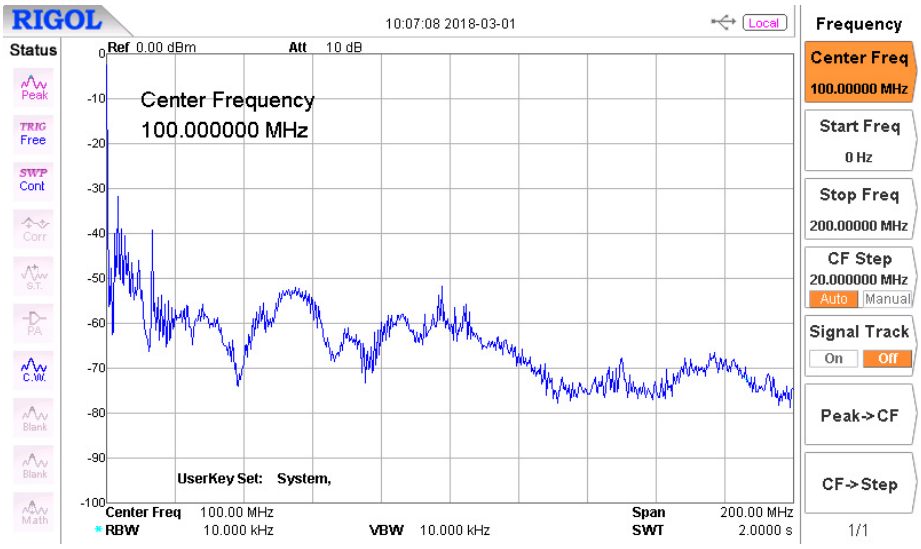
Table 3.2. Key Parameters for Periodic and Aperiodic switching signals

Parameter	**Reference**	**Aperiodic Modulation A**	**Aperiodic Modulation B**
$f_S = 1/T_S$ (carrier frequency)	500 kHz	500 kHz	500 kHz
$f_m = 1/T_{SS}$ (modulation frequency)	NA	107 kHz	107 kHz
V_P (Peak value of carrier signal)	1 V	1 V	1 V
Phase angle (ϕ)	NA	41°	41°
'h' (peak-peak value of modulation signal)	NA	0.48 - 0.52	0.47 - 0.53

A list of the related parameters of various modulation schemes is given in Table 3.2. The experimental platform for the conducted EMI analysis is shown in Appendix A. 4. The conducted EMI was measured via a standard line-impedance stabilization network (LISN) [15] and the EMI spectra were plotted on a RIGOL DSA815 RF spectrum analyzer.



a)



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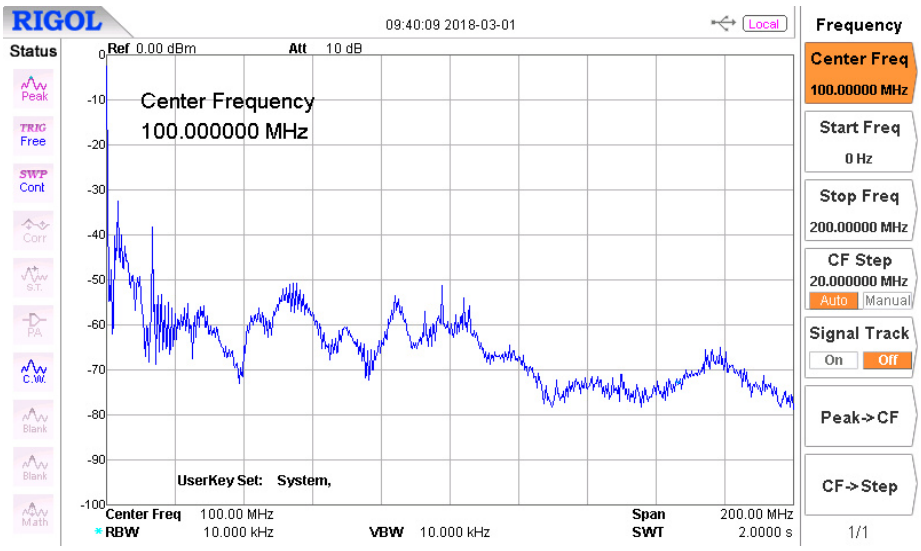


c)

Figure 3.11. Spectrum of conducted EMI (0 ~ 200 MHz) for a) reference PWM, b) aperiodic modulation A and c) aperiodic modulation B.

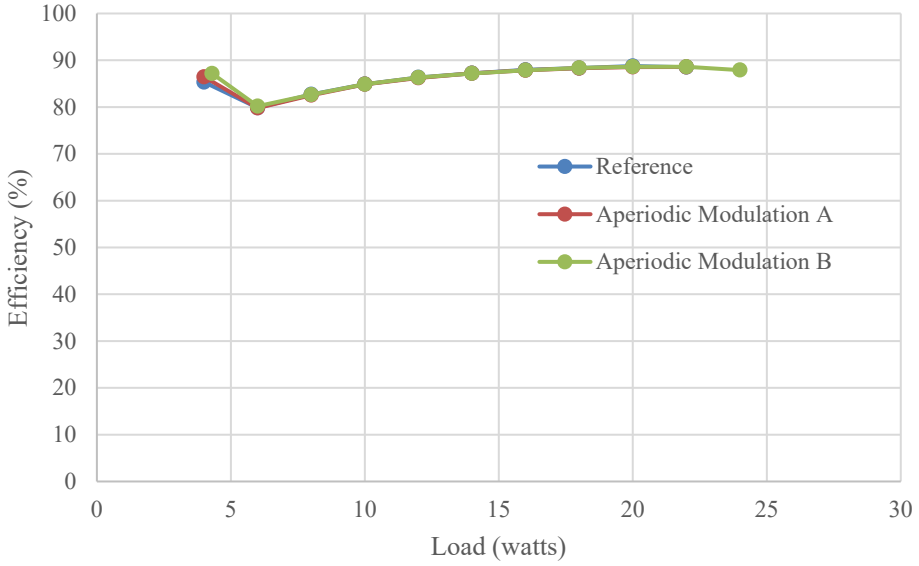


Figure 3.12. Efficiency vs load index for the reference and proposed modulation schemes.

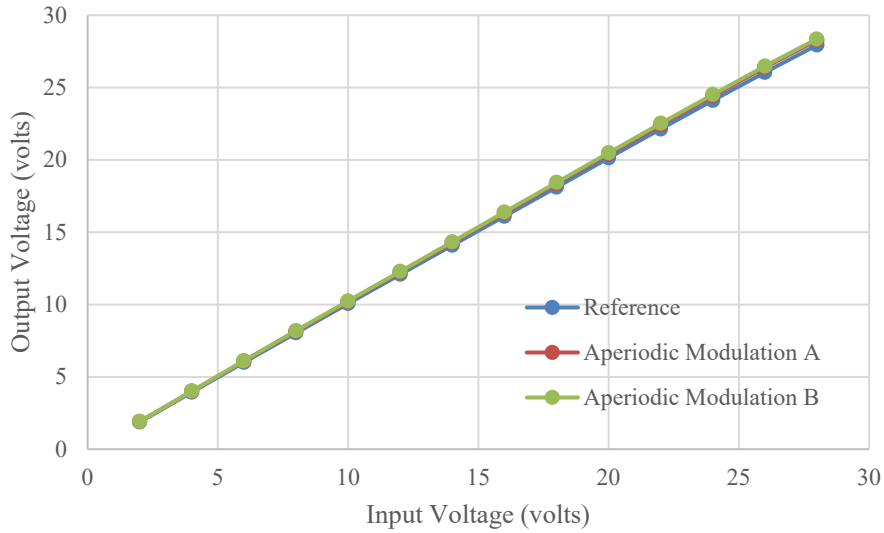


Figure 3.13. Voltage-gain index for the reference and proposed modulation schemes.

The EMI spectra for the conventional and the proposed aperiodic modulation schemes are shown in Fig. 3.11. It is clear that the EMI suppression increases with increasing 'h'. Fig. 3.11 (b and c) show the EMI spectra for the aperiodic modulations A and B, respectively. Since a hybrid pulse modulation (pulse-position modulation leads to pulse-width modulation) has been applied to a GaN SEPIC converter to depict the EMI suppression, the efficiency analysis as well as the voltage gain of SEPIC converter being a classical DC-DC converter is very important to consider. Therefore, the efficiency and the

voltage gain related measurements are presented in Figs. 3.12 and 3.13 respectively. It can be observed from the voltage gain and efficiency vs load index that there is no adverse effect on these two important parameters due to the proposed EMI suppression techniques. The peak efficiency approaches 90% around the 20 watts rated load, as per the design considerations. Hence the power converter operates in its optimal condition along with low EMI.

3.5.2. Switching-Frequency Impact on the EMI and Thermal Performance

In this section, some empirical results are given which provide another insight into the EMI of power converters. Specifically, the impact of the switching frequency on the EMI noise levels for the SEPIC converter is presented. Eight different combinations, listed in Table 3.3, were used to obtain the conducted EMI spectra, which are shown in Fig. 3.14. The load, input voltage and duty ratio were fixed at 20 watts, 24 volts and 50%, respectively.

Table 3.3. Key Parameters for Periodic and Aperiodic PWM signals

Legend	Switching Frequency (kHz)
a1	400
a2	500
a3	600
a4	700
a5	800
a6	900
a7	1000
a8	1100

The spectrum analyzer was set to detect the positive peak of the EMI, hence some of the EMI spectra given in Fig. 3.14 only the positive peaks in the shape of an envelope are evident. In reality, there are still constituent switching harmonics which add up to make

the envelope. This can be verified by zooming in the area under an envelope, as shown in Fig. 3.15.

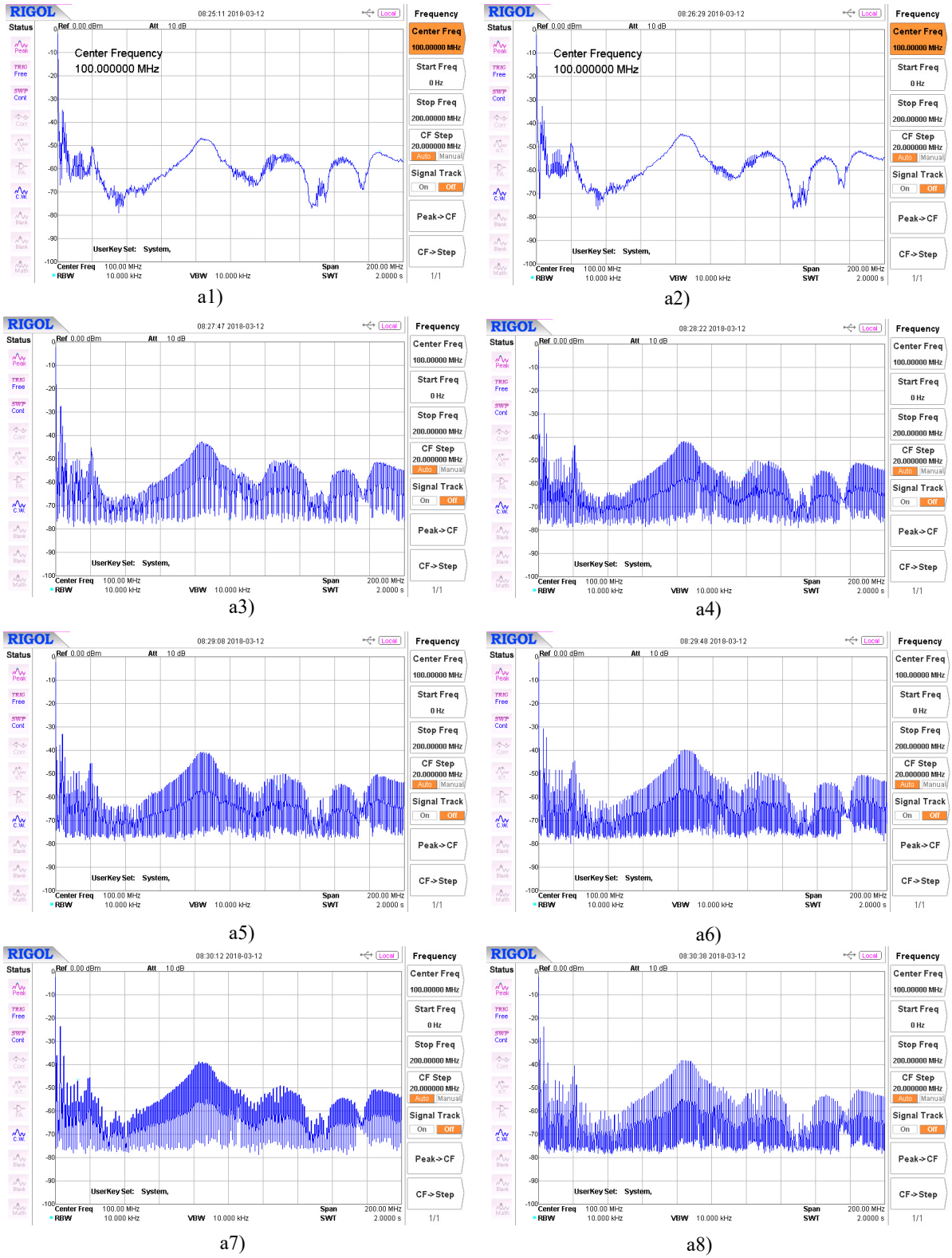


Figure 3.14. EMI spectra for various switching frequencies.

A proportional relationship between the peak EMI and the switching frequency can be observed. Higher switching frequency not only shifts the harmonics towards the higher harmonic range [4] but also the noise produced is increased. This can be understood simply by the fact that the number of switching transitions for a fixed time period increases for a power converter operated at a high switching frequency as compared to a power converter operated at a lower switching frequency. Furthermore, a thermal camera was used to observe if the aperiodic modulation impacts on the thermal performance of the SEPIC converter. The results are illustrated in Fig. 3.16 and it can be seen that no adverse impact eventuated.

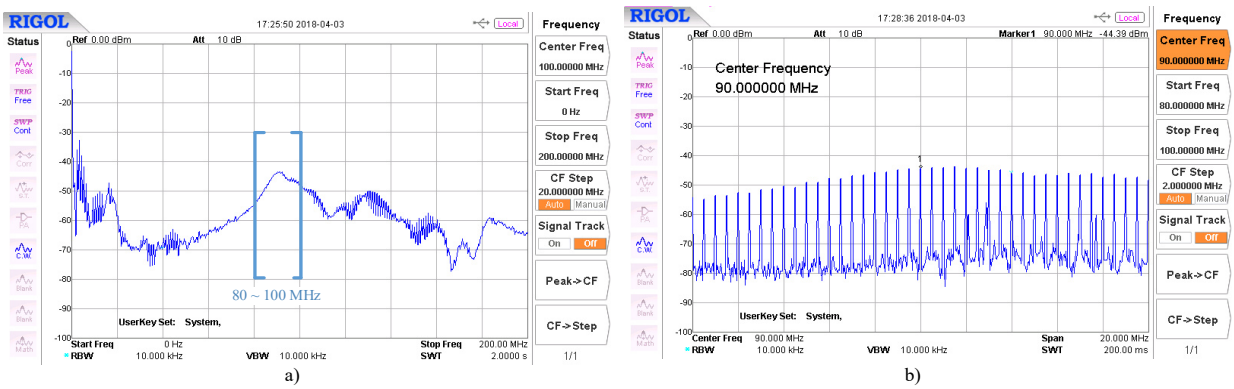
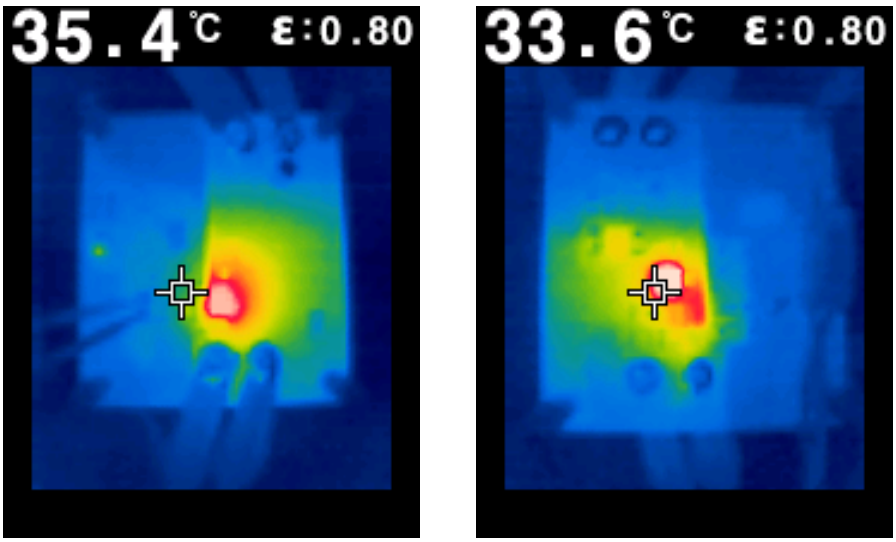


Figure 3.15. a) Envelope zoomed in to show b) its constituent harmonics.



a) b)

Figure 3.16. Top thermal image capture for the SEPIC converter with a) reference and b) aperiodic modulation scheme.

3.6. Summary and Conclusions

In this chapter, firstly, a simple implementation of the aperiodic PWM signal is presented along with its associated spectral analysis. The implementation methodology can be realized with both analog and digital techniques. Furthermore, the aperiodic PWM was applied to a hard-switched SEPIC converter to learn more about the EMI associated with a power converter as well as to get the EMI suppression results. A SEPIC converter was chosen as the laboratory prototype because of its simple design and minimal components. Various design steps for calculation of associated parameters are also given along with the high-frequency PCB design. It has been demonstrated via simulation and experimental results that the proposed modulation method leads to EMI suppression. Finally, there are no adverse effects on the power converter's natural performance.

Chapter 4

Aperiodic Modulation for Cascade GaN HEMT-based qZS DC-DC Converter

In this chapter, the application of the aperiodic modulation methodology is extended and applied to a galvanically isolated quasi-Z-source (qZS) DC-DC converter. A qZS network with an H-bridge and a voltage doubler is a very attractive topology which offers galvanic isolation, buck-boost operation and a natural low-pass filter (due to the qZS network) at the input dc side of the converter [69], [70]. Moreover, for the presented experiment, this topology is implemented with cascode GaN HEMTs, making the overall circuit undergo sharp voltage and current transitions. Consequently, this produces high EMI noise generation [4] and hence provides an attractive prototype for EMI analysis.

Firstly, the devised topology is introduced and various proposed modulation techniques for the isolated qZS DC-DC converter are presented and compared in terms of the diverse

realizations and limitations. Then, a sawtooth-carrier-based aperiodic carrier signal is proposed, which is further extended to implement the aperiodic version of various modulation schemes [44], [54], [55], [71]. The proposed EMI suppression methodology is supported by analytical and experimental results. Finally, the chapter is concluded with a summary of the main points described here.

4.1. Introduction to an Isolated qZS DC-DC Converter Topology

An isolated qZS-based DC-DC converter is shown in Fig. 4.1 which can be disassembled as a combination of a quasi-Z-source (qZS) network, an H-bridge, an isolation transformer and a voltage doubler.

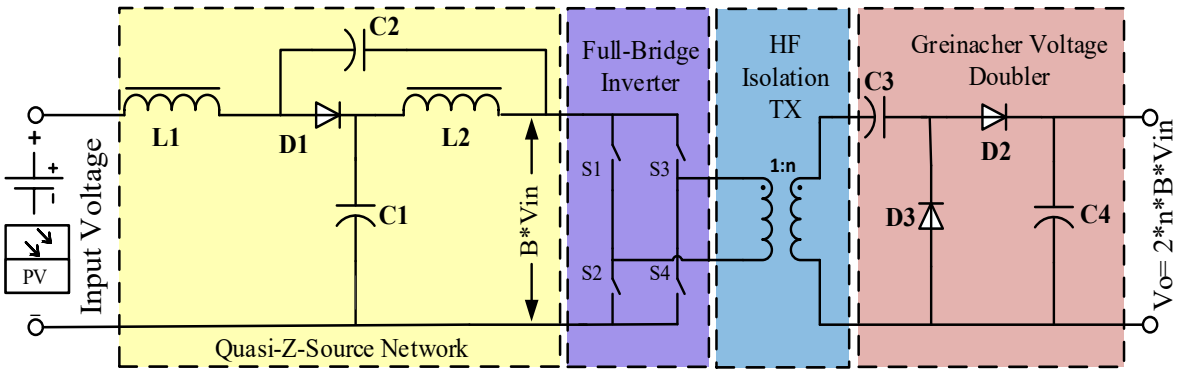


Figure 4.1. An isolated qZS DC-DC converter [44].

Like the other impedance-source (ZS) network [72] and its extended topologies [73], the qZS-based converters have two operating states: firstly, non-shoot-through states (active states and zero states, in which one switch on each side of the H-bridge conducts, on the diagonal or horizontal arm, respectively); and secondly, shoot-through states (i.e. when both switches in either or both legs of the H-bridge conduct simultaneously). The qZS impedance network in theory behaves as a low-pass filter, blocking high-frequency currents in the H-bridge switching section of the circuit from entering the supply circuit, and preventing

damage to the switching devices during the shoot-through states. Applying a volt-second balance to the qZS impedance network and switches for the two operating states, the qZS network voltage gain is given by

$$\frac{V_{out}}{V_{in}} = \frac{1}{\left(1-2*\frac{T_{ST}}{T_S}\right)} = B, \tag{4.1}$$

where B is called the voltage boost factor. The voltage gain therefore depends solely on the shoot-through state duty cycle, defined as $D_{ST} = \frac{T_{ST}}{T_S}$, in which T_{ST} is the shoot-through state duration and T_S is the period of one switching cycle. The duty cycles of the other switching states may be defined similarly, such that $D_A + D_Z + D_{ST} = 1$, in which D_A is the active-state duty cycle and D_Z is the zero-state duty cycle.

The complete DC-DC converter circuit used in this work is shown schematically in Fig. 4.1 and it has numerous advantages, as follows [74]:

i. It can realize a buck or boost function in a single stage, requiring fewer components than multistage converters and thus offer providing improved reliability.

ii. The qZS topology is not vulnerable to damage during conduction of both top and bottom switches (such “shoot-through” states are forbidden in voltage source inverter (VSI)-based converters [75].)

iii. The qZS topology allows reduced component count with reduced passive component ratings compared to the ZS-based topologies.

iv. The constant input current makes the qZS topology well-suited for applications having a wide range of input voltage [70].

v. The HF transformer provides galvanic isolation of the load from the source, which is advantageous in many applications.

vi. The voltage-doubler circuit reduces the turns ratio required by the HF transformer.

vii. Depending on the switch modulation scheme, soft switching of the active devices can be achieved for some switch transitions [76].

4.2. Cascode GaN HEMT Switches

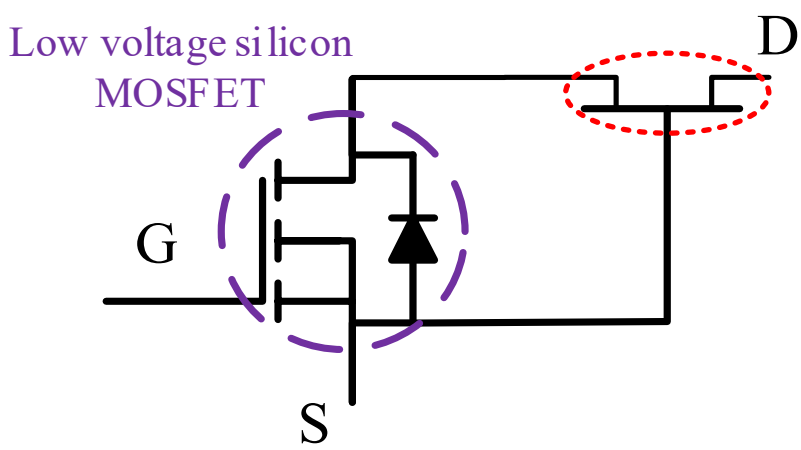


Figure 4.2. Cascode hybrid-GaN structure [77].

WBG switches, as mentioned earlier, give rise to relatively broadband EMI, i.e. to hundreds of MHz for GaN devices. As the Fourier transform of an ideal switching or signum function is $(j\omega)^{-1}$, the magnitude of the EMI produced by an ideal switch reduces by only 20 dB per decade in frequency. The prototype for the qZS DC-DC converter topology for the investigation of EMI has been implemented with cascode GaN HEMTs by transphorm TPH3006PS devices [77]. These switches offer a switching transition time in the order of a few nanoseconds, more likely making the power converter generate higher EMI noise. This is comparable to if it had been implemented with silicon-based power switches which typically have switching transitions in the order of tens or hundreds of nanoseconds.

In recent years GaN HEMTS have become available on silicon substrates, significantly reducing their cost relative to devices fabricated on other suitable substrates, such as silicon carbide. GaN HEMTs are also available as either enhancement-mode (normally off) or depletion-mode (normally on) switching devices. Hybrid devices are also available in which a silicon MOSFET drives a depletion-mode GaN HEMT in a cascode configuration, as shown schematically in Fig. 4.2, resulting in enhancement-mode functionality. The latter devices can be driven by commercially available gate-driver integrated circuits.

4.3. Overview of Reference Modulation Schemes for qZS DC-DC Converter

Numerous modulation schemes have been reviewed in [76], developed for an isolated qZS DC-DC converter. Principally, these modulation schemes are differentiated by the relative positions of the three basic switching states (active, zero and shoot-through) in one switching cycle. The following part in this section discusses two of these modulation schemes, taken as reference modulation schemes to compare the performance when the aperiodic modulation methodology is applied to these schemes.

The switching pattern to govern the H-bridge switches ($S1 \sim S4$) is shown in Fig. 4.3 for two different modulation schemes. The modulation scheme shown in Fig. 4.3 (a) is based on the generation of shoot-through states by the overlap of active states [78]. Hence, there is no zero-state in this modulation scheme, which confines the voltage regulation factor, but on the other hand this modulation scheme has its own advantages such as fewer switching transitions in each cycle, reduced conduction losses (as both of the legs are shorted during

the shoot-through cycle) and the equal frequency also leads to equalized switching loss in each switch.

An improved version of the modulation scheme is presented in Fig. 4.3 (b) and reported in [74]. This modulation scheme has a number of desirable features: i) independent control of the active and shoot-through states; ii) fewer switch commutations per switching cycle; iii) only two shoot-through states per switching cycle; and iv) all the three switching states are available, which permits voltage regulation and compensation. The possible block diagrams for generating the reference modulation schemes are shown respectively, in Fig. 4.4.

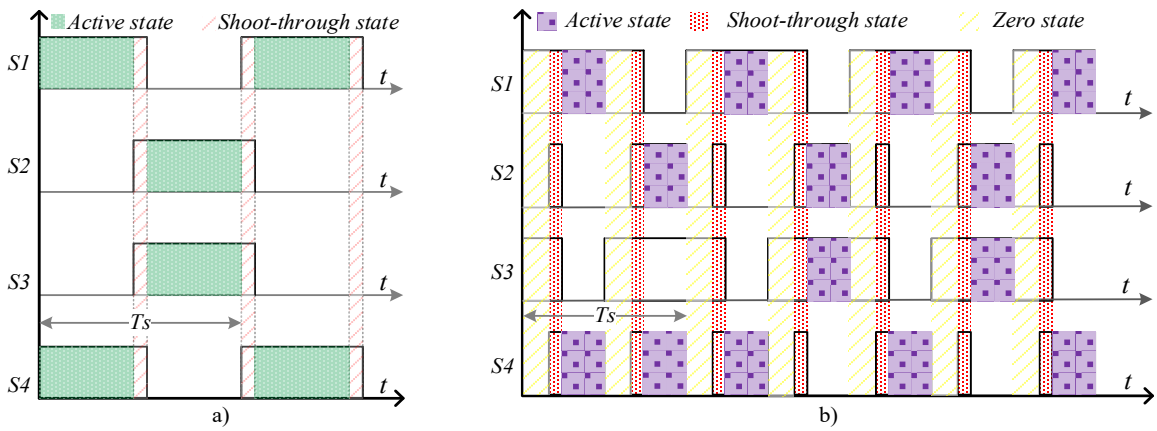


Figure 4.3. Reference modulation schemes containing a) active and shoot-through states only [78], and (b) active, zero and shoot-through states [74].

It can be observed that although the PWM signals governing the H-bridge switches are generated by comparing a sawtooth carrier signal with a modulation signal which is a DC constant, these signals can also be generated with other types of carrier signals, for instance a triangular carrier signal which requires the implementation method being modified [76]. The aperiodic modulation methodology presented in this work is based on utilization of an aperiodic sawtooth carrier signal as presented in the next section. For simplicity, the

modulation schemes presented in Fig. 4.3 (a and b) are further termed reference scheme A and reference scheme B, respectively.

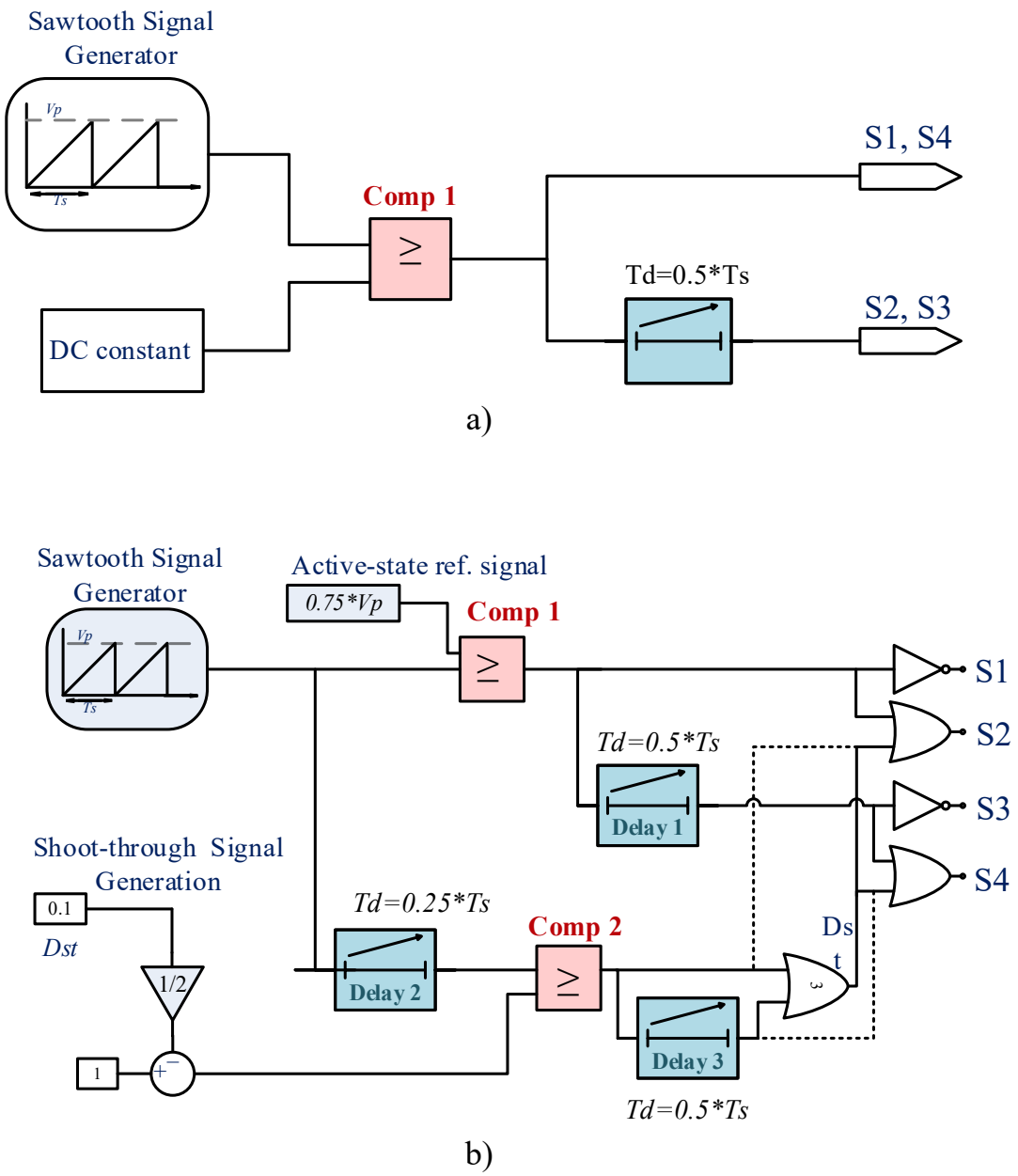


Figure 4.4. Block diagram to implement modulation scheme containing a) active and shoot-through states only, and (b) active, zero and shoot-through states.

4.4. Aperiodic Modulation Methodology for EMI suppression in a qZS DC-DC Converter

The EMI-suppression pulse modulation method used in this work relies on modulation of switching pulse parameters, as shown in Fig. 2.11, in which the switching waveform $q(t)$ is shown. Several possibilities are revealed in Table 2.1 and these schemes are readily applied to single-switch converter topologies. However, there are very few reports of their application in converters with multiple switches, as the coordination of multiple switching signals can be difficult, especially if the switching cycle duration varies. In single-switch converter topologies the switching harmonics may be suppressed by modulating the carrier frequency. However, in more complicated power converter topologies (e.g. impedance source converters) modulating the carrier frequency is not convenient. In such cases it is desirable to generate a sawtooth carrier in which the amplitude and/or duration of each successive ramp function is modulated aperiodically, but the overall switching period is constant [53].

A simple implementation of a hybrid pulse-width modulation technique is shown in Fig. 3.1 in which both the pulse position and the pulse width are modulated in each switching cycle. The theoretical basis of EMI suppression by modulating one or more parameters of $q(t)$ is discussed in [37], [43], [58] and the spectra of several such PWM techniques, including the hybrid PWM presented here, have been calculated analytically [58].

4.4.1 Aperiodic Modulation Methodology for Reference Scheme A

The modulation methodology shown in Fig. 4.3 (a) has been implemented by utilizing an aperiodic carrier signal. The generation of aperiodic carrier signal, its related parameters

and spectral analysis have been discussed in section 3.1. A logic diagram to generate the aperiodic version of the reference modulation technique is shown in Fig. 4.5.

Similarly to the case presented in Section 3.1, 'h' defines the range of aperiodicity (peak pulse/width deviation) as well as the amount of overlap between the active states, which leads to the generation of shoot-through states. Moreover the variables a1, a2 and a3 symbolically indicate the height and width variation in the aperiodic pulse train. Since, for the case of reference scheme A, the shoot-through states are dependent on the active states, the shoot-through duty ratio is not strictly fixed and varies around a minimal value. Moreover, since the shoot-through duty ratio is directly associated with the gain of the qZSI DC-DC converter, it affects the voltage gain at higher values of the shoot-through ratio. Therefore, this technique is confined in terms of applicability only to the lower values of D_{ST}.

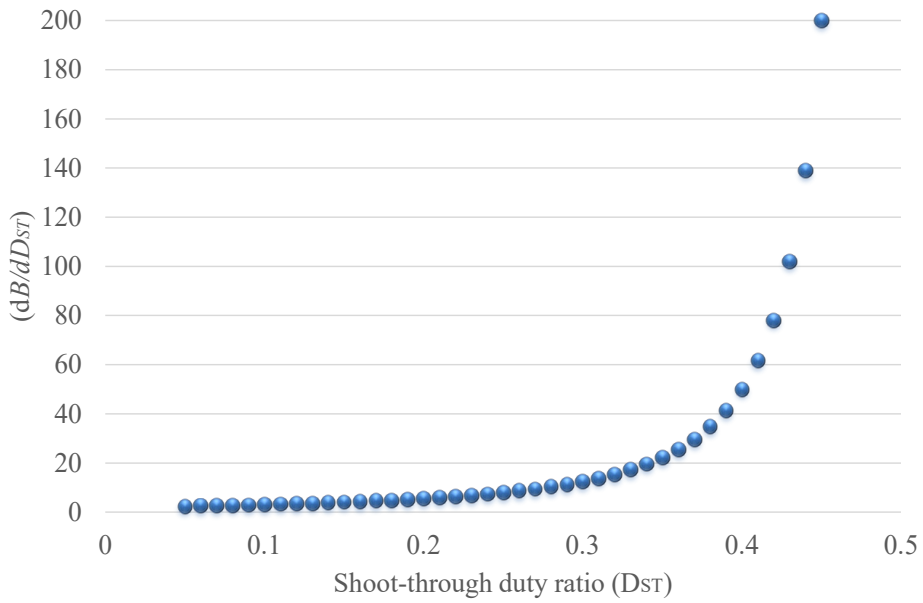
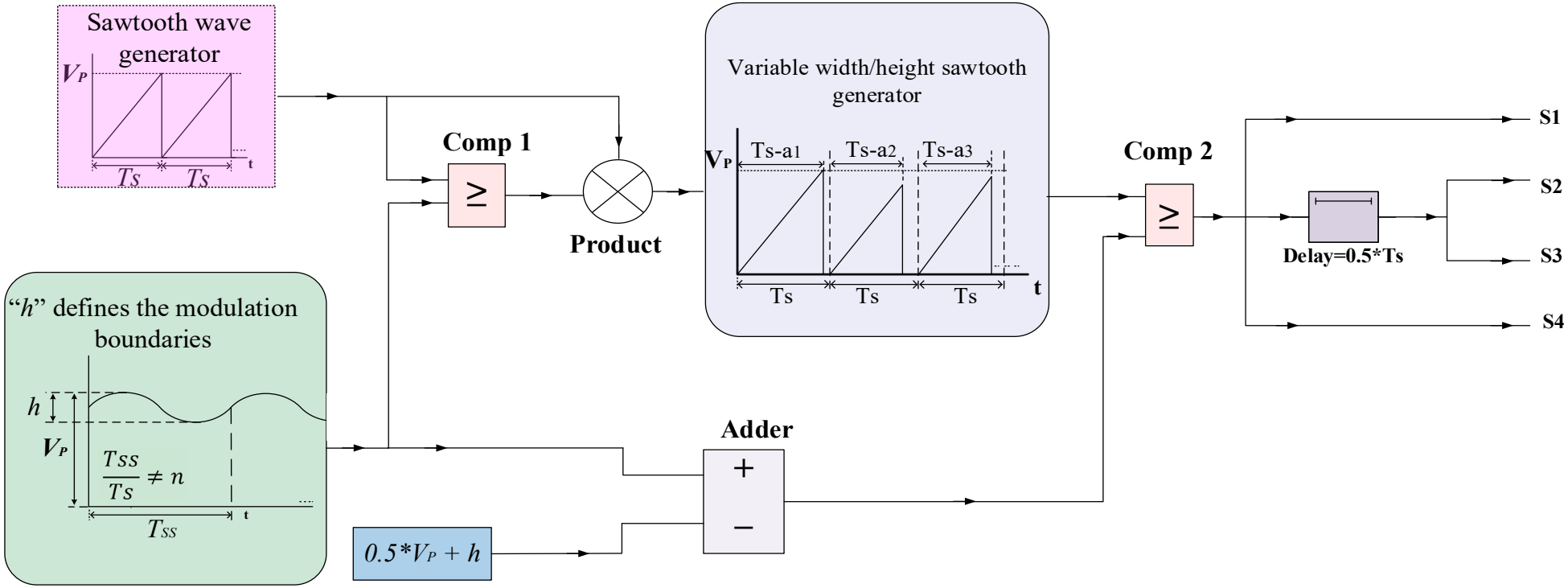


Figure 4.5. Rate of change of gain w.r.t. shoot-through duty ratio for a quasi-Z-source [71].

Fig. 4.6 presents the changing behavior of the boost factor 'B' with respect to different values of D_{ST}. It may be noted that the first-derivative (w.r.t. D_{ST}) pattern of 'B' does not

vary significantly for lower values of D_{ST}. This suggests that there should be a minimal impact on the voltage gain offered by the qZSI DC-DC converter for lower values of D_{ST} with the aperiodic modulation strategy. This hypothesis has also been justified by the experimental voltage-gain behavior of the converter presented in the next section.

Figure 4.6. L



ogic diagram to generate the aperiodic version of reference modulation scheme A [71].

The essentially aperiodic variation in switching pulse-position and duration achieved by the above method in each switching cycle prevents the accumulation of energy at harmonics of the fundamental switching frequency. It is notable that the technique is generic, and should be equally applicable to other modulation schemes [76], [79]–[82].

4.4.2 Aperiodic Modulation Methodology for Reference Scheme B

Now we present the utilization of an aperiodic carrier signal to implement the aperiodic version of the modulation scheme shown in Fig. 4.3 (b). A block diagram of the logic used to generate the switch control signals for the aperiodic modulation scheme is shown in Fig. 4.7. There are two key changes when compared to the implementation logic shown in Fig. 4.4 (b). The first difference is that the sawtooth waveform generator is programmed to generate variable-duration (with variable height) sawtooth pulses. The result is that the width of every consecutive sawtooth pulse, and hence the timing of each switching state, varies randomly within a specified range from its nominal value, Ts. The second difference is that a sinusoidal waveform is added to the reference, V_P, and is used to trigger transitions between switching states. The peak-peak magnitude of the sinewave relative to the reference value determines the range of variation in duration of each shoot-through state. It is important to note that the frequency of the sine-wave may not harmonically related to the switching-cycle repetition rate, $\frac{1}{T_S}$.

The principles underlying the design and implementation of this modulation scheme are as follows:

i. The amplitude/duration of each successive ramp is modulated aperiodically by a small amount (e.g. up to 4%) from its nominal value.

ii. Within each switching cycle the duration of the active and zero state varies aperiodically.

iii. The duty cycle of the shoot-through state, $D_{ST} = \frac{T_{ST}}{T_S}$, and hence the converter's boost factor B is kept constant, and

iv. The pairs of switching states are balanced in the duration of each switching cycle (to avoid saturation of the isolation transformer).

An example of a switching pattern fulfilling all the above requirements is shown in Fig. 4.8.

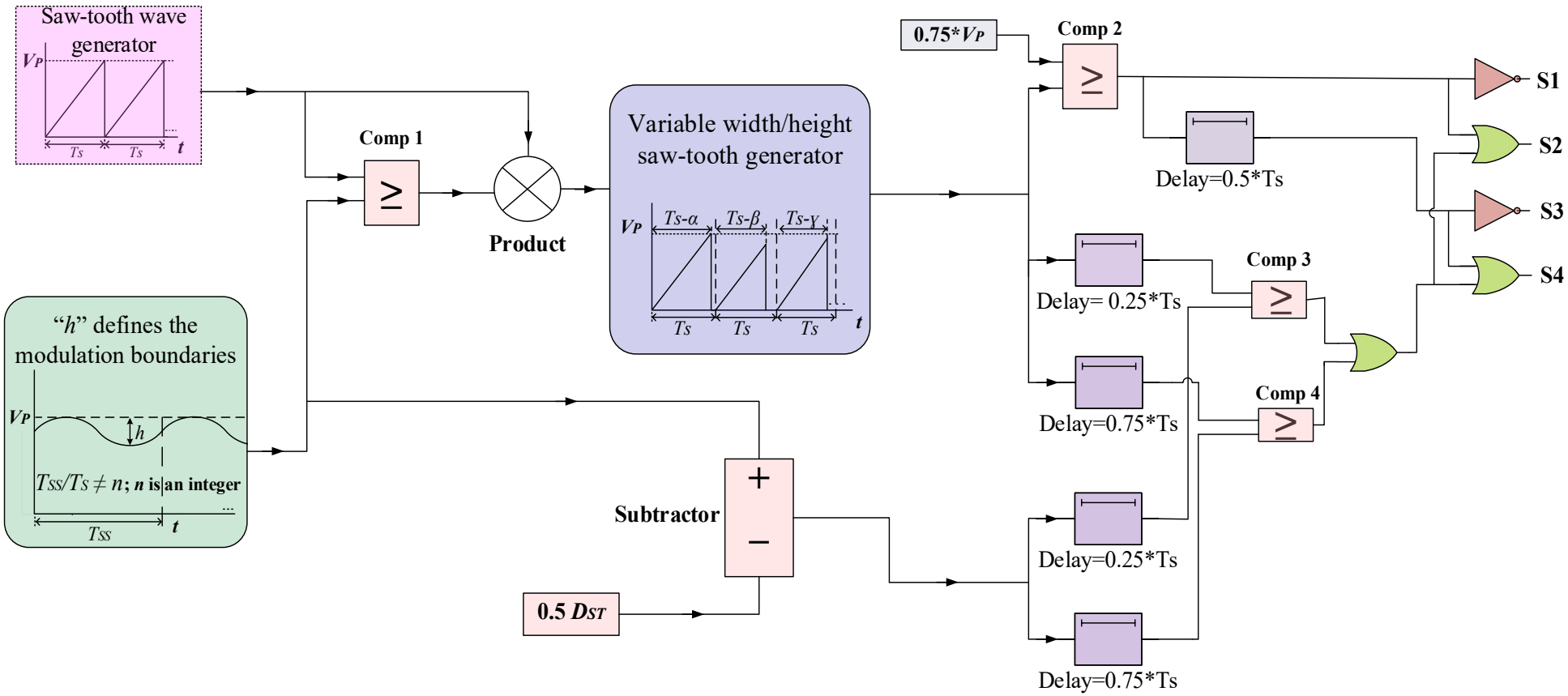


Figure 4.7. Logic diagram to implement the aperiodic version of the improved modulation scheme B [44].

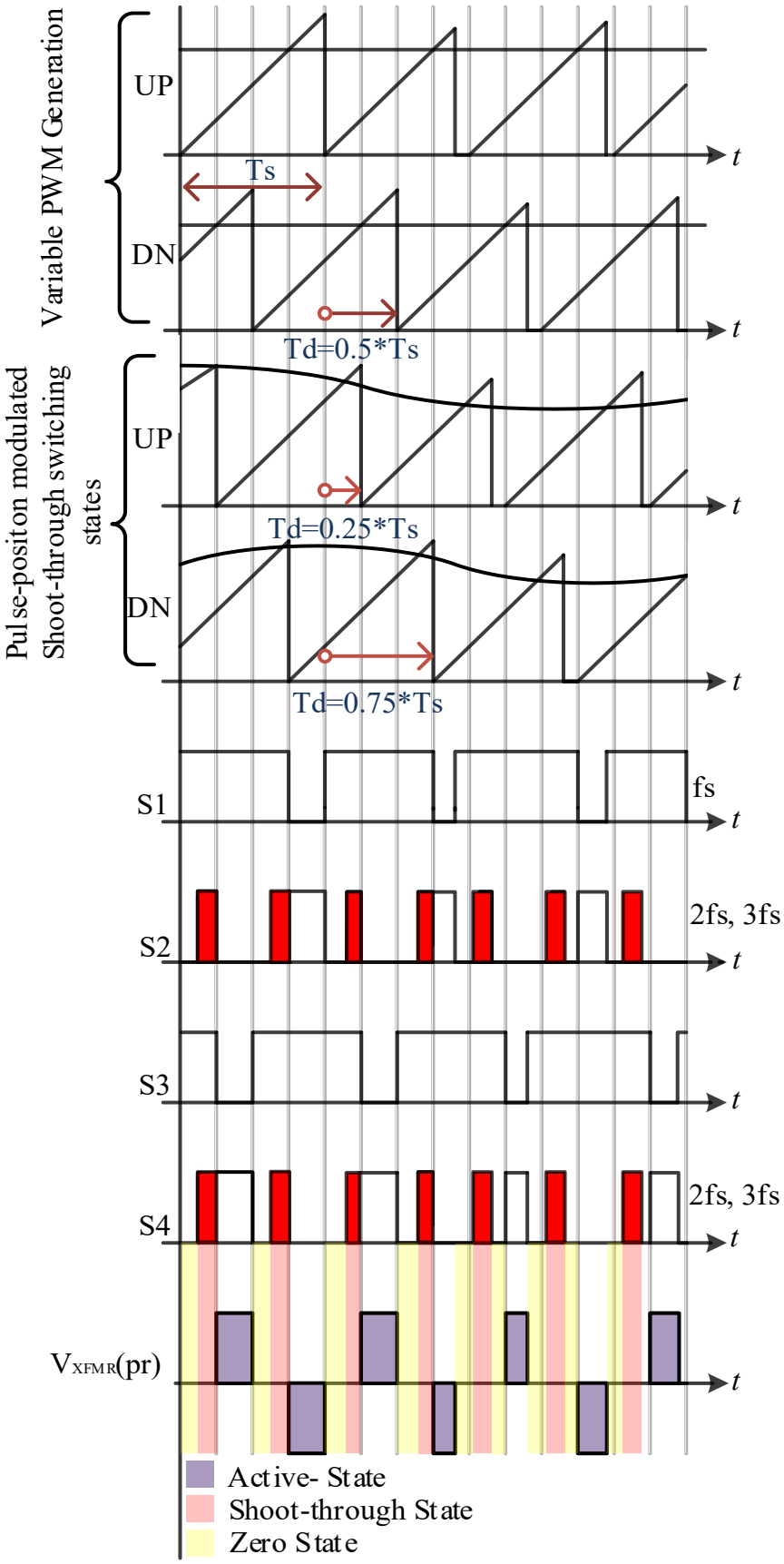


Figure 4.8. Switching sequence for an aperiodic modulation scheme for a qZS DC-DC converter.

4.5. Results and Discussion

4.5.1. Design Parameters for qZS DC-DC Converter

A prototype qZS DC-DC converter was adapted and used to test the proposed aperiodic pulse-modulation technique by measuring the reduction in EMI relative to the reference modulation schemes A and B. The key design parameters and components used in the experiment are listed in Table 4.1.

Table 4.1. Parameters and components for qZS prototype

Parameter	Value, description
Switching frequency	97 kHz and 24 kHz
Turns ratio for transformer	1:1
qZS inductors L1, L2	1.3 mH
Capacitors C1 ~ C4	1000 µF
Rectifier diodes D1-D3	SiC schottky diodes, C3D06060G
Power switches S1-S4	Hybrid GaN HEMTs, TPH3006PS
Shoot-through duty ratio	10%

It should be noted that, although GaN HEMTs usually allow high switching frequencies, the experimental results reported for reference scheme B were deliberately obtained using a 24 kHz switching frequency in order to: i) investigate the performance of the qZS network as a low-pass filter; and ii) observe a large number of switching harmonics over a broad bandwidth using a standard RF spectrum analyzer.

4.5.2. Switching Sequence of Aperiodic Version of Reference Modulation Schemes

The functional block diagrams shown in Figs 4.5 and 4.7 were programmed in MATLAB-Simulink utilizing blocks from the HDL coder library. The corresponding HDL code was

auto-generated and then compiled to run on a Xilinx Spartan 6 FPGA development board, which generated the driving signals for the GaN HEMTs [83].

The number of switching transitions in the modulation scheme A is less than that of B, therefore the switching frequency used for the implementation of these schemes is different, 97 kHz and 24 kHz, respectively. Fig. 4.9 presents reference modulation scheme A and its aperiodic version. The blurred edges in the aperiodic version depict the varying switching times in each consecutive cycle.

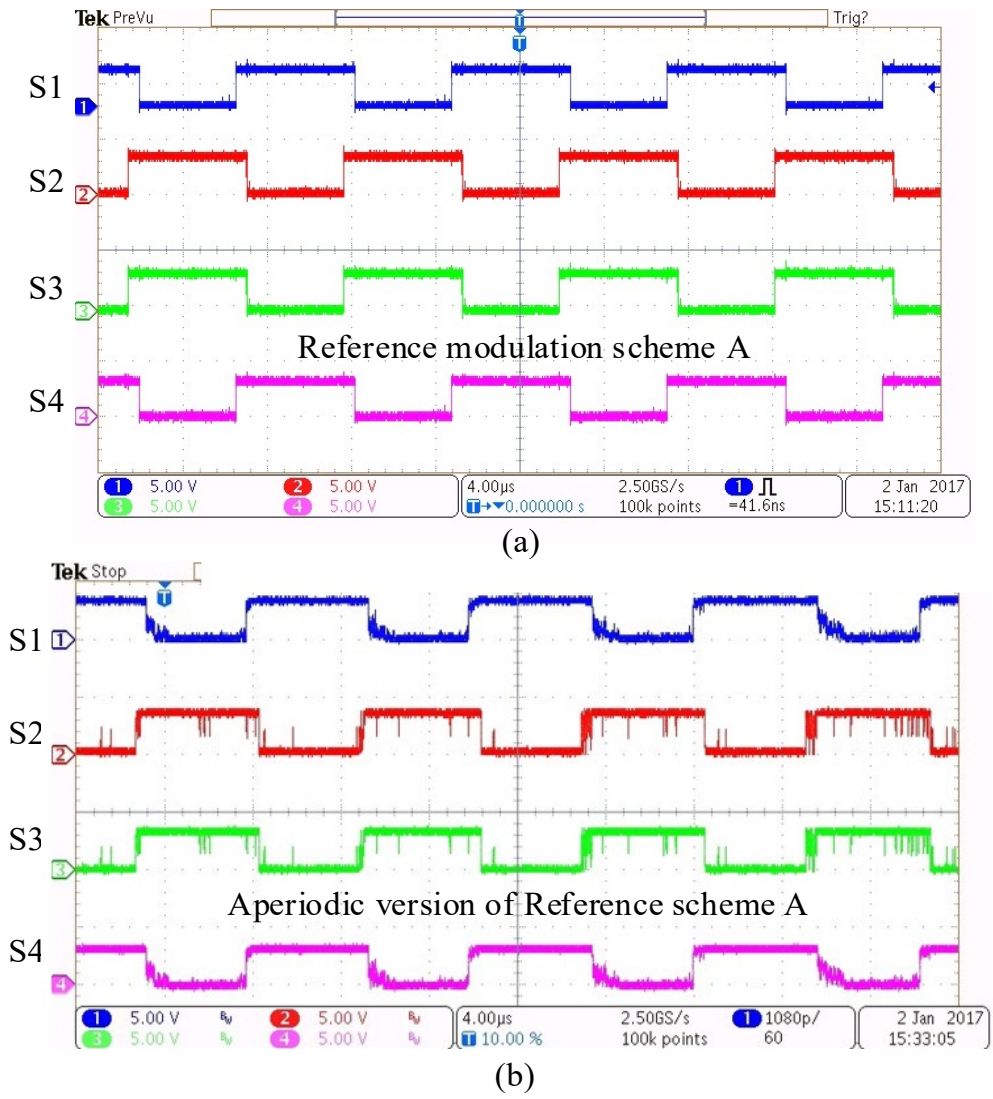


Figure 4.9. Switching pattern for a) reference scheme A and b) its aperiodic version.

Now we present the reference modulation scheme in which the shoot-through states can be controlled independently of the active states. In order to highlight the significance of the anharmonic relationship between the two constituent signals generating the aperiodic sawtooth carrier signal, a quasi-periodic modulation [54] has also been implemented.

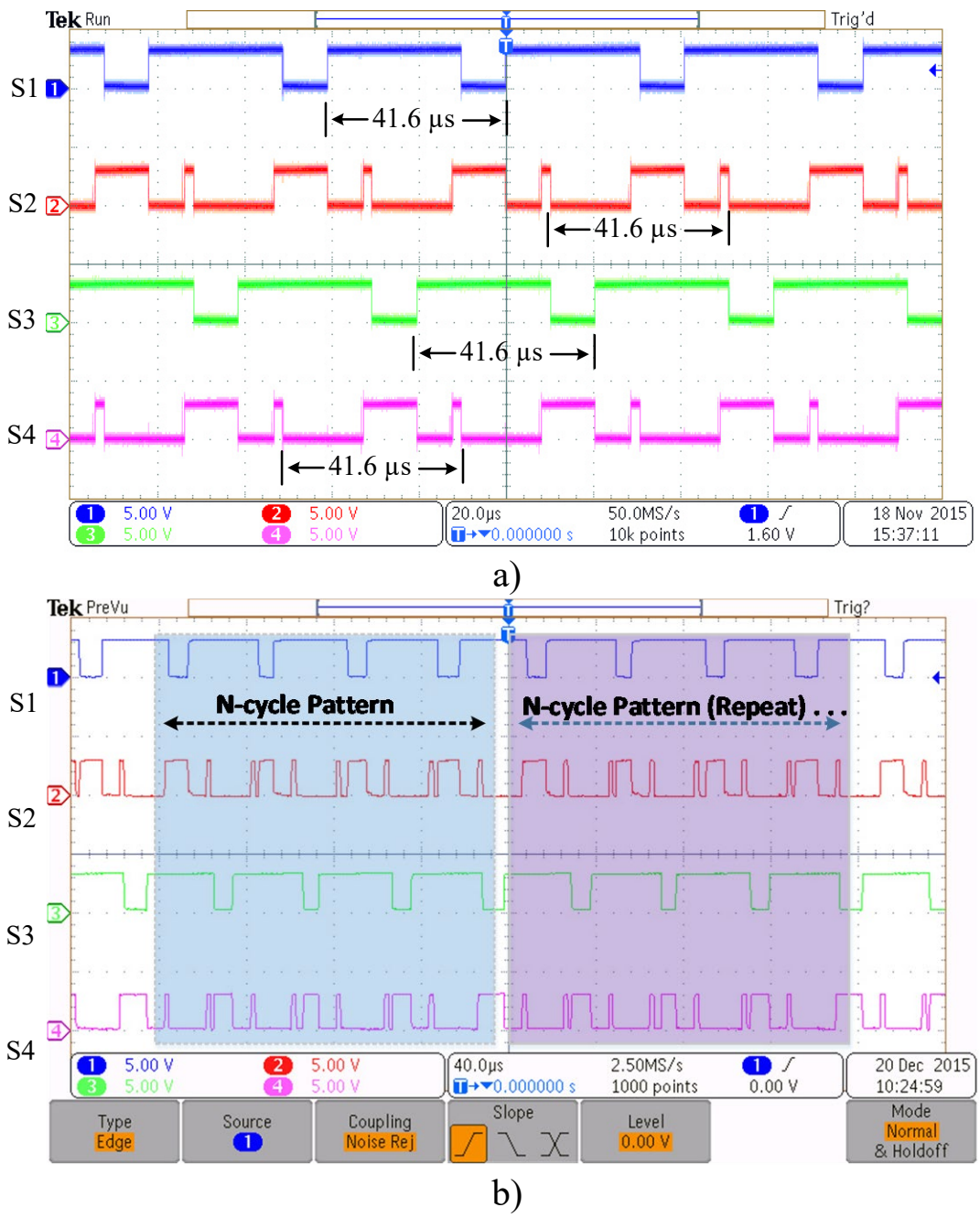


Figure 4.10. Switching pattern for a) reference scheme (Fig. 5.3 b) and b) its quasi-periodic version.

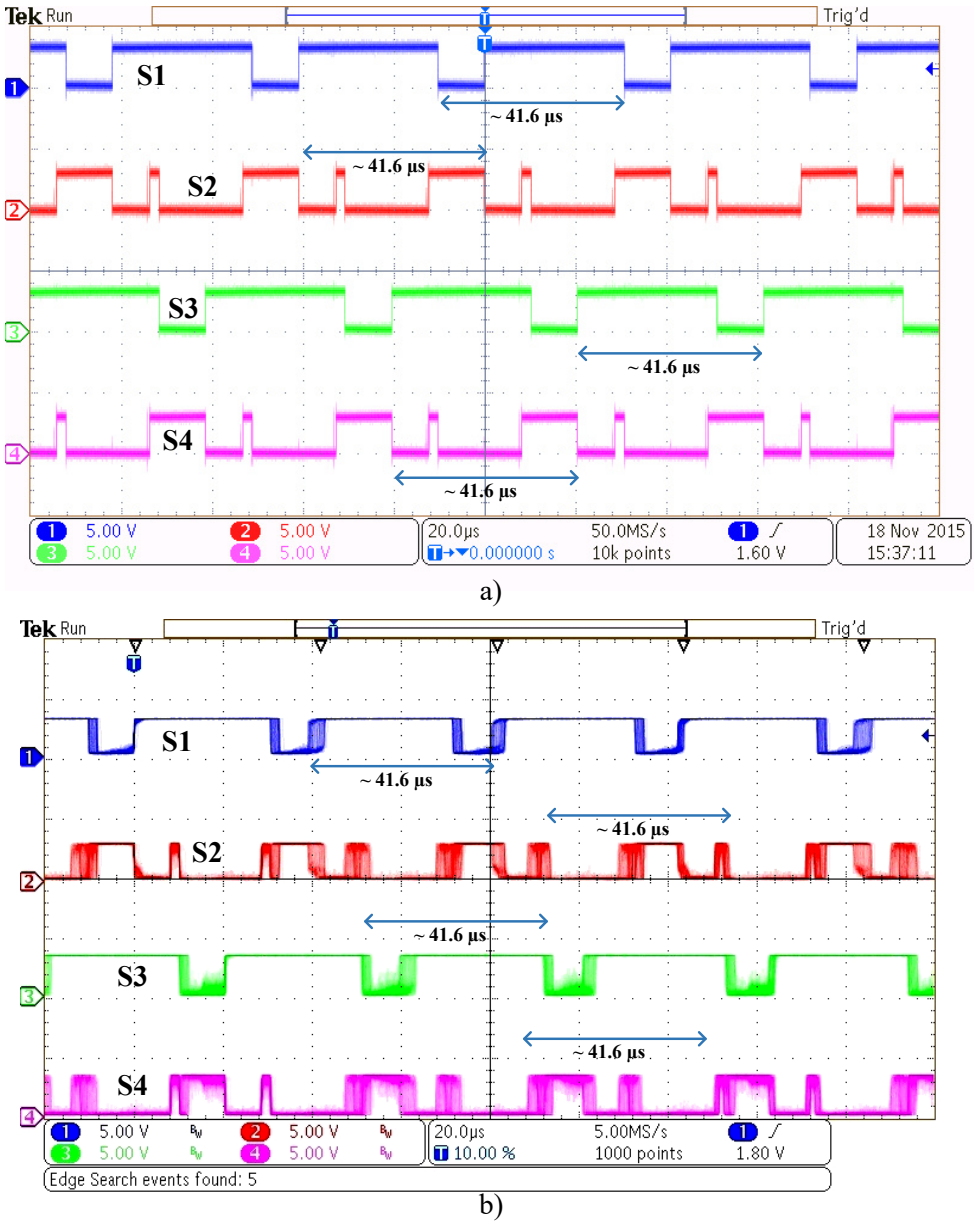


Figure 4.11. Switching pattern for a) reference scheme B and b) its aperiodic version.

It is evident that due to a harmonic relationship between the constituent signals, a repetition can be observed in the switching pattern highlighted in Fig. 4.10 (b), which explains why it is called a quasi-periodic modulation. Furthermore, the aperiodic modulation was implemented by keeping the anharmonic relationship between the sawtooth and sinusoidal signal (with the DC offset). Fig. 4.11 presents reference modulation scheme B

along with its aperiodic version. The modulation of the pulse position and hence the duty cycle is evident from the blurred edges.

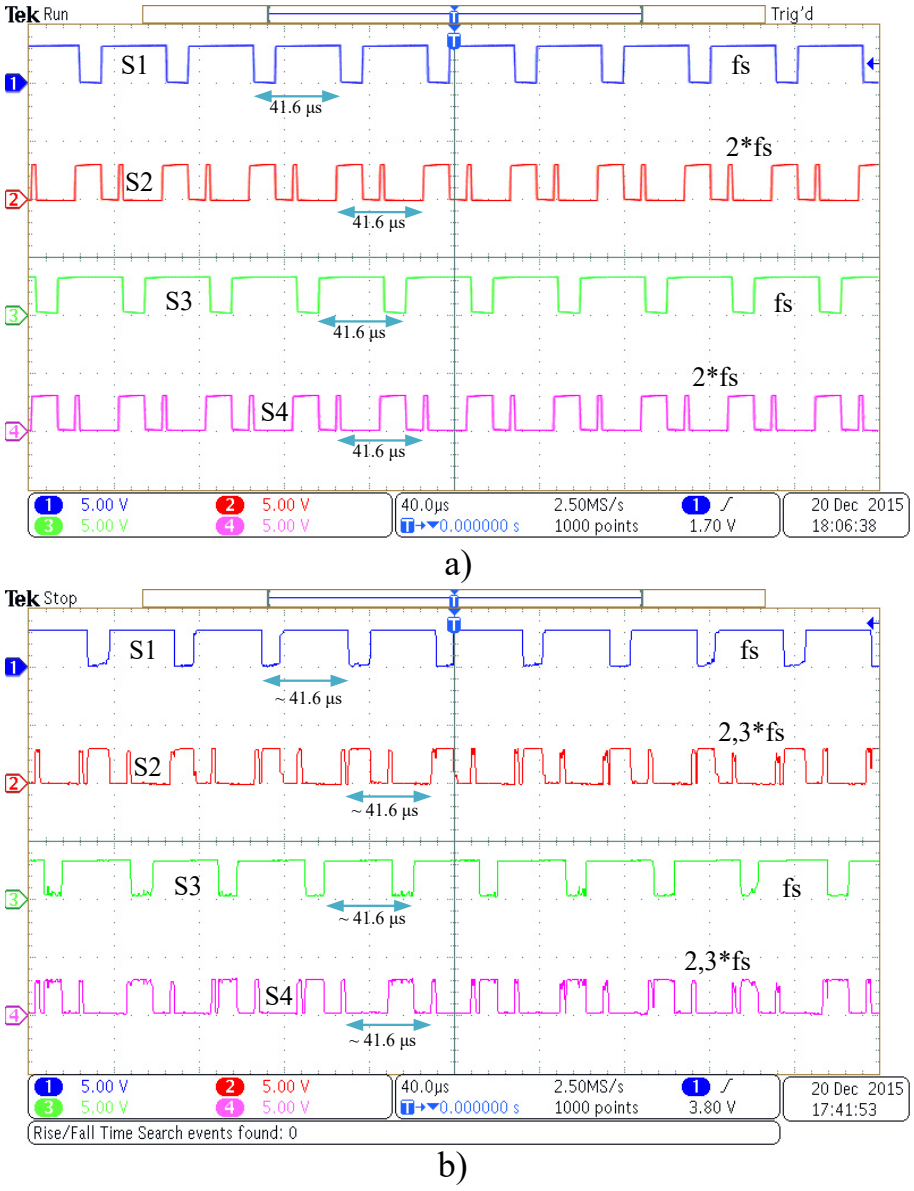


Figure 4.12. Wider temporal representation of switching pattern for a) reference scheme B and b) its aperiodic version.

Fig. 4.12 presents a wide temporal representation of the reference modulation scheme and its aperiodic version in order to show the cycle-to-cycle variation of the switch modulation more clearly. It can be observed that no pattern in terms of repetition of the sequence is obvious in the given switching sequence.

4.5.3. Voltage Gain and Efficiency Analysis

By a rule of thumb, the voltage gain of any dc-dc converter usually depends upon the duty cycle. In the proposed modulation methodology, the basis is the variation of the pulse-position and hence the pulse-width along with a constant duty cycle (for the shoot-through states). Therefore the efficiency and voltage gain are very important factors to consider. Figs 4.13 and Fig. 4.14 present the voltage gain for different values of input voltage for a constant load of 100 watts. The voltage gain for both modulation schemes and their aperiodic versions have been plotted and no significant change was found as depicted in the results. The voltage gain graphs are presented separately for both modulation schemes since there are changes in some of the parameters (due to experimental limitations). Therefore plotting a voltage gain pattern for both of the reference schemes and their corresponding versions on the same graphs does not present a fair comparison.

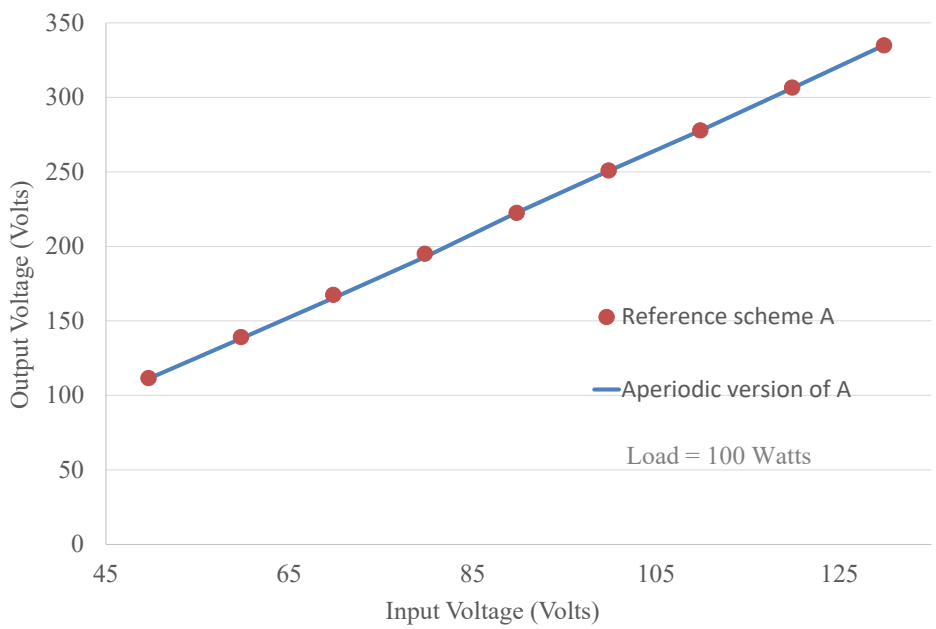


Figure 4.13. Voltage gain index for reference modulation scheme A and its aperiodic version.

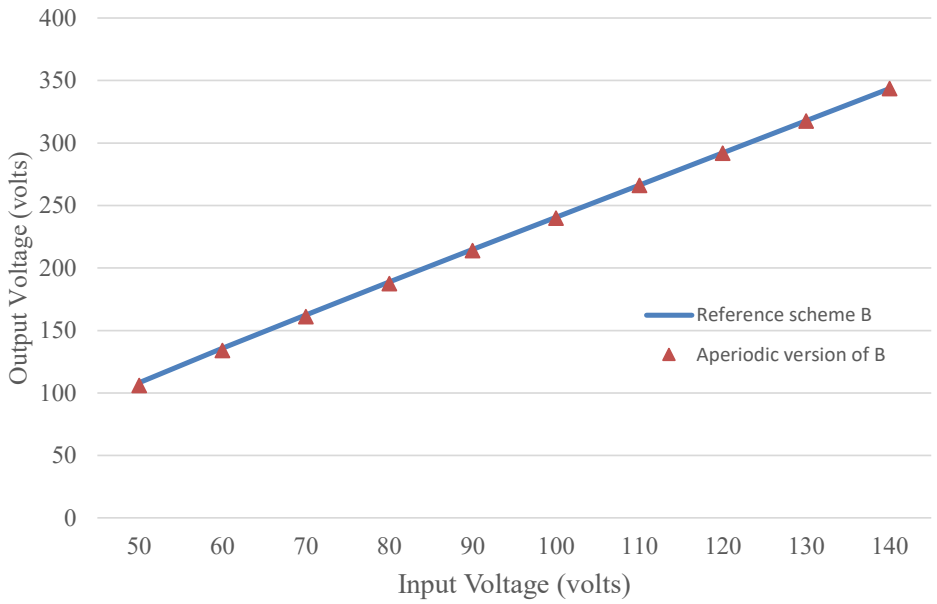


Figure 4.14. Voltage gain index for reference modulation scheme B and its aperiodic version.

Fig. 4.15 presents the efficiency vs load index for the modulation scheme presented A compared to its aperiodic version. There is no adverse impact on the efficiency vs load behavior.

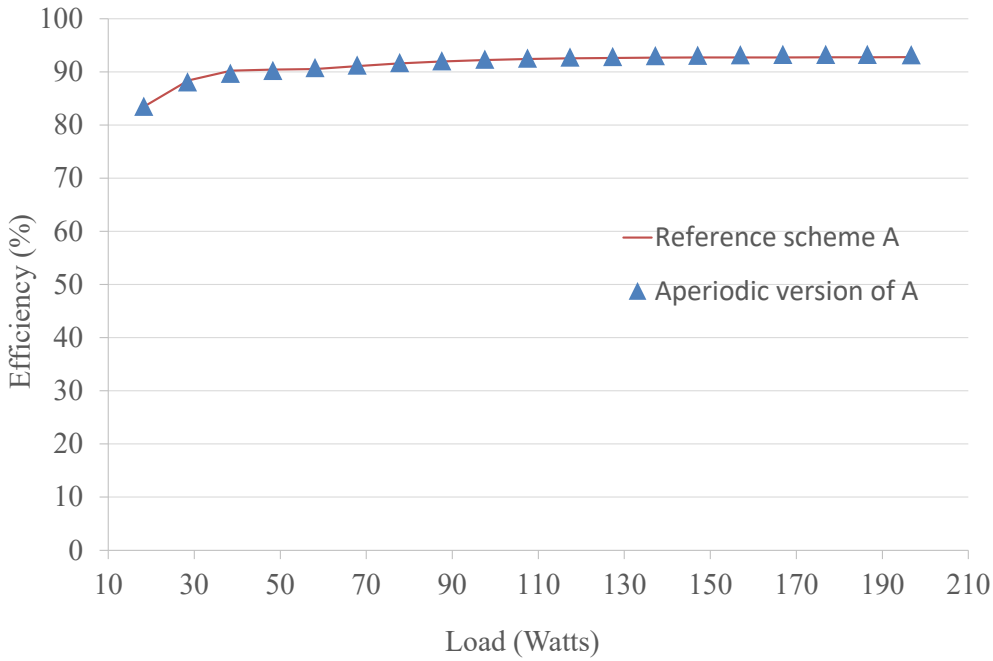


Figure 4.15. Efficiency vs load index for reference modulation scheme A and its aperiodic version for fs=100 kHz.

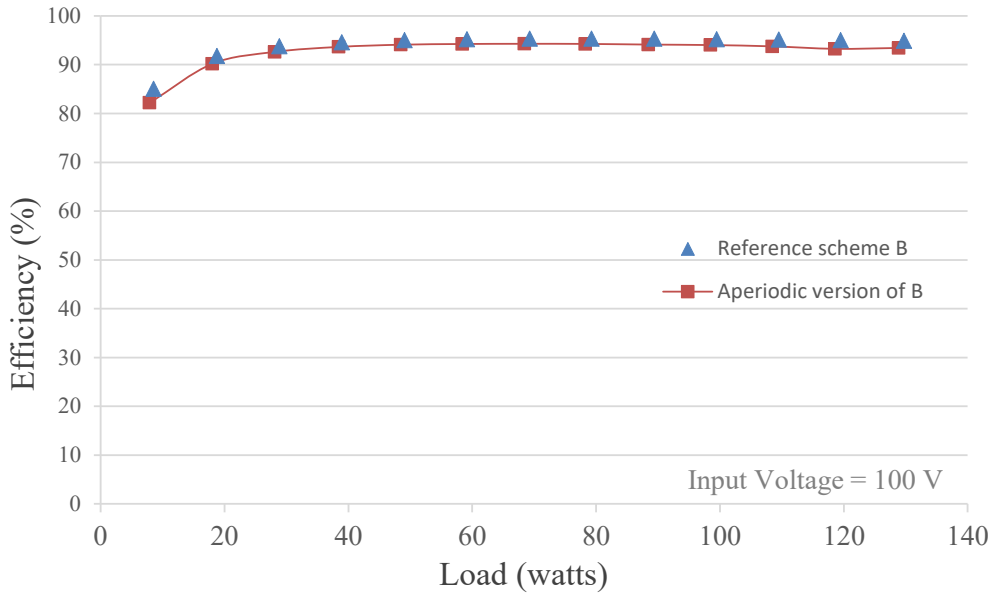


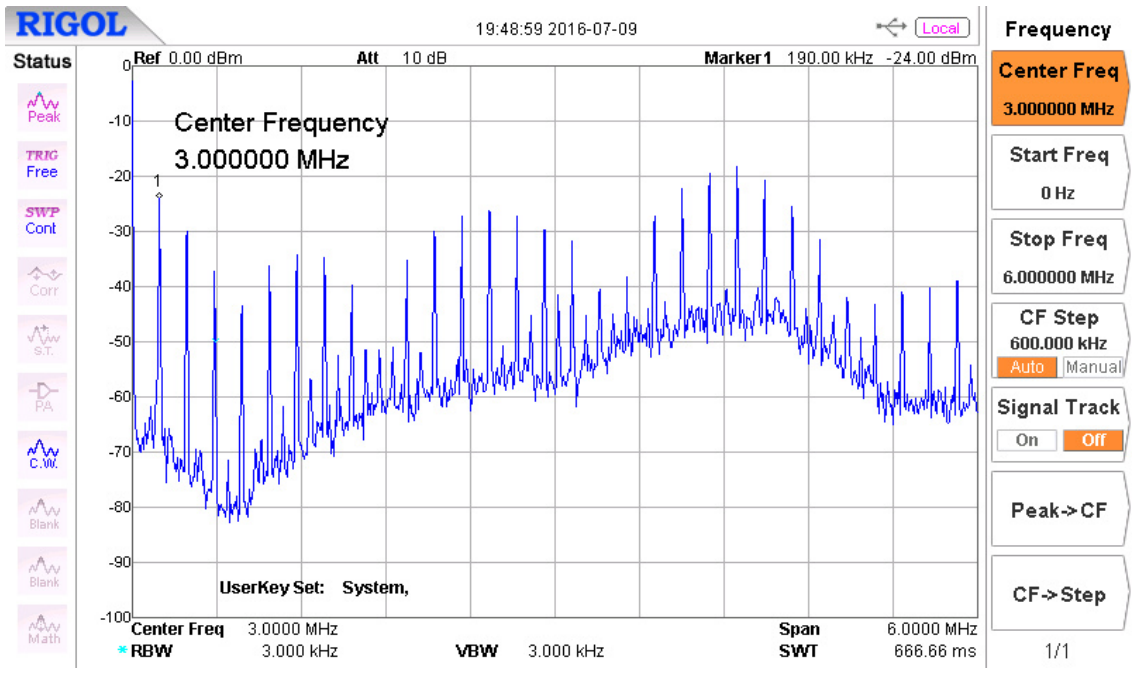
Figure 4.16. Efficiency vs load index for reference modulation scheme B and its aperiodic version for fs=24 kHz.

For reference modulation scheme B, as the pulse-position varies and causes an additional zero-state to be added in various switching cycles (evident from Fig. 4.12 b), this adds up to additional switching states and therefore increases the associated losses. For this reason a minor impact on the efficiency is indicated in Fig. 4.16. There was <1% reduction in converter efficiency with the proposed aperiodic modulation method, most likely associated with additional switching transitions of the two lower HEMTs in the H-bridge.

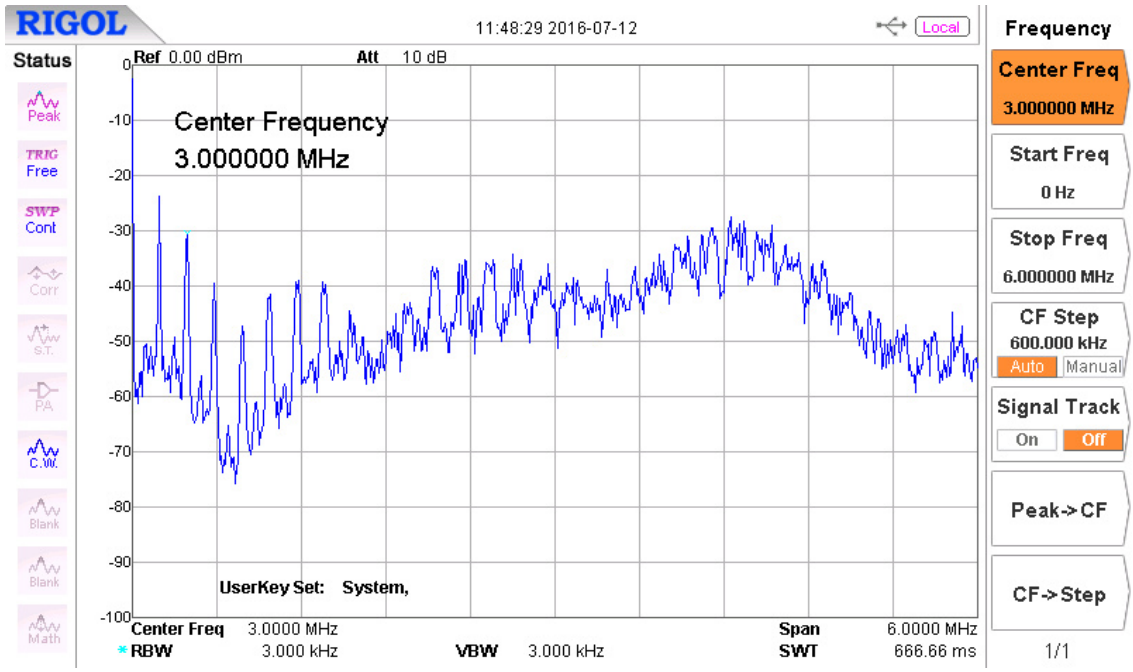
4.5.4. EMI Analysis

The EMI spectra for the reference modulation schemes and their aperiodic versions are presented in this section. To measure the conducted EMI, the qZS supply voltage was set to 100 volts and a programmable electronic DC load set to 100 watts was connected to the qZS converter output. A line impedance stabilization network (LISN) [15] was inserted between the DC source and the power converter input. The EMI spectra were displayed

over a broad bandwidth using a RIGOL DSA815 RF spectrum analyzer. The EMI measurement setup is shown in Appendix A.5.

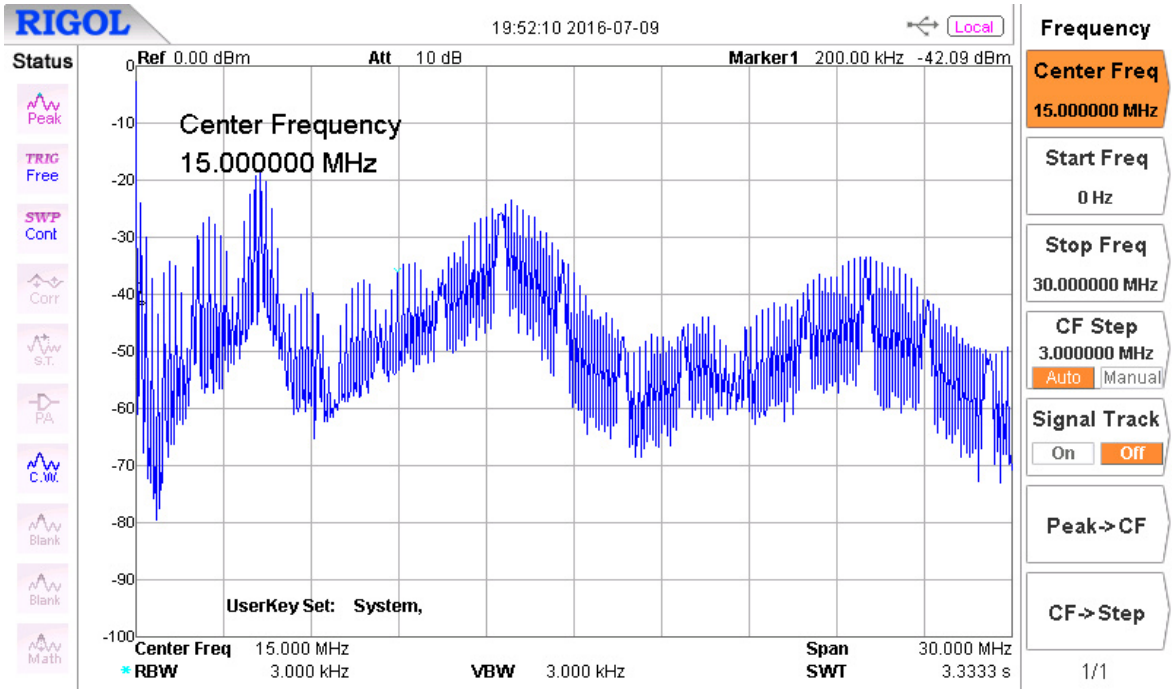


a)

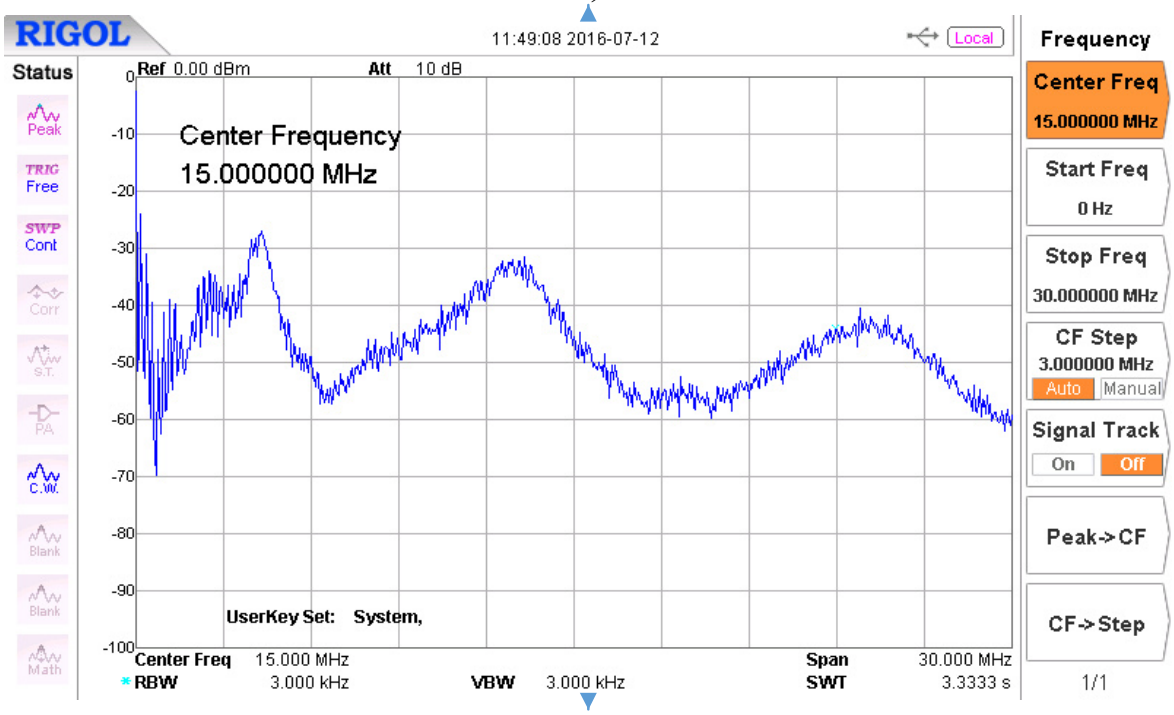


b)

Figure 4.17. Spectrum of conducted EMI [0 ~ 6 MHz] for: a) Reference scheme A, and b) its aperiodic version.



a)

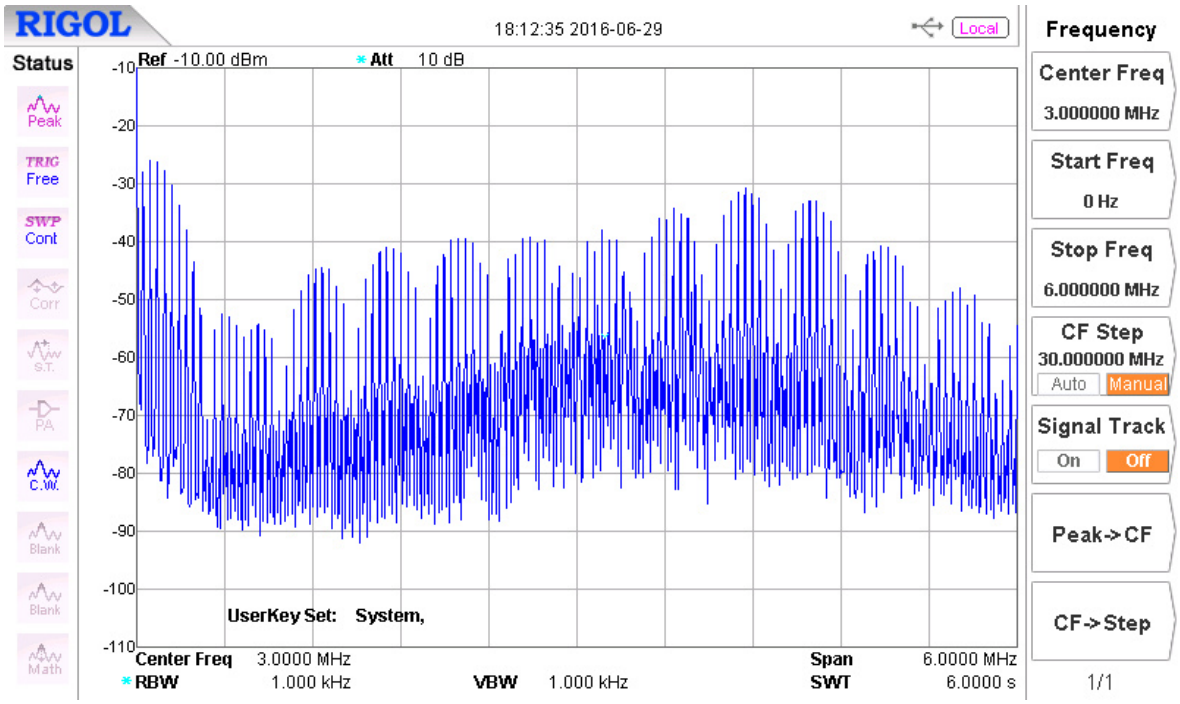


b)

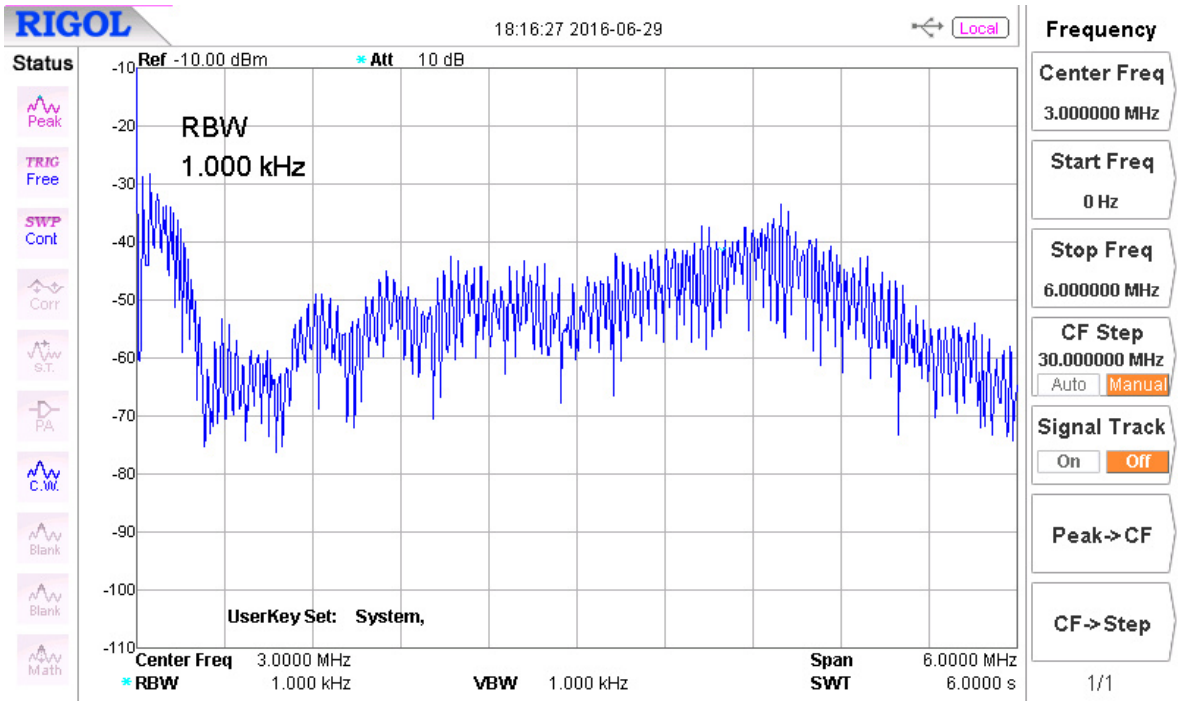
Figure 4.18. Spectrum of conducted EMI [0 ~ 30 MHz] for a) Reference scheme A, and b) its aperiodic version.

For reference modulation scheme A, the EMI spectra concerning both the reference schemes and its aperiodic version are shown are Figs 4.18 and 4.19, respectively. The

difference between these two spectra is the range of the frequency for which the EMI is measured.

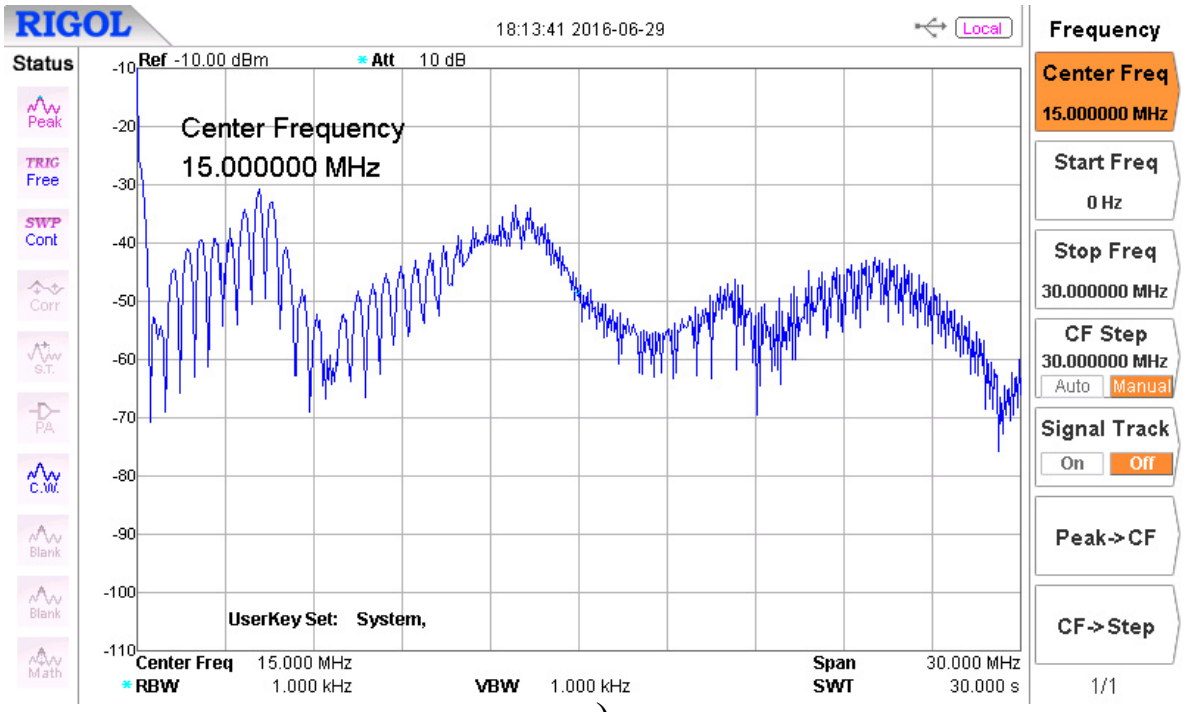


a)

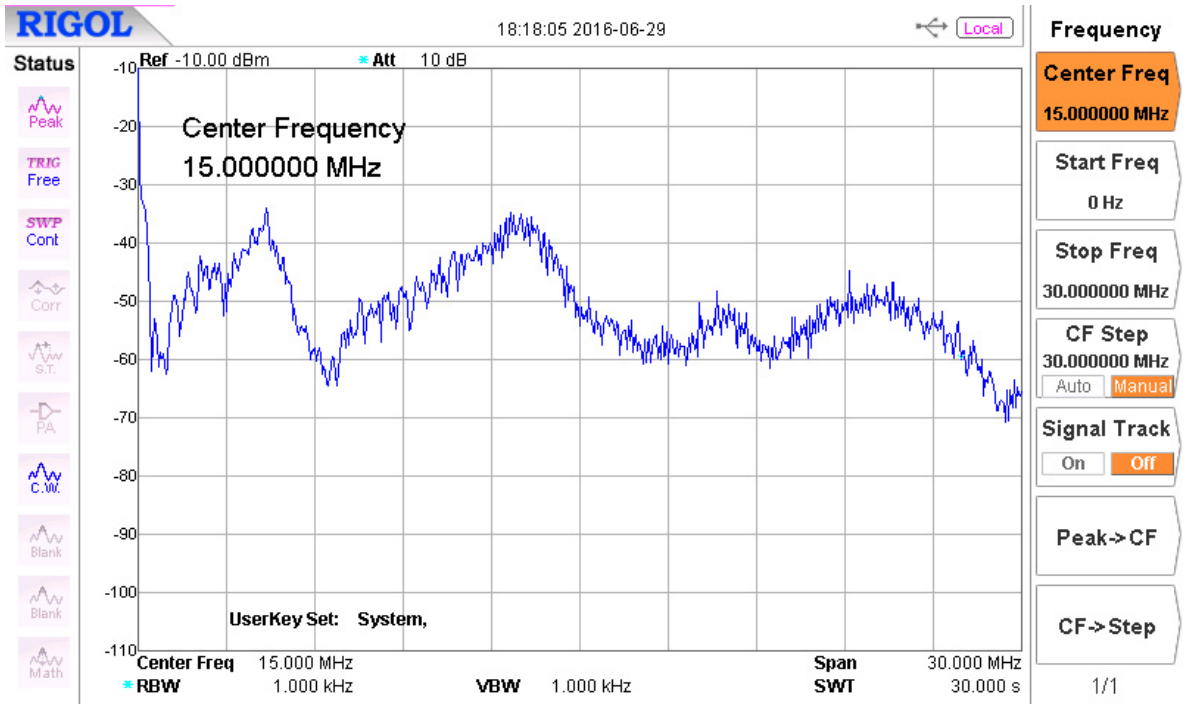


b)

Figure 4.19. Spectrum of conducted EMI [0 ~ 6 MHz], for: a) Reference scheme B, and b) its quasi-periodic version.

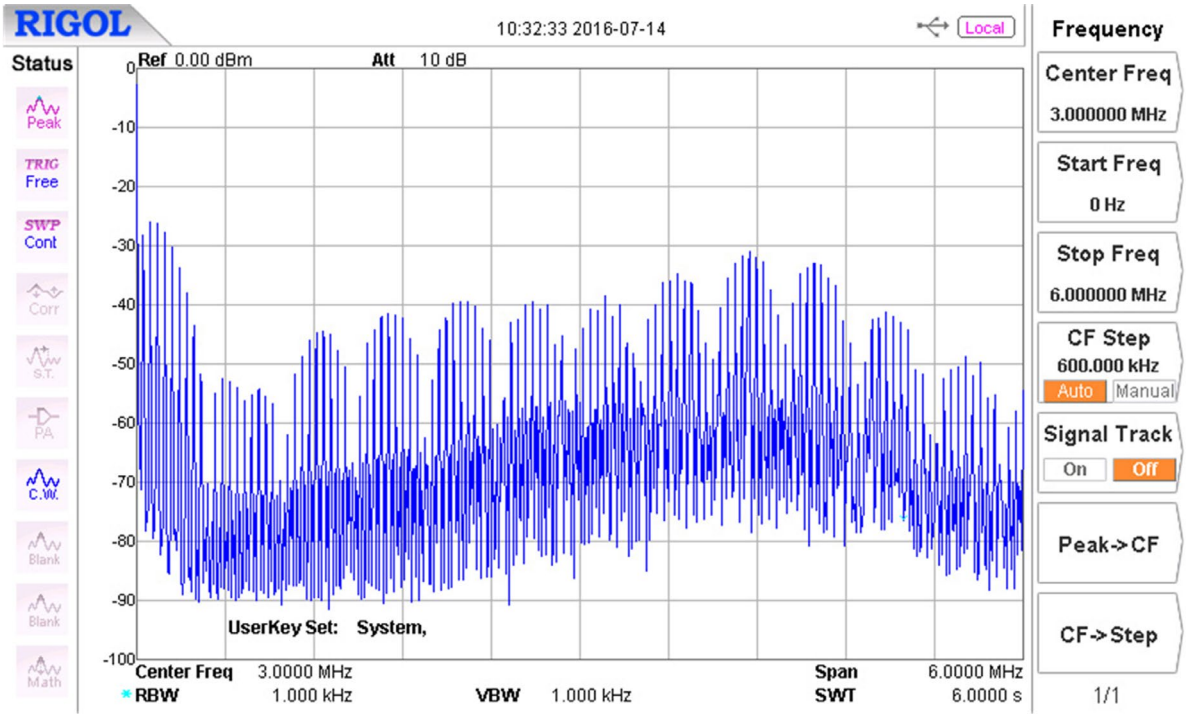


a)

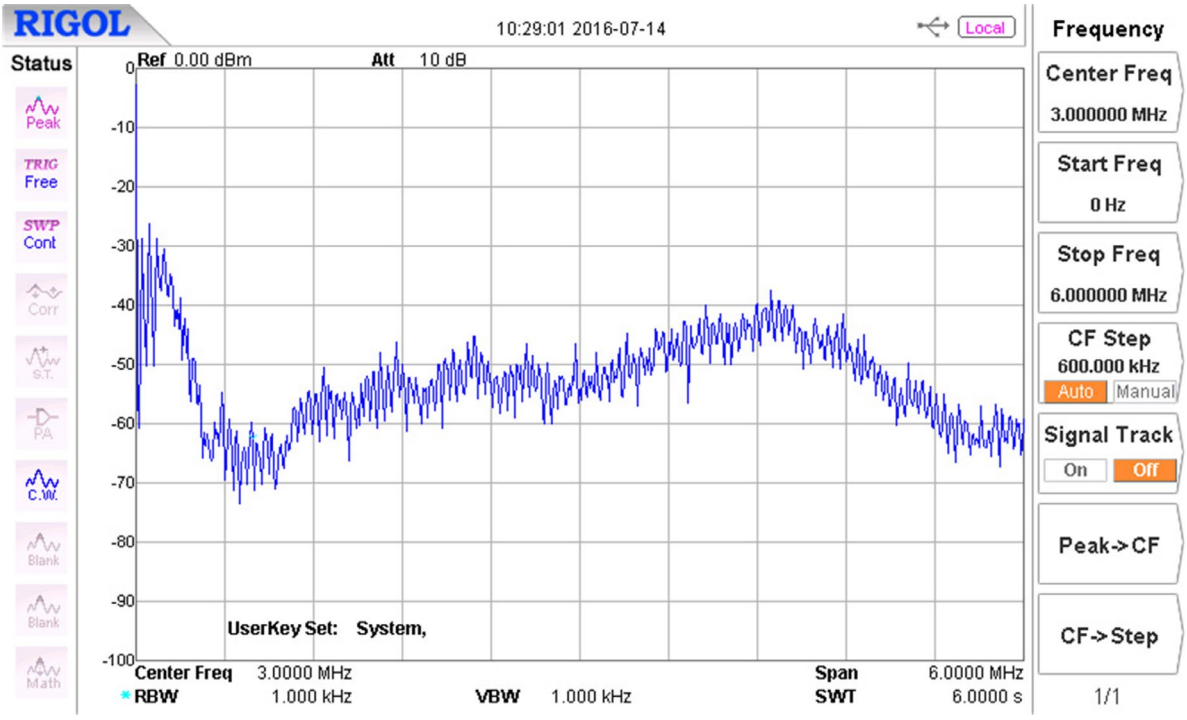


b)

Figure 4.20. Spectrum of conducted EMI [0 ~ 30 MHz], for: a) Reference scheme B, and b) its quasi-periodic version.



a)



b)

Figure 4.21. Spectrum of conducted EMI [0 ~ 6 MHz], for: a) Reference scheme B, and b) its aperiodic version.

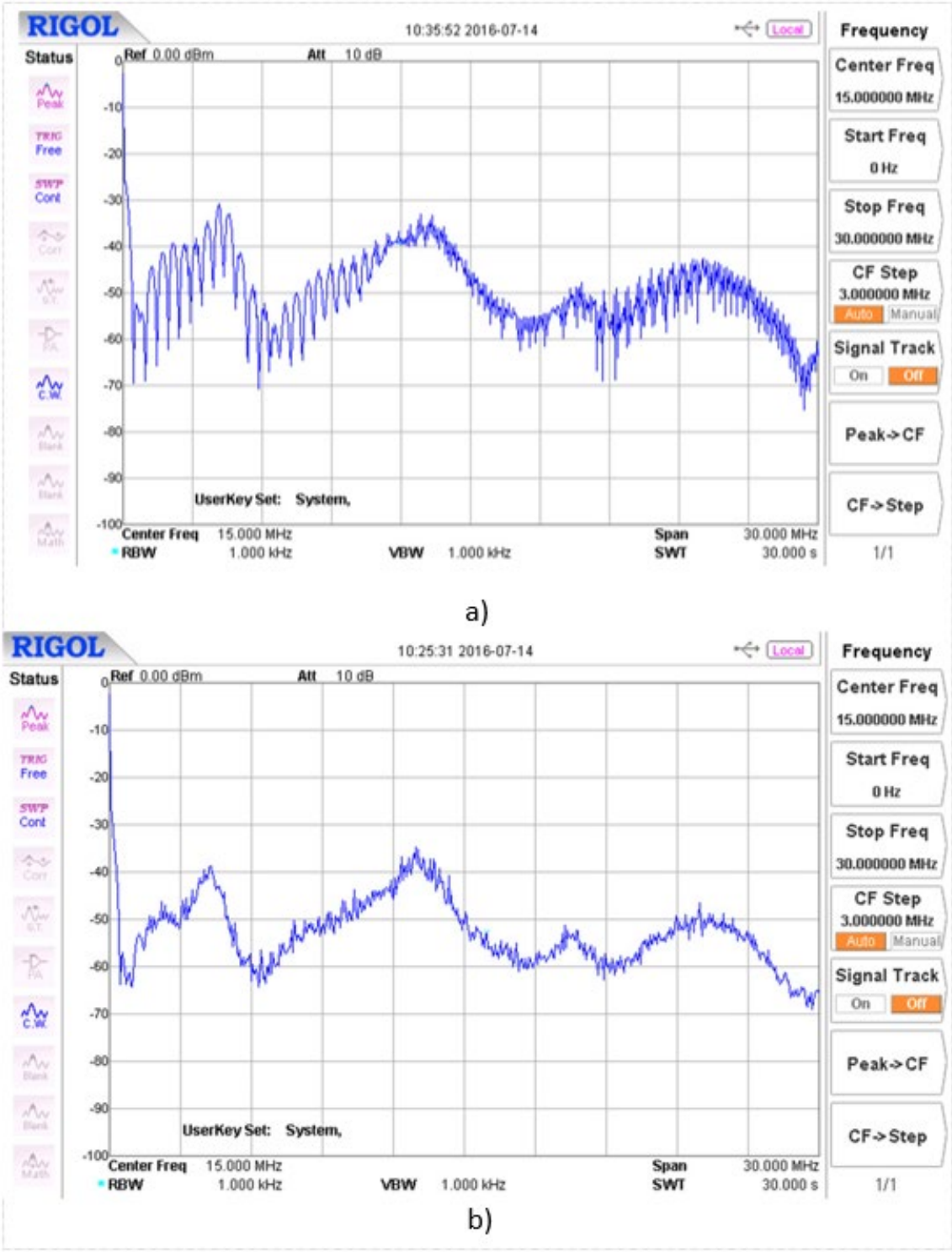


Figure 4.22. Spectrum of conducted EMI [0 ~ 30 MHz], for: a) Reference scheme B, and b) its aperiodic version.

The EMI suppression is evident from Figs 4.18 and 4.19. It can be seen that a suppression of ~ 9 dB exists through a broadband range. Moreover, the EMI suppression for the case of quasi-periodic approach has also been observed. For the quasi-periodic modulation scheme,

since the switching pattern repeats (evident from Fig. 4.10 b), the expected EMI suppression is expected to be less; this is depicted by the EMI spectra shown in Figs 4.20 (0~6 MHz) and 4.21 (0~30 MHz); and a suppression of 6 dB is evident.

Finally, the EMI results for the aperiodic version concerning the reference modulation scheme B are presented in Fig. 4.22 and Fig. 4.23, respectively. An EMI suppression of ~10 dB is evident throughout the broadband spectrum.

4.6. Summary and Conclusions

Table 4.2. Comparison of quasi-periodic and aperiodic modulation in terms of efficiency, voltage gain, regulation and EMI suppression

Modulation scheme	Comparison parameters	Ref A	Ref B
Quasi-periodic	Efficiency	Better efficiency as there are only two switching states.	Better efficiency as compared to the aperiodic modulation because of repetition of switching pattern (Fig. 4.10b)
	Voltage gain	The shoot-through states are dependent on the active states, hence there is a limitation.	Independence of shoot-through states allows flexible voltage gain
	Voltage regulation and compensation	No zero-state available, hence poor voltage regulation and compensation	Availability of zero-state allows this ability
	EMI suppression	Less, as compared to aperiodic modulation	Less, as compared to aperiodic modulation
Aperiodic	Efficiency	Better efficiency as there are only two switching states	Comparatively low efficiency, as there is an additional zero-state (Fig. 4.12b).
	Voltage gain	The shoot-through states are dependent on the active states, hence there is a limitation.	Independence of shoot-through states allows flexible voltage gain
	Voltage regulation and compensation	No zero-state available, hence poor voltage regulation and compensation	Availability of zero-state allows this ability
	EMI suppression	Better as compared to quasi-periodic modulation	Better as compared to quasi-periodic modulation

In this chapter, a simple method for generating aperiodic hybrid pulse modulation to suppress EMI in a qZS DC-DC converter has been described. The method uses two anharmonically-related waveforms to produce an aperiodic sawtooth carrier signal, which can subsequently be used to generate one or more coordinated pulses modulated aperiodically in width and position within a constant switching cycle. The modulation technique and EMI suppression were validated experimentally on a quasi-Z-source DC-DC converter with four hybrid-GaN HEMTs driven by an FPGA. Up to 10 dB suppression of the peak conducted EMI in the converter's supply circuit was measured with negligible impact on the converter's voltage gain or efficiency.

A comparison showing the applicability and limitations of the quasi-periodic and aperiodic modulation methodology applied to the two reference schemes is shown in Table. 4.2. Generally, aperiodic modulation provides better EMI suppression, but there are several other parameters which may add up to decide the trade-offs. These shall be considered to evaluate a power converter's performance.

To the best of the author's knowledge, this is the first report on an aperiodic pulse-modulation method for EMI suppression, implemented in an H-bridge-based impedance-source converter, in which "shoot-through" states must be taken into account. The method for generating the aperiodic hybrid pulse modulation is generic, and is expected to be equally effective with other converter topologies.

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Chapter 5

A Novel Common-Ground Transformerless PV Inverter and Its EMI Analysis

In the previous two chapters, the objective of EMI suppression was achieved by aperiodic modulation of the switching signal(s). Two different types of DC-DC converters were used as a prototype for the EMI analysis. In this chapter, a new topological contribution is presented which helps to prevent the high EMI noise. Recently, switched-capacitor-based power conversion techniques have been reported [84]–[88] which can go along with GaN switches very well to achieve high power density and efficiency due to low conduction losses offered by the GaN switches. From the point of view of GaN offering negligible $R_{DS(On)}$, the associated capacitor charging and discharging phenomenon leads to higher inrush current spikes, hence adding to the EMI. In this chapter, a novel DC-AC inverter topology is presented [89] which utilizes a double-charging process for the storage of energy, leading to

lower EMI. Furthermore, the concept of aperiodic modulation is applied to this topology for further suppression of EMI.

This chapter is structured as follows: Firstly, a literature survey on transformerless common-ground inverters is presented followed by an introduction to a novel transformerless inverter topology. Secondly, the switching states of the proposed topology are presented to systematically understand the principle of operation. A comparison of the proposed topology with other related topologies, and various design guidelines are included. Finally, an aperiodic modulation approach is applied to attain EMI suppression. Various simulation and experimental results are given to validate of the proposed topology and EMI suppression methodology.

5.1. Literature Survey and Motivation

Grid-connected inverters for low-power photovoltaic (PV) systems usually require single-phase inverter systems. These systems had an enormous growth in recent years due to the fall in PV module prices, government policies to promote clean energy, and advances in power electronics and semiconductor technology. There has been significant progress in the research and development of new power converter topologies for PV applications. A strong trend can be seen in terms of improving the reliability, power density, efficiency and operability of PV systems [90]. 2016 was a record year for solar as the solar power capacity worldwide exceeded 300 GW after the 200 GW and 100 GW marks were crossed in 2015 and 2012 respectively [91].

A single-phase DC-AC inverter is used in low power (<5 kW) single-phase grid-connected applications. This usually comes with galvanic isolation provided by a line-frequency or a

high-frequency (HF) transformer as a part of the inverter topology which can also provide voltage transformation. As the research focuses increasingly on compact and portable solutions by utilizing advances made in power electronics and semiconductor technologies, conventional iron and copper-based transformers are not preferred because they add to the weight and cost of the power converters whilst reducing the power density and efficiency. Therefore, transformerless inverter-based topologies are preferred for reducing the cost and weight with improved efficiency and power density. However, with the exclusion of a transformer from the circuit, the galvanic isolation is lost, which reciprocates to a common-mode current due to a high frequency Common-Mode Voltage (CMV).

The CMV is the average value of the voltages between the output terminals and the common reference of the inverter [92]. This CMV depends on various aspects of the inverter circuit and its modulation strategy, leading to the leakage current. The major cause of this leakage current is the presence of naturally occurring capacitance between the PV frame and its ground [93], [94]. Its value depends on various factors such as atmospheric conditions, size and structure of the PV system [95]. The leakage current adds to the grid-current harmonics and system losses. Additionally, conducted and/or radiated electromagnetic interference (EMI) is caused, which is not desired and needs to be kept within allowable limits as per various electromagnetic compatibility (EMC) standards. Most importantly, the leakage current leads to safety concerns and hence it must be kept under the recommended limits [21], [90], [96], [97]. Leakage current can be eliminated by keeping the CMV constant at all times during the inverter's operation.

Various transformerless inverter topologies have been proposed to achieve higher efficiencies and lower leakage currents. These include decoupling of the dc side from the ac

side by clamping the CMV during freewheeling states [96], [98]–[101] or using common-ground configurations [102]–[107]. The CMV-clamping-based topologies help to reduce the leakage current at the expense of a relatively large number of active and passive components, which adds to the complexity, cost and size of the inverter. Moreover, as the decoupling of the ac and dc sides is done employing additional switches, the leakage current may not be completely eliminated, as the switch parasitic capacitance still exists [106]. Additionally, the conduction losses increase in such topologies, as the number of devices operating in active states is larger. Therefore, common-ground type inverter topologies are preferred, which theoretically eliminate the leakage current completely. In addition, the component count is less, which increases efficiency and reduces the cost.

Common-ground transformerless topologies employing a capacitor as a virtual DC bus constitutes a popular concept in which the negative output voltage is generated by utilizing this capacitor. This idea was first introduced in [106] and has evolved to yield numerous improved topologies in recent years. The novel topologies presented in [107] offer minimal leakage currents with high efficiencies, but the inrush-current phenomenon during the capacitor charging state [108] has not been addressed. The capacitor charging current becomes crucial when the virtual DC bus capacitor is charged directly via a switch. A θ-converter is presented in [104] which offers minimal leakage current, output voltage ripple and total required capacitance, but the reported efficiency is comparatively low. A novel inverter topology is reported in [103] with an increased number of active and passive components, which increases the cost.

The concept of a “charge pump” in the transformerless inverter topologies is explained in [109], in which some switches endure high current peaks due to the capacitor charging

phenomenon. An improved "flying inductor"-based topology is presented in [110] which has buck-boost capability, but the switch stress and associated losses are increased with the voltage conversion ratio, so there is relatively poorer efficiency. Various multilevel inverters are also introduced [94], [111] which can curtail the leakage current, however such topologies usually require higher levels of input dc-link voltages along with additional switches. Several common-ground transformerless inverter topologies are presented, and each topology comes with different advantages and disadvantages. An optimal common-ground transformerless topology, therefore, is based on the following attributes:

i. Minimal number of active and passive components.
ii. Smaller filter requirement.
iii. Flexibly chargeable virtual DC bus capacitor for intermediate energy storage to be utilized during the provision of negative power cycle.
iv. Minimal leakage current or constant CMV.
v. Low switch stress.
vi. Peak output voltage equal to the input dc-link voltage; and
vii. Controlled capacitor charging current.

The topology presented in this chapter specifically has a major advantage over the common-ground transformerless topologies mentioned in [107] in terms of offering a low inrush current (due to the capacitor charging phenomenon). This is a major issue associated with the capacitor charging phenomenon. From the perspective of EMI, this topology is beneficial because of an inductor present in the topology which lessens the EMI as compared to switched capacitor circuits.

This chapter is organized as follows: Section 5.2 describes the proposed topology and its principle of operation along with its various operation modes. Section 5.3 has a comparative analysis of the proposed topology and discusses various important parameters related to the design and operation of the topology. Section 5.4 describes the implementation methodology of an aperiodic sinusoidal pulse-width modulation (SPWM), which can benefit EMI suppression. Simulation and experimental results for a 1 kW inverter are presented in Section 5.5 and the chapter is concluded in Section 5.6 with a summation of the main themes covered here.

5.2. Proposed Topology and Principle of Operation

The proposed topology and its modulation pattern are presented in Fig. 5.1. It contains 5 switches, one diode, one capacitor, one small inductor and a small filter at the output stage. A simple unipolar SPWM technique is used to modulate the inverter to produce the required operation, which further minimizes the output current ripple, switching loss and output LC filter requirements. Additionally, the capacitor C_O is charged through a dedicated switch S_C which is switched at a high frequency, which in-turn can give flexibility in terms of the dimensions of L and C_O. C_O is utilized as a virtual DC bus [106] to provide the negative power cycle of the inverter.

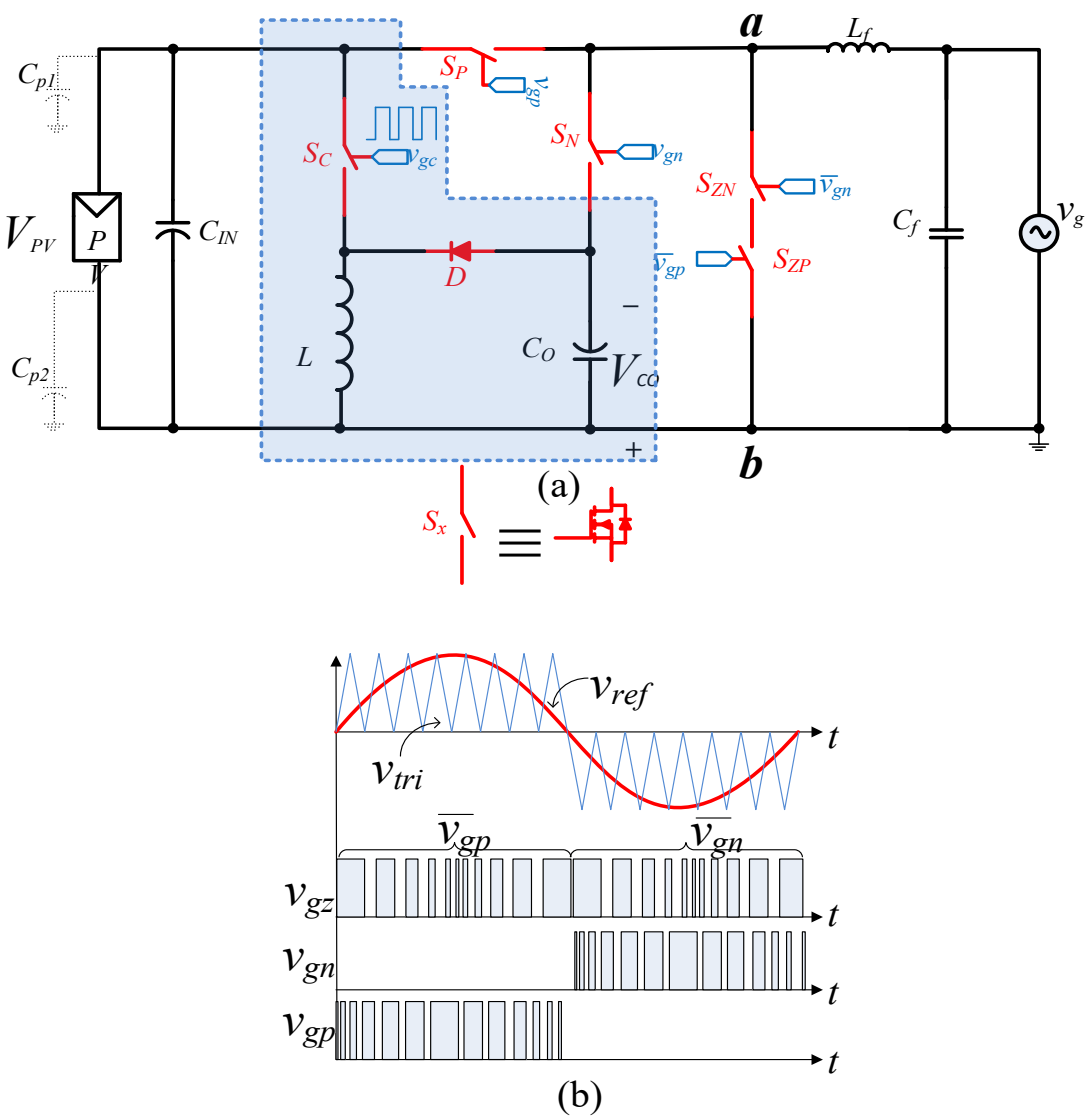


Figure 5.1. (a) Proposed transformerless common-ground topology and (b) corresponding unipolar SPWM.

5.2.1. Principle of Operation of Proposed Inverter Topology

The proposed topology utilizes a capacitor C_O as a virtual DC bus to provide the negative power cycle of the inverter. This capacitor C_O, is charged by a dedicated switch S_C, which switches regardless of any switching states of the inverter, and therefore this phenomenon makes this topology more attractive since the capacitor continuously charges while it is supplying the negative power cycle of the inverter. The charging phenomenon is fairly simple

as C_O is charged through the inductor L by a double charging process as used in a classic buck-boost DC-DC converter, as shown in Fig. 5.2.

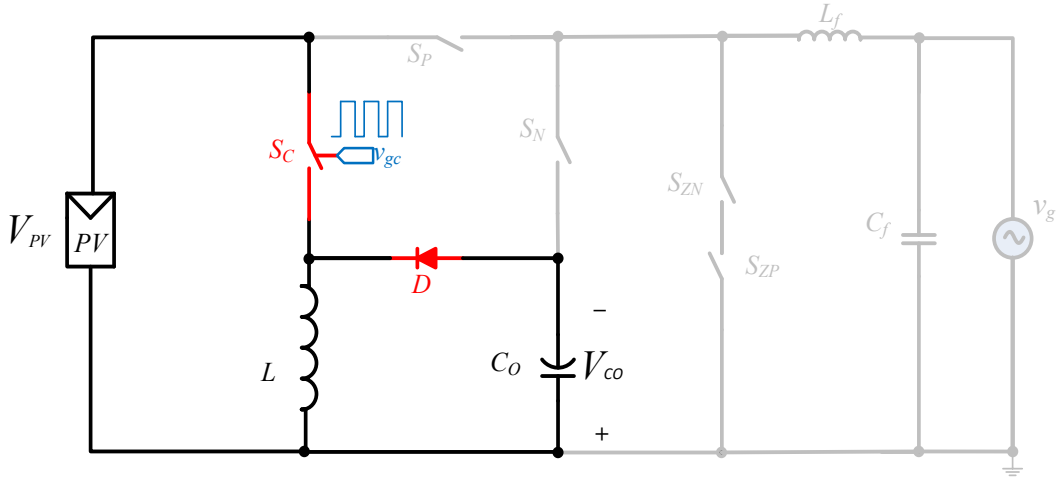


Figure 5.2. Charging of the virtual DC bus capacitor.

As illustrated in Fig. 5.2, energy is first stored in the inductor L and then in the second step, this stored energy is discharged into the capacitor. By using volt-second balance, the voltage across C_O can be expressed as

$$V_{CO} = V_{PV} * \left(\frac{d}{1-d}\right). \tag{5.1}$$

where d is the duty cycle of the switch S_C.

The switching condition of the diode D depend on the switching state of S_C:

$$D = \begin{cases} 0 & for\ S_C = 1, \\ 1 & for\ S_C = 0. \end{cases} \tag{5.2}$$

The rest of the topology consists of four active switches (S_P, S_N, S_{ZP} and S_{ZN}) and a small LC filter. These switches are modulated using a standard unipolar SPWM. The various switching states are explained in the next sub-section.

5.2.2. Operating States of the Proposed Topology

The operating states of the proposed inverter can be broken down into 3 switching states (positive, negative and zero), as indicated in Figs 5.3 ~ 5.6. Note that the red dotted line shows the active current path, the blue dotted line shows the charging current path for C_O, which always passes through S_C, and the violet dotted line represents the free-wheeling current path.

i) Positive Cycle (active)

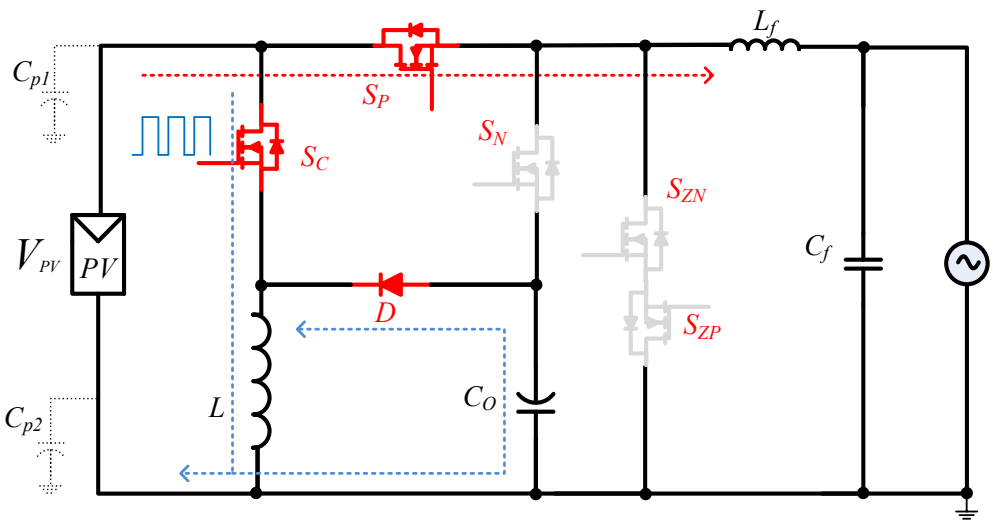


Figure 5.3. Positive Cycle active state of the proposed topology.

This operating state is shown in Fig. 5.3. In this state, the switch S_P switches in an SPWM manner to provide the positive power cycle of the inverter. The correct switching logic is implemented by comparing the positive half of the modulation signal with a triangular carrier signal. While the switch S_P is being switched to provide the positive half cycle of the inverter, the switch S_C keeps on switching at a higher frequency to precharge the capacitor for its utilization in the negative half cycle. The switches S_{ZP} and S_{ZN} remain off during this state. These switches are only used to provide the zero-states so that a

unipolar voltage is created before the filter. The switch S_C and the diode D switch complementarily to each other in alliance with the double charging process. Moreover, only one switch (S_P) is being used to provide the positive voltage before the LC filter, carrying the positive load current, and hence there are minimal conduction losses are evident during this state.

ii) Positive Cycle (zero)

In this state (Fig. 5.4) the switches S_P and S_N are off while the switch S_{ZP} switches in a complementary manner to that of S_P during the positive cycle to provide the zero state. This creates a unipolar positive voltage before the filter which then generates a clean positive sinusoidal voltage and current provided to the load. During this stage, the body diode of S_{ZN} conducts in series with S_{ZP} to allow a path for the free-wheeling current and hence provide zero voltage across the filter. Moreover, the switch S_C, keeps switching and retains the capacitor C_O being precharged at the same voltage level same as V_{PV}. Since the capacitor is not utilized as a DC bus in the positive power cycle, a simple PI controller can be implemented to reduce the switching transients to lessen the associated losses.

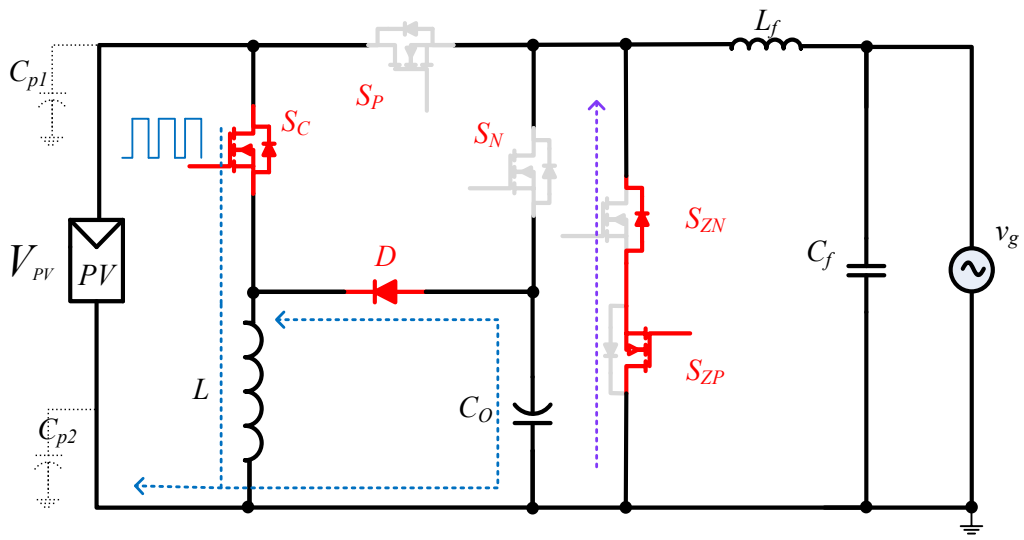


Figure 5.4. Positive Cycle zero state of the proposed topology.

iii) Negative Cycle (active)

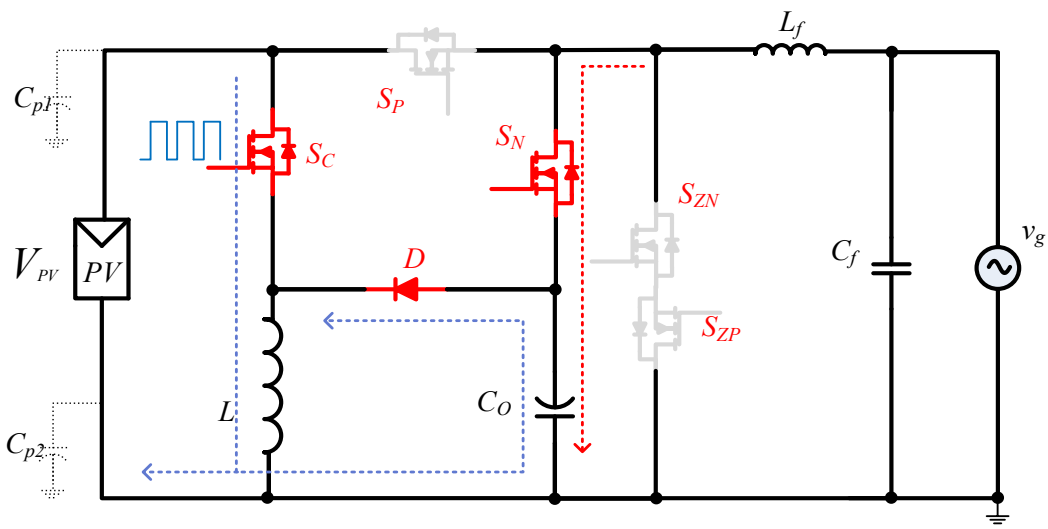


Figure 5.5. Negative Cycle active state of the proposed topology.

In this state, S_N is switched in an SPWM manner; this is implemented correctly by comparing the negative cycle of the modulation signal with the unipolar negative triangular carrier signal. While switch S_C is being switched at a high frequency regardless of any switching states, in this state the precharged capacitor C_O is utilized as a virtual DC bus [106] to provide the negative power cycle of the inverter. The switch S_P is off for this entire negative cycle. Since only one switch (S_N) is used to provide the negative voltage before the LC filter, this leads to lower conduction losses compared to the case of other common-ground transformerless inverter topologies [107]. Both of the switches S_{ZP} and S_{ZN} are off during this state.

iv) Negative Cycle (zero)

In this state, S_P and S_N are off while S_{ZN} switches in a complementary manner to that of S_N to provide a path for the free-wheeling current through the body diode of switch S_{ZP}. This creates a zero voltage before the filter, hence a unipolar negative voltage is created

before the LC filter during the negative power cycle. The switch S_C keeps on charging the capacitor C_O. As the capacitor is used as a DC bus to provide the negative power cycle, a constant voltage equal to V_{PV} is required to be maintained by C_O, as the peak amplitude of the negative power cycle depends on V_{CO}. A simple PI controller can be utilized to ensure that the power drain from the capacitor is balanced by the charge being filled into it, governed by switch S_C.

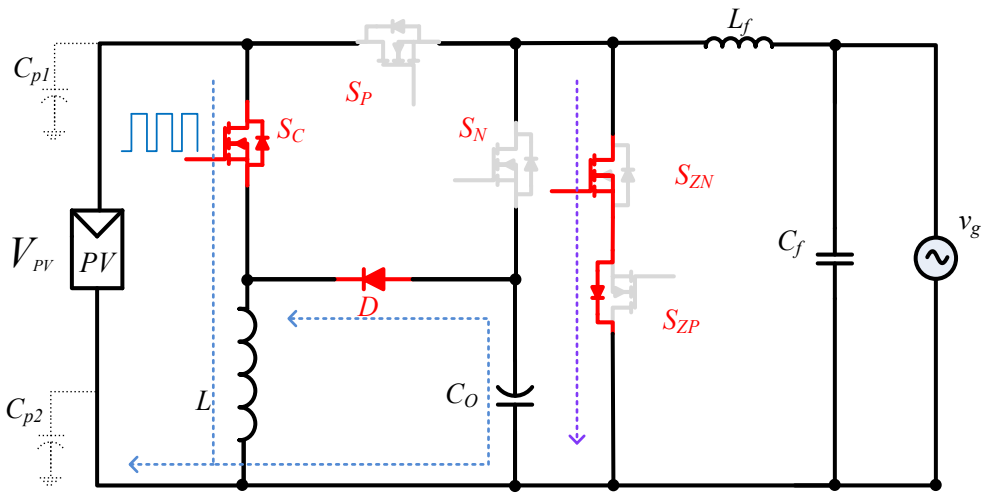


Figure 5.6. Negative Cycle zero state of the proposed topology.

Table 5.1. Summary of the switching states of the proposed topology.

	S_P	S_N	S_{ZP}/D	S_{ZN}/D	S_C
Positive (active)	1	0	0/0	0/0	X
Positive (zero)	0	0	1/0	0/1	
Negative (active)	0	1	0/0	0/0	
Negative (zero)	0	0	0/1	1/0	
X= 0/1, independent of other variables					

The aforementioned operating states are summarized in Table. 5.1. These states repeat in every consecutive power cycle to create a unipolar positive and negative voltage before the LC filter. This chopped DC voltage is then filtered out of the LC filter to provide a clean sinusoidal voltage and current to the load. Note that the switching frequency and state of the switch S_C are independent of the operating states listed in Table. 5.1. This helps to

independently control the voltage across the capacitor, and hence any offset in the output ac voltage and current is eliminated. The presented topology, being modulated with SPWM, leads to small filter requirements, low switching losses, low EMI and low ripple in the output current. Compared with other transformerless inverter topologies, this topology can be implemented using two industry-standard half-bridge modules, which has various benefits, for example increased power density, quick and cost effective implementation. Moreover, since WBG-based HF power converters are very attractive due to the fact that they offer a small size, small filter requirements, high efficiency and portability. Consequently, customized half-bridge modules such as [112] can be used to implement this topology to achieve contemporary benefits.

5.3. Comparative Analysis and Design Guidelines

The following sub-section compares the proposed topology with similar transformerless common-ground topologies to analyze its merits and demerits. Various design guidelines and essential insights related to the proposed topology are presented in the following sub-sections for better understanding and easy operation and implementation.

5.3.1. Comparison with Similar Topologies

Table 5.2 presents a comparative overview of the proposed topology, with other various other topologies while considering key parameters. These include the number of active and passive components required to build the inverter topology, the number of semiconductor devices in the load current path, input voltage requirement, output filter requirements, inrush current considerations, voltage stress across the active switches and leakage current,

etc. Although there are numerous common-ground transformerless topologies, the comparison has been focused on topologies which utilize a capacitor as an intermediate energy storage element.

Table 5.2. Comparison of Proposed Topology with various other transformerless topologies.

Transformer-less inverter topology with intermediate energy storage capacitor	Number of components				No. of switches in the load current path		V_{in} (V)	Leakage Current (mA)	Output Filter			Voltage stress on semiconductor or switches	Inrush current spikes **	Efficiency (%)
	S	D	C*	L	Positive Cycle	Negative Cycle			Lf1 (mH)	Lf2 (mH)	Cf (μF)			
Proposed topology [89]	5	1	2	1	1	1	400	≈ 0	0.35	-	2.2	$V_{SP} = V_{SN} = V_{SZP} = V_{SZN} = 2V_{in}$, $V_{SC}=V_{in}$	Low	95.2 @1.6 kVA
Type-I [107]	4	1	2	0	2	2	400	≈ 0	0.35	-	2.2	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{in}$	High	99.2 @ 1 kVA
Type-II [107]	4	1	2	0	1	2	400	≈ 0	0.35	-	2.2	$V_{S1} = V_{S2} = V_{S4}$= Vin, $V_{S3} = 2V_{in}$	High	99.25 @1 kVA
Type-III [107]	4	0	2	0	1	1	400	≈ 0	0.8	-	10	$V_{S1} = V_{S4} = V_{in}$, $V_{S2} = V_{S3}$ = 2Vin	High	97.8 @1 kVA
Flying capacitor [113]	4	0	3	0	2	2	≥ 800	NA	3	-	2.2	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = 3V_{in}$	High	NA
Virtual DC bus [114]	5	0	2	0	2	2	400	≈ 0	8	0.8	0.34	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S3} = V_{in}$	High	95.2 @ 0.5 kVA
Extended H-6 type [115]	6	6	2	0	3	3	400	13	1x4	0.5x2	2.2	$V_{S1} = V_{S2} = V_{S4} = V_{S5} = 2V_{in}$, $V_{S3} = 2V_{S6}=V_{in}$	Low	98.2 @ 1kVA
Charge pump [109]	4	2	4	0	2	1	400	≈ 0	4	2	2.2	$V_{S1} = V_{S2} = V_{S3} = V_{in}$, $V_{S4}= 2V_{in}$	High	97.4@0.5 kVA
Flying Inductor [110]	5	0	2	2	2	2	100	≈ 0	0.3	-	2.2	$V_{SX} > V_{in}$ ***	Low	92.5 @ 200 kVA

Where, S= Switch, D= diode, C= Capacitor, L= Inductor, Lf1, Lf2, Cf= passives associated with the output filter, Vin= Input voltage for ~230 V applications, NA= Not application or not available in the publication, *Including input DC capacitor(s), ** Inrush current analysis is based on the high charging current for the capacitor, *** Switch stress dependent on the boost factor.

5.3.2. Virtual DC Bus Capacitor Sizing

The virtual DC bus capacitor is important especially during the negative power cycle, so subsequently the capacitor must be sized appropriately for a seamless transition of the ac waveform from positive to negative cycle. The size of the capacitor is a function of the average current drained out of it during the negative power cycle, the carrier switching frequency for the SPWM, the DC link voltage and the voltage ripple requirements. To begin the analysis, the following assumptions are made: i) the current (negative part) provided through C_O forms a pure sinusoidal waveform after passing through the LC filter; and ii) the capacitor is fully charged before the negative cycle starts (with or without the PI control).

The control strategy is based on simple SPWM strategy (by comparing a bipolar carrier signal with a reference sinusoidal signal, as shown in Fig. 5.2b). The reference signal $v_{REF}(\theta)$ can be expressed as:

$$v_{REF} = m\sin(\theta), \tag{5.3}$$

where m is the modulation index and $\theta = \omega_C t$. ω_C is the angular frequency which is equal to $2\pi f_{grid}$. Note that f_{grid} is 50/60 Hz as per the standards. The RMS value of the output voltage for S_C being switched at a 50% duty cycle is given as:

$$V_{OUT} = \frac{m\,V_{PV}}{\sqrt{2}}. \tag{5.4}$$

From (5.1),

$$\theta = \sin^{-1}\left(\frac{1}{m}\right) + \pi. \tag{5.5}$$

The voltage ripple on a capacitor (ΔV_C) is estimated by the maximum discharging time ($t_{DIS\,(max)}$), the average current (I_{avg}) and the size of the capacitor:

$$\Delta V_C = \frac{I_{avg}\,.\,t_{DIS\,(max)}}{C_O} \tag{5.6}$$

The discharging time can be intuitively represented as:

$$t_{DIS\,(max)} = \frac{m\pi}{\omega_{SPWM}}, \tag{5.7}$$

where m implies the maximum discharge time and ω_{SPWM} is the angular frequency, equal to $2\pi f_{SPWM}$. Note f_{SPWM} is the carrier frequency used for generating the SPWM signals.

The average current through the capacitor (I_{avg}) is given by

$$I_{avg} = I_{L(avg)} * t_{SPWM}, \tag{5.8}$$

where $I_{L(avg)}$ is the average current flowing through the inductor L, given as:

$$I_{L(avg)} = \frac{1}{\pi}\int_{\pi}^{2\pi} i_C(\theta)\, d\theta. \tag{5.9}$$

Here, $i_C(\theta)$ is same as the output current, given as:

$$i_C(\theta) = i_{OUT}(\theta) = I_P \sin(\theta - \phi), \tag{5.10}$$

where ϕ is the power factor angle.

Solving equation (5.6) for finding the value of C_O for a 20% allowable ripple across the DC-bus capacitor gives:

$$C_O = \frac{20\sqrt{2}\,\pi m\, P_{OUT}}{V_{grid}\,\omega_{SPWM}^2}, \tag{5.11}$$

where P_{OUT} is the output power and V_{grid} is the RMS value of the grid-side voltage.

5.3.3. Common-mode Behavior and Leakage Current

The common-mode voltage (v_{CM}) and leakage current (i_{CM}) analysis of the proposed topology is presented in this section. An equivalent model for the common-ground transformerless inverter topology presented here is shown in Fig. 5.7. Z_G corresponds to the ground resistance, which is ~ 5 Ω as per standards [116] and the naturally occurring parasitic capacitance between the photovoltaic (PV) panel and ground (C_{PV}) ranges from tens of nF up till μF. The value of C_{PV} depends on various factors such as atmospheric conditions, the size and the structure of the PV system, etc. Therefore 100 nF/kW can be used for various analyses [95].

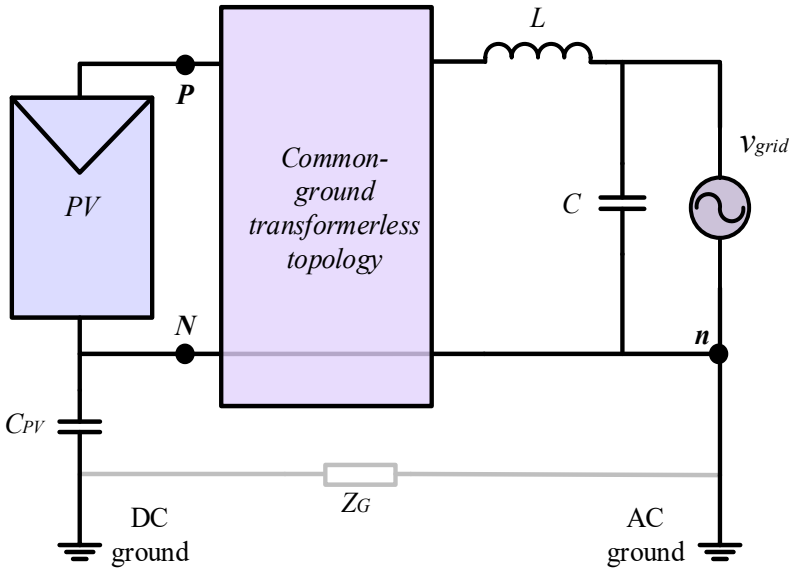


Figure 5.7. Equivalent model for analysis of common-mode voltage and leakage current for the proposed converter.

In principle, the common-mode leakage current i_{CM} is generated by a non-uniform or inconsistent common-mode voltage. The common-mode leakage current leads to increased system losses, reduction in the quality of the grid current, increased electromagnetic interference (EMI) and safety issues [98]. Consequently the solution to prevent i_{CM} in

transformerless inverter topologies is to keep the common-mode voltage constant. As per [117], the common-mode voltage (v_{CM}) is given as:

$$v_{CM} = \frac{(v_{Pn}+v_{Nn})}{2}, \tag{5.12}$$

where P and N are the positive and negative terminals of the PV panel respectively, and n corresponds to the ground terminal of the AC side. Referring to the proposed topology, since there is a common ground and N is literally shorted to n, in addition to the fact that the peak of the AC side is the same as the DC input, therefore $v_{Pn} = V_{PV}$ and $v_{Nn}= 0$. This leads to the common-mode voltage expression being simplified to:

$$v_{CM} = \frac{V_{PV}}{2}. \tag{5.13}$$

The above expression mathematically verifies there is no leakage current as v_{CM} is constant and contains no frequency-related components.

5.3.4. Voltage and Inrush Current Control of the Virtual DC Bus Capacitor

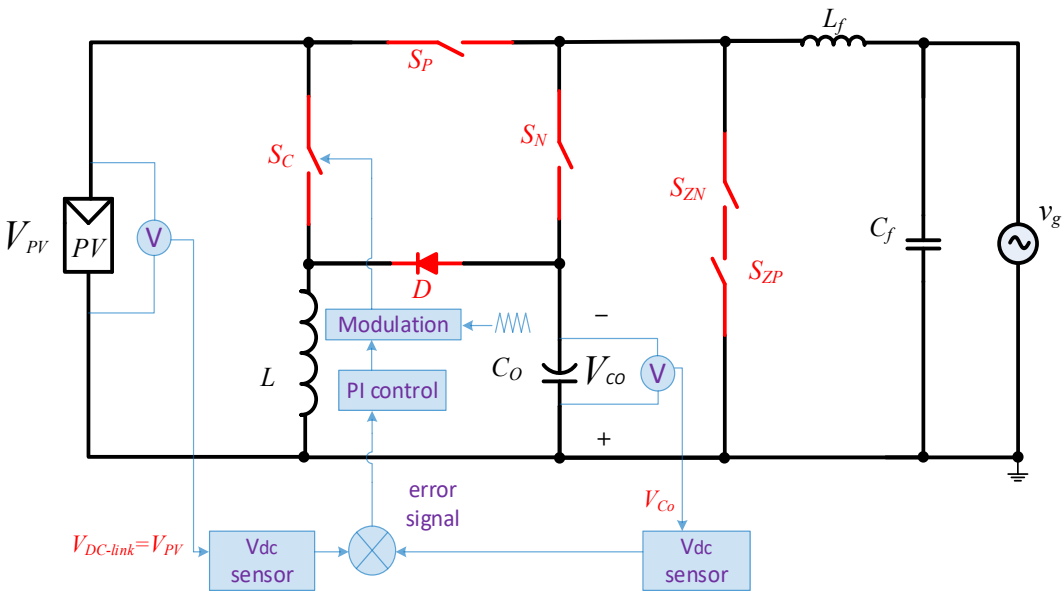


Figure 5.8. PI control for the proposed topology.

The capacitor C_O is used as a virtual DC bus to provide the negative power cycle of the inverter. It is required to be charged enough during the provision of negative power cycle to the load. A simple PI control method, shown in Fig. 5.8, can be used to keep a stable voltage across the capacitor C_O. This ensures that the peak of the ac voltage in the negative power cycle is the same as in the positive power cycle, and both cycles appear symmetrical and undistorted. In addition to the voltage control across the capacitor, the controller will also ensure optimal switching of S_C, which increases the inverter's efficiency.

Fig. 5.9 shows a comparative investigation with and without a PI controller integrated in the modulation of the proposed inverter. It is noted that the output voltage becomes distorted when SC is switched at constant duty cycle with an open-loop control. As per the simulation results, a 14% ripple reduction was achieved using a dedicated PI controller for switching S_C.

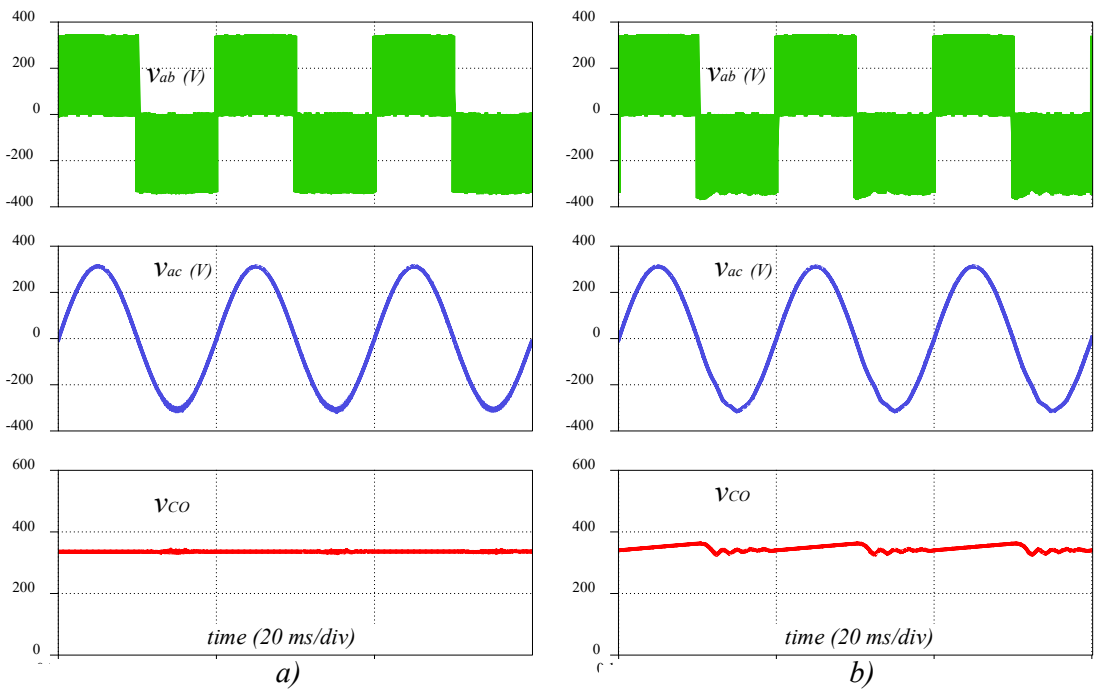


Figure 5.9. Key simulated waveforms (V_{PV} = 340 VDC, v_{av}= 220 V) a) with PI and b) without PI control.

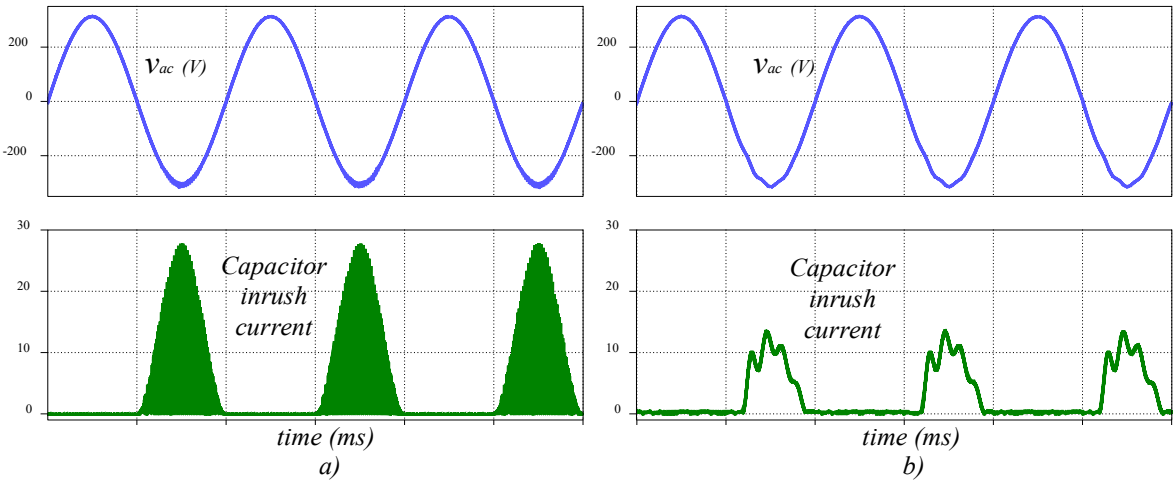


Figure 5.10. Simulated waveforms for output voltage and capacitor charging current a) with and b) without PI control.

A double charging process to charge C_O significantly helps to reduce the high charging current problems, unlike the other virtual DC bus capacitor-based topologies [107]. The direct capacitor charging via a switch leads to overburdened switch current stress [108]. In the proposed topology, the capacitor peak charging current is particularly important to consider during the negative power cycle because the capacitor is being discharged and charged simultaneously. This is also noticeable in the simulation results shown in Fig. 5.10.

It must be noted that there is a trade-off between the handling of the capacitor charging current and establishing a symmetrical positive and negative power cycle: As PI control will limit the S_C switching during the positive half cycle which, this will prevent the losses, and hence increase the efficiency; yet on the other hand, while the capacitor is used as a virtual DC bus, S_C will switch more often to keep the capacitor filled with energy. Consequently, the charging current will be severe in this case and both cases are demonstrated in Fig. 5.10.

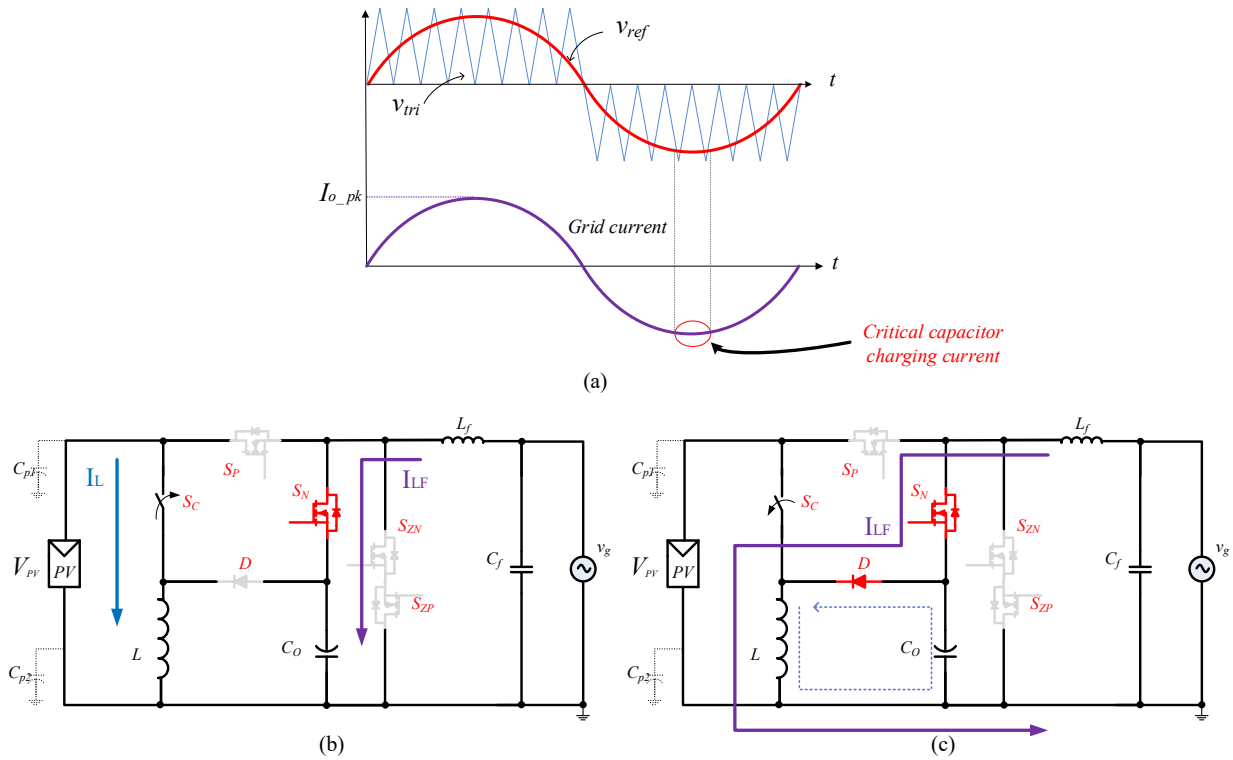


Figure 5.11. a) Analysis of capacitor charging current; sub-classification of negative (active) state when b) S_C is ON (active state 1) and c) S_C is OFF (active state 2).

The peak capacitor charging current can be determined based on the understanding that the active state during the negative power cycle (see Fig. 5.11c) can be sub-divided into two sub-states; one when S_C is on and another when it is off. These two sub-states, named active state 1 and active state 2, are shown in Fig. 5.11 (b and c).

Assuming a unity power factor, the output current waveform will be in phase with the sinusoidal reference as shown in Fig. 5.11 (a). The worst-case condition for the capacitor charging current occurs when the grid current is at the negative peak. For active state 1, when S_C is on, the capacitor current ($i_{Co,1}$) is the grid current (I_{LF}) as shown in Fig. 5.11 (b). When the grid current is at its peak during the negative half-cycle, the capacitor current will be:

$$i_{Co,1} = -I_{o\_pk} \tag{5.14}$$

during active state 1, whereas, for active state 2, when S_C is off, the capacitor current ($i_{Co,2}$) can be determined using charge second balance:

$$i_{Co,2} = \frac{D}{1-D} i_{Co,1} \approx i_{Co,1}. \tag{5.15}$$

The peak capacitor charging current is approximately I_{o_pk} for the case when S_C is switched to keep the voltage across C_O, the same as the dc-link voltage. The current carried by the inductor L (I_{L2}) during the active state 2 can be determined using KCL as $2 . I_{o\_pk}$. Therefore, switch S_C and D must be sized to handle at least twice the load current.

5.4. Aperiodic Sinusoidal PWM for EMI Reduction

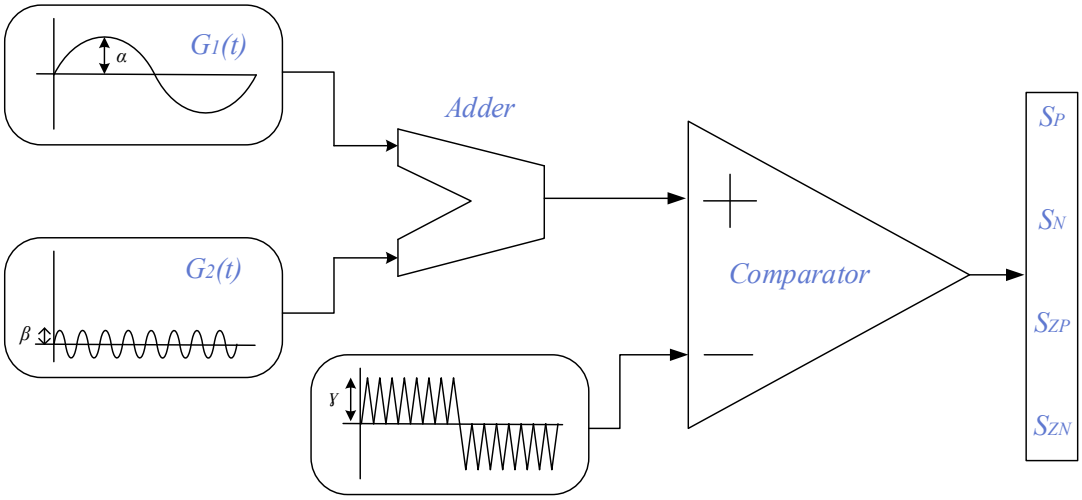


Figure 5.12. Aperiodic implementation of SPWM.

The aperiodicity can be added, in either or both of the modulation signal and the carrier signal, to generate an aperiodic switching signal for a power converter to reduce the EMI. In this scenario of the novel topology which is modulation by SPWM, the aperiodicity is applied to the modulation signal. The SPWM generation methodology is shown in Fig. 5.1 (b) and the aperiodic SPWM generation methodology follows a similar arrangement i.e.

comparing a sinusoidal reference signal with a bipolar carrier signal. The additional feature adapted in the aperiodic SPWM generation is one where the reference signal is superimposed by a small perturbation signal $G_2(t)$ as shown in Fig. 5.12.

In Fig. 5.12:

$G_1(t) =$ modulation signal= $\alpha(\sin\omega_1 t + \phi_1)$,

$G_2(t) =$ superimposition signal= $\beta(\sin\omega_2 t + \phi_2)$,

$\frac{\alpha+\beta}{\gamma} \approx m$ (modulation index),

$\phi_1 \neq \phi_2$ and $\omega_1 \neq \omega_2$.

It can be noted that $G_1(t)$ is basically the traditional modulation signal which defines the modulation index as well as serves as the reference signal leading to the generation of SPWM switching pattern. Therefore, the fundamental frequency of $G_1(t)$ is kept 50 Hz to match the frequency requirements of the AC side. Furthermore, as $G_2(t)$ is a superimposed signal on $G_1(t)$, therefore, it is anharmonic multiple of $G_1(t)$ and its peak-peak value is defined to keep the overall aperiodic reference signal (out of the adder block) to be equal 'm'. Conclusively, these parameters are defined in such a way that the SPWM pattern is maintained for the four switches but the pulse-positions are varied in every fundamental cycle. In other words, the switching pattern in each fundamental cycle is broken and hence EMI suppression is achieved [44]. In this way the benefits of using unipolar SPWM are still achieved in addition to the EMI suppression. The experimental results are presented in the next section which justify the proposed EMI suppression technique.

5.5. Simulation and Experimental Results

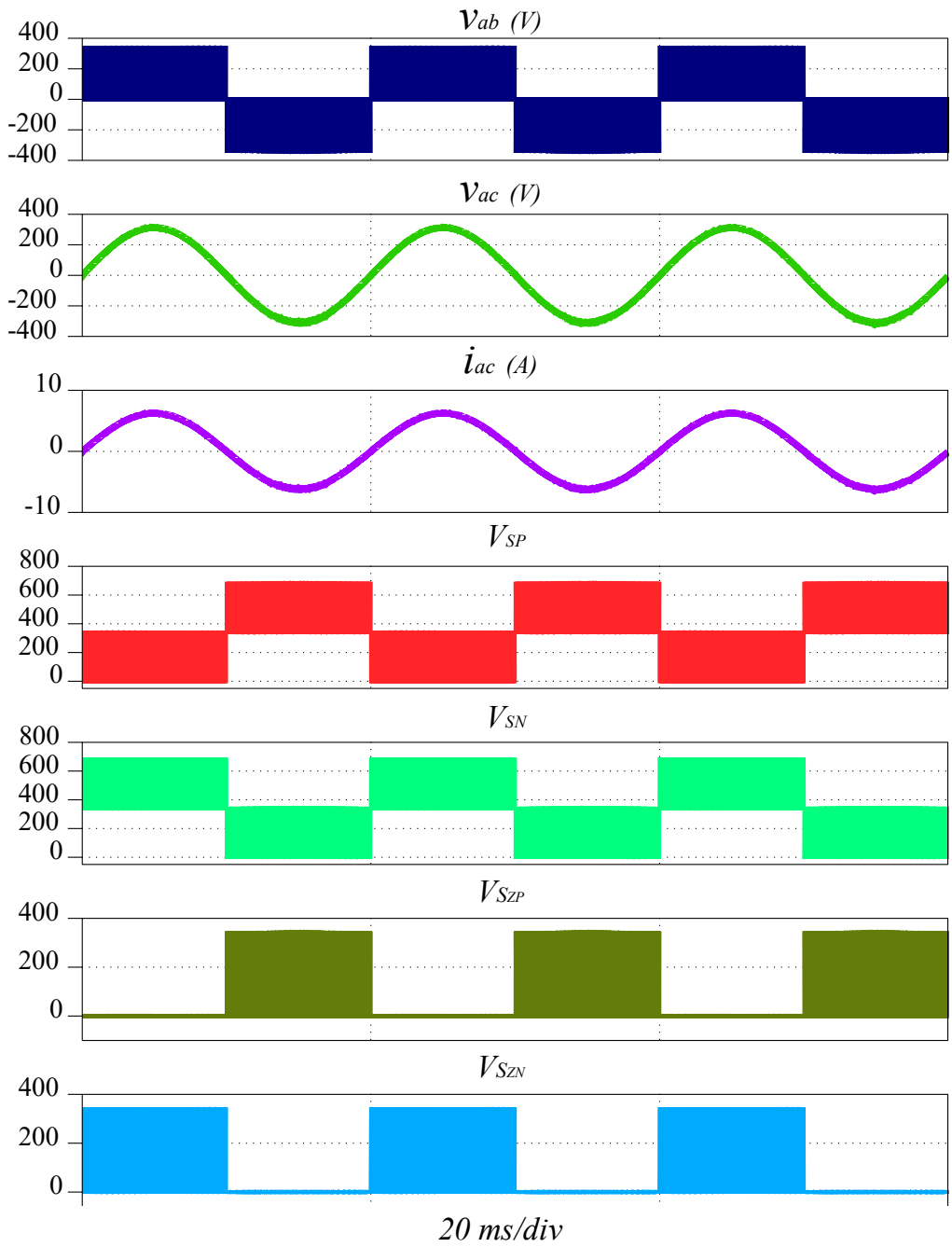


Figure 5.13. Key simulated waveforms for output voltage/current, unipolar voltage across filter and switch stresses.

The simulations of the proposed topology have been carried out in PSIM and MATLAB-Simulink using the PLECS toolboxes to verify its working principle and analyze various

aspects in terms of key waveforms, voltage stress across various semiconductor devices and leakage current etc. Additionally, PSIM was used to examine the leakage current for both the traditional SPWM and its aperiodic version. The thermal analysis and the heat-sink calculation were based on [118].

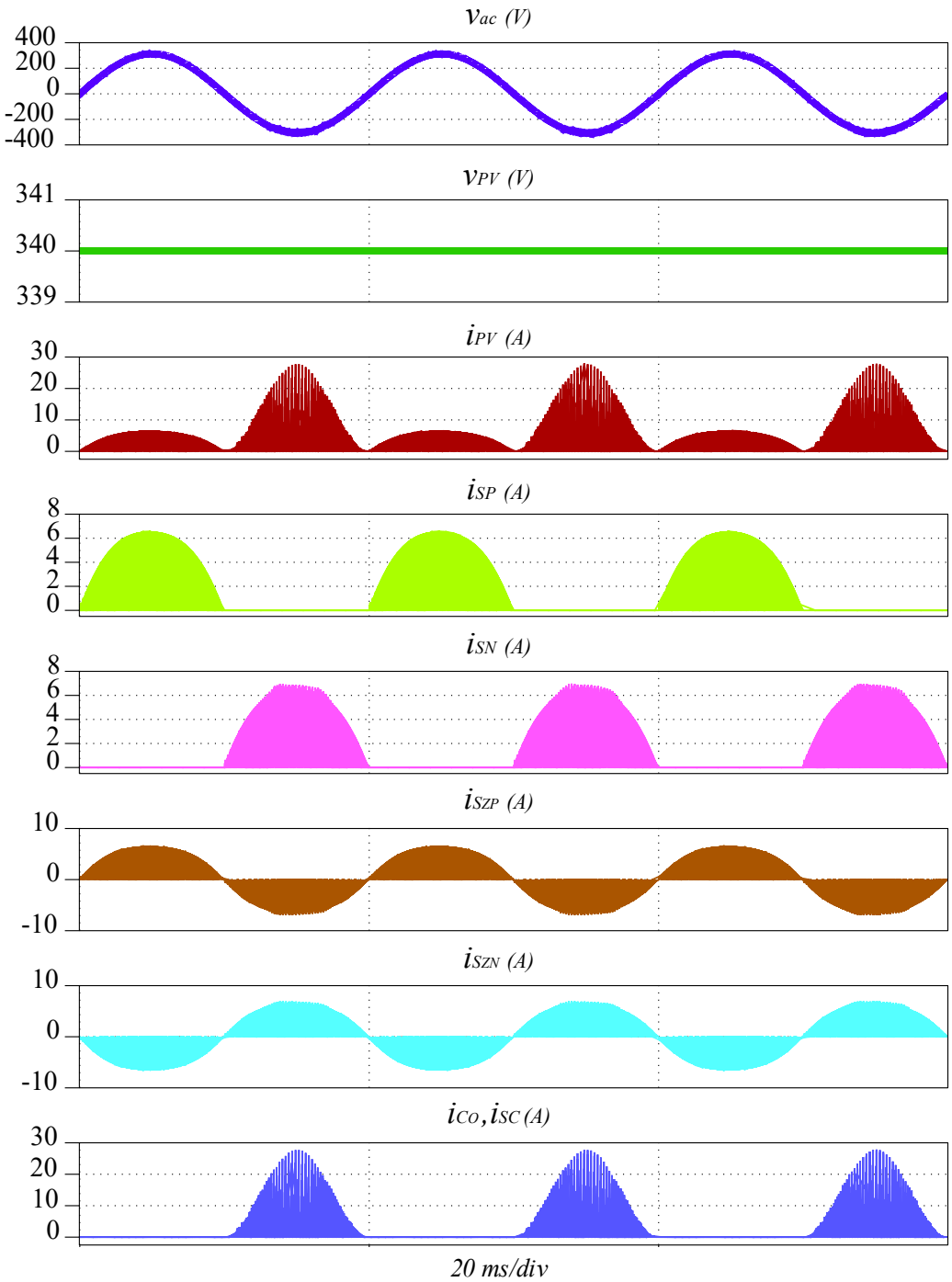


Figure 5.14. Key simulated waveforms for current stress across various switches.

5.5.1. Simulation Results

The simulation model of 1 kVA of the proposed topology was built as per the parameters listed in Table. 5.3.

Table 5.3. Parameters and Components Used in Simulation.

Parameter	Value, Description
Power switches	SiC MOSFET C3M0120090D
Carrier frequency	25 kHz
Line frequency	50 Hz
Virtual DC bus capacitor	100 μF
Filter capacitor	2.4 μF
Filter Inductor	0.37 mH
Inductor for Co	0.37 mH
Switching frequency for S_c	100 kHz
Load	48 Ω

The key simulated waveforms for various parameters such as the output voltage (v_{ac}) and current (i_{ac}), the chopped DC voltage (v_{ab}) before the LC filter and the switch-stress across various switches are shown in Fig. 5.13 which validate the theoretical basis of the proposed topology.

The rms value of the output voltage is 220 V with a dc-link voltage of 340 V. The modulation index (m) is kept at 0.92 and the corresponding rms value of load current is 4.6 A with a resistive load of 48 Ω. The three-level unipolar voltage before the filter denoted as v_{ab} is also shown which filters out as a smooth sinusoidal voltage and current denoted as v_{ac} and i_{ac}, respectively. The voltage stress across various switches is also shown and it is double that of the dc-link voltage for S_P and S_N and the same as the dc-link voltage for S_{ZP} and S_{ZN}. Moreover, the voltage across S_C and D is also twice the value of the dc-link voltage.

The waveforms of the currents passing through different power switches are shown in Fig. 5.14, enabling us to better comprehend in-depth understanding of switching patterns and their amplitude levels. Since the switch S_C is utilized to provide the charging current

of the DC bus capacitor, it experiences the maximum current stress relative to the other switches due to the in-rush charging current phenomenon of C_O especially in the negative power cycle. Moreover, it can be seen that the current flows bi-directionally through the two switches S_{ZP} and S_{ZN} to provide a zero state before the LC filter. The switches S_P and S_N conduct in the positive and negative power cycles, respectively.

The traditional SPWM and its aperiodic version were applied to the proposed inverter topology to investigate the modulation scheme's impact on leakage current. The simulation model similar to the one shown in Fig. 5.7 with a value of S_{PV} =100 nF and $Z_G = 5\ \Omega$, was built in PSIM environment and there was no significant impact on the leakage current. In fact, the leakage current was ≈ 0 in both cases. The simulation result for the leakage current for both cases is shown in Fig. 5.15. The simulated leakage currents were found to be 0.041 mA and 0.038 mA respectively for the aperiodic and simple SPWM modulation. This suggests the proposed aperiodic modulation has no adverse effect.

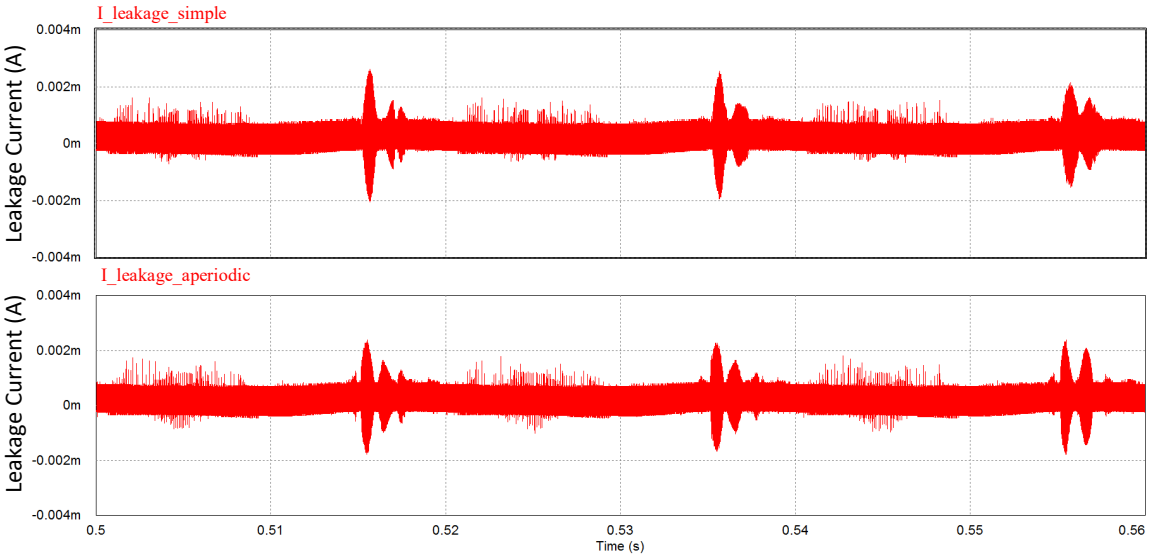
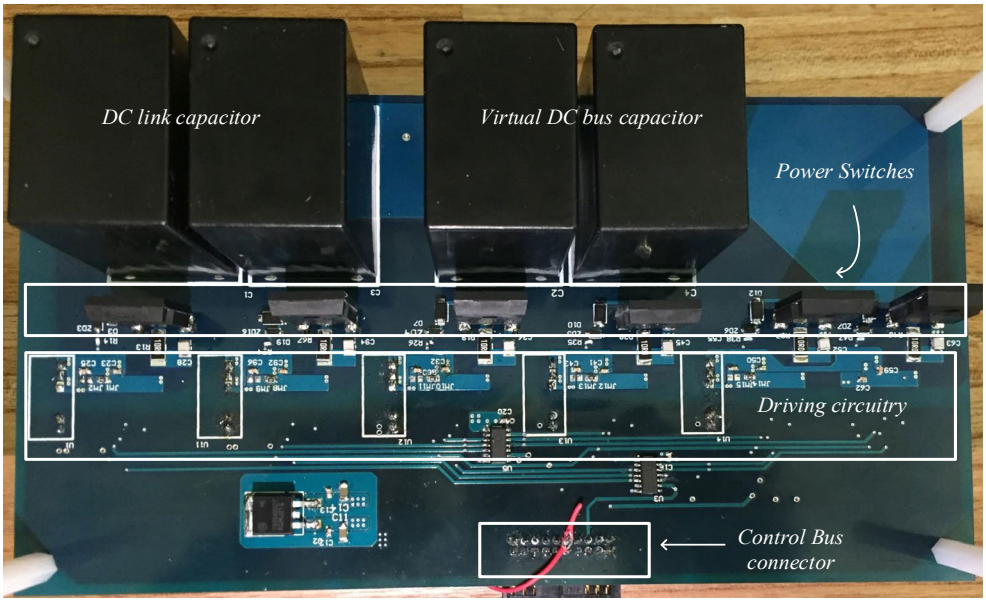


Figure 5.15. Leakage current pattern for the proposed inverter topology for simple and aperiodic modulation schemes

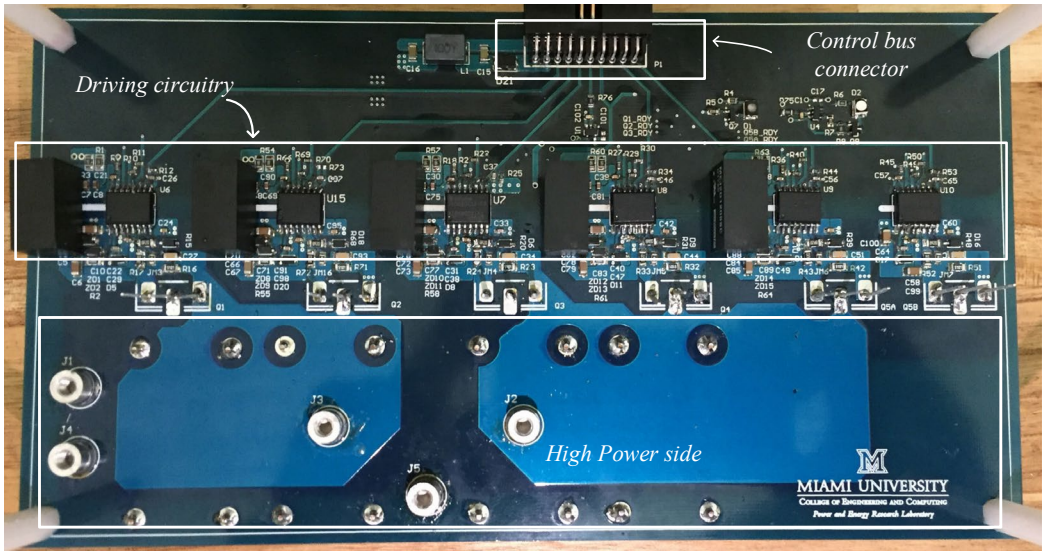
There is a good match between the theoretical analysis and the simulation results, which are also supported by the experimental results discussed in the following subsection.

5.5.2. Experimental Results

The prototype picture is shown in Fig. 5.16, and the switch driving signals were realized via a $C2000$ Peripheral Explorer Kit using the SimCoder block of PSIM.



a)



b)

Figure 5.16. Picture of both sides of the laboratory prototype of the proposed topology.

i) Converter Operation

Fig. 5.17 presents the key waveforms depicting the correct operation of the proposed topology to validate the theoretical and simulation based discussion in the previous sections.

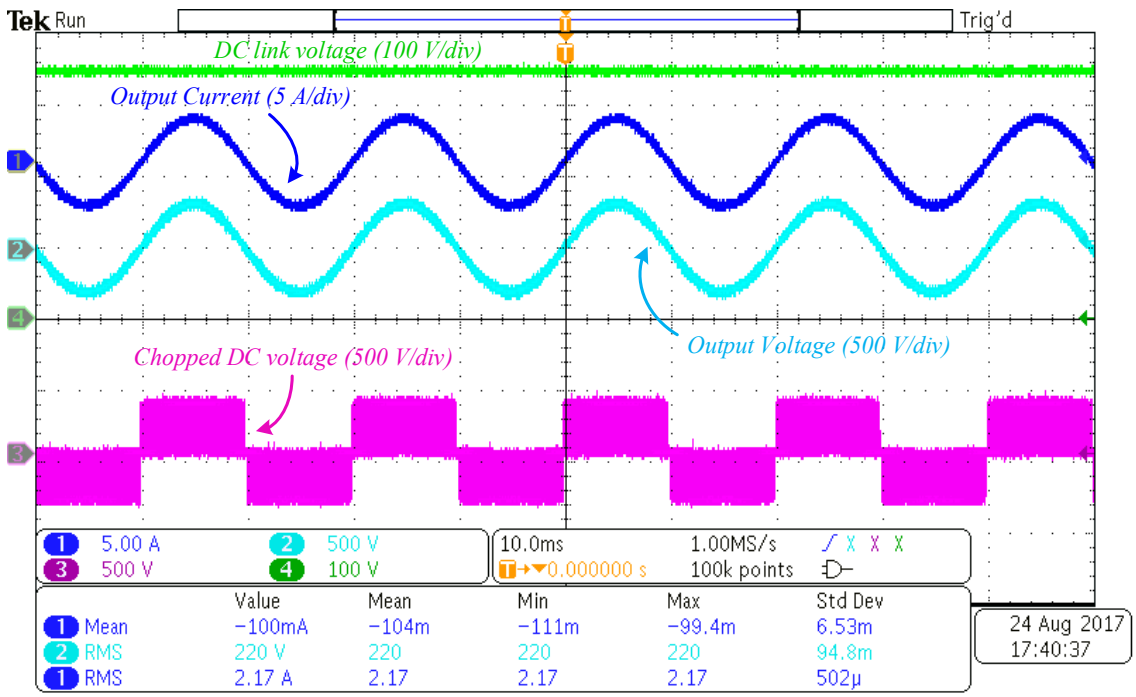


Figure 5.17. Key experimental results for the proposed topology.

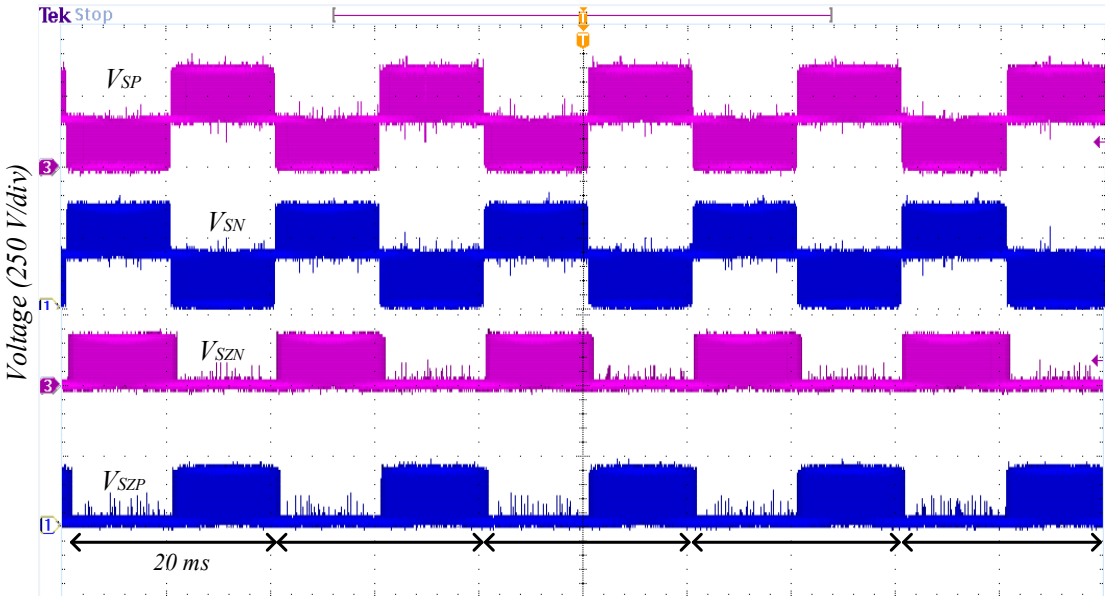


Figure 5.18. Switch voltage stress for the switches operated in the SPWM manner

It can be noted from the key waveforms shown in the experimental results that the rms value of the output voltage is 220 V with a dc-link voltage of 340 V. The modulation index 'm' was kept at 0.92, and it shows a peak efficiency of 95.2% at an output power of 1.6 kW. Additionally, the voltage and current are in-phase for a resistive load of 48 Ω.

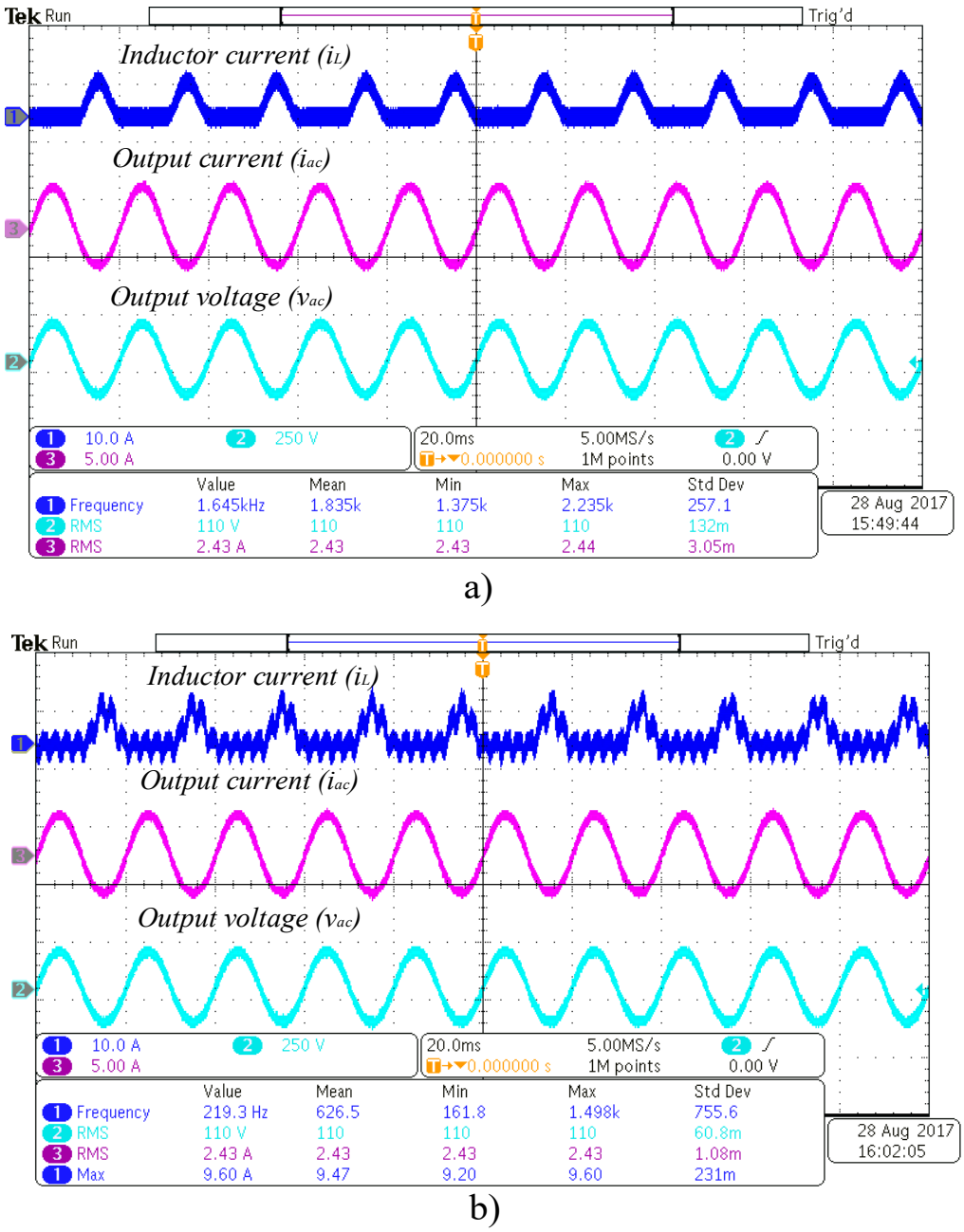


Figure 5.19. Key waveforms comparing operation of a) simple vs b) aperiodic SPWM.

The switch stress across the four switches, which are operated in an SPWM manner, are shown in Fig. 5.18, and correlate with the simulation results. The switch stress results are captured while the rms value of the output voltage was 110 V. The maximum voltage across the two main switches (S_P and S_N) which deliver the full load current was double the dc-link voltage, whereas the voltage across the switches providing zero states (S_{ZP} and S_{ZN}) was equal to the dc-link voltage as depicted in Fig. 5.18. The voltage across S_C and D is also twice that of the dc-link voltage. Additionally, the diode D was replaced by a SiC MOSFET, which could be used as a synchronous rectifier to achieve a better switching performance and an enhanced efficiency.

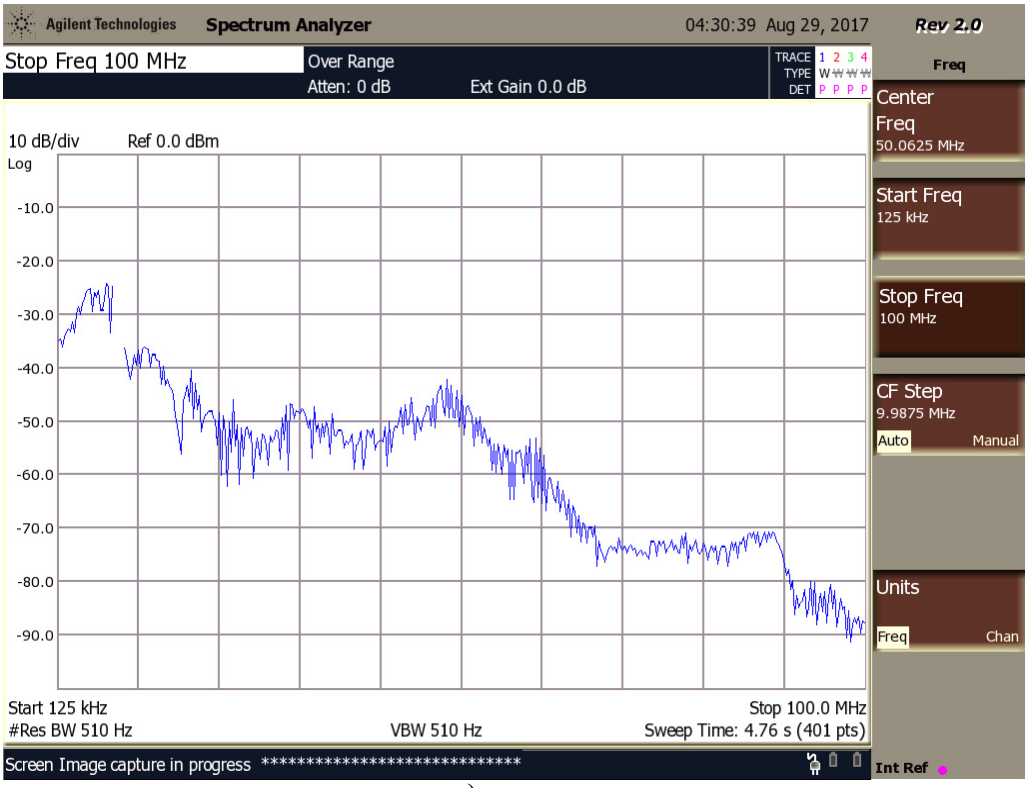
The proposed aperiodic SPWM technique was implemented and had no adverse effect on the operation of the inverter. Fig. 5.19 compares the key waveforms, showing smooth inverter operation for simple and aperioidic SPWM.

The charging current for C_O in Fig. 5.19 is denoted by i_L because the capacitor C_O is charged through the inductor L. It can be seen in Fig. 5.19 (b) that the peak value of the capacitor's charging current is increased when implementing aperiodic SPWM due to the fact that the capacitor is being charged in an aperiodic modulation pattern. Hence, the inrush charging current of C_O dominates and the peak current value is increased.

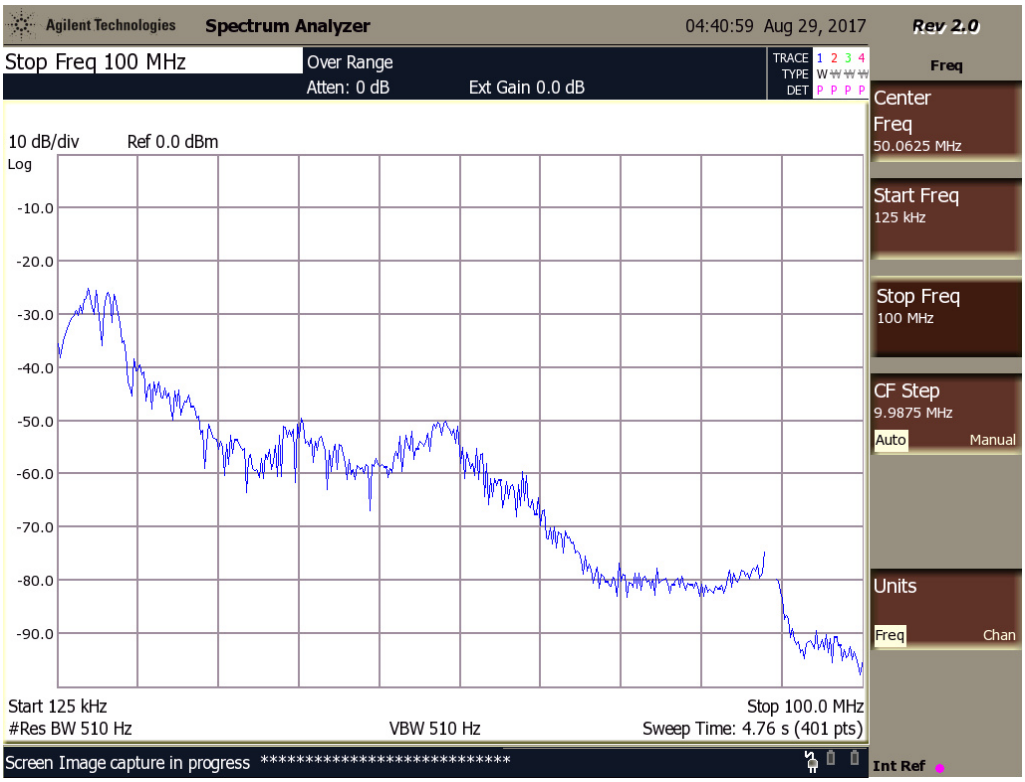
ii) EMI Suppression

A line impedance stabilization network (LISN) filter [119] was added between the DC source and the inverter input to filter out the conducted noise to be shown on a spectrum analyzer to analyze and compare the implication of the proposed aperiodic SPWM. The

comparative results are shown in Fig. 5.20 and EMI suppression is noticeable especially for higher frequency harmonics.



a)



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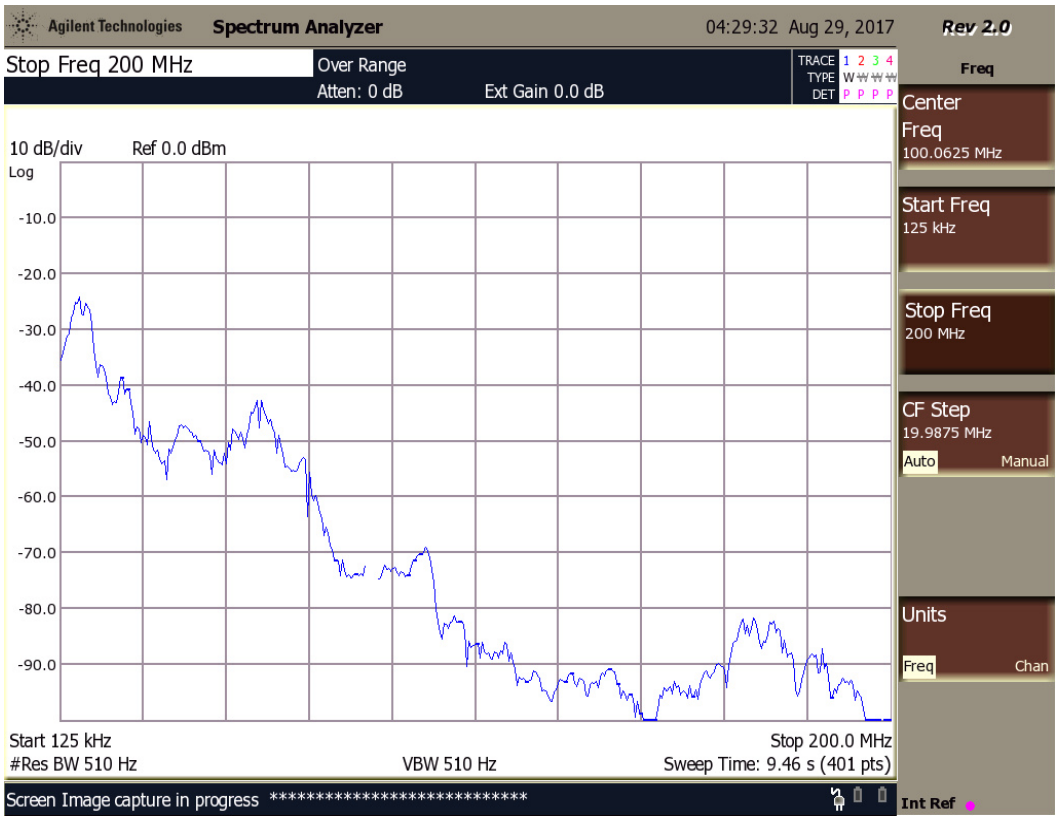

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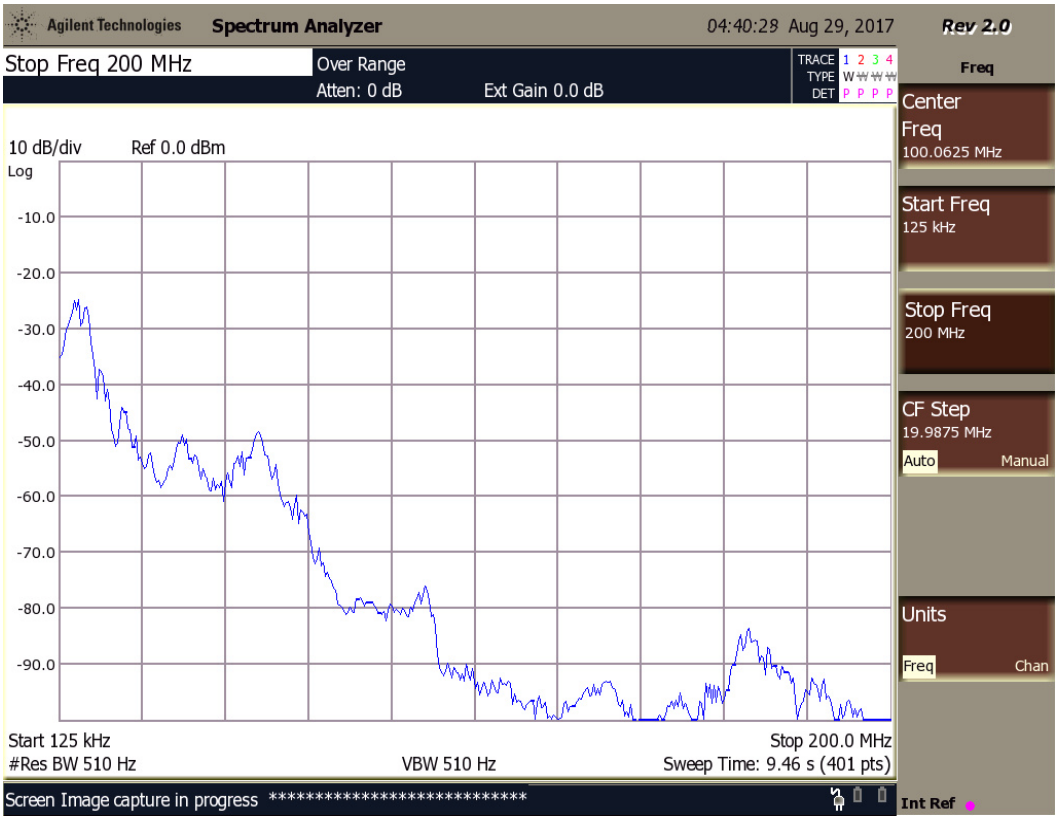


d)

Figure 5.20. Spectrum of conducted EMI for a) simple SPWM (125 kHz ~ 100 MHz), b) aperiodic SPWM (125 kHz ~ 100 MHz), c) simple SPWM (125 kHz ~ 200 MHz) and d) aperiodic SPWM (125 kHz ~ 200 MHz).

Fig. 5.20 (a and c) present the EMI spectrum for two different frequency ranges (125 kHz ~ 100 MHz and 125 kHz ~ 200 MHz) concerning the simple SPWM, whereas Fig. 5.20 (b and d) illustrate the reduced EMI spectra for aperiodic SPWM. It may be noted that a suppression of 6 ~ 8 dB can be noticed at high frequency harmonics. Therefore, a significant suppression is demonstrated which is more visible for high frequency harmonics.

The EMI test-bench setup is shown in Appendix A.6. To ensure that there is only a minimal amount of noise picked up by the surroundings, an 8X4 ft^2 base of ground plane was built and connected to the earth of the building. The current carrying wires were also kept higher than the ground plane to minimize any type of interference. Additionally, the earth terminal of the LISN as well as the heat sink were grounded with the main earth.

iii) Efficiency and Loss Analysis

The key parameters given in Table. 5.3 were used to measure the efficiency of the proposed inverter. The graph comparing the efficiency vs load performance of the proposed inverter with traditional SPWM and with aperiodic SPWM is shown in Fig. 5.21. The measurements were done using a high-precision power analyzer Hioki PW3390, and the maximum efficiency measured was 95.2% at a load of 1.6 kW.

A good match is be found between the theoretical and experimental losses, as presented in Fig. 5.22, and a major loss breakdown pertaining to the conduction, switching and switch parasitic capacitor losses is presented in Fig. 5.23. The difference between the theoretical and practical losses becomes minimal around 1 kVA. Moreover, as the peak current passing through the capacitor charging path is double the grid current and since both switch S_C and D are operating at relatively higher switching frequency as compared to the other four

SPWM switches. Therefore S_C and D make a major contribution to both the conduction and switching losses.

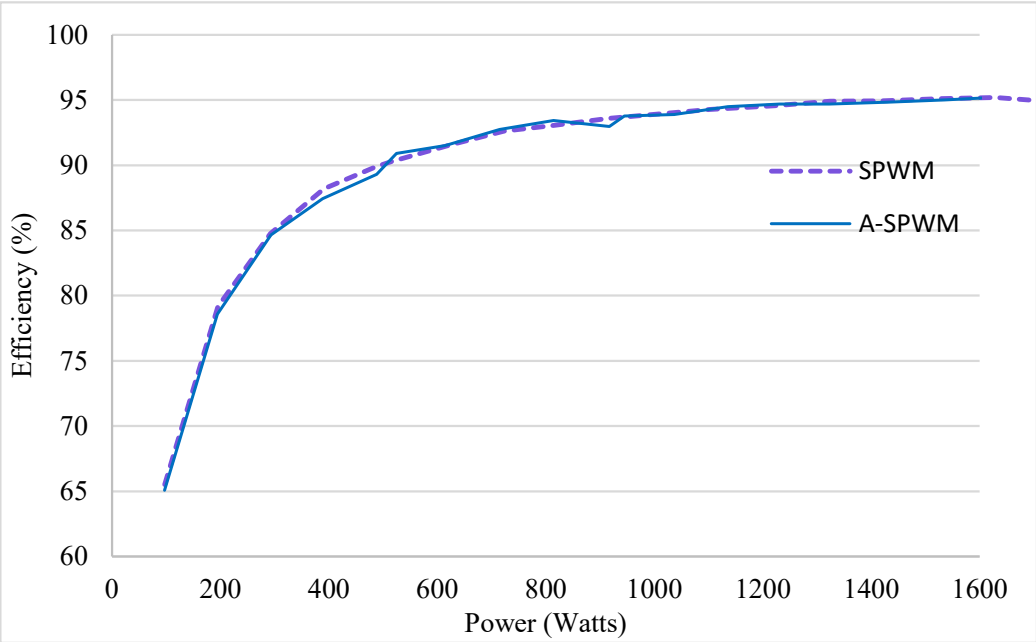


Figure 5.21. Efficiency vs load performance comparison for simple vs aperiodic SPWM.

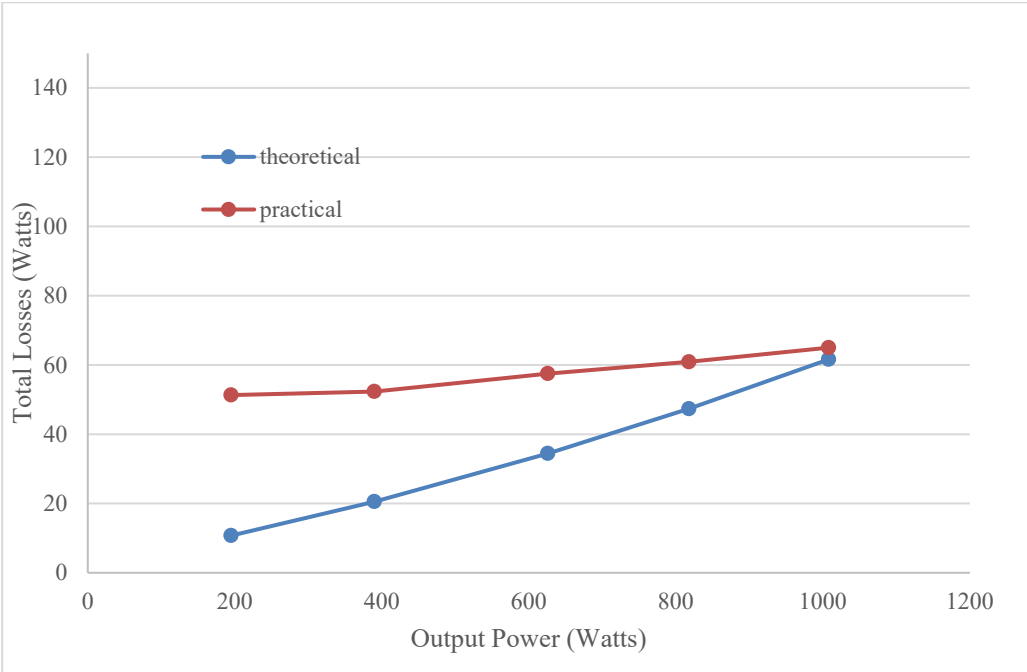


Figure 5.22. Comparison of theoretical vs practical losses for different load values.

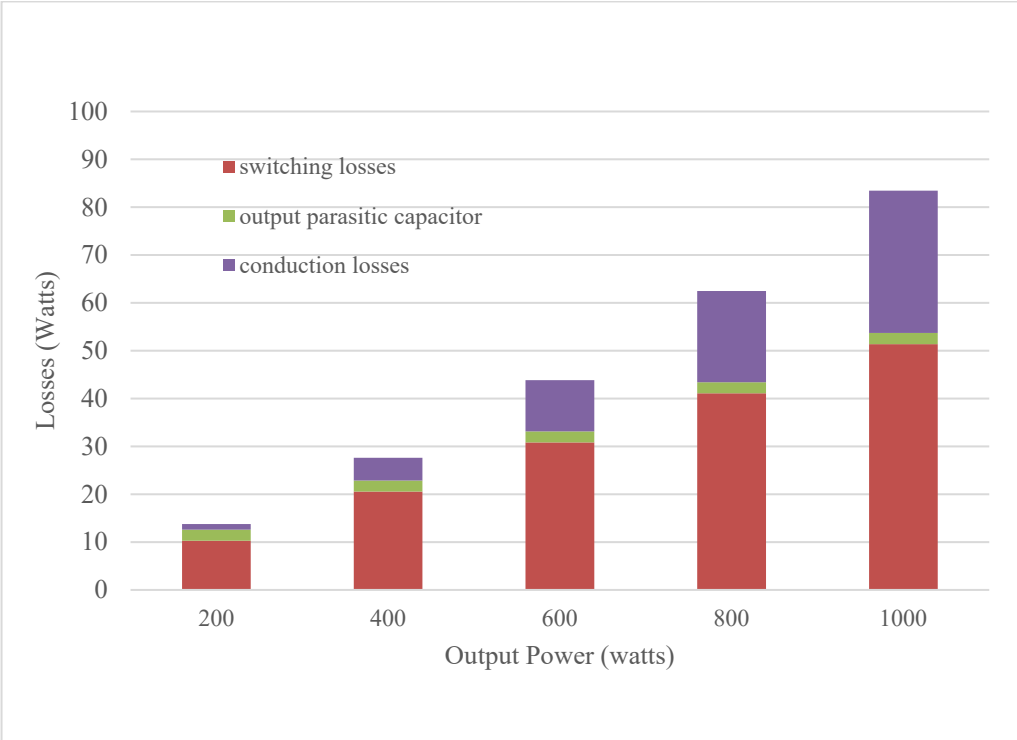


Figure 5.23. Efficiency vs load performance comparison for simple vs aperiodic SPWM.

The theoretical power loss calculations are plotted in Fig. 5.22 based on the following equations:

$$P_{cond\_SPWM} = i_{RMS}^2 * R_{DS(ON)} \tag{5.16}$$

$$P_{cond\_Sc/D} = \left(\sqrt{2} * i_{RMS}\right)^2 * R_{DS(ON)} \tag{5.17}$$

$$P_{sw\_SPWM} = \frac{1}{2} V_{DS} * i_{RMS} * f_{SW} * (t_{ON} + t_{OFF}) \tag{5.18}$$

$$P_{sw\_Sc/D} = \frac{1}{2} V_{DS} * \sqrt{2} * i_{RMS} * f_{SW} * (t_{ON} + t_{OFF}) \tag{5.19}$$

$$P_{coss\_Sx} = \frac{1}{2} (V_{DS})^2 * f_{SW} * C_{oss} \tag{5.20}$$

Where,

P_{cond_SPWM}= Conduction losses associated with SPWM driven switches,

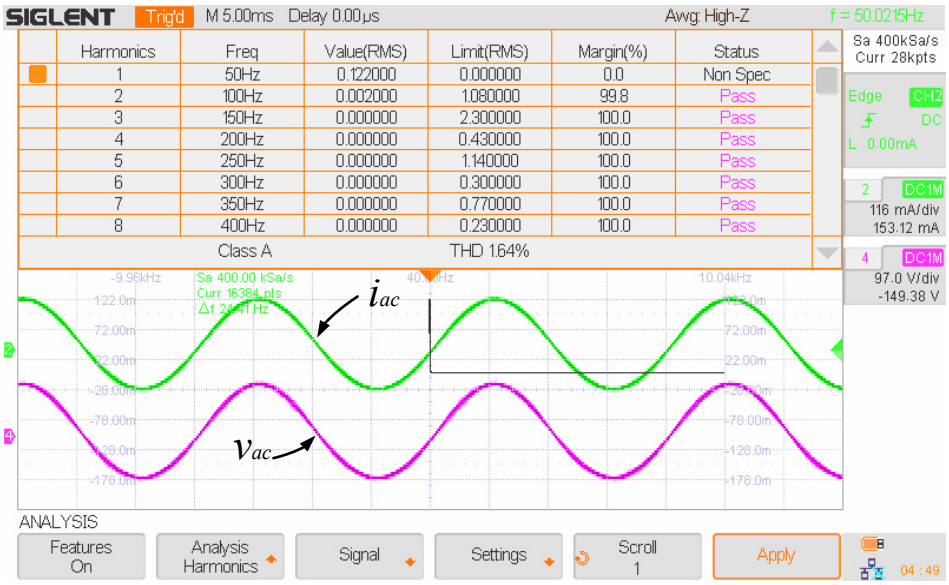
$P_{cond\_Sc/D}$= Conduction losses associated with the switch S_C and D,

P_{sw_SPWM}= Switching losses associated with SPWM driven switches,

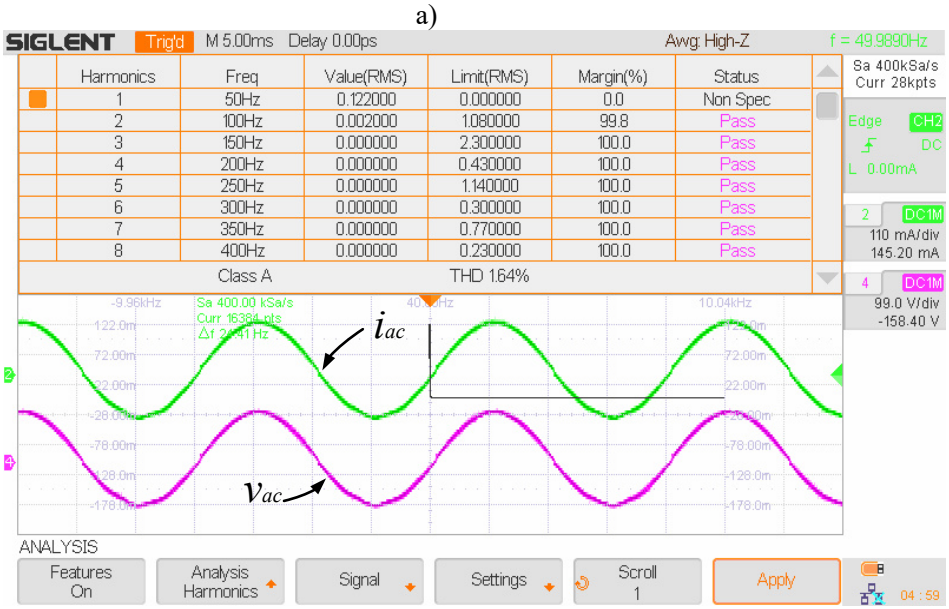
$P_{sw\_Sc/D}$= Switching losses associated with the switch S_C and D, and

P_{coss_Sx} = Losses due to output capacitance of a switch.

It can be observed that the efficiency is quite high for a wide range of loads. Also, there is no significant difference in the efficiency vs load performance while using either of the simple or aperiodic SPWM modulation schemes. This provides a sound basis for the validity of the proposed modulation scheme.



a)



b)

Figure 5.24. THD measured for the output current waveform for a) simple SPWM and b) aperiodic SPWM.

iv) Total Harmonic Distortion

The total harmonic distortion (THD) of the output current was tested using a SIGLENT SDS2104X oscilloscope. The THD for both the simple SPWM and aperiodic SPWM was measured as $< 2\%$ which complies well with the IEEE standard 519. The waveforms and the THD measurements are shown in Fig. 5.24.

5.6. Summary and Conclusions

This chapter presents a common-ground transformerless PV inverter topology which is based on the concept of a virtual DC bus capacitor. It is charged by a double-charging process through an inductor to minimize the inrush current. The proposed topology offers a minimal leakage current, and its simple operation based on unipolar SPWM results in small filter requirements, low switching losses, low EMI and low ripple in the output current. Additionally, only one switch is operated in the active state which reduces the associated conduction losses. Given that the inrush current phenomenon adds to di/dt and dv/dt, and with the increased current and voltage transitions, more EMI is produced. In the proposed topology, the utilization of an inductor as an intermediate energy storage component contributes to the suppression of EMI. Furthermore, an aperiodic SPWM technique was proposed and demonstrated for a 1 kVA laboratory prototype which further reduces the peak conducted EMI promising a practical grid-connected PV system. Moreover, the topology can flexibly be implemented with two industry-standard half-bridge modules. These in turn can reduce cost, promote ease of implementation and achieve a high power density, paving the way for the topology serving as a micro-inverter which can be installed at the back of solar panels.

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Chapter 6

Conclusion and Future Work

WBG switches allow faster switching and a higher switching frequency, which enables improved efficiency and higher power density. Sharp switching transients in power converters lead to increased levels of EMI. In this thesis, a new and simple methodology to implement aperiodic modulation schemes in power converters is presented. Aperiodic modulation is a classic way to reduce EMI in power converters. Therefore, a generic framework for the implementation of an aperiodic modulation methodology has been presented which was compliantly applied to a coupled inductor-based SEPIC, an isolated quasi-Z-source dc-dc converter and a novel transformerless common-ground dc-ac inverter. The modulation methodology is demonstrated to be generic and was applied successfully to all of the above-mentioned power converters. Supporting results such as EMI suppression, voltage gain and efficiency vs load index, are also presented which justify the applicability of the aperiodic modulation methodology.

6.1. Thesis Summary and Conclusions

The research has been applied to various types of power converters and supported with simulation and experimental results. In this regard, the main contributions of this thesis are summarized as follows:

- A general overview of the phenomenon of EMI and its associated dynamics is discussed in Chapter 2. Various EMI measurement/analyzing techniques are also presented to enlighten the reader about different possibilities in terms of which EMI can be analyzed. Furthermore, EMI suppression techniques are discussed and a detailed classification of spread-spectrum-based EMI suppression techniques is given.
- A framework for generating the aperiodic carrier signal has been presented and modified suitably to a high-frequency GaN-based SEPIC converter. The issue of the EMI becomes more critical in WBG-based power converters, so for this reason the aperiodic modulation methodology was applied to suppress EMI, and supporting experimental results were presented. A hard-switched SEPIC converter was designed to operate at high frequency and a four-layer PCB board was designed to support the high-frequency operation. Various design insights are given to retain the high-frequency parasictics to a minimum. This work is reported in Chapter 3.
- The aperiodic carrier signal is extended for application to an isolated qZS DC-DC converter containing an H-bridge. A coordinated hybrid pulse-width modulation technique, in which both the pulse position and the pulse width are modulated in each switching cycle, was used to switch the four switches in a coordinated way. We report this as the first description of the aperiodic modulation applied to an H-bridge-based

power converter having "shoot-through" states. The EMI suppression results and supporting experimental results are presented.

- In Chapter 5, a novel transformerless common-ground dc-ac inverter is presented. The topology combines a dc-dc converter and an SPWM modulated H-bridge, linked in such a way to utilize a capacitor as a virtual DC bus. A double-charging process was adopted to reduce the inrush current which can add to the EMI reduction of the power converter. Furthermore, the concept of aperiodic modulation is applied to inverter, and several simulation and experimental waveforms are presented in support of the EMI suppression. Moreover, there was no adverse impact on the efficiency, leakage current and THD, which supports the standard inverter's operation.

6.2. Future Work Avenues

In recently highlighted research streams of power electronics, switched capacitor-based power conversion is reported as being well suited with GaN switches to improve the overall performance of powers converters [86]. However, it has been contended that the switched capacitor-based topologies generate significant amounts of common-mode noise. As these topologies pave the way towards nearing magnetics-free power conversion solutions, which makes a significant contribution to highly efficient and high power density compact power converters, EMI analysis for such topologies is an indispensable and interesting topic to those considering the adoption of switched-capacitor based power converters.

Some of the proposed/ongoing future streams are briefly described as follows:

- Recently, as a collaborative effort involving the author, a novel switched-capacitor-based five-level boost inverter with a common ground for PV applications has been proposed, and shown in Fig. 6.1 [120]. The prototype offered a peak efficiency of ~ 99% and was based on MOSFET switches. As the EMI analysis of switched-capacitor-based power converters is one of the proposed future research directions, it is intended to implement this topology with GaN and analyze the EMI behavior. Furthermore, applying the aperiodic modulation in the GaN-based hardware will generate improved results.

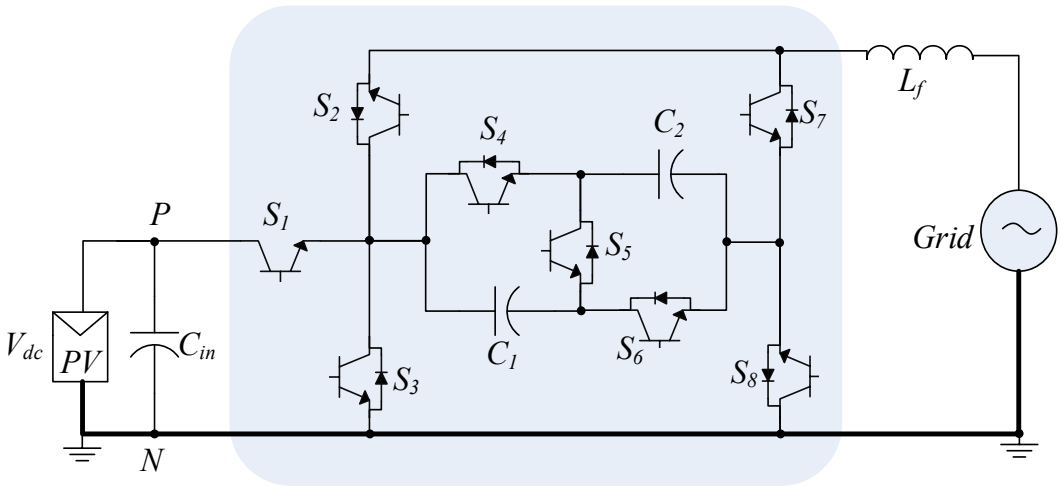

Figure 6.1. Novel 5-level transformerless inverter topology [120].

- Recent developments in the availability of powerful tools for designing PCB designing have facilitated users' ability to predict and analyze the EMI behavior well before fabrication. This facility can be utilized in order to optimize the PCB design; as more research is pushing towards high frequency operation. In this way the parasitics involved become more significant and can be taken care of before the PCB fabrication.
- One of the enabling factors of high efficiency in high frequency power converters is soft-switching, which usually requires tuning of the parameters of the switching signal.

It would be interesting to accommodate both soft-switching tunings (via intelligent control) to follow an aperiodic pattern because it will further assist in EMI reduction.

- The EMI measurements presented in this dissertation elicit the relative suppression behavior of the power converters and have not been compared with the standard threshold values provided by various EMC standards due to laboratory setup limitations. The aperiodic modulation methodology can be implemented in a standard EMI measurement setup (for both conducted and radiated EMI) as per the EMC standards, and the compliance testing can be done.
- The theoretical analysis of the aperiodic modulation techniques in power converters still needs to be investigated in order to predict the amount of suppression in real examples. Moreover, various trade-off parameters must also be accommodated to validate the standard operation of a power converter. These parameters are numerous but not limited to, voltage gain, efficiency, THD, reactive power compensation, etc.

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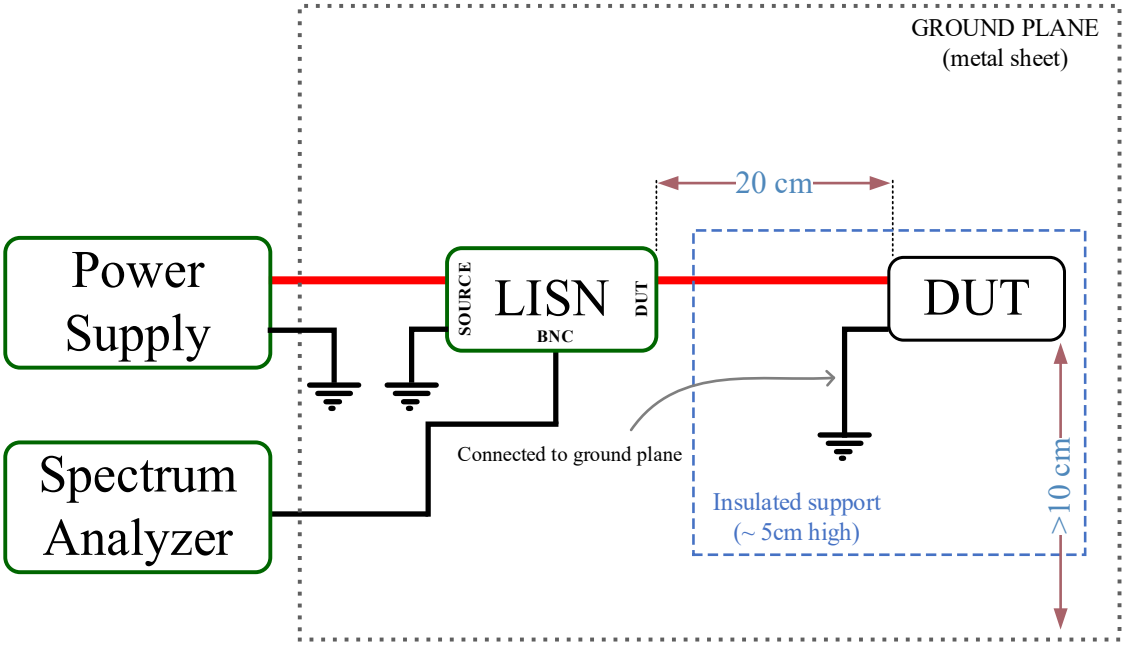
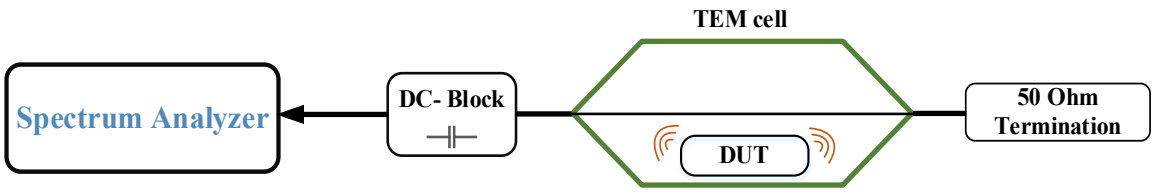
Appendix A

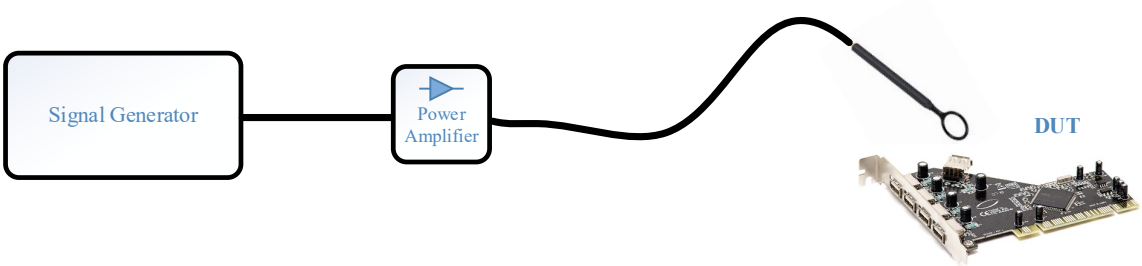
Pictures of Test Setups



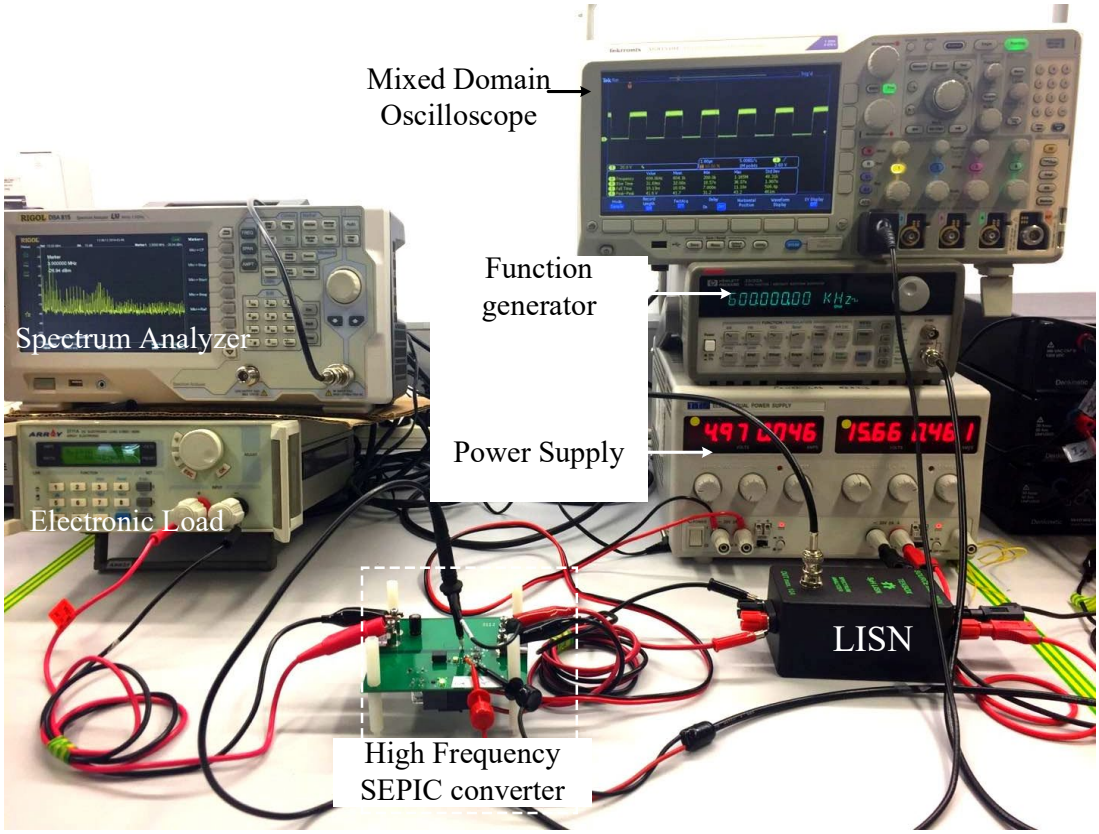
A 1. A conducted EMI measurement setup using LISN



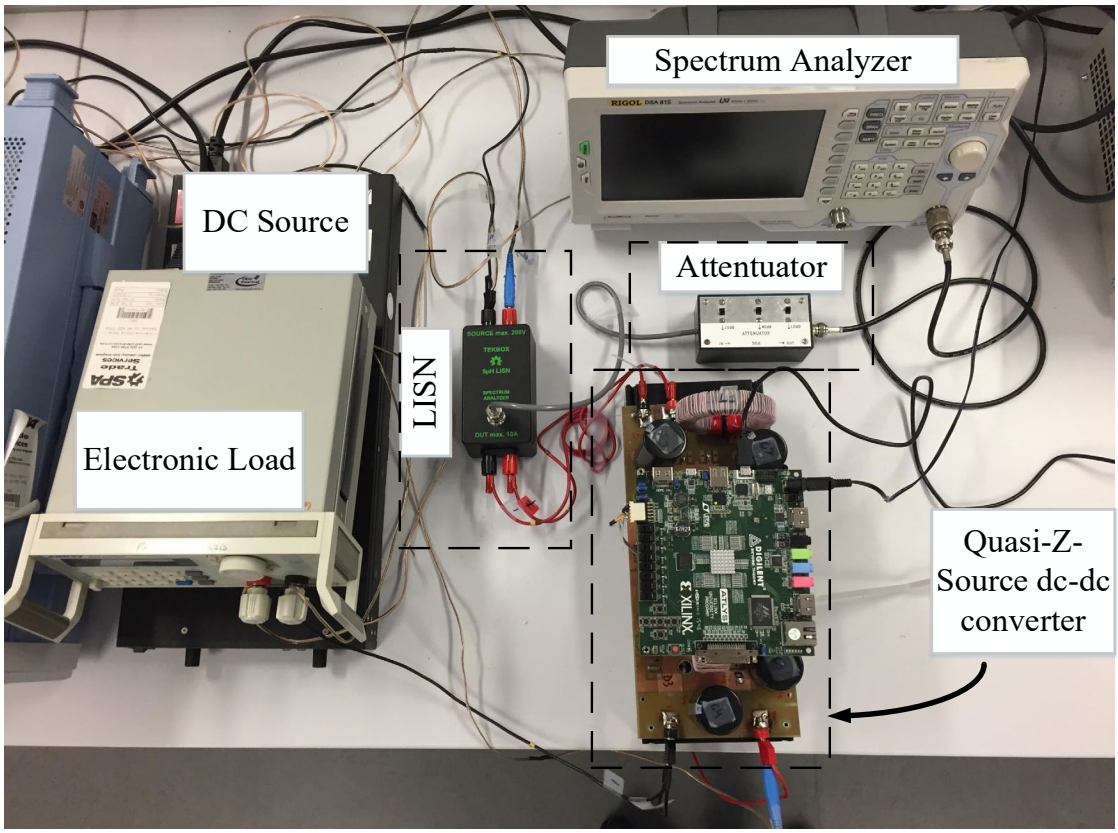
A 2. A radiated EMI measurement setup using a TEM cell



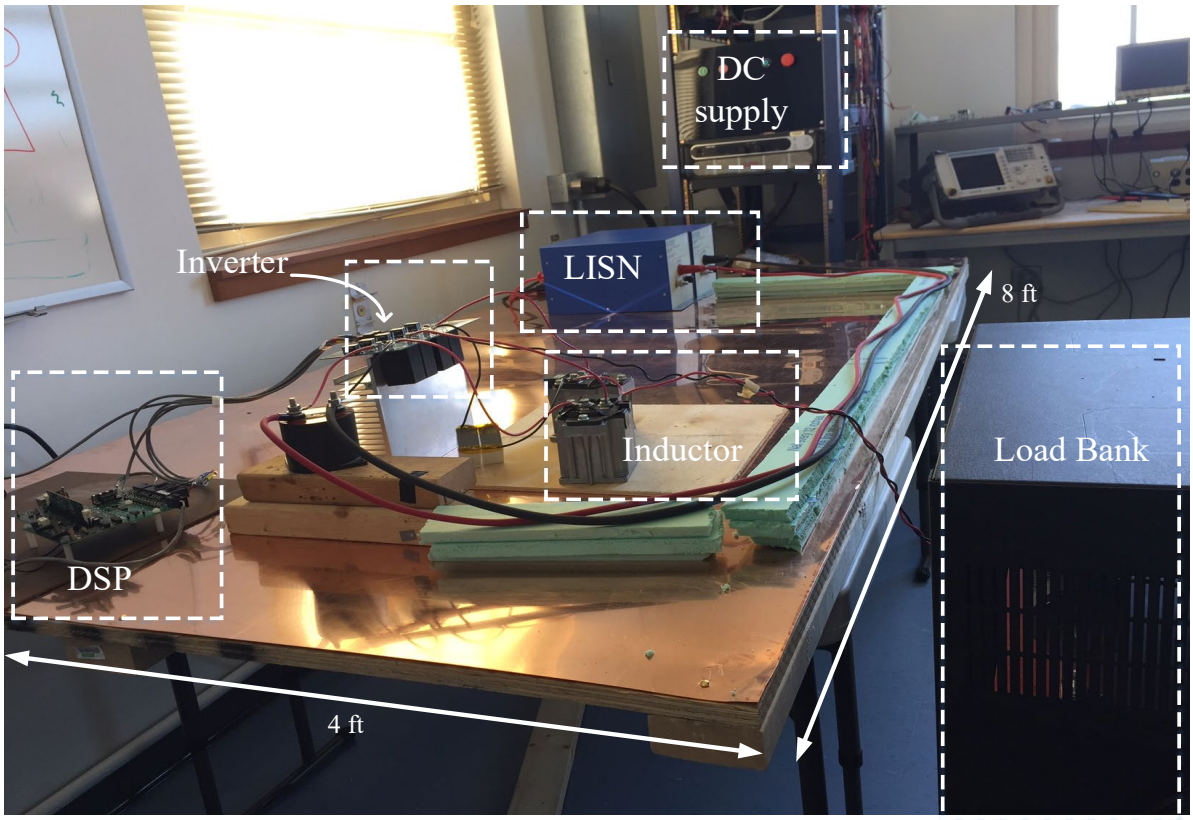
A 3. Localizing a susceptible region of a PCB



A 4. Bench setup for conducted EMI test of HF SEPIC Converter



A 5. Bench setup for conducted EMI test of qZS DC-DC converter



A 6. Bench setup for conducted EMI test of the novel transformerless common-ground PV inverter*

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Appendix B

List of Acronyms

ACMA..... Australian Communications and Media Authority

CCM..... Continuous conduction mode

CISPR..... International Special Committee on Radio Interference

CM..... Common-mode

DCM..... Discontinuous conduction mode

DM..... Differential-mode

DPS..... Distributed Power System

DUT..... Device under test

EMC..... Electromagnetic Compatibility

EMI..... Electromagnetic Interference

EUT..... Equipment under test

FCC..... Federal Communications Commission

GaN..... Gallium Nitride

HEMT..... High Electron Mobility Transisitor

IEC..... International Electrotechnical Commission

LED..... Light emitting diodes

LISN..... Line Impedance Stabilization Network

PCB..... Printed Circuit Board

PPM..... Pulse position modulation

PSD..... Power Spectral Density

PV..... Photovoltaic

qZS..... Quasi-Z-Source

$R_{DS(ON)}$ ..... On-state resistance

SEPIC..... Single Ended Primary Inductor Converter

SiC..... Silicon Carbide

SPWM..... Sinusoidal Pulse Width Modulation

TEM..... Transverse Electromagnetic

THD..... Total Harmonic Distortion

WBG..... Wide Bandgap

Wi-Fi..... Wireless Fidelity

ZCS..... Zero Current Switching

ZS..... Impedance Source

ZVS..... Zero Voltage Switching

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Bibliography

[1] L. M. Tolbert *et al.*, "Power Electronics for Distributed Energy Systems and Transmission and Distribution Applications," *Ornl/Tm-2005/230*, no. December, pp. 65–91, 2005.

[2] B. Ozpineci and L. M. Tolbert, "Comparison of wide-bandgap semiconductors for power electronics applications," U.S. Dept. Energy, Oak Ridge Natl. Lab., Oak Ridge, TN, USA, Dec. 12, 2003.

[3] K. K. Tse, H. S. H. Chung, S. Y. R. Hui, and H. C. So, "A comparative investigation on the use of random modulation schemes for DC/DC converters," *Ind. Electron. IEEE Trans.*, vol. 47, no. 2, pp. 253–263, 2000.

[4] F. Zare, D. Kumar, M. Lungeanu, and A. Andreas, "Electromagnetic interference issues of power, electronics systems with wide band gap, semiconductor devices," *2015 IEEE Energy Convers. Congr. Expo. ECCE 2015*, pp. 5946–5951, 2015.

[5] F. Zare, D. Kumar, M. Lungeanu, and A. Andreas, "Electromagnetic interference issues of power, electronics systems with wide band gap, semiconductor devices," in *Proc. IEEE. Energy Convers. Congr. Expo.*, Montreal, QC, Canada, 2015, pp. 5946–5951.

[6] "IEC. "Available basic EMC Publications," [Online]. Available: http://www.iec.ch/emc/basic_emc/basic_emc_general.htm. [Accessed: 15-May-2018].

[7] P. S. Ruggera and E. R. O'Bryan, "Studies of apnea monitor radio frequency electromagnetic interference," in *Proc. 13th Annu. Int. Conf. IEEE Engineering in Medicine and Biology Society*, Orlando, FL, Oct. 31–Nov. 3, 1991, vol. 13, no. 4, pp. 1641–1643..

[8] EMC standards. "Another EMC resource from EMC Standards," 2016 [Online]. Available: https://www.emcstandards.co.uk/files/emi_stories_761-855.pdf [Accessed: 15-May-2018]. [9] H. Li, "er ta ss Di Ho ng Di ss er tio n Ho ng Li," 2009.

[10] M. J. Schneider, "Design Considerations to Reduce Conducted and Radiated EMI," MS thesis, Dept. Elec. & Comp. Eng. Tech, Purdue University, 2010.

[11] Silicon labs. "Understanding Radiated EMI, " [Online]. Available: https://www.silabs.com/Marcom%20Documents/Resources/EMI-guide.pdf [Accessed: 15-May-2018].

[12] D. Hamza, "Electromagnetic Interference Mitigation in Switched Mode Power Converters Using Digital Sampling Techniques," Ph.D. dissertation, Dept. Elec. & Comp. Eng. Queen's University, 2011.

[13] H. Li, Z. Li, B. Zhang, W. K. S. Tang, and W. A. Halang, "Suppressing electromagnetic interference in direct current converters," *IEEE Circuits Syst. Mag.*, vol. 9, no. 4, pp. 10–28, 2009.

[14] Tekbox. “EMC pre-compliance testing, ” [Online]. Available: https://www.tekbox.net/images/documents/testequipment/guide/EMC_pre_compliance_testing.pdf [Accessed: 15-May-2018].

[15] Tekbox. “TBOH1 5µH LISN Manual, ” [Online]. Available: https://www.tekbox.com/product/TBOH01_Manual.pdf [Accessed: 15-May-2018].

[16] Tekbox. “Open TEM cells for EMC pre-compliance testing, ” [Online]. Available: https://www.tekbox.com/product/Tekbox_TEM_Cell_Manual.pdf [Accessed: 15-May-2018].

[17] Keysight A. Note, “EMI Troubleshooting : The Need for Close Field Probes,” [Online]. Available: http://literature.cdn.keysight.com/litweb/pdf/5991-0144EN.pdf?id=2349297 [Accessed: 15-May-2018].

[18] IEC. “IEC 60050 - International Electrotechnical Vocabulary,” [Online]. Available: http://www.electropedia.org/iev/iev.nsf/display?openform&ievref=161-01-07. [Accessed: 29-May-2018].

[19] DigiKey. “Understanding Electromagnetic Standards” [Online]. Available: https://www.digikey.com.au/en/articles/techzone/2012/jun/understanding-electromagnetic-compatibility-standards-for-switch-mode-power-supplies. [Accessed: 18-May-2018].

[20] C. Nguyen, “ACMA mandated EMC standards,” [Online]. Available: https://www.acma.gov.au/-/media/Technical-Regulation-Development/Regulation/pdf/EMC_Standards_List.pdf?la=en.[Accessed: 18-May-2018].

[21] IEC. “Guidance for users of the CISPR Standards,” 2016 [Online]. Available: http://www.iec.ch/emc/pdf/cispr_guide_2015.pdf. [Accessed: 18-May-2018].

[22] M. O. Hara, “A generic automotive EMC test standard,” [Online]. Available: http://www.autoemc.net/Standards/2000TS0DR%20Generic%20EMC%20Specification.pdf. [Access ed: 18-May-2018].

[23] CISPR 32, “Electromagnetic compatibility of multimedia equipment – Emission requirements,” [Online]. Available: https://infostore.saiglobal.com/preview/293330663163.pdf?sku=101079_SAIG_AS_AS_212367. [Accessed: 12-Oct-2018].

[24] K. Mainali and R. Oruganti, “Conducted EMI mitigation techniques for switch-mode power converters: A survey,” *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2344–2356, 2010.

[25] M. Hartmann, H. Ertl, and J. W. Kolar, “EMI filter design for a 1 MHz, 10 kW three-phase/level PWM rectifier,” *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1192–1204, 2011.

[26] I. A. Makda and M. Nymand, “Differential mode EMI filter design for ultra high efficiency partial

parallel isolated full-bridge boost converter," *Proc. Int. Conf. Power Electron. Drive Syst.*, no. 75, pp. 99–103, 2013.

[27] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, 2010.

[28] Y. Chu, S. Wang, and Q. Wang, "Modeling and stability analysis of active/hybrid common-mode EMI filters for DC/DC power converters," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6254–6263, Sep. 2016

[29] W. Chen, X. Yang, and Z. Wang, "An active EMI filtering technique for improving passive filter low-frequency performance," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, pp. 172–177, 2006.

[30] M. Esteki, M. Mohammadi, M. R. Yazdani, E. Adib, and H. Farzanehfard, "Family of soft-switching pulse-width modulation converters using coupled passive snubber," *IET Power Electron.*, vol. 10, no. 7, pp. 792–800, 2017.

[31] H. Chung, S. Y. R. Hui, and K. K. Tse, "Reduction of power converter EMI emission using soft-switching technique," *IEEE Trans. Electromagn. Compat.*, vol. 40, no. 3, pp. 282–287, 1998.

[32] G. Hua and F. C. Lee, "Soft-Switching Techniques in PWM Converters," *IEEE Trans. Ind. Electron.*, vol. 42, no. 6, pp. 595–603, 1995.

[33] J. Shao, R. L. Lin, F. C. Lee, and D. Y. Chen, "Characterization of EMI performance for hard and soft-switched inverters," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, vol. 2, no. 1, pp. 1009–1014, 2000.

[34] K. K. Tse, H. S. H. Chung, S. Y. R. Hui, and H. C. So, "A comparative study of carrier-frequency modulation techniques for conducted EMI suppression in PWM converters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 3, pp. 618–627, 2002.

[35] F. Mihalic and D. Kos, "Reduced conductive EMI in switched-mode DC–DC power converters without EMI filters: PWM versus randomized PWM," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1783–1794, Nov. 2006.

[36] G. M. Dousoky, M. Shoyama, and T. Ninomiya, "FPGA-Based spread-spectrum schemes for conducted-noise mitigation in DCDC power converters: Design, implementation, and experimental investigation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 429–435, 2011.

[37] C. Qi, X. Chen, and Y. Qiu, "Carrier-based randomized pulse position modulation of an indirect matrix converter for attenuating the harmonic peaks," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3539–3548, 2013.

[38] A. M. Stankovic, "Random Pulse Modulation with Applications to Power Electronic Converters," Ph.D. dissertation, Dept. Elect Eng and Comp. Sci, MIT, 1993.

[39] B. Zhang and X. Wang, Chaos Analysis and Chaotic EMI Suppression of DC–DC Converters. Hoboken, NJ, USA: Wiley, 2014.

[40] F. Costa and D. Magnon, "Graphical analysis of the spectra of EMI sources in power electronics," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1491–1498, 2005.

[41] A. M. Stankovic, G. C. Verghese, and D. J. Perreault, "Analysis and synthesis of randomized modulation schemes for power converters," IEEE Trans. Power Electron., vol. 10, no. 6, pp. 680–693, Nov. 1995.

[42] M. M. Bech, "Analysis of random pulse-width modulation techniques for power electronic converters," Ph.D. dissertation, Aalborg Univ., Aalborg, Denmark, 2000, ISBN: 87-89179-32-3.

[43] H. D. T. Mouton, B. McGrath, D. G. Holmes, and R. H. Wilkinson, "One-dimensional spectral analysis of complex PWM waveforms using superposition," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6762–6778, 2014.

[44] S. U. Hasan and G. E. Town, "An Aperiodic Modulation Method to Mitigate Electromagnetic Interference in Impedance Source DC–DC Converters," *IEEE Trans. Power Electron.,* vol. 33, no. 9, pp. 7601-7608, Sept. 2018.

[45] D. González *et al.*, "Conducted EMI reduction in power converters by means of periodic switching frequency modulation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2271–2281, 2007.

[46] S. Mohseni and A. Roomizadeh, "Study on periodic and non periodic frequency modulation techniques for EMI suppression in SMPS," *2011 2nd Power Electron. Drive Syst. Technol. Conf. PEDSTC 2011*, no. 3, pp. 615–619, 2011.

[47] Santolaria, J. Balcells, D. González, and J. Gago, "Evaluation of switching frequency modulation in EMI emissions reduction applied to switching power converters," in *Proc. 29th Annu. Conf. IEEE Ind. Electron. Society, IECON 2003*, pp. 2306–2311.

[48] K. K. Tse, H. S. H. Chung, S. Y. Hui, and H. C. So, "Analysis and spectral characteristics of a spread-spectrum technique for conducted EMI suppression," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 399–410, 2000.

[49] H. Li, Z. Li, B. Zhang, F. Wang, N. Tan, and W. A. Halang, "Design of analogue chaotic PWM for EMI suppression," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 1001–1007, 2010.

[50] H. Li, Y. Liu, J. Lu, T. Zheng, and X. Yu, "Suppressing EMI in power converters via chaotic SPWM

control based on spectrum analysis approach," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 6128–6137, 2014.

[51] P. Glendinning, "Chaos" in *Stability, Instability and Chaos: An Introduction to the Theory of Nonlinear Differential Equations*, 1st ed. New York, NY, USA: Cambridge Univ. Press, 1994.

[52] K. Kyamakya, W. Mathis, R. Stoop, J.C. Chedjou, Z. Li, "*Recent Advances in Nonlinear Dynamics and Synchronization*", vol. 109. Springer, 2017.

[53] S. U. Hasan and G. E. Town, "Modulation method and apparatus to reduce EMI in a power converter," AU Patent WO2017120644 A1, Jan. 15, 2016 "WO2017120644-PDOC-142.pdf.".

[54] S. U. Hasan and G. E. Town, "A quasi-periodic modulation strategy to mitigate EMI for a GaN-based quasi-Z-source DC-DC converter," *ECCE 2016 - IEEE Energy Convers. Congr. Expo. Proc.*, 2016.

[55] S. U. Hasan and G. E. Town, "An FPGA-based aperiodic modulation strategy for EMI suppression in quasi-Z-source DC-DC converters," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017.

[56] Z. Song and D. V. Sarwate, "The Frequency Spectrum of Pulse Width Modulated Signals (preprint)," *Elsevier - Signal Process.*, vol. 83, no. June 2003, pp. 2227–2258, 2003.

[57] Z. Ghassemlooy, "Pulse position modulation spectral investigation," *Int. J. Electron.*, vol. 74, no. 1, pp. 153–158, 1993.

[58] E. Fitch, "The spectrum of modulated pulses," *J. Inst. Electr. Eng. - Part IIIA Radiocommun.*, vol. 94, no. 13, pp. 556–564, 1947.

[59] D. J. Perreault *et al.*, "Opportunities and Challenges in Very High Frequency Power Conversion," *2009 TwentyFourth Annu. IEEE Appl. Power Electron. Conf. Expo.*, vol. 1926, pp. 1–14, 2009.

[60] J. Betten, "Benefits of a coupled-inductor SEPIC converter," *Analog Appl. J. Texas Instruments Inc.*, pp. 7–19, 2011.

[61] GaN Systems. "GS61008P 100V Enhancement Mode GaN Transistor," [Online]. Available: https://gansystems.com/gan-transistors/gs61008p/ [Accessed: 18-May-2018].

[62] K. Zou, M. J. Scott, and J. Wang, "Switched capacitor cell based dc-dc and dc-ac converters," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 224–230.

[63] J. (Texas I. I. Falin, "Designing DC / DC converters based on SEPIC topology," *Analog Appl. J.*, pp. 18–23, 2008.

[64] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4,

pp. 2008–2015, 2014.

[65] W. Kangping, M. Huan, L. Hongchang, G. Yixuan, Y. Xu, Z. Xiangjun, and Y. Xiaoling, "An optimized layout with low parasitic inductances for GaN HEMTs based DC-DC converter," in Proc. *Appl. Power Electron. Conf. Expo.,* Mar. 2015, pp. 948–951.

[66] A. M. Trzynadlowski, F. Blaabjerg, J. K. Pedersen, R. L. Kirlin, and S. Legowski, "Random pulse width modulation techniques for converter-fed drive\nsystems-a review," *IEEE Trans. Ind. Appl.*, vol. 30, no. 5, pp. 1166–1175, 1994.

[67] S. U. Hasan, Y. R. Kafle, and G. E. Town, "Simple spread-spectrum pulse-modulation technique for EMI mitigation in power converters," in *2017 Australasian Universities Power Engineering Conference (AUPEC)*, 2017, pp. 1–5.

[68] TI , "Peripheral Explorer Kit Overview" [Online]. Available: http://www.ti.com/lit/ml/sprugm2a/sprugm2a.pdf [Accessed: 18-May-2018].

[69] Y. Li, J. Anderson, F. Z. Peng, and D. Liu, "Quasi-Z-Source Inverter for Photovoltaic Power Generation Systems," in *Proc. 24th Annu. Applied Power Electronics Conf. Expo. (APEC 2009)*, 15–19 Feb. 2009, pp. 918–924.

[70] D. Vinnikov and I. Roasto, "Quasi-Z-Source-based isolated DC/DC converters for distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 192–201, 2011.

[71] S. U. Hasan, Y. R. Kafle, and G. E. Town, "Aperiodic pulse-modulation technique to reduce peak EMI in impedance-source DC-DC converters," in *Proc. IEEE Energy Convers. Congr. Expo. ECCE*, pp. 5369–5374, 2017.

[72] Fang Zheng Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, 2003.

[73] J. Anderson and F. Z. Peng, "Four quasi-Z-Source inverters," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, pp. 2743–2749, 2008.

[74] Y. P. Siwakoti and G. Town, "Improved modulation Technique for voltage fed quasi-Z-source DC/DC converter," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 1973–1978, 2014.

[75] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion Part I: A topological review," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, 2015.

[76] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, and S. Yang, "Impedance-source networks for electric power conversion part II: Review of control and modulation techniques," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1887–1906, 2015.

[77] Transphorm. “TPH3006PS,” [Online]. Available: https://www.transphormusa.com/sites/default/files /public/TPH3006PS.pdf [Accessed: 18-May-2018].

[78] I. Roasto, L. Liivik, and D. Vinnikov, “Control of quasi-Z-source DC-DC converter by the overlap of active states: New possibilities and limitations,” *Proc. Bienn. Balt. Electron. Conf. BEC*, vol. 2015–Novem, pp. 217–220, 2014.

[79] D. Vinnikov, I. Roasto, L. Liivik, and A. Blinov, “Four novel PWM shoot-through control methods for impedance source DC-DC converters,” *J. Power Electron.*, vol. 15, no. 2, pp. 299–308, 2015.

[80] I. Roasto, D. Vinnikov, J. Zakis, and O. Husev, “New shoot-through control methods for qZSI-based DC/DC converters,” *IEEE Trans. Ind. Informatics*, vol. 9, no. 2, pp. 640–647, 2013.

[81] I. Roasto and D. Vinnikov, “Analysis and evaluation of PWM and PSM shoot-through control methods for voltage-fed qZSI based DC/DC converters,” *Proc. EPE-PEMC 2010 - 14th Int. Power Electron. Motion Control Conf.*, pp. 100–105, 2010.

[82] T. Jalakas, M. Jarkovoi, I. Roasto, J. Zakis, and A. Garganeev, “Investigation of radiated emissions of a galvanically isolated qZS DC-DC converter,” *Int. Conf. Power Eng. Energy Electr. Drives*, vol. 2015–Septe, pp. 176–181, 2015.

[83] Y. P. Siwakoti and G. E. Town, “Design of FPGA-controlled power electronics and drives using MATLAB Simulink,” *2013 IEEE ECCE Asia Downunder - 5th IEEE Annu. Int. Energy Convers. Congr. Exhib. IEEE ECCE Asia 2013*, pp. 571–577, 2013.

[84] C. Li *et al.*, “A 2 kW Gallium Nitride based switched capacitor three-port inverter,” *Wide Bandgap Power Devices Appl. WiPDA 2013 - Proc.*, pp. 119–124, 2013.

[85] M. J. Scott, K. Zou, E. Inoa, R. Duarte, Y. Huang, and J. Wang, “A Gallium Nitride switched-capacitor power inverter for photovoltaic applications,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 46–52, 2012.

[86] M. J. Scott, “Applications, Benefits , and Challenges of Wide Bandgap Based Power Inversion,” Ph.D dissertation, Dept. Elec. & Comp. Eng., Ohio State University, 2015.

[87] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, “A new design method for high-power high-efficiency switched-capacitor DC-DC converters,” *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 832–840, 2008.

[88] M. D. Seeman and S. R. Sanders, “Analysis and optimization of switched-capacitor DC-DC converters,” *IEEE Trans. Power Electronics*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[89] S. U. Hasan, B. Shaffer, H. A. Hassan, M. J. Scott, Y. Siwakoti, and G. E. Town, “Common-Ground

Transformerless Inverter for Solar Photovoltaic Module," in *Proc. - IEEE Appl. Power Electron. Conf. Expo. APEC.,* pp. 167–172, 2018.

[90] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology," *IEEE Ind. Electron. Mag.*, vol. 9, no. 1, pp. 47–61, 2015.

[91] "Global Market Outlook for Solar Power 2017-2021," Jun. 2015 [Online]. Available: http://www.solarpowereurope.orgSolarPower Europe.

[92] T. Kerekes, R. Teodorescu, and M. Liserre, "Common mode voltage in case of transformerless PV inverters connected to the grid," *IEEE Int. Symp. Ind. Electron.*, pp. 2390–2395, 2008.

[93] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems-an overview," in *Proc. IEEE International Symposium on Industrial Electronics. ISIE'98* , vol. 1, pp. 224–229.

[94] G. Vazquez, P. R. Martinez-Rodriguez, J. M. Sosa, G. Escobar, and M. A. Juarez, "Transformerless single-phase multilevel inverter for grid tied photovoltaic systems," in Proc. *Industrial Electron. Conf. IECON*, 2014, pp. 1868–1874.

[95] T. Kerekes, *Analysis and Modeling of Transformerless Photovoltaic Inverter*, Ph.D. dissertation, Institut for Energiteknik, Aalborg Univ., Aalborg, Denmark, 2009.

[96] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, 2010.

[97] Ó. López *et al.*, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, 2010.

[98] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, 2012.

[99] X. Huafeng, X. Shaojun, C. Yang, and H. Ruhai, "An Optimized Transformerless Photovoltaic Grid-Connected Inverter," *Ind. Electron. IEEE Trans.*, vol. 58, no. 5, pp. 1887–1895, 2011.

[100] B. Ji, J. Wang, and J. Zhao, "High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 2104–2115, 2013.

[101] Y. R. Kafle, G. E. Town, X. Guochun, and S. Gautam, "Performance comparison of single-phase transformerless PV inverter systems," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo.*, pp.

3589–3593, 2017.

[102] S. V. Araújo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3118–3128, 2010.

[103] J. F. Ardashir, Y. P. Siwakoti, M. Sabahi, S. H. Hosseini, and F. Blaabjerg, "S4 grid-connected single-phase transformerless inverter for PV application," *IECON Proc. (Industrial Electron. Conf.*, pp. 2384–2389, 2016.

[104] Q. C. Zhong and W. L. Ming, "A Θ-Converter That Reduces Common Mode Currents, Output Voltage Ripples, and Total Capacitance Required," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8435–8447, 2016.

[105] M. Gommeringer, F. Kammerer, A. Schmitt, and M. Braun, "A transformerless single-phase PV inverter circuit for thin-film or back-side contacted solar modules," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 1148–1153.

[106] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, 2013.

[107] Y. P. Siwakoti and F. Blaabjerg, "Common-ground-type transformerless inverters for single-phase solar photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100–2111, 2018.

[108] A. Kaknevicius and A. Hoover, "Managing Inrush Current," [online]: http://www.ti.com /lit/an/slva670a/slva670a.pdf [Accessed 11th Jan, 2018].

[109] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei, and G. B. Gharehpetian, "A Single-Phase Transformerless Inverter with Charge Pump Circuit Concept for Grid-Tied PV Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5403–5415, 2017.

[110] M. Tofigh Azary, M. Sabahi, E. Babaei, and F. Abbasi Aghdam Meinagh, "Modified Single-Phase Single-Stage Grid-Tied Flying Inductor Inverter With MPPT and Suppressed Leakage Current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 221–231, 2018.

[111] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron.,* vol. 28, no. 2, pp. 730–739, Feb. 2013.

[112] Transphorm. "TPD3215M, GaN Power Hybrid HEMT Half - Bridge Module," [online]:http://www. transphormusa.com/document/datasheet-tpd3215m-600v-cascode-gan-module/[Accessed 11th Jan,

2018].

[113] M. Islam, S. Mekhilef, and M. Hasan, "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review," *Renew. Sustain. Energy Rev.*, vol. 45, pp. 69–86, 2015.

[114] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li and X. He, "Transformerless inverter with virtual DC bus concept for cost-effictive grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793-805, Feb. 2013.

[115] M. Islam, N. Afrin, and S. Mekhilef, "Efficient Single Phase Transformerless Inverter for Grid-Tied PVG System with Reactive Power Control," *IEEE Trans. Sustain. Energy*, vol. 7, no. 3, pp. 1205–1215, 2016.

[116] Fluke, "Principles, testing methods and applications," [online]: http://support.fluke.com/findsales/Download/Asset/2633834_6115_ENG_A_W.pdf [Accessed 11th Jan, 2018].

[117] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A New high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, 2011.

[118] N. Seshasayee, "Understanding Thermal Dissipation and Design of a Heatsink," *TI, Texas Instruments*, no. May, pp. 1–4, 2011.

[119] Com-Power Corporation. "Line Impedance Stabilization Network,", LI-550A, [online]: https://www.compower.com/datasheets/LI-550A.pdf [Accessed 11th Jan, 2018].

[120] B. Shaffer, H. A. Hassan, M. J. Scott, S. U. Hasan, and G. E. Town, "A Common-Ground Single-Phase Five-Level Transformerless Boost Inverter for Photovoltaic Applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. APEC*, pp. 368–374, 2018