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Long-Term Degradation Effects in Power Amplifiers: Analysis, Modelling and Remedies

A thesis for the Master of Research degree

By

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The work presented in this thesis was carried out at the Department of Engineering, Macquarie University, Sydney, Australia, between February and November 2018. This work was principally supervised by Dr. Sourabh Khandelwal. To the best of my knowledge, the materials presented in this thesis, which are considered as thesis's novelty, are original and has not been submitted in whole or part for a degree in any other university or institution other than Macquarie University. The whole information obtained from other publications are all referred in the text and corresponding references are mentioned at the end of thesis.

Hossein Eslahi

Acknowledgments

I would like to express my deepest and sincerest gratitude to my principal supervisor, Dr. Sourabh Khandelwal, for his excellent support and quality supervision during this research work. I highly acknowledge his invaluable guidance and encouragement for successful and timely completion of this milestone.

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List of Publications

- **H. Eslahi**, A. Bahrani, D. Mahajan, S. Khandelwal, "An Analytical and Theoretical Age model to Predict Reliability of Classic Power Amplifiers", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 2018 (Submitted).

- **H. Eslahi**, A. Bahrani, D. Mahajan, S. Khandelwal, "A Tuneable Input-Impedance Matching Approach for Long-term Degradation effects of Power Amplifier", *IEEE International RF and Microwave Conference (RFM)*, Penang, Malaysia, 2018.

- D. Mahajan, A. Bahrani, **H. Eslahi**, S. Khandelwal, "A Study of Hard Switching Characteristics of GaN-based DC-DC Boost Power Converter using ASM-GaN Compact Model," *Australian Universities Power Engineering Conference (AUPEC)*, Auckland, New-Zealand, 2018.

Abstract

The wireless communication systems seen with an impressive progress over the last decades. To continue this progress and reach better performance, device dimensions should be down-scaled and this downward trend causes several effects which lead to less reliable systems. The reliability problems are more severe in high frequencies which degrades performance. To address this looming challenge this thesis proposed a new concept of "Reliability-Aware Design". This thesis shows that there exist trade-offs between performance and reliability. If reliability is considered from the beginning of the design phase, intelligent sweet-spots can be identified which deliver both reasonable performance and reliability. Among different RF circuits, power amplifier (PA) is more vulnerable to degradation since it must deliver high power to a load. Therefore, we focus our work on PA's. The aim of this thesis is to describe physical and analytical model for PA reliability which clearly shows the trade-offs with performance in the design phase of PAs.

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Chapter 1

Introduction

1.1 Background

Wireless communication systems have made impressive progress over the last decades. Hardly a month goes without a new report about new applications of integrated circuits (ICs) published in the media. To continue this ever-growing progress, reach better performance (like greater speed, better frequency response), and integrate all the different parts of a transceiver into a single chip, down-scaling of device dimensions is inevitable as predicted by Moore's law. However, this downward trend in devices dimension causes them to face several challenges such as short-channel effects, higher electric field on a transistor's channel, trapping charges into gate insulator, breakdown, etc. The overall performance, as a consequence, will degrade. So, device reliability has become a complex problem during the design and modelling process [1-4].

It is anticipated that radio-frequency (RF) circuit performance also degrades after device degradation due to scaling, stress and ageing. To further clarify this, note that circuit performance (noise figure, linearity, gain, matching, etc.) are all functions of device DC parameters such as the threshold voltage (V_{th}), mobility (μ_0), transconductance (g_m), and small-signal characteristics like gate-source (C_{gs}) and gate-drain (C_{gd}) capacitors. Therefore, device degradation imposes degradation of circuit performance. This unwanted degradation will be more catastrophic when the devices work at radio frequencies where they operate under both DC and AC stresses [1-3].

The most important physical mechanisms responsible for device degradation are Hot-Carrier Injection (HCI) due to a high lateral field in short-channel devices, Time-Dependent Dielectric Breakdown (DB) favoured by a high vertical field in thin oxide layers, and Bias Temperature

Instability (BTI). The former is becoming a first-order concern for RF applications, which can also accelerate breakdown phenomena [3, 5-10].

Among RF circuits, power amplifiers (PAs) are more vulnerable to hot-electron effects. This is because, due to the necessity of delivering high power to a load, the drain voltage in PAs can experience unusual peak values, even more than twice the supply voltage [5-7, 11]. Degradation of a power amplifier, being a main part of a transceiver chain, can also affect the overall performance of a transceiver. However, none of the research, published in the literature, has compared the classic classes of PA in terms of reliability. Those studies are restricted to three main fields, namely (i) DC/RF stress effects on device and circuit reliability, (ii) high-temperatures effects, and (iii) a circuit modification approach to mitigate long-term degradation in RF devices and circuits [6, 12-20]. Therefore, analytically modelling reliability in power amplifiers could be an innovative research topic. In addition, if reliability is considered at early steps of a design phase, intelligent sweet-spots can be identified, reasonable performance and reliability can be delivered, and looming challenges can be addressed.

Two main steps in reliability evaluation in RF circuits are to analyse degradation mechanisms and then to find a precise age model to predict the degradation of devices. It is valuable to solve these models and analytically investigate circuit reliability without repeating time-consuming simulations by the RelXpert simulator. All reliability models, therefore, should be solved using numerical solutions, as is performed in the RelXpert simulator. The aim of this thesis is to describe a physical and analytical age model for PA degradation which clearly shows the trade-offs with PA performance. This predictive model is a function of conduction angle and, therefore, it is valid for the different classes of PAs. Based on the results shown in this thesis, it is claimed that reliability must be considered as one of the key design parameters and, therefore, a new concept of "Reliability-Aware Design" is formed.

1.2 Motivation and Objectives

The automotive industry has recently become one of the main areas for making use of RF integrated circuits (RFICs). Almost all electrical systems in smart cars, such as engine controllers, air bags and assistance systems utilise ICs. In addition, safety and convenience are two important issues that should be met in this new generation of cars so automotive electronics requires a high level of reliability. Air bags, for instance, are critical for occupant safety, making their reliability vital. This problem becomes more critical when an inordinate number of cars are fabricated annually and a simple failure in device operation, induced by ageing and/or stress, may cause

heavy economic-loss. Clearly, considering device and circuit reliability during the design process can enhance the quality of products and decrease the economic losses. Besides, since there is little research in the field of circuit reliability modelling, it seems clear that much further research is needed on this topic.

1.3 Thesis Structure and Outcomes

This dissertation is divided into six chapters, the first of which is this introductory chapter, and it will be terminated by a conclusion of the whole thesis in Chapter 6. The other chapters forming the main body of the thesis are organised as follows.

A brief overview of the most well-known device degradation mechanisms (HCI, BTI, TDDB), their origin, and their effects on device performance will be presented in Chapter 2.

In Chapter 3 some models developed in the literature to predict device degradation due to static (DC) and dynamic (AC/ RF) stresses are presented. Using static models leads to wrong results, as reliability is supposed to be studied under time-varying bias conditions. Therefore, a "Quasi-Static" approach is introduced as a good approximation to create AC models based on DC counterparts. However, at the end of this chapter, one can conclude that none of the current models are applicable to predict reliability in PAs as a function of conduction angle, since they are developed at the device level.

Chapter 4 addresses this problem by describing a new degradation model which can precisely forecast PA ageing. This model is a strong function of conduction angle and can be applied to all classes of power amplifiers. A new trade-off between reliability and PA performance is introduced which helps designers to meet the needs of suitable efficiency, high output power, and reliability at the same time.

The question may come into mind whether there exist solutions to mitigate long-term degradation after the design steps. A circuit-design approach is, therefore, introduced in Chapter 5 based on variable capacitors. This approach, despite its simplicity, can be a good idea to compensate for transistor ageing and enhance circuit performance even after design process.

Three publications which have been extracted from this work are:

- **H. Eslahi**, A. Bahrani, D. Mahajan, S. Khandelwal, "An Analytical and Theoretical Age model to Predict Reliability of Classic Power Amplifiers", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 2018 (Submitted).

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Chapter 2

Degradation Mechanisms

2.1 Chapter Abstract

Recognition of the physical mechanisms responsible for device degradation is important before reliability modelling. This chapter, therefore, represents a brief overview of the main degradation mechanisms as the first step of a reliability study. Then, the correlation between circuit degradation and device degradation will be explained.

2.2 Introduction

In addition to Hot-Carrier Injection (HCI), Time-Dependent Dielectric Breakdown (TDDB), and Bias Temperature Instability (BTI) which are considered as prominent mechanisms causing device degradation [3, 7-10], new materials, higher temperatures, high currents, electro-migration phenomena, and sub-threshold leakage currents are other mechanisms can lead to reliability issues [4, 9, 11, 21]. However, these factors do not impose as catastrophic failures as the first three mechanisms on device operation. In addition, it is repeated in several references that ***TDDB may not have a significant impact on RF circuits in nominal operating conditions*** [6, 9, 22]. Therefore, only HCI and BTI degradation mechanisms are evaluated in detail in this chapter.

2.3 Hot-Carrier Injection

Hot-Carrier Injection (HCI) is a classic problem for all technologies like CMOS transistors, and is a consequence of both DC (static) and AC/RF (dynamic) stress conditions. The aggressive

down-scaling of the channel length of CMOS devices results in a higher electric field being experienced by the electrons in the channel. Then, these electrons become highly energetic and some of these energetic electrons (called hot electrons) can reach and get trapped within the oxide layer, raising the threshold voltage (V_{th}) of these devices and reducing the effective mobility, yielding a decrease in the drain current (I_d) and transconductance (g_m). The increase in V_{th} and degradation of g_m and I_d can also degrade other DC characteristics, like linear ($I_{d(lin)}$) and saturated ($I_{d(sat)}$) currents ,and small-signal elements such as gate-source and gate-drain capacitances (C_{gs} and C_{gd}) [3, 5, 6, 8, 9, 23]. Some examples of these degradations are shown in Figures 2.1 and 2.2 [3, 23].

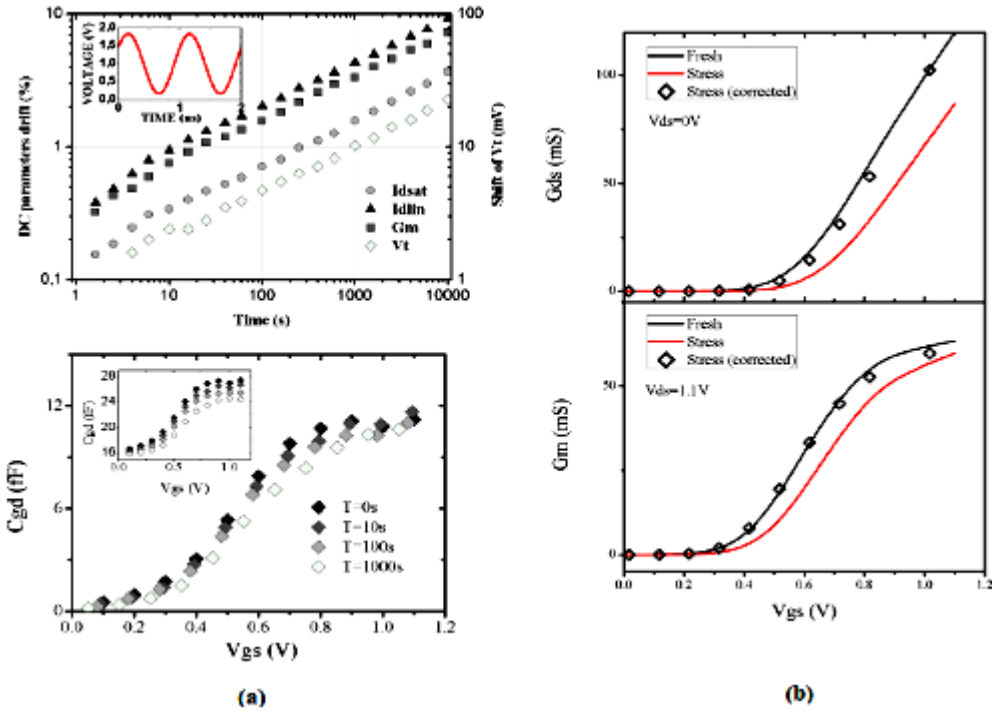

Figure 2.1: a) Drift of main DC parameters and C_{gd} as a function of V_{gs} and time after applying supply voltage $V_{ds} = 1V$ and bias voltage $V_{gs} = 1.8\,V$ to a nMOSFET with gate length $L = 40\,nm$, total gate width $W = 57.6\,um$ and number of fingers $N = 10$. b) drift of other small-signal parameters vs V_{gs}. The symbols in (b) represent parameters after devices correction [23].

From Figure 2.3 representing simulation results for a nFinFET, hot-carrier degradation (HCD) is an irreversible phenomenon even after removing stress [7]. In [10] the results for the degradation of the DC parameters, C_{gd}, and C_{gs} as a function of stress time and frequency, which are obtained after applying DC and AC stress to a BSIM3V3 model, are represented (see Figure 2.4). These data explain that the drain-current degradation due to DC stress is worse than that due to AC (dynamic) stress, but all the drain currents shift downward after stress. A summary of the parameter shifts in a BSIM3v3 after DC and AC stresses is also expressed in Table 2.1.

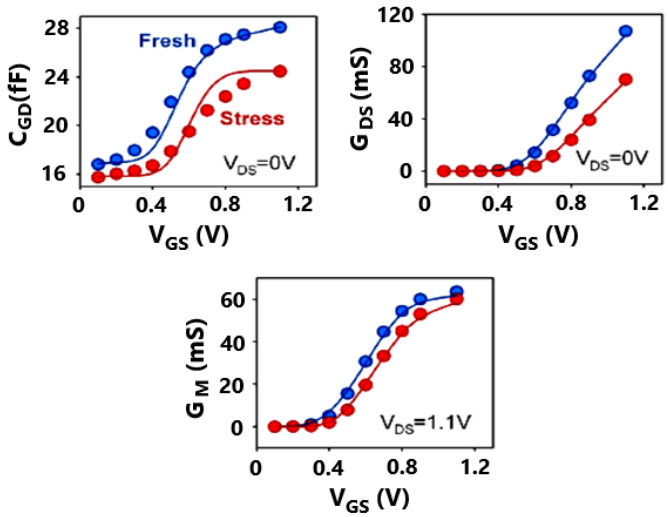

Figure 2.2: Small-signal parameter degradation under stress [3].

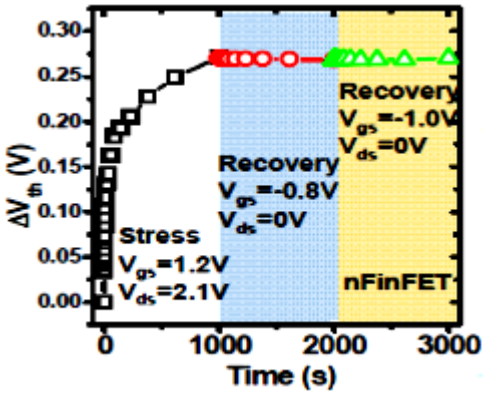

Figure 2.3: Simulation result showing that the HCD cannot be recovered after removing stress [7].

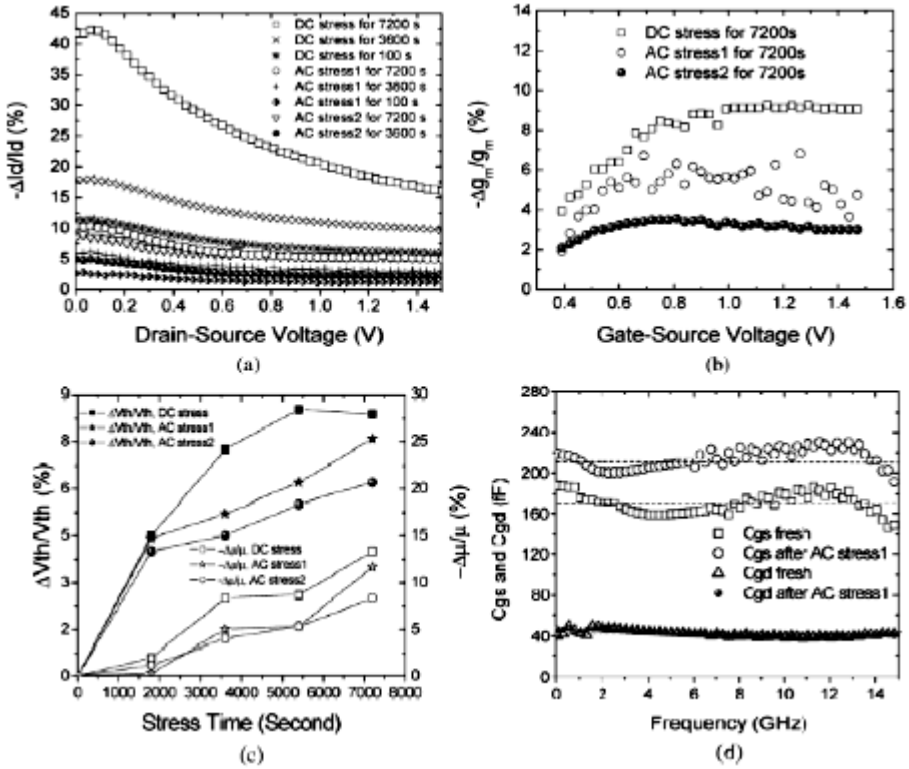

Figure 2.4: Comparison between DC and AC stress-induced degradation of DC and small-signal parameters [10].

Table 2.1: Parameter degradation for BSIM3V3 model after DC and AC stress [10].

Parameter Shift	DC stress (%)		AC stress (%)	
	For 1 hour	For 2 hours	For 1 hour	For 2 hours
ΔC_{gs}	23	32	14.31	26.47
ΔC_{db}	12.38	26	12.6	17.90
$-\Delta R_{db}$	15.86	27	13.8	20.00
$-\Delta R_{dsb}$	14.12	25.68	15	20.00
ΔR_d	11.98	16.78	8.34	12.50
ΔR_g	12.17	18.56	9.36	14.08
$-\Delta R_s$	42.86	56.00	36	50.00
ΔV_{th}	7.98	8.52	5.50	8.06
$-\Delta\mu$	8.00	12.28	5.00	11.8
$\Delta NFactor$	4.62	5.58	2.89	3.08
$-\Delta K1$	0.83	1.67	-0.76	1.26
$-\Delta U_a$	12.21	19.92	3.61	5.27
ΔV_{off}	4.31	5.73	1.68	2.29

2.4 Bias Temperature Instability (BTI)

A transistor shows changes in its characteristics initiated by temperature and bias-voltage variation over the long term. This effect is termed bias temperature instability (BTI) and can gradually degrade V_{th} [2, 9, 22, 24]. The effectiveness of BTI is different for P- and N-type FETs and it is proved that at Nano-scale, NBTI (N-type BTI) in PMOSFETs is more critical than PBTI (P-type BTI) for NMOSFETs [2, 22]. Although BTI reliability in both cases (NBTI and PBTI) has been well understood in planar devices, these phenomena can affect non-planar FETs in some cases like geometry, structure and technology. Therefore, they must be investigated in detail but there is little research about, for example, NBTI effects in PMOSFETs [22].

It is proved that the BTI is a recoverable degradation-mechanism [2, 7, 9]. As an example, Figure 2.5 (a) shows such behaviour for threshold voltage variation after NBTI degradation. It is also seen from this figure that BTI is temperature-dependent [2]. In the next chapter, relevant age models will be presented which quantify this recoverable behaviour. Finally, several simulations were performed in [22] to evaluate the time dependency of NBTI degradation under RF and DC stress. The results are shown in Figure 2.5 (b) for RF stress and the same results can be obtained after DC stress. It is clear from this figure that there is no significant difference in the time exponent between DC and RF NBTI degradations.

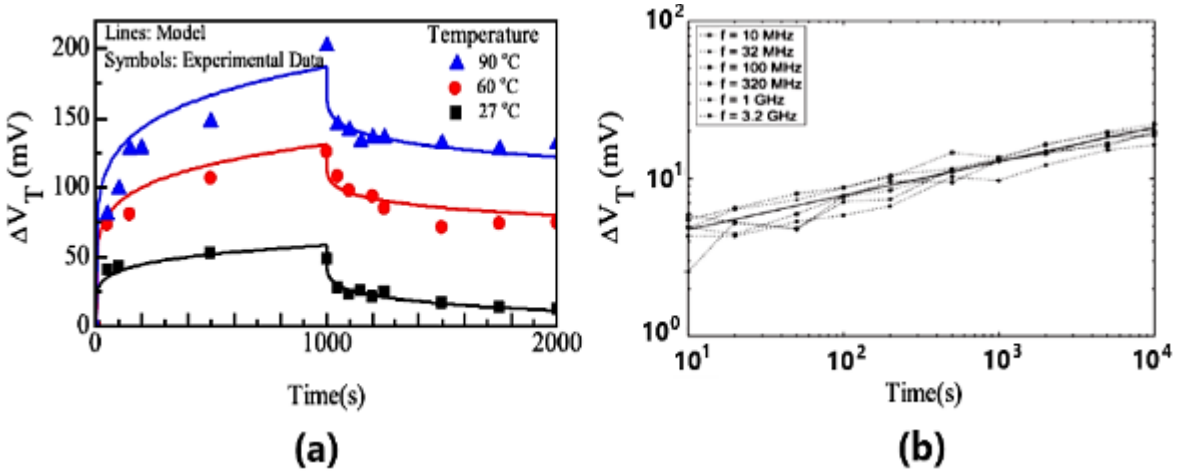

Figure 2.5: a) Degradation of threshold voltage and recovery for NBTI stress (stress voltage $V_{gs} = -4.5\ V$) at various temperatures [2], b) the threshold voltage degradation after RF NBTI stress as a function of stress time for a 90 nm p-MOSFET with channel length equal to 100 nm [22].

2.5 Comparison between BTI and HCI

Similarly to hot-carrier degradation, NBTI induced parameter shift follows a power law (which will be discussed in the next chapter) and both get worse with rising temperature. Another similarity between BTI and HCI is their frequency dependency. Some researchers believe that no frequency dependence should be found based on the reaction–diffusion model [22, 25]. The results presented in Figure 2.6, obtained under HCI and NBTI stresses, clarify this concept. As shown in this figure, no frequency dependence exists in the amount of V_{th} and saturation current, $I_{D(sat)}$ degradation. However, there are some controversial claims in the other references. For instance, it is argued in [26, 27] that the recovery mechanism can completely or partly be attributed to the de-trapping of holes in deep oxide traps and, under this assumption, some frequency dependence may be expected.

One of the differences between HCI and BTI is their behaviour during and after stress. It was shown that BTI, unlike HCI, exhibits a peculiar property of recovery when stress is removed, and device parameters can recover towards their initial unstressed value [2, 9, 22]. In terms of degradation rate, Figure 2.7 (a) shows a map displaying the HCI/NBTI degradation ratio in a P-FinFET over the whole V_{gs}/V_{ds} region. The results show that HC degradation will become larger and more catastrophic than NBTI when V_{ds} is increased. Moreover, HCI will gradually overtake NBTI as time increases, due to different degradation rates. The same results can be obtained for an N-FinFET (Figure 2.7 (b)), except that PBTI degradation is actually very small in FinFET technology [7]. Eventually, a comparison between the effects of HCI and BTI stresses on the main parameters of an InGaAs n-MOSFET is presented in Table 2.2 [24].

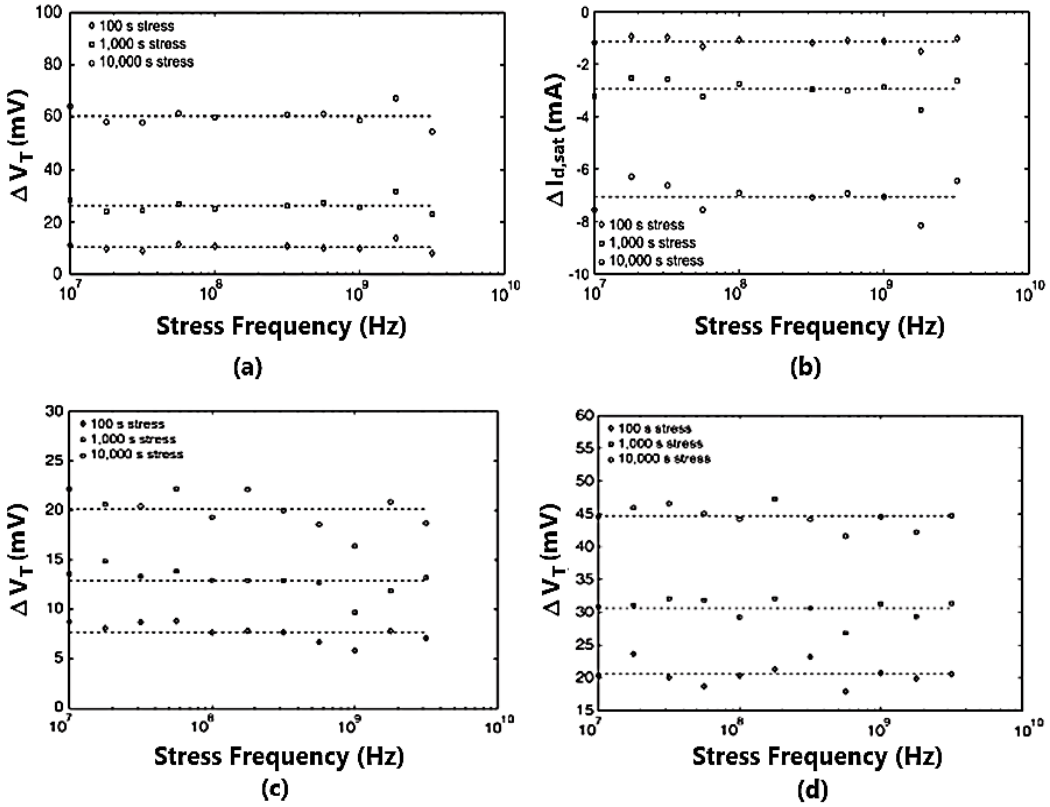

Figure 2.6: Hot-carrier induced degradation of a) V_{th} and b) $I_{D(sat)}$, and V_{th} degradation plotted against frequency for c) a 90 nm p-MOSFET and d) 130 nm p-MOSFET devices after RF NBTI stress as functions of frequency (the dashed lines are meant as a guide to the eye) [22].

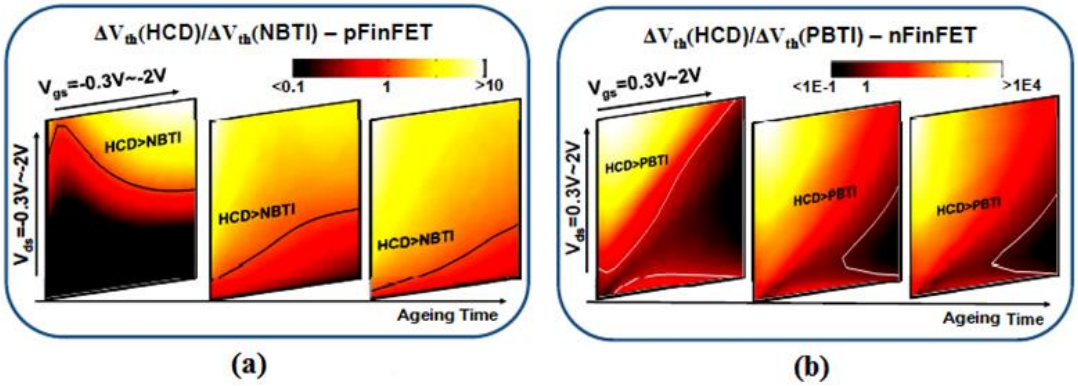

Figure 2.7: HC/BTI degradation ratio for a) P-FinFET and b) N-FinFET [7].

2.6 Circuit Degradation due to HCI and BTI

All the building blocks in a receiver chain (LNA, power amplifier, Mixer, Oscillator, etc.) are designed with their own figure of merit. For example, gain, linearity, input and output return loss, overall noise figure (NF), minimum noise figure (NF_{min}), and power consumption measure LNA performance while power-added efficiency (PAE), drain efficiency (η), ACPR, NPR, maximum power delivered to load, and linearity are considered as Power Amplifier (PA) performance measures [16, 28, 29, 30]. These figures of merit are defined by device DC and small-signal characteristics. To put it another way, the overall gain in a cascode topology is a product of the

effective transconductance of the first stage and the output impedance, while both are calculated by small-signal ($g_m, g_{ds}, C_{gs}, C_{gd}, \ldots$) elements. The degradation of DC parameters like the threshold voltage and mobility also change the overall drain current and, consequently, the effective transconductance. Therefore, there is a strong correlation between device and circuit degradation. In the following sub-sections this correlation is discussed more clearly in LNAs and PAs.

Table 2.2: Key-parameter shift after HCI and BTI stresses [24].

Unstressed	V_{th} [V] *	DC $- g_{max}$ $[mS/\mu m]$ *	$max\ f_t$ [GHz] *
$L_{gate} = 50\ nm$	-0.04 ± 0.14	0.98 ± 0.14	163 ± 40
$L_{gate} = 100\ nm$	0.05 ± 0.04	0.95 ± 0.03	156 ± 21
$L_{gate} = 2000\ nm$	0.12 ± 0.01	0.79 ± 0.01	100 ± 11
PBTI $V_G = V_{stress}, V_D = V_S = 0$ V, 1500 s, 25 °C, $L_{gate} = 50\ nm$			
V_{stress} [V]	ΔV_{th} [V]	Δg_{max} $[mS/\mu m]$	Δf_t [GHz]
2	+70	-0.08	+2
3	+84	-0.19	**o.r.
NBTI $V_G = V_{stress}, V_D = V_S = 0$ V, 1500 s, 25 °C, $L_{gate} = 50\ nm$			
V_{stress} [V]	ΔV_{th} [V]	Δg_{max} $[mS/\mu m]$	Δf_t [GHz]
-2.5	-306	-0.15	+10
-3	-403	-0.19	+6
NBTI $V_G = V_{stress}, V_D = V_S = 0$ V, 1500 s, 25 °C, $L_{gate} = 200\ nm$			
V_{stress} [V]	ΔV_{th} [V]	Δg_{max} [mS/μm]	Δf_t [GHz]
-3	-273	-0.13	-1
HCI $V_G = V_{stress}, V_D = 1$ V, $V_S = 0$ V, 1500 s, 25 °C, $L_{gate} = 100\ nm$			
V_{stress} [V]	ΔV_{th} [V]	Δg_{max} $[mS/\mu m]$	Δf_t [GHz]
1	+209	+0.09	+16

* Maximun measured f_t and extrinsic DC-g_{max} at $V_D = 0.525$ V are given
** Maximun f_t outside S-parameter measurement range (0.1 V to 0.8 V)

2.6.1 LNA Degradation

The degradation of LNA characteristics can be expressed as functions of the device characteristics. For example, an analytical equation for the minimum noise figure and its sensitivity to HCI-induced threshold voltage and mobility shift was presented in [1]. This equation, developed to show the hot-carrier injection stress effects on a three-stage low-noise amplifier (65 nm silicon-based technology), is written as:

$$\frac{\Delta NF_{min}}{\Delta NF_{min} - 1} = \frac{\Delta V_{th}}{V_{th}} \cdot \frac{V_{th}}{2(V_{GS} - V_{th}) + 3b(V_{GS} - V_{th})^2 + b^2(V_{GS} - V_{th})^3} - \frac{1}{2}\frac{\Delta \mu_n}{\mu_n} \qquad (2.1)$$

where b accounts for the mobility degradation due to the vertical electrical field from the gate. From (2.1), when the threshold voltage increases ($\Delta V_{th} > 0$) and/or electron mobility decreases ($\Delta \mu_n < 0$), the normalised minimum noise figure will increase. The degradation of supply current, drain current, transconductance, and input matching network (all caused by hot carriers) and their catastrophic effects on NF_{min} are shown in Figure 2.8.

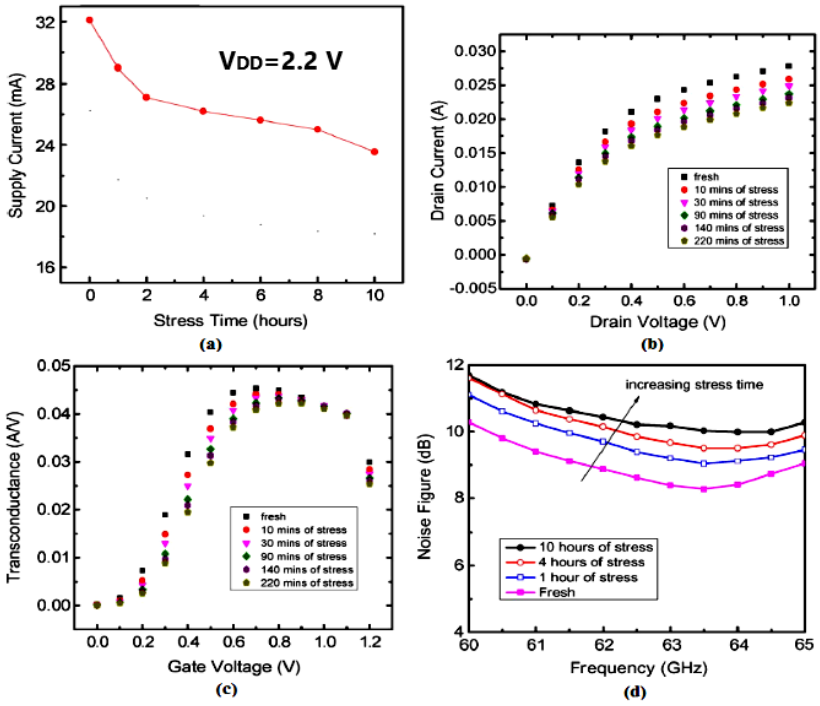

Figure 2.8: Degradation of a) supply current versus HC stress-time, b) drain current versus drain voltage for various stress-times, c) transconductance versus gate voltage and d) noise figure of LNA studied in [1].

In [9] the impacts of transistor ageing on CMOS technology are evaluated by comparing the extracted results for an RF single-ended cascode LNA and an LC folded-cascode LNA (Figure 2.9). The degradation of the overall gain and noise figure are represented by equations (2.2) and (2.3) based on transconductance and gate-source capacitor, indicating that the NF and overall gain will degrade after g_m decreases and C_{gs} increases due to both BTI and HCI mechanisms. In (2.2), A is a function of is the parasitic resistance of the inductor at the input (R_l), the internal resistance of the signal source (R_s), and the gate resistance of the input. Figure 2.10 shows the simulation results for the gain and NF degradations caused by ageing in a folded-cascode LNA. Both degradations are significantly worse than those for the cascode LNA (see Table 2.3) because the supply voltage is shared by two transistors in cascode LNA. Consequently, the drain-to-source voltage stress affecting the input transistor is reduced [9]. A similar conclusion is reported in [5].

$$\frac{\Delta NF_{LNA}|_{ageing}}{NF_{LNA} - A} \approx -\frac{\Delta g_m}{g_m} + \frac{\Delta C_{gs}}{C_{gs}} \tag{2.2}$$

$$\frac{\Delta G}{G}\Big|_{ageing} = \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} \tag{2.3}$$

2.6.2 Reliability in Power Amplifier

In order to analyse and predict reliability in PAs, accurate modelling and testing are required, since the reliability of a power amplifier is crucial for a transceiver and its degradation can directly affect the whole receiver performance [11]. In some articles, such as [5], the effect of the oxide thickness of a cascode transistor on alleviating oxide stress in PAs is studied. It was shown that there is a trade-off between increase in thickness and output voltage swing. However, these studies have been done based on gate-oxide stress not on HC stress.

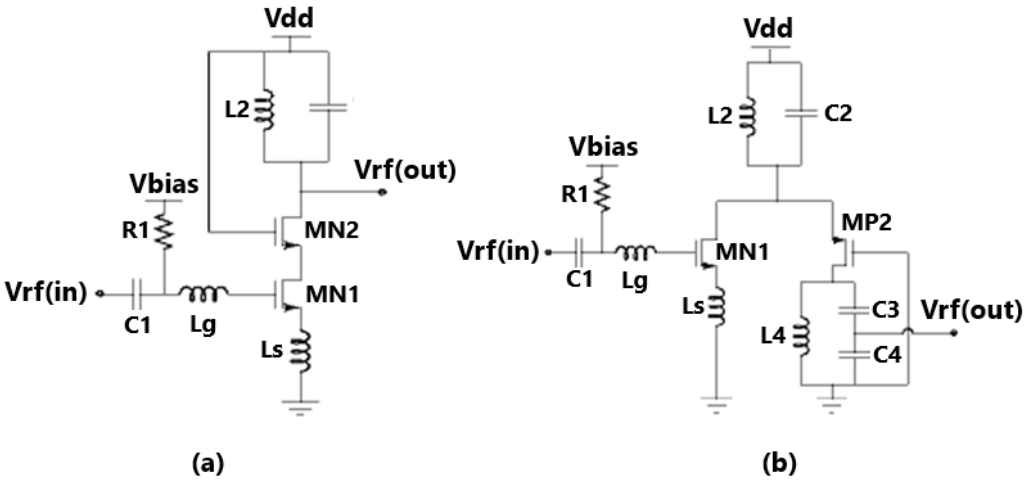

Figure 2.9: (a) Cascode and (b) Folded-Cascode LNA structures considered in [9].

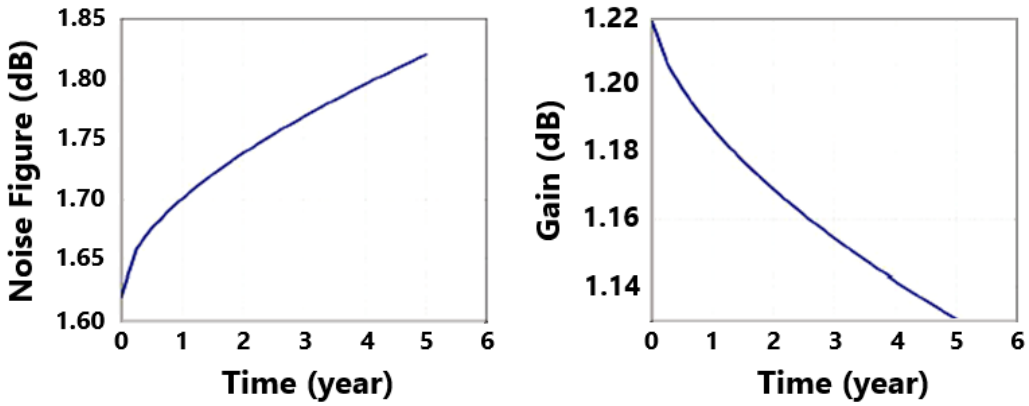

Figure 2.10: Degradation of NF and gain for folded-cascode over ageing [9].

A cascode class-E power amplifier (PA) operating at 5.2 GHz has been designed in [5] using Advanced Design System (ADS) simulation to evaluate the hot-electron effect on class-E PA degradation. Here, again, RF circuit performance such as the output power and power-added efficiency before and after DC (increase in V_{dd}) and RF stresses have been experimentally investigated. The proposed class-E PA is shown in Figure 2.11.

Table 2.3: Comparison between two various LNA topologies due to Degradation [9].

Topology and Performance		Nominal Value	Average Degradation (%)
Cascode LNA	$NF\ (dB)$	1.1925	+0.6
	$NF_{min}\ (dB)$	1.0190	+0.7
	$Gain\ (dB)$	11.905	-1
Folded-Cascode LNA	$NF\ (dB)$	1.6198	+13
	$NF_{min}\ (dB)$	1.0424	+13.7
	$Gain\ (dB)$	12.453	-8.6

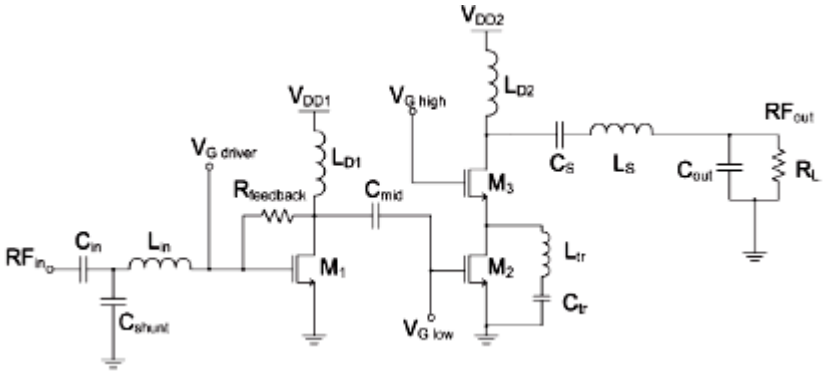

Figure 2.11: Cascode class-E PA proposed in [5].

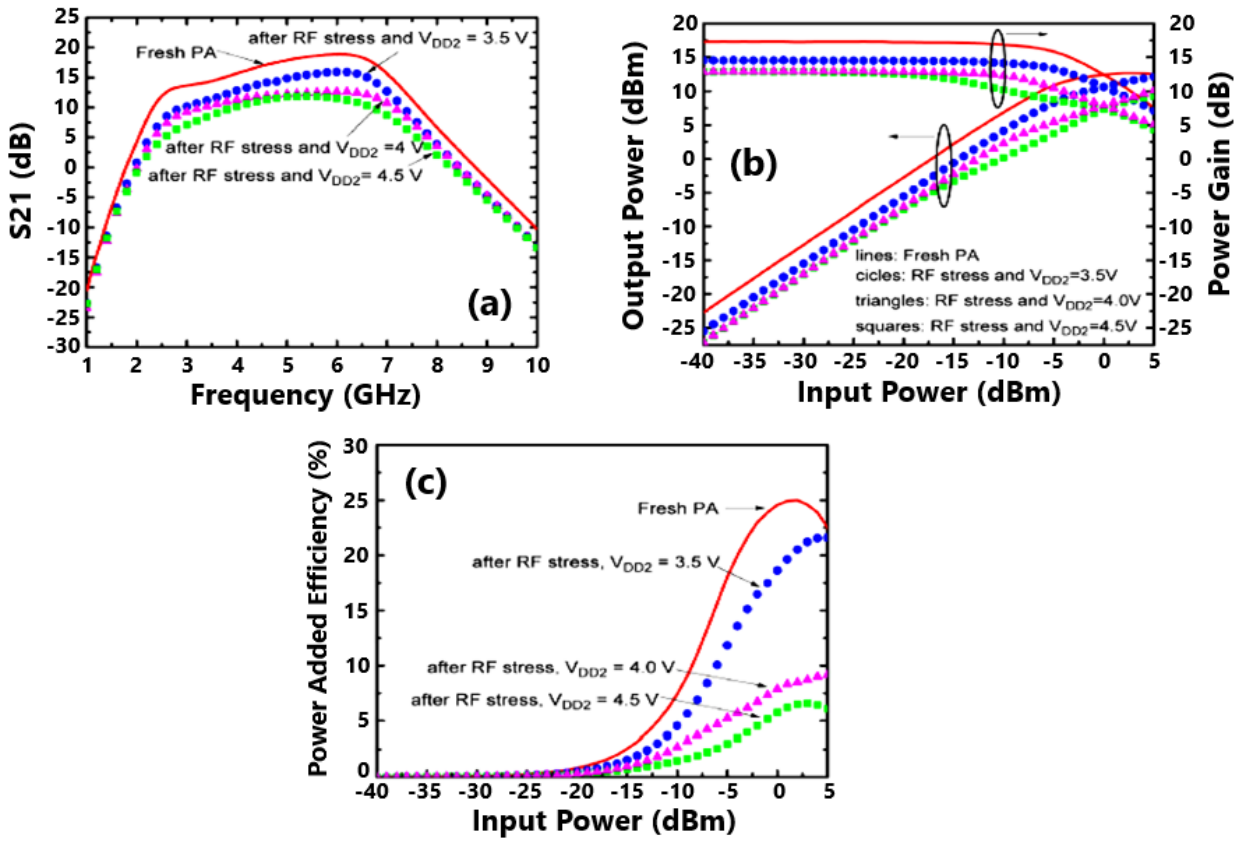

Figure 2.12: Measured a) S_{21} versus frequency, b) output power and power gain versus input power, c) power-added efficiency versus input power before and after RF stress for PA presented in Figure 2.11. During the RF stress, P_{in} is at 0 dBm and V_{dd2} was kept at 3.5, 4, or 4.5 V [5].

It can easily be seen that the cascode transistor (M_3) tolerates more voltage stress at its drain than the main transistor (M_2). On the other hand, at high input power, the cascode transistor could suffer from the hot-electron effect when gate-source and drain-source voltages are high during switching transients. Figure 2.12 (a) shows the measured small-signal gain, S_{21}, versus frequency after applying stress. From this figure, it is proved that the larger the stress is at high V_{dd2}, the more the S_{21} degrades over a wide range of frequencies. What is more, the measured output power, power gain and power-added efficiency before and after the RF stress are also plotted in Figure 2.12 (b) and (c). These curves prove that the PA performance decreases after RF stress, particularly when the V_{dd2} stress level is increased, and this is attributed to the hot-electron effect on the output transistor. Table 2.4 summarises the small-signal gain S_{21} at 5.2 GHz, output power at the input power of 0 dBm, power gain at the input power of -20 dBm, and maximum power-added efficiency before and after RF stress for the Class-E PA presented in Figure 2-11. Their normalized parameter shifts ($\Delta S_{21}/S_{21}, \Delta P_{out}/P_{out}, \Delta(P_{out}/P_{in})/(P_{out}/P_{in}), \Delta\eta_{added}/\eta_{added} \times 100\%$) are also presented, indicating considerable degradation due to hot-electrons.

Table 2.4: Degradation of PA performance designed in [5] after RF stress.

RF parameter	S_{21} at 5.2 GHz	P_{out} at $P_{in} = 0$ dBm	gain at $P_{in} = -20$ dBm	PAE
Fresh	18.2 dB	12.5 dB	17.3 dB	25%
After RF stress1	15.2 dB	10.6 dB	14.5 dB	21.6%
After RF stress2	12.3 dB	7.9 dB	12.9 dB	9.1%
After RF stress3	11.9 dB	7.3 dB	12.9 dB	6.6%
Change1	-16.5%	-15.2%	-16.2%	-13.6%
Change2	-32.4%	-36.8%	-25.4%	-63.6%
Change3	-34.6%	-41.6%	-27.7%	-73.6%

RF stress1: $P_{in} = 0$ dBm, $V_{dd2} = 3.5$ V for 10 hours, RF stress3: $P_{in} = 0$ dBm, $V_{dd2} = 4.5$ V for 10 hours
RF stress2: $P_{in} = 0$ dBm, $V_{dd2} = 4.0$ V for 10 hours

The reliability concept in a single-stage class-AB PA was investigated in [10], the simplified schematic of which is shown in Figure 2.13. Simulation results for the power-added efficiency (PAE), third-order intermodulation, and output power degradation as a function of the input power are given in Figure 2.14, showing an increase in third-order intermodulation (IM3) and a decrease in the output power after stress. Eventually, the simulation results extracted before and after AC stress for ACPR (adjacent-channel power ratio) and NPR (noise power ratio) are summarised in Table 2.5 [10]. These results prove that both parameters are degraded after AC stress.

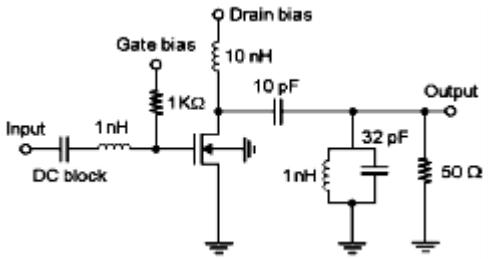

Figure 2.13: Class-AB PA mentioned in [10] for reliability studies.

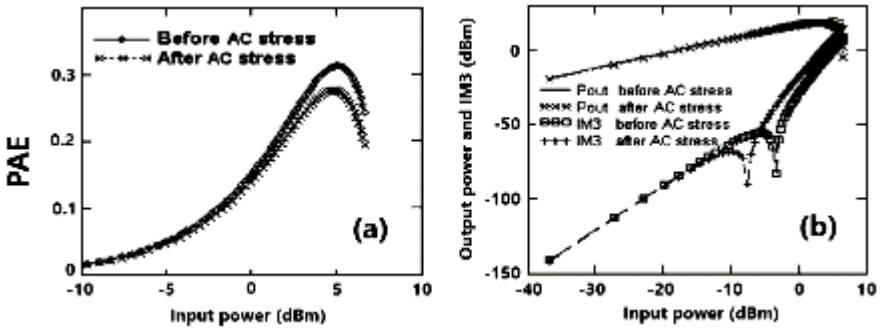

Figure 2.14: a) PAE and b) output power and IM3 degradation due to AC stress for Class-AB power amplifier in Figure 2.13 [10].

Table 2.5: Results indicating the degradation of ACPR and NPR for class-AB PA after AC stress [10].

Output power (dBm)	ACPR (dBm)		Input power (dBm)	NPR (dBm)	
	Fresh	Stressed		Fresh	Stressed
−20	69.11	62.30	−40	53.50	47.87
−10	64.59	57.92	−30	39.39	34.39
0	43.50	38.38	−20	17.53	13.14
10	23.68	19.58	−10	13.66	12.49
20	17.82	13.62	0	12.94	9.13

2.7 Conclusion

Two physical-degradation mechanisms in silicon-based devices, called Hot-Carrier Injection (HCI) and Bias Temperature Instability (BTI), were studied in this chapter. Then, these mechanisms were compared, and it is concluded that HCI will make more destructive effects on device DC and small-signal characteristics. Because of device degradation, RF circuits will experience performance degradation, and this unwanted change was illustrated by comparing LNA and PA performance before and after stress. This information is necessary, as the first step, to find reliability models predicting device ageing during the design process. The next chapter will discuss how to model ageing mechanisms and will present some analytical models published in the literature, which can provide us with a clear path to find our final age model for power-amplifier ageing.

Chapter 3

Physical Models to Describe Device Degradation

3.1 Chapter Abstract

After identification of the main ageing/degradation mechanisms, developing theoretical models able to predict degradation is now the second step toward design modification to improve reliability. Each model is expected to predict degradation under both DC and RF stresses. So, the concept of the Quasi-Static approach is, then, explained to change static (DC) models into RF counterparts.

3.2 Introduction

All degradation models consist of items describing physical mechanisms initiating degradation in devices. For example, due to holes generated via impact ionisation, there is a correlation between the hot-carrier rate and the substrate current in NMOS. So, an age model can be extracted as a function of the substrate current in n-type MOSFETs. For PMOS, charge trapping into the oxide layer is responsible for the degradation and this degradation can also be modelled by using the gate current [4, 31, 33-36]. In addition, DC stresses (V_{gs} and V_{ds}) may be defined as determinative factors in models. Finally, a model is expected to cover recoverable behaviour after removing BTI stress. In this chapter the Power Law, as the basis of almost all ageing models, and its derivatives for HCI and BTI under DC and AC bias conditions, are explained. Then, some examples of such predictive age-models will be represented and summarised in a table.

3.3 Power Law and Quasi-Static Approach

Reliability models, irrespective of whether they predict device degradation due to either HCI, BTI, or other mechanisms, are expressed in the form of a Power Law which has been empirically verified as equation (3.1) [3, 7]:

$$\Delta P = A \cdot t^n \tag{3.1}$$

where P is a device electrical parameter, ΔP is the degradation of the parameter P from its original value under stress, A is a pre-factor obtained according to the technology used, and t is the stress time. In [3], three main criteria were mentioned which can affect the pre-factor A: (i) Single Vibrational Excitation (SVE), (ii) Electron-Electron Scattering (EES), and (iii) Multiple Vibrational Excitation (MVE). However, in [7] it is indicated that the power law is based on HC transport mechanisms including single-carrier events (SCE) and multi-carrier events (MCE). Power n represents the degradation rate, the value of which varies between 0.1 and 1 dependant on the technology used in the design. Based on RelXpert parameters for BSIM4 model, n is 0.344.

The power law in the form of (3.1) only works to describe device degradation under DC or low-frequency stress (static mode). However, transistors in actual circuits usually operate under time-varying bias conditions (such as those in local oscillators and power amplifiers). Therefore, the conventional form of power law should be extended into an AC/RF or dynamic one, otherwise the evaluation will be inaccurate. This conversion is executable if history effects are neglected and the "Quasi-Static" approximation is considered as a sequence of DC conditions [3, 20, 30, 31, 32, 37-39]. The final formalism for the power law in the RF domain, after applying this approximation, can be written as (3.2) called "age function" [3].

$$\Delta P = \left[\int_0^t A^{\frac{1}{n}}(t)\, dt' \right]^n \tag{3.2}$$

Based on these two cases, all mechanisms are modelled, and their effects are predicted. The following sub-sections represents models developed to predict the ageing due to HCI, BTI, TDDB, and sub-threshold leakage currents in both static and dynamic modes.

3.3.1 HCI-based Models

HC models are based on carrier-transport mechanisms and can be written in the form of (3.1) or of a saturation power law as (3.3), where N_0 is density of dangling bonds [3, 7]:

$$\Delta P = N_0 \times [1 - exp(-A.\, t^n)] \tag{3.3}$$

Some references expand (3.1) for a specific DC parameter. For instance, (3.4) presents a static model to predict the HC-induced threshold-voltage degradation in CMOS transistors where $n_{HC} \approx 0.5$ represents the time exponent and α_3 and α_4 are technology-dependent voltage-scaling parameters [9]. The effect of V_{gs} and V_{ds} on the degradation is also modelled in this equation.

$$\Delta V_{th} \approx \frac{1}{\sqrt{L}} e^{(\alpha_3 V_{gs})} . e^{(\alpha_4 V_{ds})} . t^{n_{HC}} \tag{3.4}$$

Another derivative of the power law is introduced based on the substrate current I_{sub}, or the impact-ionisation current I_{ii}, as a consequence of the correlation between the number of HCs and the number of holes generated via the impact-ionisation effect, as mentioned before. In these models, $\frac{I_{sub}}{I_d}$ or $\frac{I_{b,ii}}{I_d}$ is used as a criterion representing probability that a single carrier has sufficient energy to start device degradation [34]. A physical model describing the worsening of the saturated current, $I_{d,sat}$, over time is, for instance, expressed as [3, 4]:

$$-\Delta I_{d,sat}\% = \left[K_{HC} \frac{I_d}{W} \left(\frac{I_{b,ii}}{I_d} \right)^m t \right]^n \tag{3.5}$$

where W is the channel width and m represent the ratio between the critical energy that an electron must have in order to create an interface trap (φ_{it}) and the minimum energy that a hot electron must have in order to create an impact ionisation (φ_i) [31].

Recently, it has been found that HCD can follow an apparent two-stage law under some stress conditions in planar devices because of generating more than one kind of trap. So, the traditional approaches to evaluate HC effects can be faced with several challenges during the scaling process. Additionally, self-heating effects can aggravate the FinFET operation due to its narrow structure and HCD study is faced with great challenges for FinFETs [7]. Therefore, in [7] hot-carrier degradation was studied for this technology from a trap-based approach rather than using a conventional carrier-based approach (equations (3.1)-(3.5)) so that, for the first time, considers the self-heating issue. The proposed trap-based HC model, which was verified in both n- and p-type FinFETs, improves the design margin and is introduced for threshold-voltage degradation as follows [7]:

$$\Delta V_{th} = N_0 \times [1 - exp(-AR_1 . t^n)] + AR_1 \times log(1 + C_1 t) + AR_2 \times log(1 + C_2 t) + k.BTI \tag{3.6}$$

with

$$k = 1 - 0.5 \left(\frac{V_{ds}}{V_{gs}} \right), AR = A(V_{gs} - V_{th})^m \, exp\left(\frac{-b}{V_{ds} - V_{dsat}} \right) \tag{3.7}$$

where AR is the age rate and b is a factor. Refer to [7] for more information and finding equations required to calculate AR_1 and AR_2. Only a portion of BTI should be counted in the total degradation because BTI is measured under $V_{ds} = 0V$, while under HCD bias conditions, non-zero V_{ds} can raise the potential and decrease the BTI near the drain side. The comparison between predicted and experimental results for nFinFETs and pFinFETs using the model expressed in (3.6) is presented in Figure 3.1, indicating acceptable agreement between the two cases.

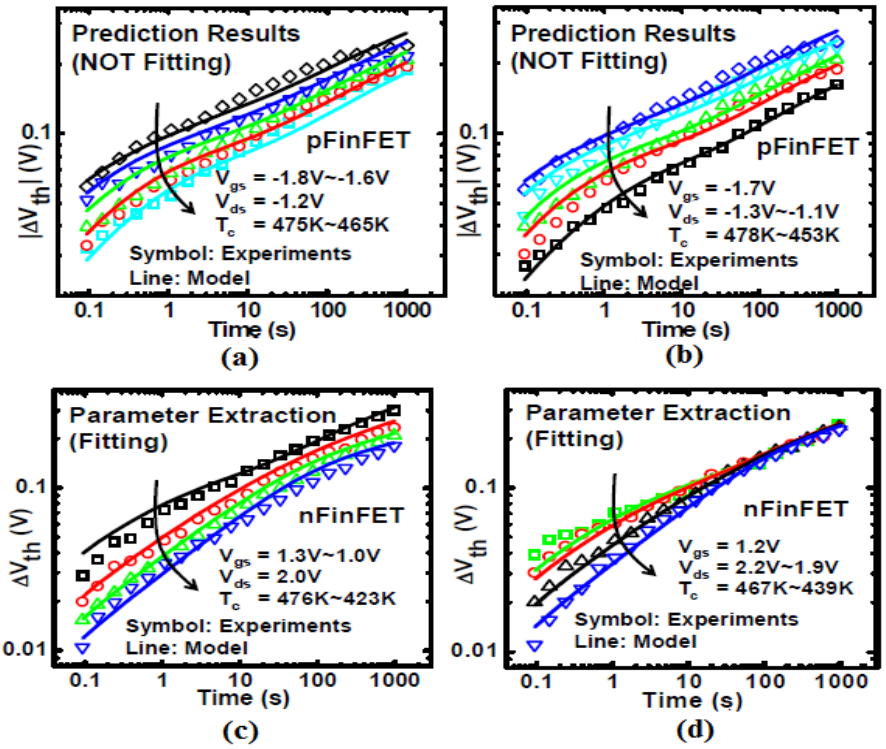

Figure 3.1: Comparison of predicted and experimental data for a) pFinFET (V_g-dependence), b) pFinFET (V_d-dependence), c) nFinFET (V_g-dependence), d) nFinFET (V_d-dependence) [7].

3.3.2 BTI-based model

The BTI is best modelled based on the threshold-voltage degradation under AC stress [2, 7, 9]:

$$\Delta V_{th} \approx e^{(\alpha_1 V_{gs})} t^{n_p} + V_{gs}^{\alpha_1} [C_R + n_R \, log \, t] \tag{3.8}$$

Here, α_1 and α_2 are voltage-scaling factors and n_p and n_R are time exponents. All these parameters, along with C_R, are all technology dependent. The first part of (3.8) shows the degradation during the stress time and the second one accounts for the relaxation or recovery of the BTI degradation after the stress is removed. Another stress and recovery NBTI model is presented in [2] for a field-effect transistor using a range of stress voltage, time, and temperature. Since parasitic series resistance and capacitance play an important role in nano-scale circuit performance, the model mentioned in this article also includes scalable geometry-dependent

parasitic capacitance and resistance of the nano-wire FET. The complete threshold-voltage degradation model presented in [2] is:

$$\Delta V_{th} = A e^{\beta E_{ox}} e^{-E_a/KT} t^n + \Delta V_{th0}[1 - \alpha(t - t_0)^n] \quad (3.9)$$

where A and β are constants including technology-dependent effects such as gate dielectric, gate metal and other related processes, E_{ox} is the oxide field at the $Si - SiO_2$ interface, E_a shows the activation energy, k is the Boltzmann constant and T refers to the temperature. Also, ΔV_{th0} is the degradation at the end of the stress period or at the beginning of the recovery period, t_0 indicates the stress period, and α is a proportionality constant. Refer to Figure 2.5 (a) to see how this equation predicts the recoverable nature of BTI degradation.

3.3.3 Sub-threshold modelling

The increase of leakage current in deep sub-micrometre MOS transistors, operating below threshold, is also becoming a reliability concern. Prediction of RF stress-induced leakage is important since several RF elements are used to design a PA and they multiply the leakage current, indirectly affecting the circuit degradation. In some papers it is illustrated that hot carriers can also be generated when the transistor is turned-off. In addition, at high frequencies and when the gate voltage goes below the threshold voltage, the lateral field can change the device and circuit specifications [4, 40, 41].

As depicted in Figure 3.2 (a), two main leakage currents are present below V_{th}: the gate-induced drain-leakage (GIDL) current which equals the bulk current when $V_g < 0$ and the drain-induced barrier-lowering (DIBL) current which equals the drain current when $0 < V_g < V_{th}$. GIDL and DIBL respectively refer to the *whole current* and the *enhanced electron channel current* flowing in the Sub-V_{th} region due to the reduction of V_{th} at high V_{ds}. There are other mechanisms affecting the gate leakage current, but their degradation effects are negligible and have rarely been taken into account in the literature [4, 42].

One of the frailties of conventional DC Hot-Carrier models is that they do not consider the degradation occurring in the sub-threshold region ($V_g < V_{th}$) [3, 4]. In [4] a new DC degradation model valid for this area was proposed which is also suitable for being extended to high frequencies. By means of RF stress measurements in this reference, the frequency dependency of the sub-threshold region is also evaluated, and the Quasi-Static sum is validated. Additionally, it is possible to replace the current ratio ($\frac{I_{b,ii}}{I_d}$) in equation (3.5) with a more empirical power function of drain voltage V_d in order for the model to be extended into the sub-V_{th} region (until the OFF-

state point V_g = 0). The proposed degradation model and its extension to the RF domain are introduced as (3.10) and (3.11), respectively:

$$-\Delta I_{d,sat}\,\% = \left[\left(D\frac{I_s}{W}V_d^{m_1} + G\frac{I_b}{W}V_d^{m_2}\right)t\right]^n \tag{3.10}$$

$$-\Delta I_{d,sat}\,\% = \left[\int_0^t \left(G\frac{I_b(t)}{W}V_d^{m_2}(t)\right)dt\right]^n \tag{3.11}$$

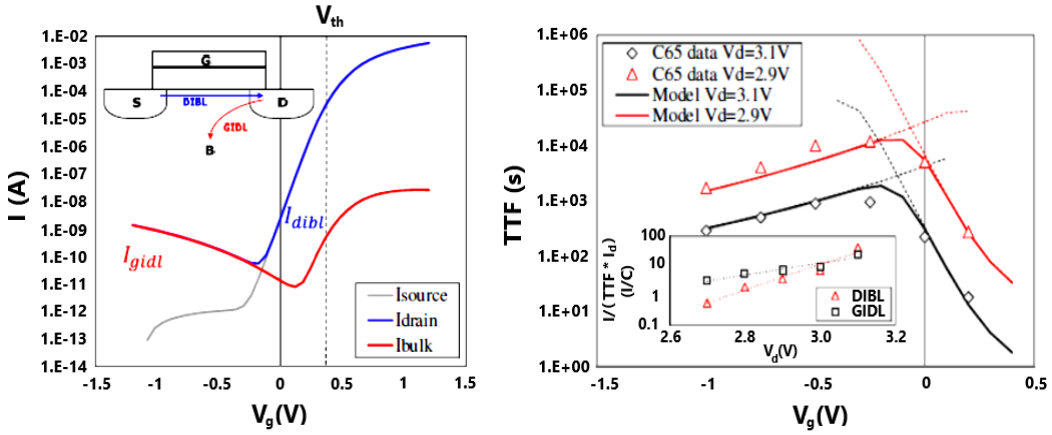

Figure 3.2: a) Illustration of GIDL and DIBL leakage currents in Sub-Threshold region, b) TTF (10% degradation of $I_{d,sat}$) for different $V_g - V_d$ configurations in the sub-threshold area [4].

The DIBL contribution is neglected in (3.11) since no current is flowing along the channel and the whole degradation will be due to GIDL stress. Figure 3.2 (b) shows the simulation results for 10% degradation of $I_{d,sat}$ (TTF[1]) for several V_g and V_d values. The simulation results for the contribution of each term are plotted by dotted lines. It is revealed from Figure 3.2 (b) that in the sub-V_{th} region (when $V_g > 0$), DIBL degradation is predominant, but below $V_g = 0$ the GIDL current reduces drastically the time to failure, de-escalating the device performance.

Eventually, the authors in [40, 41] quantified the behaviour of the stress-induced leakage current in terms of the stress experienced by a Heterojunction Bipolar Transistor (HBT) under RF operating conditions. The damage characteristics observed during RF operation, particularly the base leakage and collector-base (CB) junction failure, are investigated in detail using DC stress methods. The model predicting RF degradation, and the total leakage lifetime, are given as (3.12) and (3.13), respectively:

$$\Delta I_B \propto \sqrt{I_E \cdot e^{-\frac{\beta}{(V_{CB}+V_{bi})^{1/2}}} \cdot t} \tag{3.12}$$

$$\Delta I_{B,lifetime} = \Delta I_{B,dev} \cdot n \cdot \sqrt{t \cdot d} \tag{3.13}$$

[1] Time to Failure

where β is a factor close to 0.53, V_{CB} is the collector-base voltage, I_E is the emitter current, $\Delta I_{B,dev}$ represents the leakage from a single device in one second, n shows, here, the total number of parallel devices, d refers to the duty cycle, and V_{bi} is input bias voltage. With various bias voltages, the predicted excess base currents are in reasonable agreement with the RF stress results, as shown in Figure 3.3 [40].

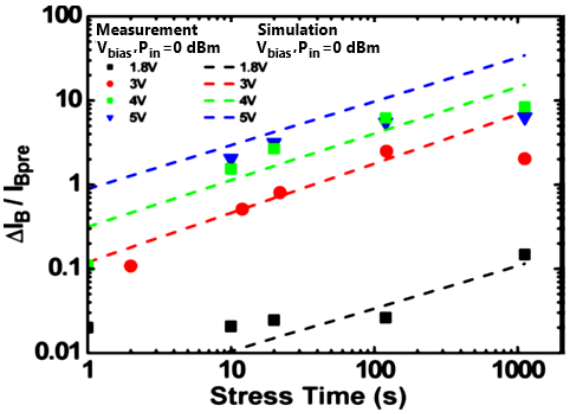

Figure 3.3: Comparison of predicted and measured RF stress-induced ΔI_B, scaled by predicted base current $I_{B,pre}$ [40].

Table 3.1 summarises several models proposed in the literature to model device reliability under different kinds of stresses. As is easily seen, HCI is considered as the most important phenomenon affecting all DC and small-signal parameters and, consequently, device RF performance. Clearly, BTI is the next physical mechanism which can degrade the performance of a device. However, there is no direct model to predict the degradation induced by time-dependent breakdown mechanisms, and the simple power law in (3.1) is the only equation available to model TDDB.

3.4 Conclusion

Reliability is becoming an undeniable part of RF device and circuit design. A correct and precise reliability evaluation contains two main steps: (i) identification of physical mechanisms accelerating device ageing and, then, (ii) introducing analytical models for these mechanisms to predict degradation of device parameters. This chapter provides us with an overview of reliability models for HCI, BTI, and sub-V_{th} induced degradation. It is theoretically shown in Table 3.1 that hot carriers impose damaging effects on all parameters and HCI is, therefore, considered as the most severe degradation phenomenon. However, all models have been developed at the device level. If these device-level models are combined with circuit-design concepts, more dependable circuits are implemented using the new generation of reliability models. One state-of-the-art age model for PA design will be developed in the next chapter, combining device and circuit characteristics.

Table 3.1: A brief overview of models mentioned in the literature to study the effects of various mechanisms on device degradation.

Mechanism	Affected Device Parameters			Stress	Model		Device	Reference
	DC	Small-signal	RF		DC	Quasi-Static		
HC	I_{dsat} I_{dlin} V_{th} U0 SS**	C_{gd}, C_{gs}, G_m, G_{ds}, G_{db}, R_d, R_s, R_g, R_{db}	f_t, f_{max}, NF_{min} Gain IIP3	Ageing DC RF AC Dynamic	1-DC Power Law [22] 2- $\Delta I_{ds(lin)} = A(t)\,t^n$, [3] 3- $\frac{\Delta NF_{min}}{NF_{min}-1} = -\frac{1}{2}\frac{\Delta g_m}{g_m}$, [1] 4- $\Delta g_m = \frac{\partial g_m}{\partial V_{th}}\Delta V_{th} + \frac{\partial g_m}{\partial \mu_n}\Delta \mu_n$, [1] 5- $\Delta V_{th} \approx \frac{1}{\sqrt{L}} e^{(\alpha_3 V_{gs})}.e^{(\alpha_4 V_{ds})}.t^{n_{HC}}$, [9] 6- $-\Delta I_{d,sat}\% = \left[\left(D\,\frac{I_s}{W}V_d^{m_1} + G\,\frac{I_b}{W}V_d^{m_2}\right)t\right]^n$ [4] 7- $\Delta V_{th} = N_0 \times [1 - exp(-AR_1.t^n)] + AR_1 \times log(1 + C_1 t) + AR_2 \times log(1 + C_2 t) + k.BTI$ $k = 1 - 0.5\left(\frac{V_{ds}}{V_{gs}}\right), AR = A(V_{gs} - V_{th})^m\, exp\left(\frac{-b}{V_{ds} - V_{dsat}}\right)$, [7] 8- $\Delta I_B \propto \sqrt{I_E \cdot e^{-\frac{\beta}{(V_{CB}+V_{bi})^{1/2}}} \cdot t}$, for HBT, [41]	1- $\Delta I_{ds(lin)} = \left[\int_0^t A(t)^{\frac{1}{n}}\,dt'\right]^n$, [3] 2- $-\Delta I_{d,sat}\% = \left[\int_0^t \left(G\,\frac{I_b(t)}{W}V_d^{m_2}(t)\right)dt\right]^n$ [4]	1- Global Foundaries 45 nm RFSOI 2- nMOSFET (Si) 3-pMOSFET (Si) 4-CMOS (160 nm) 5- CMOS (65 nm) 6- CMOS (28 nm) 7- MOSFET (InGaAs) 8- FinFET 9- SiGe HBT	[1-4] [6-10] [22-24]
BD/ TDDB*	I_{dsat} V_{th} $U0$	G_m, G_{ds}	f_t, f_{max}, N_{min}, Gain IIP3	Dynamic DC RF	1- DC power law [22]		1- MOSFET 2- nMOSFET (90 and 130 nm) 2- CMOS (160 nm) 3- CMOS (28 nm)	[1] [6,8] [10] [22]
BTI (NBTI, PBTI)	V_{th} I_{dsat}	G_m	Gain NF f_t	RF AC DC [12,14]	1- DC power law [22] 2- $\Delta V_{th} \approx e^{(\alpha_1 V_{gs})}t^{n_p} + V_{gs}^{\alpha_1}[C_R + n_R\, log\, t]$, [9] 3-$\Delta V_{th} = Ae^{\beta E_{ox}}e^{-E_a/KT}t^n + \Delta V_{th0}[1 - \alpha(t - t_0)^n]$, [2]		1- GlobalFoundaries 45nm RFSOI 2- MOSFET (90 and 130 nm) 3- CMOS (28 nm) 4- FinFET 5- MOSFET (InGaAs)	[2] [9] [22] [24]

***The voltages at which TDDB happens are typically not used for analogue circuits in 28 nm technology, so TDDB may have no significant impact on RF circuits in nominal operating conditions [11], **Sub-threshold Swing.**

Chapter 4

Analytical Age Model for Power Amplifiers

4.1 Chapter Abstract

Power Amplifiers are classified based on conduction angle indicating in which time duration output current is flowing through the circuit. A model for aging of FETs due to HCI mechanism, which is a main cause of aging in FETs, is introduced in this chapter as a function of conduction angle (a circuit concept), device parameters, and bias voltages. This model fits very well the simulation results of the RelXpert simulator. By using this model, for the first time all PA classes can be compared in the field of reliability.

4.2 Introduction

Of all RF circuits, the power amplifier is more vulnerable to degradation because of its high peak output voltages, and degradation of a PA, being a main part of a transceiver chain, can affect the overall performance of a transceiver. [5-7, 11, 12, 39]. However, research in the field of PA reliability is restricted to these three main areas: (i) the effect of DC/RF stress on a device and, subsequently, on circuit performance, (ii) the effect of higher temperatures on a device, and (iii) circuit modification approaches to mitigate long-term degradation in RF devices and circuits [6, 12-20]. Clearly, none of the studies published up till now have compared the classic classes of a PA in terms of degradation. In addition, the correlation between the conduction angle and reliability is not apparently studied and only a few studies have been performed to evaluate PA reliability from this point of view. The authors in [39], for instance, proved that the conduction

angle affects the rate of the de-trapping process so that, the lower is the conduction angle, the fewer interface states are filled and, then, the more performance of PA is recovered over frequency. Yu et al. [6] also modelled the effect of the degradation on the efficiency and output power of a class-AB PA as functions of the conduction angle (θ), maximum drain current (I_m) and maximum output voltage (V_m) as follows:

$$\frac{\Delta P_{out}}{P_{out}} \approx \frac{\Delta I_m}{I_m} + \frac{\Delta \theta}{f_1(\theta)} \tag{4.1}$$

$$\frac{\Delta \eta}{\eta} \approx \frac{\Delta V_m}{V_m} + \frac{\Delta \theta}{f_2(\theta)}, \tag{4.2}$$

with

$$f_1(\theta) = \frac{\theta - \sin\theta}{1 - \cos\theta} \tag{4.3}$$

$$f_2(\theta) = \left(\frac{1 - \cos\theta}{\theta - \sin\theta} - \frac{\theta}{4} \frac{\sin\frac{\theta}{2}}{\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2}} \right)^{-1} \tag{4.4}$$

They also demonstrated that, due to HCI-induced degradation, the conduction angle decreases, and the PA moves from class-AB, through class-B, to the class-C mode of operation. This concept is illustrated in Figure 4.1 for three different temperatures (320, 360, and 400 K). As may be seen, the degradation of the conduction angle with stress time is significant when the temperature increases, since the threshold voltage increases, and interface traps are filled more and more.

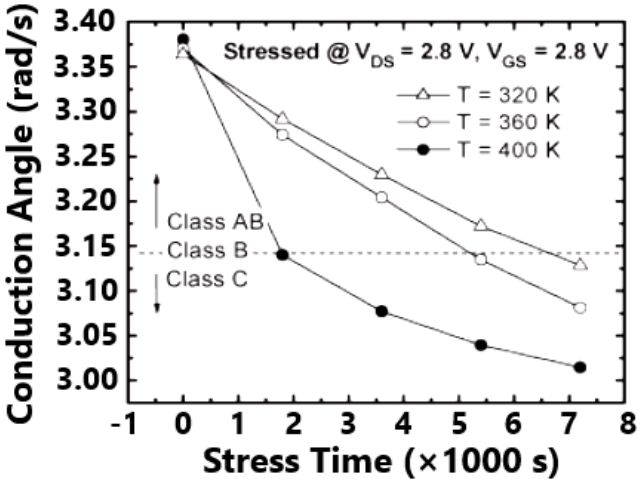

Figure 4.1: Variation of conduction angle as a function of stress time [6].

It is expected that, for various θ, the ageing will change in power amplifiers. In the current chapter, the effect of the conduction angle on the degradation of classic power amplifiers is investigated and an age model is extracted by using the "Lucky-Electron" concept, which just

predicts HCI-induced degradation. To develop this model and since age cannot be calculated for the case of a sinusoidal input (this fact will be clarified further in the following sections), a numerical solution, as performed in RelXpert simulator, is considered. In the rest of this chapter all the steps required to define the proposed age model are explained in detailed. The age model will be validated under DC and AC stresses and, then, it is explained how to design PAs based on a trade-off between age, maximum efficiency and normalised maximum output power, offering a good method to design high-performance power amplifiers.

4.3 Methodology

4.3.1 Lucky-Electron Model

As mentioned, there is a correlation between the hot-carrier rate and the substrate (for NMOS) or gate (for PMOS) currents. So, an age model should be extracted as a function of the substrate current in an n-type MOSFET [4, 31, 32-35]. One of the most well-known device-lifetime models based on HC effects is the "Lucky-Electron" model which was, first, introduced by Shockley to model impact ionisation in a p-n junction [33]. This model, which has frequently been repeated in several articles [31, 33, 42], uses a ratio between the substrate (I_{sub}) and drain-source (I_{ds}) currents as a criterion representing the probability that a single carrier has sufficient energy to start device degradation [34]. A precise version of the lucky-electron model has been released by Infineon Technologies and written as [44]:

$$\frac{\Delta P}{P} = A.\left(\frac{I_{ds}}{W}\right)^{n}\left(\frac{I_{sub}}{I_{ds}}\right)^{m.n}.t^{n}.L^{-p}.\exp\left(\frac{-E_a}{k}\left(\frac{1}{T}-\frac{1}{T_{ref}}\right)\right) \tag{4.5}$$

where P is a device electrical parameter, ΔP is the degradation of the parameter P from its original value under stress, W and L are channel width and length, respectively, T is temperature and T_{ref} shows the temperature where the device has been stressed and the parameters have been measured afterwards (e.g. -40 °C for HCI), k is Boltzmann's constant, E_a indicates activation energy, p is a power equal to unity and $m = 3$ in BSIM4 model, which is a good approximation of the exact value of 2.9 mentioned in [31]. Equation (4.5) is the basis of age modelling in this chapter.

4.3.2 Substrate Current

Substrate or bulk terminal current consists of several parts, namely junction-diode current, gate-to-body tunnelling current, substrate current due to impact ionisation (I_{ii}), gate-induced drain leakage current (I_{gidl}), and source leakage current (I_{gisl}). Conceivably, when hot carriers

accelerate in a channel, they can release more electron-hole pairs by damaging crystalline bonds. This effect is named impact ionisation and, since the HCs causing this effect and the HCs responsible for bulk current are triggered by the same field, so, of all those parts, impact ionisation is the most substantial one. For this reason, the impact-ionisation current (I_{ii}) is utilized instead of I_{sub} as an acceptable approximation. To model substrate or impact-ionisation current, (4.6) is used, which was defined for the BSIM4 model and has an exponential form as follows [32, 45]:

$$I_{sub} = \frac{\alpha_0 + \alpha_1 L_{eff}}{L_{eff}}\left(V_{ds} - V_{dseff}\right) \times \exp\left(\frac{-\beta_0}{V_{ds} - V_{ds(eff)}}\right) I_{ds}\,, \tag{4.6}$$

where α_0 and β_0 (a V_{ds}-dependent factor) are impact-ionisation coefficients, α_1 is a channel-length scaling parameter of the impact-ionisation current, L_{eff} is the effective channel length, V_{ds} represents the drain-source voltage of the transistor, and $V_{ds(eff)}$ is the effective V_{ds} and is given for short-channel devices by:

$$V_{ds(eff)} = \frac{V_{ds}\left(V_{gs} - V_{th}\right)}{V_{ds} + \left(V_{gs} - V_{th}\right)}\,, \tag{4.7}$$

By inserting (4.7) into (4.6), we can write (4.6) more compactly as

$$I_{sub} = k_1 \exp(-k_2)\ I_{ds} \tag{4.8}$$

with

$$k_1 = \left(\frac{\alpha_0 + \alpha_1 L_{eff}}{L_{eff}}\right)\left(\frac{V_{ds}^2}{V_{ds} + \left(V_{gs} - V_{th}\right)}\right) \tag{4.9}$$

$$k_2 = \frac{\beta_0\left(V_{ds} + \left(V_{gs} - V_{th}\right)\right)}{V_{ds}^2}\,. \tag{4.10}$$

4.3.3 Age Equation for Power Amplifier

Figure 4.2 illustrates the drain current in a power amplifier for a sinusoidal input signal. From this figure, therefore, the PA's drain current can be expressed in terms of a quiescent current I_q and an AC current $I_p \cos\theta$ as:

$$I_{ds}(\theta) = I_q + I_p \cos\theta\,, \qquad -\alpha \le \theta \le \alpha \tag{4.11}$$

here, I_p is the peak value of the AC current and θ is the conduction angle. Given that $I_{ds}(\theta = \alpha) = 0$, it follows that I_q and I_q are related as $I_q = -I_p \cos\alpha$. With this relation, we can rewrite (4.11) in the form of (4.12) by using $I_{max} = I_q + I_p$.

$$I_{ds}(\theta) = \frac{I_{max}}{1-\cos\alpha} \cdot (\cos\theta - \cos\alpha), \qquad -\alpha \le \theta \le \alpha \tag{4.12}$$

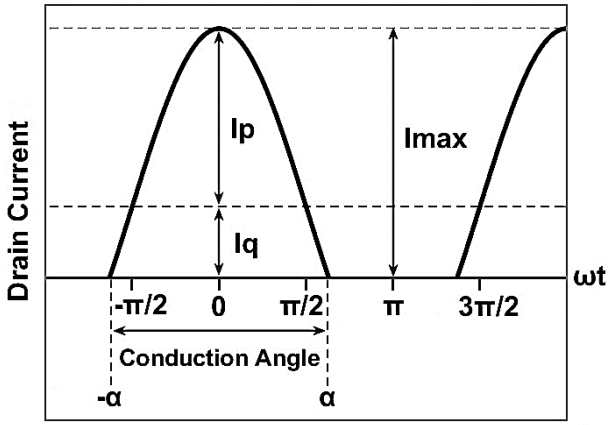

Figure 4.2: Illustration of DC and AC parts of PA's drain current based on conduction angle.

On the other hand, device age is defined for static (DC) case in terms of ΔP as [44]:

$$\frac{\Delta P}{P} = F_c \; age^n \,, \tag{4.13}$$

where F_c is a failure criterion having a value between 0 to 1. Equivalently, age can be written by changing (4.13) into:

$$age = \left(\frac{1}{F_c}\frac{\Delta P}{P}\right)^{1/n}. \tag{4.14}$$

Also, by taking advantages of quasi-static approach for dynamic bias, this latter equation modifies to:

$$age = \int_0^t \left(\frac{1}{F_c}\frac{\Delta P}{P}\right)^{1/n} dt'. \tag{4.15}$$

Given that I_{ds} and I_{sub} are both functions of the conduction angle (see equations (4.8) and (4.12)), we can write (4.15), using (4.5), as

$$age = N\left(\frac{A}{F_c.L^p}\right)^{1/n} \frac{1}{W\;\omega} \exp\left(\frac{-E_a}{k}\left(\frac{1}{T}-\frac{1}{T_{ref}}\right)\right) \times \int_{-\alpha}^{\alpha} \frac{I_{sub}^m(\theta)}{I_{ds}^{m-1}(\theta)} d\theta \;. \tag{4.16}$$

where N is the number of cycles during the stress time. Equation (4.16) can be re-written as follows using (4.11) and (4.12),

$$age = N\;k_3 \int_{-\alpha}^{\alpha} k_1^m \cdot \exp(-mk_2) \times \frac{I_{max}}{1-\cos\alpha}(\cos\theta - \cos\alpha)\; d\theta \tag{4.17}$$

with

$$k_3 = \left(\frac{A}{F_c.L^p}\right)^{1/n} \times \frac{1}{W \cdot \omega} \exp\left(\frac{-E_a}{k}\left(\frac{1}{T} - \frac{1}{T_{ref}}\right)\right) \tag{4.18}$$

The integrand in (4.17) is a complicated function of the conduction angle. This dependence comes through the term $cos\,\theta$ and also the dependence of k_1 and k_2 on θ due to their dependence on V_{ds} and V_{gs}. Due to this complexity, (4.17) cannot be solved analytically. Several approximations are, therefore, needed to obtain an analytical expression which can be fitted to the simulation results of RelXpert.

4.3.4 Approximations

Because of the sinusoidal nature of input and output voltages in power amplifiers, following expression can be considered for drain-source (V_{ds}) and gate-source (V_{ds}) voltages:

$$V_{ds}(\theta) = V_{ds,q} + v_{ds,p} \cos\theta, \tag{4.19}$$

$$V_{gs}(\theta) = V_{gs,q} + v_{gs,p} \cos\theta, \tag{4.20}$$

where $V_{ds,q}$ and $V_{gs,q}$ are the DC drain-source and gate-source voltages, and $v_{ds,p}$ and $v_{gs,p}$ are the peak values of the AC gate-source and drain-source voltages, respectively. Equations (4.19) and (4.20) make age equation, mentioned in (4.17), unsolvable since V_{ds} and V_{gs} appearing in k_1 and k_2. Therefore, it seems necessary to replace (4.19) and (4.20) with other mathematical functions as approximations of a sinusoidal function. Two approximations are considered as follows.

First approximation: One can replace V_{ds} by a term V'_{ds} defined as

$$V'_{ds} = V_{ds,q} + a_1\, v_{ds,p} + a_2\, v^2_{ds,p}\,, \tag{4.21}$$

where a_1 and a_2 are two constants. All class of PA is characterized by the same set of a_1 and a_2 which are extracted by simulation.

Second approximation: V_{gs} is also replaced by a term V'_{gs} defined as

$$V'_{gs} = V_{gs,q} + b_1\, v_{gs,p}\,, \tag{4.22}$$

with $b_1 = 0$ for a class-A PA, and $b_1 = 1$ for class-AB, -B, and -C PAs.

Considering these approximations, both gate-source and drain-source voltages are modelled as constant functions and the final solution for (4.17) is:

$$age = \mathbb{K}\left(\frac{2\sin(\alpha) - 2\alpha\cos(\alpha)}{1 - \cos(\alpha)}\right), \tag{4.23}$$

$$\mathbb{K} = N\, k_1^m\, k_3\, \exp(-mk_2)\, I_{max}\,. \tag{4.24}$$

4.4 Validation of Age Model

In this section the model mentioned in (4.23) is validated by forming reliability simulations. For the first step, age model is tested under input DC stress considering a constant voltage over drain-source. As some parameters of impact ionisation are not available in user's manual published for BSIM4 model, therefore, all these parameters can be extracted during DC simulation by comparing calculation and simulation results. Keeping these unknown parameters unchanged, the next steps is to investigate how age model respond to the fluctuations across V_{ds}. So, the proposed age model will be validated under various peak values of drain-source voltage. All reliability simulations were run in the RelXpert simulation tool in the Cadence Spectre RF simulator for an ageing time of $t_{stress} = 5000\ s$ under DC and AC stresses.

4.4.1 DC Analysis

Figure 4.3 shows the test bench used to validate the model. As the transistor model, we used the BSIM4 FET model with a channel length and width of 30 µm and 210 nm, respectively. Clearly, drain current in (4.11) is equal to quiescent point current for DC bias condition. Therefore, The DC counterpart of (4.17) is:

$$age = k_1^m\, k_3\, \exp(-mk_2)\, I_q\, t_{stress}. \tag{4.25}$$

The parameters in (4.25), which are the same parameters involved in (4.24), were extracted by fitting (4.25) to the simulation results of RelXpert under DC stress. The biasing conditions under DC stress were set as: $V_{ds} = 2$ V, V_{gs} was swept to 3 V, and $R_d = 100\ \Omega$. The $I_d - V_g$ and $I_{sub} - V_g$ characteristics of the BSIM4 transistor model are shown in Figure 4.4. From (4.25) and Figure 4.4 it is anticipated that ageing of transistor follows the variation of substrate current since age model is a strong function of I_{ii}.

Figure 4.5 presents a comparison between simulated and calculated age results showing an appropriate compatibility. This compatibility proves that our proposed model is able to exactly follow variation of substrate current as a function of V_g and properly predict ageing of transistor so that the maximum age will occur around absolute peak value of substrate current (near $V_g = 0.9\ V$). Figure 4.5 also illustrates that RelXpert cannot calculate transistor ageing for $V_g < 0.636\ V$. This means that, for $V_g = 0.636\ V$ transistor is biased at the edge of conduction which is

suitable bias point for class-B operation mode. Additionally, if transistor is biased for gate voltages bellow 0.636 V, transistor is off, and it will operate in class-C.

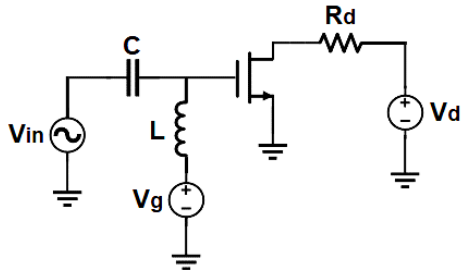

Figure 4.3: Proposed test bench to validate age model.

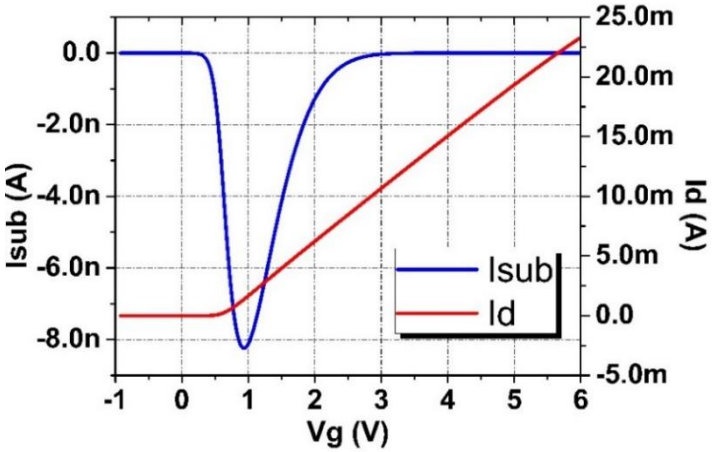

Figure 4.4: $I_{sub} - V_g$ and $I_d - V_g$ characteristics of transistor used in Figure 4.3.

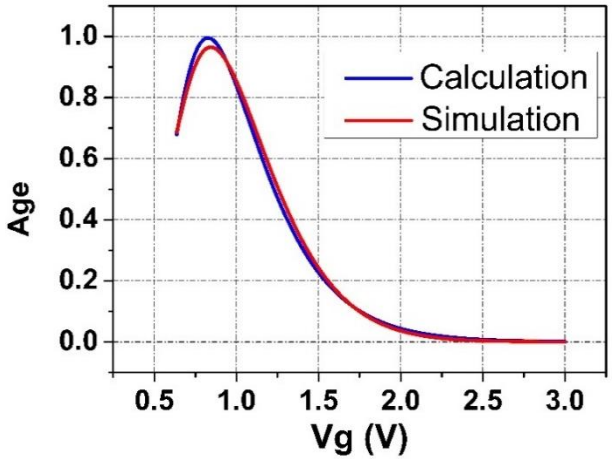

Figure 4.5: Calculation and simulation age results versus gate voltage.

4.4.2 AC Analysis

To obtain the AC counterpart of Figure 4.5, we considered a constant drain-source voltage of $V_{ds} = 2$ V and a small AC fluctuation and performed simulations for a range of bias points for class-A, the single bias point of class-B, two bias points for class-AB ($V_g = 0.7$ V and 0.67 V, corresponding to $\theta = 250°$ and $290°$ respectively), and four bias points for class-C ($V_g = 0.5$ V,

0.4 V, 0.25 V, 0 V, corresponding to $\theta = 140°, 123°, 106°$, and 90°, respectively). Figure 4.6 shows the results of age calculation and simulation plotted versus gate bias point. As illustrated, the fit is excellent.

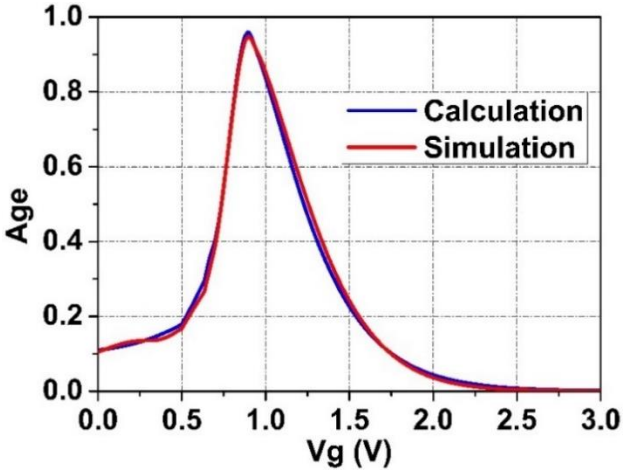

Fig 4.6: Age versus gate voltage.

Table 4.1: Variation of $v_{ds,p}$ and age for different values of R_d for three bias points in class-A.

$R_d(\text{k}\Omega)$			0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.3	1.5	1.8
Class A1	$V_{ds,p}\ (mV)$		42.4	80.4	114.7	146.2	175	202	226	248.6	269.6	289.2	340.9	370.84	409.4
	age	Calculation	0.055	0.07	0.09	0.11	0.14	0.17	0.21	0.25	0.29	0.34	0.51	0.66	0.9
		Simulation	0.045	0.057	0.073	0.094	0.12	0.15	0.18	0.22	0.26	0.31	0.48	0.63	0.82
Class A2	$V_{ds,p}\ (mV)$		43.73	83.6	119.86	152.71	182.7	210.5							
	age	Calculation	0.362	0.448	0.547	0.661	0.79	0.936							
		Simulation	0.378	0.448	0.544	0.664	0.808	0.974							
Class A3	$V_{ds,p}\ (mV)$		44	84.4	121.16										
	age	Calculation	0.662	0.745	0.972										
		Simulation	0.634	0.735	0.959										

Table 4.2: Variation of $v_{ds,p}$ and age for different values of R_d for class-B and two bias points in class-C.

$R_d(\text{k}\Omega)$			0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
Class B	$V_{ds,p}\ (mV)$		46.35	89.2	127.3	166	201	233	263.2	292	318	343.3
	age	Calculation	0.234	0.187	0.15	0.12	0.093	0.073	0.057	0.045	0.035	0.028
		Simulation	0.267	0.176	0.122	0.087	0.083	0.079	0.049	0.065	0.059	0.055
Class C1	$V_{ds,p}\ (mV)$		58.65	112.9	163	210.5	253.8	294.5				
	age	Calculation	0.134	0.076	0.049	0.04	0.028	0.02				
		Simulation	0.134	0.065	0.032	0.022	0.014	0.01				
Class C2	$V_{ds,p}\ (mV)$		58.65	113	160	210	254	294				
	age	Calculation	0.114	0.0637	0.0487	0.0347	0.0244	0.0161				
		Simulation	0.105	0.0534	0.037	0.0188	0.012	0.0085				

In order to validate the model under AC stress (i.e. under large signal fluctuations), we gradually increased the output resistance so as to raise the fluctuation over the drain terminal. Three different bias points for class-A (A1, A2, and A3 corresponding to $V_g = 2\ V,\ 1.4\ V$ and $1.2\ V$ respectively), the single bias point of class-B, and two bias points for class-C (class C1 and C2 corresponding

to $V_g = 0.25\ V$ and $0\ V$) were considered for this validation. Now, output resistor is gradually increased to raise the fluctuation over drain-source.

Conceivably, R_d cannot increase unlimitedly in class-A operation mode because the age cannot exceed unit value and age > 1 is meaningless. As a consequence, maximum R_d is restricted by the maximum value of age. Tables 4.1 and 4.2 show the list of R_d used for this validation, the variations in $V_{ds,p}$ due to this change in R_d, and the age values obtained from calculation and simulation. Figures 4.7 and 4.8 also illustrate a comparison between the proposed model and the RelXpert simulation results for age variations versus output resistance. As it can be seen from these figures, there is a good agreement between simulation results and calculation ones obtained from age model in (4.23). It can, therefore, be claimed that proposed model can predict age in power amplifiers. For the last step, it is explained in the next section how PA reliability is evaluated.

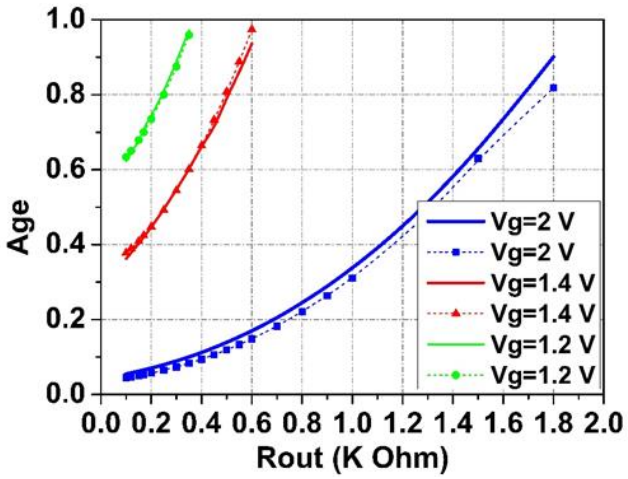

Figure 4.7: Simulation and calculation age results versus output resistor for three class-A modes extracted under AC and DC stresses (solid and dashed lines show calculation and simulation results, respectively).

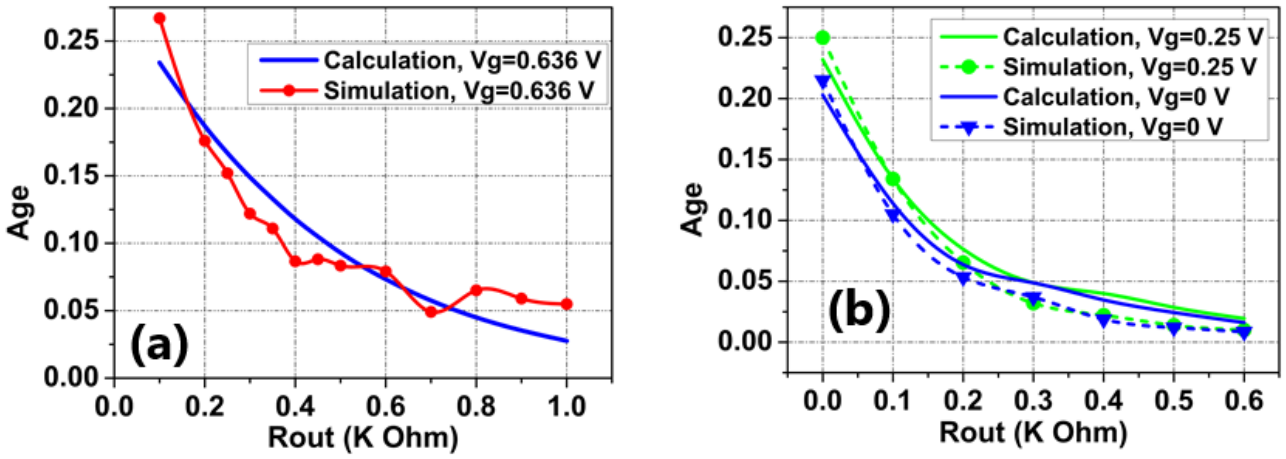

Figure 4.8: Simulation and calculation age results versus output resistor for a) class-B and b) two class-C modes extracted under AC and DC stresses.

4.5 Reliability versus Conduction Angle: Results and Discussion

Figure 4.9 shows the age variation versus conduction angle. Besides the excellent fit of the proposed model to the simulation results of RelXpert, this figure shows clearly that a class-A PA exhibits the worst performance as compared to Class-AB, -B and -C PAs in terms of reliability. This drives us toward a new trade-off between the different classes of PA, which includes reliability as a must-be-considered criterion in the design of a PA besides the normalized maximum output power ($P_{out,max,(norm)}$) and maximum efficiency (η_{max}), given by:

$$P_{out,max,(norm)} = \frac{1}{\pi}\left(\frac{2\alpha - \sin(2\alpha)}{1-\cos(\alpha)}\right) \tag{4.26}$$

$$\eta_{max} = \frac{1}{4}\cdot\left(\frac{2\alpha - \sin(2\alpha)}{\sin(\alpha) - \alpha\cos(\alpha)}\right). \tag{4.27}$$

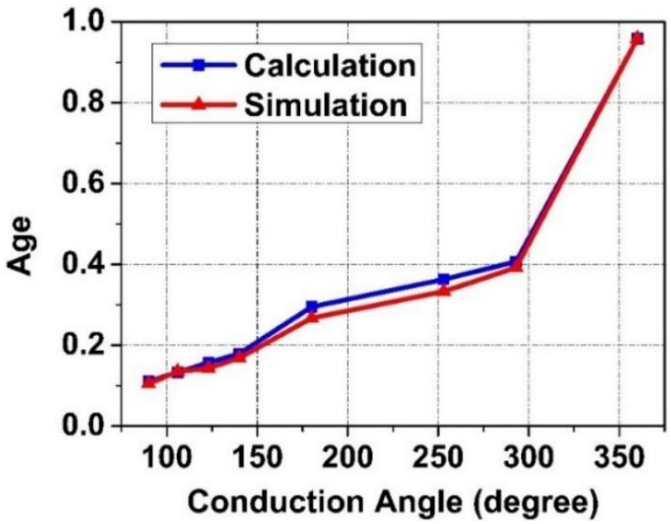

Figure 4.9: Age versus conduction angle from 90° to 360°

This new trade-off is illustrated in Figure 4.10. Although class-A shows the best linearity, it offers the lowest efficiency, high power consumption, and also the worst reliability. The output power has the highest value for $\theta = 240°$ in class-AB. The best performance in reliability, efficiency, and power consumption can be obtained in class-C at the cost of the lowest linearity.

To further clarify this trade-off, variations of η_{max}, $P_{out,max,(norm)}$ and age versus I_q/I_p are illustrated in Figure 4.11. It is worth noting that a transistor never turns on for $I_p = -I_q$ (or equivalently, $I_q/I_p = -1$). At this condition, the conduction angle is equal to 0. Also, $I_q/I_p = 0$ corresponds to the condition where the device works in class-B (see Figure 4.2). Figure 4.11 shows that the maximum age occurs when $I_p = I_q$, where the transistor is biased at the edge of class-AB. For $I_q/I_p \geq 1$, the conduction angle remains unchanged at 360° and the age shows a

downward trend with increasing I_q/I_p. Also, for $I_q/I_p > 1$, the maximum efficiency and the normalized maximum output power remain constant with increasing I_q/I_p, because they are functions of just the conduction angle.

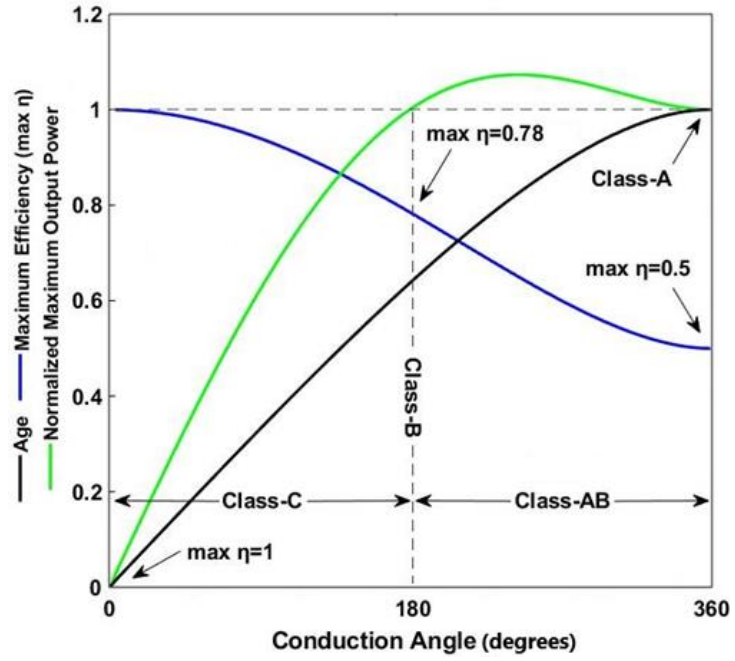

Figure 4.10: Trade-off between maximum efficiency, normalized maximum output power, and age as functions of conduction angle.

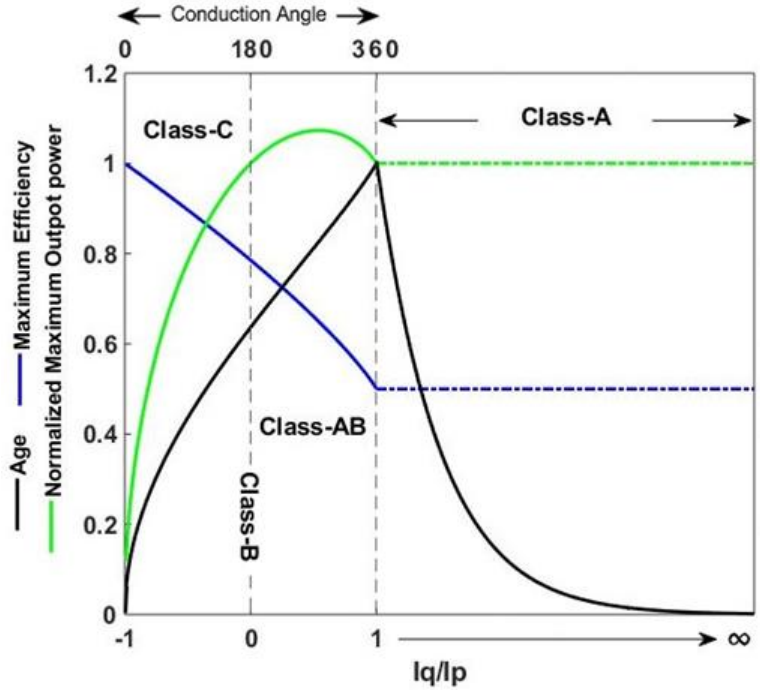

Figure 4.11: variation of three PA design criteria versus $\frac{I_q}{I_p}$ ratio.

4.6 Conclusion

An analytical model for age is presented in this chapter which predicts very well HCI-induced degradation in power amplifiers. This model gives an expression for age versus conduction angle. Utilizing this model, all the classic classes of PA were compared in terms of reliability. A new trade-off for PA design was introduced by introducing reliability as a figure of merit at the beginning steps of the design phase. It was proved in this chapter that whereas a class-A power amplifier shows reasonable normalized maximum output power, it suffers from the highest degradation. It was further shown that the lower is the conduction angle, the lower is the age, and the higher is the maximum efficiency of a PA.

Chapter 5

Modification of Long-Term Degradation Effects of Power Amplifier

5.1 Chapter Abstract

This chapter presents a simple, but innovative, approach to compensate for long-term degradation in circuits. Due to ageing, circuit performance will degrade even after following design steps considering the reliability concept. This beneficial approach is performed based on variable capacitors and can be a good idea to retrieve fresh performance over time.

5.2 Introduction

Although the increase of V_{th} and degradation of g_m and I_d after HCI effects are well known, it is found in our research that the degradation in small-signal elements such as gate-source and gate-drain capacitors (C_{gs} and C_{gd}) can severely affect PA performance. However, mitigating the effect of transistor ageing on circuit performance, taking a circuit approach, was never reported in the literature. The only report about circuit modification was published in [8]. The authors suggested that if a cascode is used instead of a single-stage structure, V_{ds} is reduced and, then, the HCI effect is expected to decrease in turn. In addition, the breakdown effect can be decreased by using lower voltage swings. Therefore, a cascode structure can be used to satisfy circuit modification in terms of reliability.

In this chapter, an approach is presented compensating for the effect of transistor ageing on the gain, input and output return losses of a power amplifier. At first, we discuss the PA circuit and analyse long-term degradation effects. Then, simulation results of the effect of HCI on this PA, using the RelXpert simulation tool, will be presented. Next, the device-level parameter degradation which is responsible for long-term degradation of the PA performance is analysed. Based on our analysis we present a new PA circuit to mitigate these effects. The simulation results for the new PA are also presented and a conclusion is drawn as final part of this chapter.

5.3 Power-Amplifier Design

Figure 5.1 shows the PA designed in the 45nm-RFSOI CMOS process, for which the long-term degradation effects have been studied. We chose this as our vehicle to investigate degradation effects as this design was fabricated in [46], yielding promising results. In [46] no analysis of the long-term degradation of this PA's performance was performed, but it is one of the subjects of this thesis. In our simulation we were able to reproduce the experimental results of [46] and this gives us credibility to use our simulations to be used as a tool to study reliability in this structure.

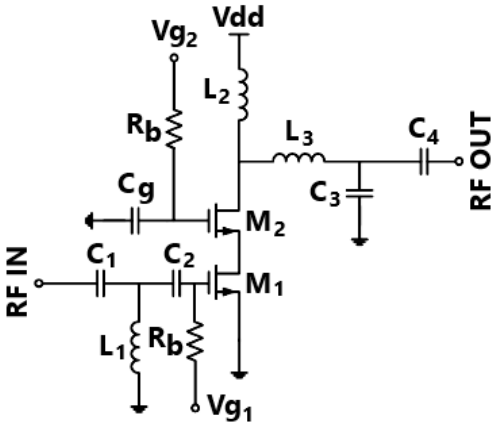

Figure 5.1: The n-MOS power amplifier proposed in [46] and used in this thesis for reliability studies.

The simulation results are shown in Figure 5.2. It is clear that the peak values of S_{21}, S_{11} and S_{22} of the "fresh" circuit are equal to 14 dB, -18.6 dB and -16.6 dB, respectively, which all are quite similar to those results reported in [46]. This figure also shows that the overall gain, input and output matching suffer from degradation and frequency shift. The study of the degradation of device parameters can help in finding an approach for overcoming the effect of this degradation on the circuit performance. In the next section we investigate the device-level parameters which cause the degradation of circuit performance.

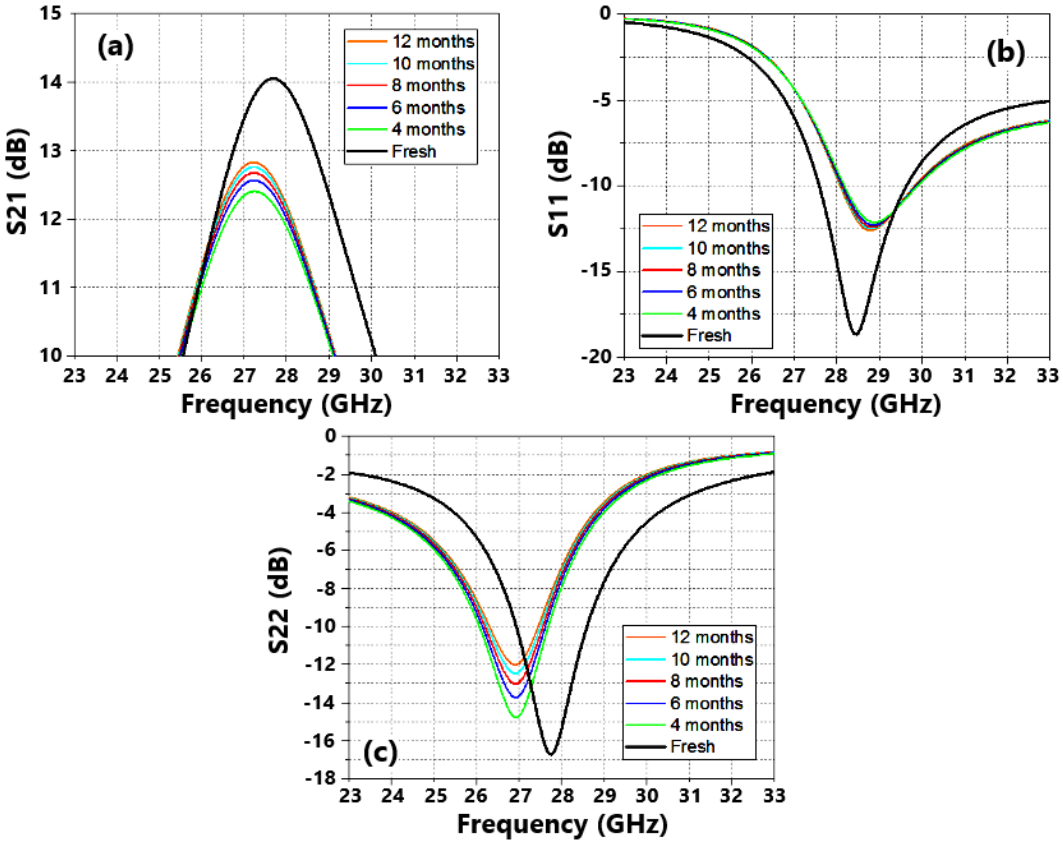

Figure 5.2: Simulation results for the fresh and degraded a) S_{21}, b) S_{11}, and c) S_{22} for 4, 6, 8, 10, and 12 months of ageing time.

5.4 Modified Power-Amplifier Structure

The input impedance (Z_{in}), output impedance (Z_{out}) and overall transconductance (G_m) are all functions of device DC and small signal parameters. This is further illustrated in the next sub-sections by analysing the PA of Figure 5.1 and presenting the equations that describe G_m, the resonance frequency and Z_{in}. The normalized variations of gate-drain and gate-source capacitors versus stress time are extracted and plotted in Figure 5.3. From this figure, these parameters are degraded under HCI stress in accordance with power law.

The input and output return losses (S_{11} and S_{22}) of an amplifier are, respectively, related to the input and output impedances, where Z_{in} and Z_{out} are related to small-signal parameters. The overall transconductance of an amplifier is also related, as shown below, to C_{gs1} (i.e., C_{gs} in M_1). So, degradation of small-signal parameters causes the S-parameters S_{11}, S_{21} and S_{22} to degrade. In what follows we present the relations between the overall gain, transconductance, and centre frequency and the small-signal parameter C_{gs1}. This will allow us to propose a PA design which is immune to degradation.

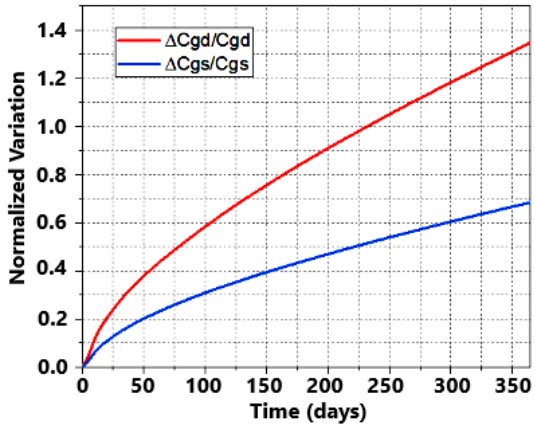

Figure 5.3: Normalized variation C_{gd} and C_{gs} for 45 nm RFSOI model considered in this research.

5.4.1 Gain

Considering the small-signal model for the PA, the overall gain A_v and transconductance G_m can be written as follows if $C_1 \gg C_{gs1}$ is met in the design:

$$A_v = G_m \, Z_{out} \, , \tag{5.1}$$

$$G_m \approx \frac{g_m}{1 + \frac{C_{gs1}}{C_2}} \tag{5.2}$$

Based on (5.2), G_m is indirectly proportional to C_{gs1}. As M_1 degrades over time, C_{gs1} increases, causing G_m and the gain to decrease. Interestingly, it is possible mitigate this decrease in G_m by tuning C_2, so that we can design it as a bias-dependent varactor.

5.4.2 Input Impedance

The input impedance of the PA of Figure 5.1 is given by

$$Z_{in} = \frac{1}{j\omega C_1} + \frac{1}{j\omega\left(C_{eq} - (1/L_1\omega^2)\right)} \, , \tag{5.3}$$

where $C_{eq} = \frac{C_2 C_{gs1}}{C_2 + C_{gs1}}$. From (5.3), the resonance frequency is given by

$$\omega_0 = \left(\frac{\left(1 + (C_{gs1}/C_2)\right)}{L_1 C_1 \left(1 + (C_{gs1}/C_2) + (C_{gs1}/C_1)\right)} \right)^{1/2} . \tag{5.4}$$

Note that, again, when $C_1 \gg C_{gs1}$, ω_0 simplifies to

$$\omega_0 \approx \left(\frac{1}{L_1 C_1}\right)^{1/2} . \tag{5.5}$$

From (5.5), we can also adjust the operating frequency using a second bias-dependent varactor in place of C_1. When the operating frequency changes after degradation, the value of C_1 is tuned a little to get the initial operation frequency, so that the gain is not noticeably affected by this change. By replacing these two capacitors with two varactors, the circuit mentioned in Figure 5.1 is changed into Figure 5.4.

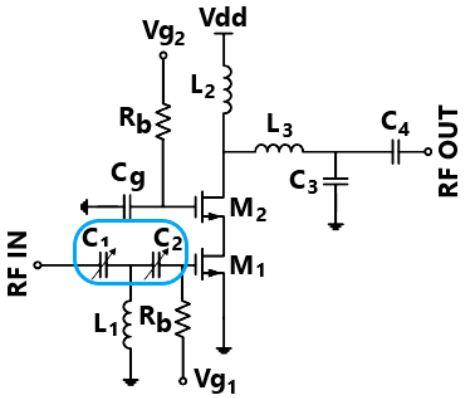

Figure 5.4: The proposed degradation-immune PA.

5.5 Results and Discussion

In this section we present the results of the proposed PA where tuning the capacitors C_1 and C_2 can alleviate the effect of long-term performance degradation to a reasonable extent. To clearly explain this, we first define

$$\alpha(t) = C_{1,tuned}(t)/C_{1,fresh}\ , \tag{5.6}$$

$$\beta(t) = C_{2,tuned}(t)/C_{2,fresh}\ , \tag{5.7}$$

where $C_{1,fresh}$ and $C_{2,fresh}$ are the two capacitors C_1 and C_2 for the fresh circuit, $C_{1,tuned}$ and $C_{2,tuned}$ are the values of C_1 and C_2 required for the degraded circuit, and t is the ageing time. We have found that, to solve the long-term degradation of the PA performance, α and β must vary, at each given ageing time, as shown in Figure 5.5. As can be seen from Figure 5.3, there is a significant change in C_{gs1} at the initial stage of transistor ageing. This is then followed by a gradual change of this parameter as the transistor ages further. So, the initial changes in C_1 and C_2 are considerably larger than those at later times. The required tuning in C_1 and C_2 is possible with the help of the proposed topology in which C_1 and C_2 are implemented as varactors. The variation in the capacitance required is well within the tuneable range of typical varactors.

Figure 5.6 shows the simulation results for the gain, input and output matching using this input-matching tuning approach. As shown in this figure, the gain at all ageing times is approximately 14 dB, which is the same as the gain of the fresh circuit, and the difference in centre frequency

between the S_{21} curves for the fresh and degraded circuits is lower than 200 MHz. Also, as shown in Figures 5.6 (b) and 5.6 (c), the degradation in the input and output return losses is, to a large extent, resolved, that is, both S_{11} and S_{22} have been modified and have reached close to the S_{11} and S_{22} of the fresh circuit.

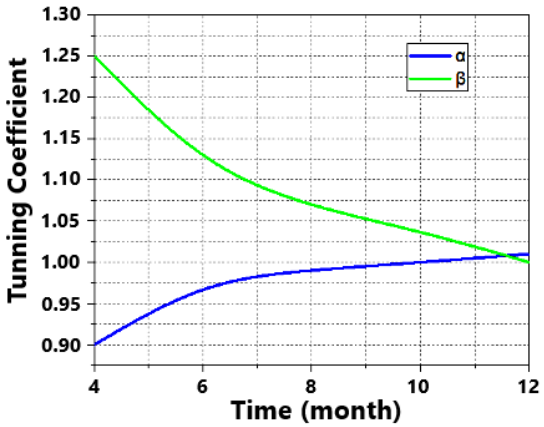

Figure 5.5: The variation of the normalized C_1 and C_2 with the ageing time.

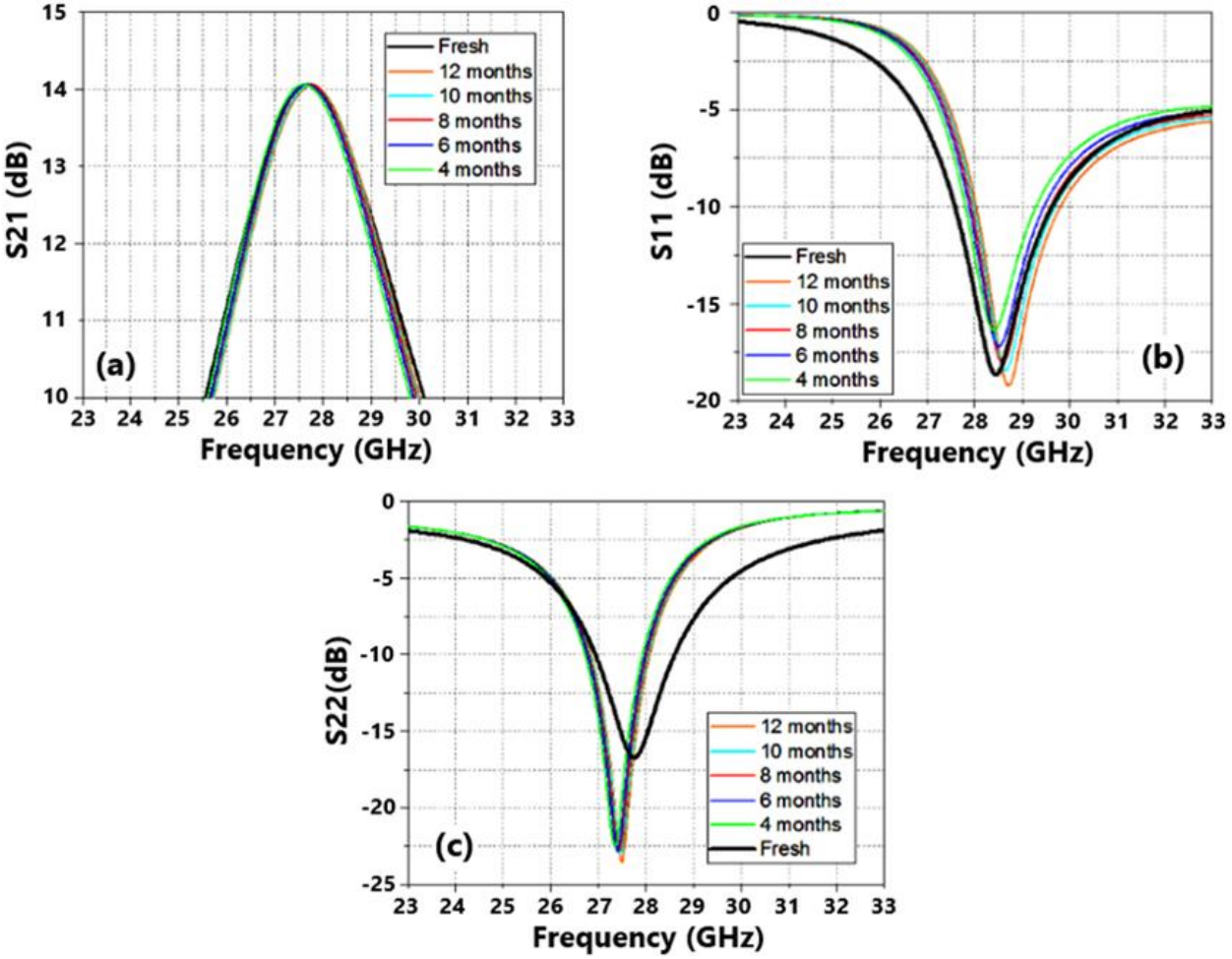

Figure 5.6: Simulation results for the degradation of a) S_{21}, b) S_{11}, and c) S_{22} after proper tuning of the varactors used in the input matching network.

5.6 Conclusion

DC and RF stress are found to change the input capacitances which disturb the matching, causing significant performance degradation of the circuit. Circuit modification approach to compensate for long-term degradation of a 45nm RFSOI PA was investigated in this chapter. Proposed approach was to design a tuneable input matching network which is implemented by inserting two varactors instead of regular capacitors in the input network. With this tuneable network, the degradation in the gain and the shift in the operating frequency of the power amplifier are resolved and simulation results after applying this new approach are in a good agreement with the results obtained for fresh circuit. This simple approach may be a trigger point for designers to reach more innovative ideas in terms of revitalizing fresh performance over time.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Reliability in radio-frequency circuits, especially in power amplifiers, was the author's research topic for the MRes candidature carried out at the School of Engineering, Macquarie University, Sydney, Australia, between February and November 2018.

This thesis is divided into six chapters consisting of an introduction and a comprehensive literature review presented in Chapters 1-3. At first, the predominant ageing mechanisms in silicon-based devices were introduced and it was indicated that hot carriers are the most important phenomenon affecting all DC and small-signal device parameters. Then, the necessity of device reliability modelling was explained by introducing the correlation between device-level degradation and the degradation of electronic circuits. It was shown that the circuit performance (gain, linearity, noise figure, efficiency, PAE, etc.) is a function of small-signal and DC parameters (such as threshold voltage, transconductance, drain current, C_{gs}, C_{gd}, etc.) and it will degrade after device degradation.

In Chapter 3, some models developed to predict the behaviour of degradation mechanisms were presented and it was mentioned that, if these models are generalised to the circuit level, new circuit-levels model are extracted and, consequently, reliability can be embedded into the design process. The "Reliability-Aware Design" concept was, then, defined by introducing a trade-off between reliability and circuit performance (for PA design in this thesis, for example).

Power Amplifier classes has never been compared to each other for their degradation. The main idea of Chapter 4 is to find a circuit-level age model able to provide designers with a tool to

enhance their designs in terms of reliability. It was analytically proved by using a proposed age model that class-A suffers from the most ageing compared with other classes. Indeed, the lower the conduction angle, the lower the ageing and the higher efficiency will be. All the calculated results were in a good agreement with simulation results extracted by reliability simulations performed in RelXpert simulation tools. This agreement proved the validity of the presented PA reliability model.

The next step is to find an approach to mitigate degradation even after circuit design. A simple, but effective, solution was presented in Chapter 5. In this solution, two capacitors in the input matching network were replaced by two varactors and the HCI-induced degradation of the gate-source capacitor was compensated for by tuning these new varactors. Apparently, the gain, the input return loss, and the output return loss can be set to fresh values, as shown in this chapter.

A conference paper and a transaction article were published using the results mentioned in Chapters 4 and 5. The first one is accepted in IEEE International RF and Microwave Conference (RFM), Penang, Malaysia, 2018. The other one has been submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.

6.2 Future work

Reliability studies were carried out for a Si-based transistor model (BSIM4) in this thesis. However, the degradation process in other technologies may be much more complicated. For example, GaN-based power transistors suffer from certain parasitic and reliability issues that limit their static and dynamic performance and the maximum switching frequency.

Due to the high mobility and high density of the electrons in the two-dimensional electron gas (2DEG), GaN-based high-electron-mobility transistors (HEMTs) have emerged as excellent devices for application in the power conversion field. Those two properties result in a significant reduction of the switching losses when the devices are operated in a switching-mode power converter [47-50]. Unlike what is already assumed during converter design, switches are not ideal and some parasitic capacitors such as the off-state output capacitor, C_{oss}, can affect switching performance. So, as a starting point for future work, the hard-switching characteristics of a DC-DC Boost converter were studied by the author of this thesis and his colleagues. This converter is designed based on GaN devices using an ASM-GaN compact model. This is proved that accurate prediction of the off-state output capacitance results in the expected prediction of the dynamic character of switching losses across the power transistor. These simulations can thus be used to

predict the switching losses, and furthermore help in the optimisation of a power-converter design during the initial phase of design. Our results in this field are published as a conference paper which has recently been accepted in the Australian Universities Power Engineering Conference (AUPEC), Auckland, New Zealand, 2018.

However, despite the excellent performance of GaN devices, other technological aspects must be met before GaN power HEMTs can find wide application in the market. For instance, these devices suffer from trapping and early degradation mechanisms that affect the dynamic performance, degradation of the off-state capacitor, and, finally, the reliability of the transistors. The following relevant processes are reported as the main ageing mechanisms in these devices: (i) trapping of electrons in the buffer, which is induced by off-state operation; (ii) trapping of hot electrons, which is promoted by semi-on state operation; (iii) trapping of electrons in the gate insulator, which is favoured by the exposure to positive gate bias. Moreover, we will describe one of the most critical reliability aspects of Metal-Insulator-Semiconductor HEMTs (MIS-HEMTs), namely time-dependent dielectric breakdown [47-50].

Modelling all these mechanisms will definitely need long research because they are considerably more complicated than the degradation mechanisms in FETs. Therefore, evaluating reliability in GaN-based devices and improving the performance of circuits designed by these devices will be my future work. The wide application of GaN devices in the industrial, automotive and photovoltaic fields is a good motivation for me to follow this research topic.

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