A KU-KA BAND LOW NOISE AMPLIFIER IN 0.25 μM SIGE BICMOS TECHNOLOGY

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STATEMENT OF CANDIDATE

I, Jiawei SHEN, declare that this report, submitted as part of the requirement for the award of Bachelor of Engineering in the Department of Electronic Engineering, Macquarie University, is entirely my own work unless otherwise referenced or acknowledged. This document has not been submitted for qualification or assessment an any academic institution.

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ABSTRACT

Low Noise Amplifiers(LNA) are electronic circuits that provide high gain but maintain as low noise as possible. LNA is one of the main building blocks of the RF receiver circuit. It is used at the front-end of the receiver. These receivers require high-performance LNA with wide bandwidth, high gain and low noise. This report presents the design of a LNA operating over 14.3 GHz to 37.46 GHz, with midband gain of 18.25 dB at around 25 GHz. This circuit can be used for Ku-Ka band receiver application. The circuit is designed using IHP SG25H1 library (0.25 μm SiGe BiCMOS technology). The proposed LNA design consists of two stages. In the first stage, a cascode topology is used followed by the a common-emitter stage. The aim for this LNA design was to achieve a wide operating bandwidth, with at least 15 dB of gain and noise figure below 5dB. The simulation results for designed LNA meets the above mentioned specifications. All the simulations are done in AWR. The useful formula and theory are also included in this report.

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Chapter 1

Introduction

1.1 Background

Low Noise Amplifiers are the electronic circuits that provide high gain but adds as low additional noise as possible. They preserve the Signal-to-noise ratio of the input signal. LNA is an important building block of a receiver front-end architecture. It is found close to the receiving antenna. The primary goal of the LNA is to amplify the weak input signal and to keep a low noise figure of the input signal [13].

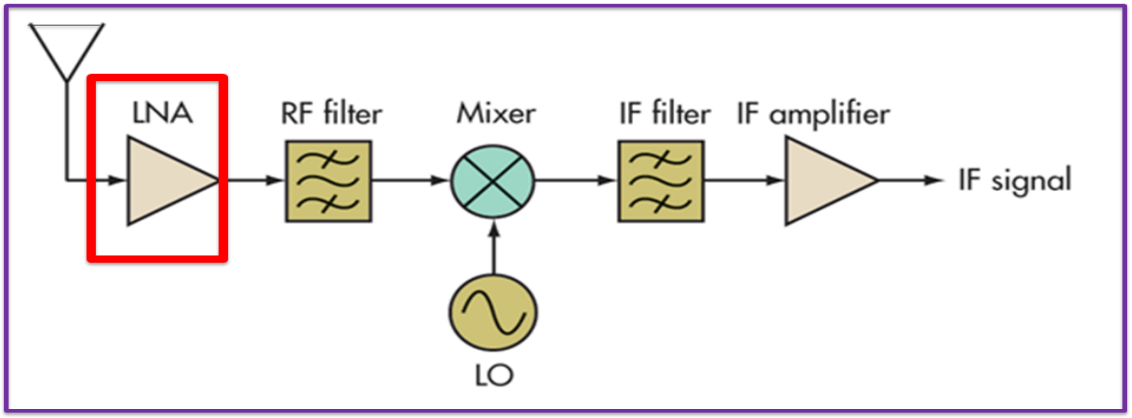


Figure 1.1: Block diagram of a receiver.

In this project, the design of a LNA suitable for K-Ka band receiver is presented. Different devices and different topologies can be used for the LNA design. Bipolar Junction transistor (BJT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are the most commonly used active devices in different electronic circuits. These transistors form the backbone of the electronic circuit design. Therefore a brief overview of these transistors and the different configurations are presented in the chapter.

1.2 Basics of BJT

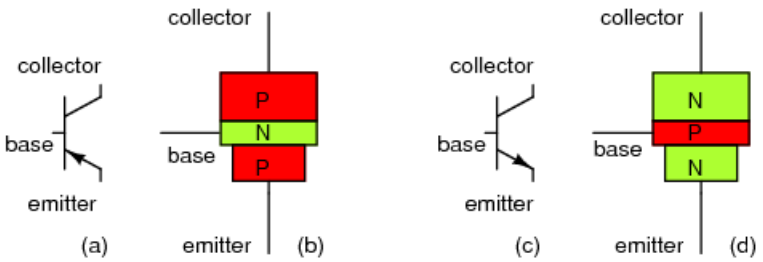
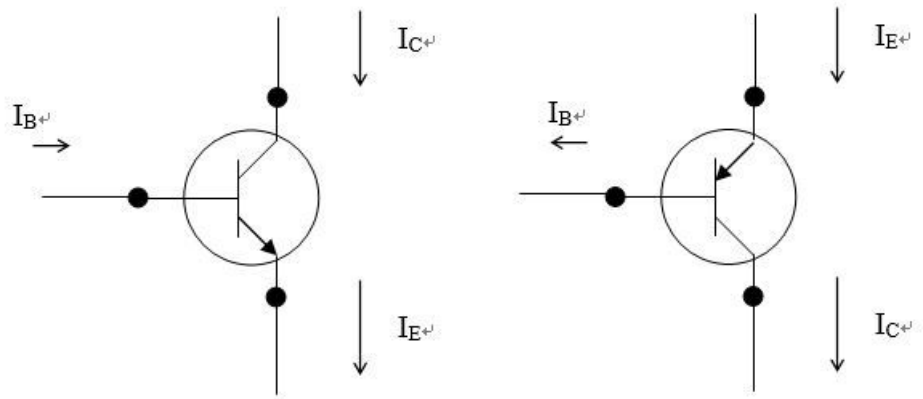


Figure 1.2: NPN and PNP BJT.

Transistors are three terminal active devices made of semiconductor materials. Bipolar Junction Transistor (BJT) is a common electronic device that is widely used in different electronic circuits. It can be used for different applications such as an amplifier, a switch, a buffer, an oscillator, a non-linear circuit etc [5].
BJT is made of P and N type semiconductor material. The basic structure of Bipolar Transistor consists of two PN-junctions producing three connecting terminals. Each of these terminals are identified by a name, such as Emitter (E), Base (B) and Collector(C). The emitter terminal is identified by an arrow in the symbol fig 1.2, the collector terminal is opposite to the emitter and the other remaining terminal is the base.
The BJT can be classified into two types based on the three semiconductor regions. If the emitter region is n-type, the base region is p-type and the collector region is n-type, then it is called a NPN transistor. The other type of BJT is called PNP transistor in which the emitter is p-type, base is n-type and the collector is p-type. The principle of operation for these two types of transistors, NPN and PNP are same, but their biasing and the polarity of the power supply are different [9].
In the symbols (fig 1.2), the arrows represent the direction of the DC current flow for both the NPN and PNP transistors. BJT is a current controlled device. In both the PNP and the NPN transistors, the base current is very small in the order of microampere, whereas the collector and the emitter currents are larger and in the order of milliampere. For the NPN transistor, the base current flows into the transistor while for the PNP transistor the base current flows out of the transistor. The collector and emitter currents flow in the same direction and in the direction of the arrow (fig 1.3 showing current direction). Following the KCL, the emitter current is the sum of the base and the collector currents.

Depending on the bias condition (forward or reverse) of each of the two junctions, emitter-base junction and collector-base junction, BJT operates in different modes of operation active, saturation or cut-off. In the active mode, the transistor can operate as an amplifier. In the cut-off and the saturation modes, the transistor can be made to operate as a switch used for logic circuits.



(a) NPN transistor with direction of the current

(b) PNP transistor with direction of the current

Figure 1.3: Transistor with direction of the currents

1.3 Bipolar Transistor Configuration

There are three possible ways to connect the BJT in an electronic circuit as it is a three terminal device, in which one of the terminals is common to both the input and the output. These three configurations are :
Common Base Configuration (has Voltage gain, no Current gain)
Common Emitter Configuration (Both Voltage gain and current gain)
Common Collector Configuration (No Voltage gain, has Current gain)

1.3.1 Common Base Configuration

In this configuration, the base is common to both the input and the output signal, hence it is named common base (CB) configuration. The input signal is applied between the base and the emitter terminals and the output signal is taken between the base and the collector terminals (fig 1.4). The base terminal is either grounded or connected to a fixed bias voltage. The input emitter current is larger than the output collector current as the emitter current is the sum of base and collector currents. It has high output resistance and low input resistance, that gives a high output to input resistance ratio. Therefore this configuration is suitable for voltage gain but it does not give any current gain. The common base circuit is used in amplifier circuits such as microphone pre-amplifiers or radio frequency (RF) amplifiers due to its very good high frequency response and wide bandwidth [9].

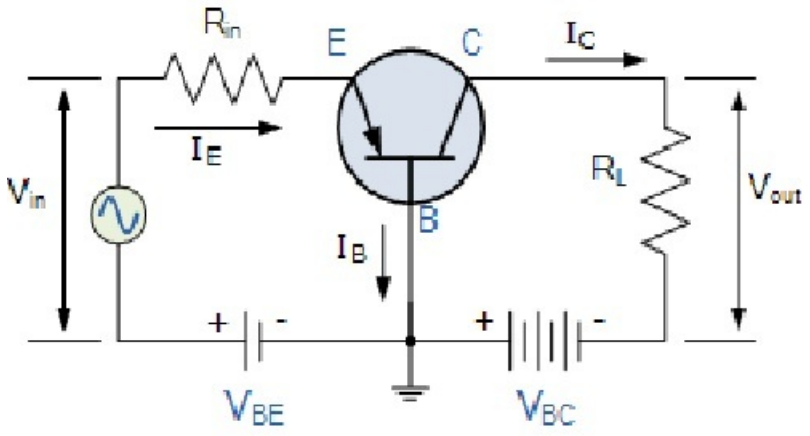


Figure 1.4: Common-base.

1.3.2 Common Emitter Configuration

In the common emitter (CE) configuration(fig 1.5), the input signal is applied between the base and the emitter terminals and the output signal is taken between the collector and the emitter terminals. Therefore the emitter terminal is common to both the input and the output signals, hence it is called common emitter configuration. This configuration gives the highest current and the power gain among all the three BJT configurations. As the load resistance is connected to the collector terminal in this configuration, the current gain is quite large in this case as it is the ratio of the collector to the base current ($I_C/I_B = \beta$). The current gain, power gain and the input impedance are greater than the common base topology, but the voltage gain is smaller. CE configuration is commonly used in amplifier circuits.

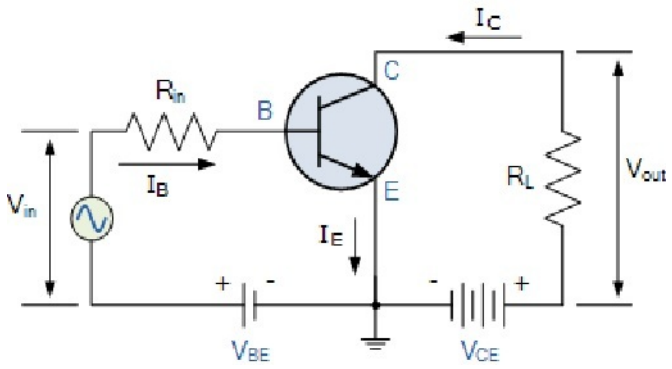


Figure 1.5: common-emitter.

1.3.3 Common Collector Configuration

In this case, the input signal is connected to the base, the output signal is taken from the emitter, while the collector terminal is common through the supply. This configuration is also known as Voltage follower or Emitter Follower. As the output resistance is connected with the emitter terminal, the output current is equal to the emitter current. Therefore this configuration has a very high current gain equal to the ratio of emitter current to the base current ($I_E/\ I_B = \beta + 1$). It has high input impedance and relatively low output impedance. Therefore it is very useful for impedance matching applications. It cannot provide any voltage gain.

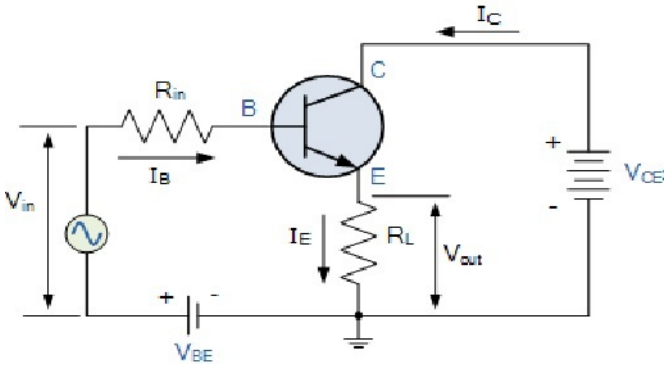


Figure 1.6: Common-collector.

1.4 MOSFET

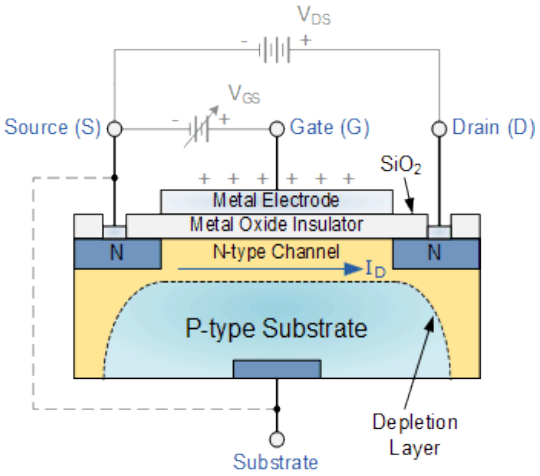
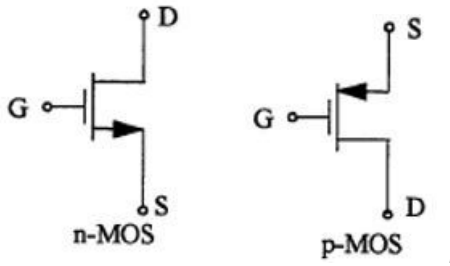


Figure 1.7: MOSFET.

MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a voltage controlled field effect transistor. A typical field effect transistor (FET) has three terminals, source,

drain and the gate. A conducting channel is formed between the source and the drain where the number of charge carriers in the channel is controlled by the gate. In a MOSFET, the gate is separated from the conducting channel by an insulating silicon dioxide (SiO2) layer. The current control mechanism is based on an electric field that is established by the voltage applied at the control terminals. MOSFETs are widely used in digital and analog integrated circuits for various applications [11].
MOSFETs can be classified into two types based on the charge carriers in the channel : NMOS and PMOS. A NMOS or n-channel MOSFET consists of P-type substrate. The source and the drain regions consist of two heavily doped n-type regions, electrons flow in the conducting channel. As the gate terminal is separated from the main current carrying channel, no current flows into the gate. PMOS or p-channel MOSFET consists of n-type substrate. The source and the drain regions of a PMOS consist of two heavily doped p-type regions, holes flow in the conducting channel.
The basic structure of a MOSFET and the symbols of PMOs and NMOS are shown in fig 1.8.



(a) n-MOS (b) p-MOS

Figure 1.8: MOSFET symbols

1.5 MOSFET Configurations

There are three basic MOSFET configurations and in each of these configurations, one terminal is common to both the input and the output circuits. These three configurations are:

1.5.1 Common Gate configuration

In this configuration, the gate terminal is common to the input and the output circuit. The input signal is applied at the source and the output signal is taken at the drain. The gate is either at ground or connected to a fixed voltage. This configuration provides a low input impedance and high output impedance. It provides voltage gain and the input and output signals are in phase.

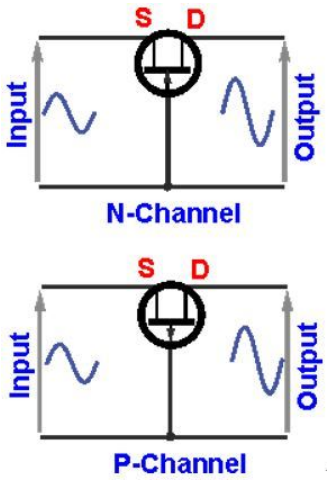


Figure 1.9: Common-gate.

1.5.2 Common Source configuration

This configuration is widely used in amplifiers. In this case the Source terminal is connected to the ground. The input signal is connected to the gate terminal and the load resistor is connected to the drain. The input circuit consist of the portion of the circuit between the gate and the source and the output is between the drain and the source. Hence this configuration is called common source. It has high input impedance, high voltage gain and high output impedance. The input and the output signals are 180 out of phase.

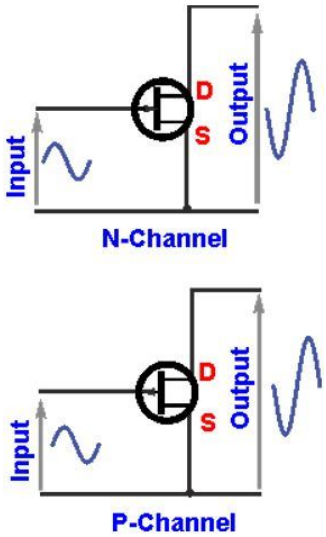


Figure 1.10: Common-source.

1.5.3 Common Drain configuration

In this case the drain is common to the input and the output circuit. The input signal is applied to the gate, the load is connected to the source and the drain is at the signal ground. This configuration is also known as the source follower as the source voltage follows the gate voltage. It has high input impedance and low output impedance. It is widely used as buffer. The voltage gain is unity but the current gain is high. The input and output signals are in phase.

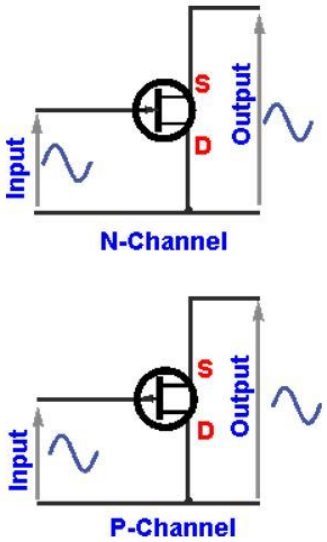


Figure 1.11: Common-drain.

1.6 Cascode Configuration

One of the most important circuit configuration for an amplifier is the Cascode configuration. It consists of two stages transconductance amplifier followed by a buffer amplifier [Ref]. This configuration offers several advantages over the single stage amplifier such as input-output isolation, high gain, improved bandwidth, high input and output impedance, better stability etc. The increase in the bandwidth can be explained by the reduction of Miller effect. This configuration improves the input-output isolation as the direct coupling from the output to the input is reduced. This significantly reduces the Miller capacitance between the output and input and thus improves the bandwidth. The Cascode configuration can be constructed using the BJT and the MOSFET. The first stage consists of common emitter or common source configuration followed by the common base or common gate stage [6] [3].

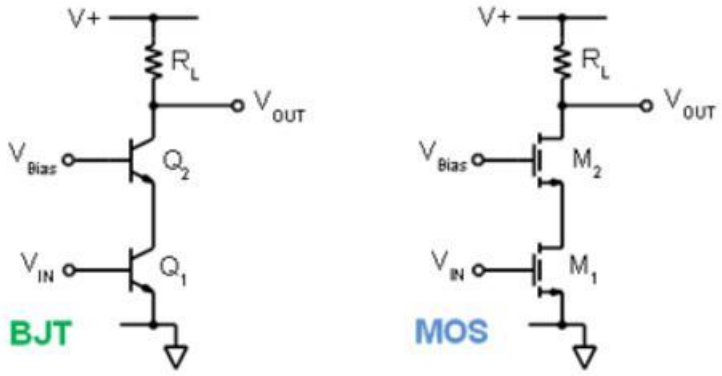


Figure 1.12: Cascode-circuit.

Chapter 2

Literature Review and Theory

In this chapter the background and the motivation for the design of the LNA is presented. The significance of the LNA design with respect to a receiver is found from the existing literature. It helped to understand the design requirements for the LNA. Based on the fundamental understanding of the Low noise amplifier design, the design parameters, different design topologies and the design flow are also briefly discussed in this chapter.

2.1 Need of LNA in RF receiver design

The developments of wireless communication services has increased the need for the communication systems which have low cost, low power and high performance [13]. Due to the increased data rates, the communication systems need to be designed for high frequency applications. The design of Ku Ka band receiver is found in the literature [7]. Many research works are reported on Ku Ka band receiver designs.
A typical receiver consists of a LNA, a down-conversion mixer, band pass filter and a power amplifier. The block diagram of a receiver is shown in fig . As seen from the block diagram of a typical receiver, the LNA is one of the important building blocks of the receiver for almost all the communication systems. The performance of a communication system can be determined by sensitivity of the receiver [12]. Therefore for designing such a highly sensitive receiver, it is important to design a LNA with good performance as it is the key component of the receiver.

2.2 LNA basics

Low Noise Amplifiers are the key components of the wireless communication receiver systems. The input signal to the receiver is usually very weak. Therefore the main objective of the LNA is to amplify these weak signals. But the challenge of these amplifier designs is to add as low additional noise as possible. The requirements a LNA are low noise, high gain, low noise figure and low power [13]. Hence the performance of the LNA can be measured by some important parameters such as gain, noise figure, return loss,

stability.
For the understanding of the LNA design, it is necessary to understand the concepts of these parameters. These parameters are described briefly in the following sections.

2.3 Scattering Parameters

Scattering Parameters or S-parameters are complex numbers that describe how the voltage waves propagate in the radio-frequency (RF) environment. It allows us to describe the properties of a complicated network as simple black boxes [4]. The S-matrix for a N-port contains NXN coefficients (S-parameters), each of these represents possible input output paths. S-parameters are complex numbers, with real and imaginary parts or magnitude and phase parts. S-parameters are usually described in matrix format. In the matrix format they characterize the complete RF behavior of a N-port network. For example, for a two port network, the characteristics of the network can be described by a set of four parameters : S11, S12, S21 and S22, as shown in Fig2.1. S-parameters are often used for microwave circuits.

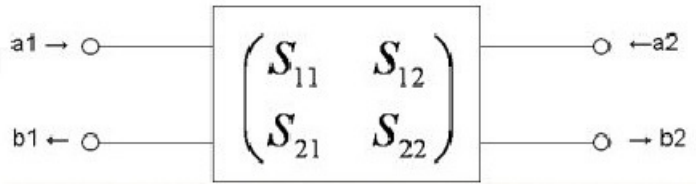


Figure 2.1: A 2-port network with incident waves a1 and a2, reflected waves b1 and b2.

S11 (input reflection co-efficient)

$$S11 = b_1/a_1, a_2 = 0$$

S12 (reverse gain co-efficient)

$$S12 = b_1/a_2, a_1 = 0$$

S21 (forward gain co-efficient)

$$S21 = b_2/a_1, a_2 = 0$$

S22 (output reflection co-efficient)

$$S22 = b_2/a_2, a_1 = 0$$

2.4 Gain

The gain of a circuit is described as its ability to amplify the amplitude or the power of the input signal. It is defined as the ratio of output to input signal and is often mentioned

in decibels.

$$Voltagegain = 10log(\frac{\frac{V_o^2}{R_o}}{\frac{V_i^2}{R_i}})$$

The power gain is defined as the ratio of the power delivered to the load to the power delivered by the source. The maximum power is obtained when the amplifier is terminated with complex conjugate impedance [8].

2.5 Noise Performance

The noise performance of the LNA can be described by the parameter called Noise Factor (F). It is defined as the ratio of the total output noise power to the output noise due to the input source. If the Noise Factor is expressed in decibels then it is called Noise Figure(NF) [8].

$$NF = 10log(F)$$

For RF applications another parameter can be used to describe the noise performance, it is called Signal-to-Noise Ratio (SNR). SNR is the ratio of the signal power to the noise power. Noise factor is the ratio of the SNR at the input to the SNR at the output of the LNA, as shown in equation

$$SNR = P_{signal}/P_{noise}$$

$$F = SNR_{in}/SNR_{out}$$

Linearity The linearity of the LNA is an important measure of its performance. If the input signal to the LNA is weak and there is a strong signal at a close frequency range then it will interfere with the intended weak input signal. In such a situation, there is a possibility of undesired inter-modulation distortion. Third-order intercept (IP3) is a

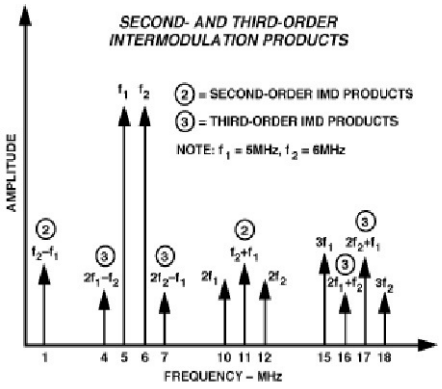


Figure 2.2: Example of third order inter-modulation product.

measure of linearity of the LNA. IP3 shows at what power level the third-order inter-modulation product is equal to the power of the fundamental signal. OIP3 shows the third-order output intercept point of a circuit. OIP3 is the intercept point at which the fundamental power and the power in the inter-modulation product intersect each other (where the output power is in dBm versus input power in dBm) [2]. The example is shown in Fig 2.3.

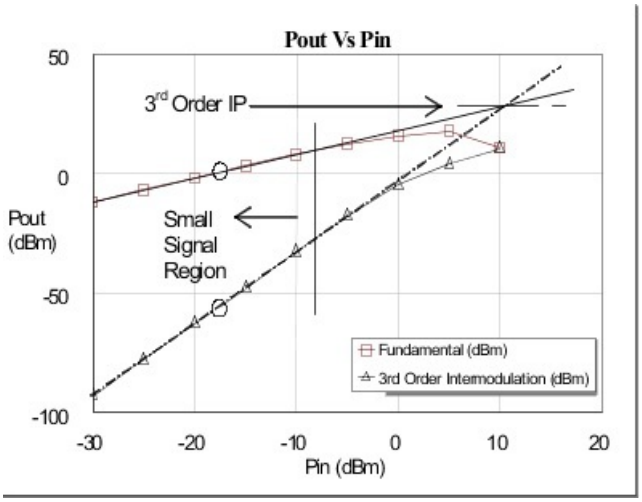


Figure 2.3: Example showing OIP3 plot (from AWR)

2.6 Stability

It is important to ensure that the LNA is stable and do not oscillate. The LNA can be either unconditionally stable or potentially unstable [8]. For a 2-port network, the condition for unconditional stability in terms of S-parameters can be described by K and B1. The necessary and sufficient conditions for unconditional stability are K1 and B1 > 0 [2].

$$K = \frac{1 - |S_{11}|^2 - |S_2 2|^2 + |\Delta|^2}{2S_{12}S_{21}}$$

Where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

2.7 Topology

One of the important steps to start the LNA design is to select the topology of the design. Various devices can be used for the LNA design such as - Heterojunction Bipolar

Transistor (HBT), Metal Epitaxial Semiconductor Field Effect Transistor (MESFET), High Electron Mobility Transistor (HEMT) [8]. Common emitter (CE) and Cascode topologies using HBT are reported in [10]. The Cascode topology has certain advantages over the CE configuration (also discussed in Chapter 1). Therefore for this project, the Cascode topology using HBT from IHP SG25H1 library is adopted for the design of the LNA.

Chapter 3

Preliminary work

In one of our course units, we were introduced to the design of a 5 GHz Wi-Fi receiver LNA. For these preliminary design work, IHP SG25H3 library was used. Mainly we explored two widely used topologies common source LNA (CS LNA) and the common gate LNA (CG LNA). In this chapter, the important results of these two topologies are reported and the possible improvements are discussed. These designs helped to understand the basics steps for the LNA design which finally helped to select the topology of the circuit for the project work.

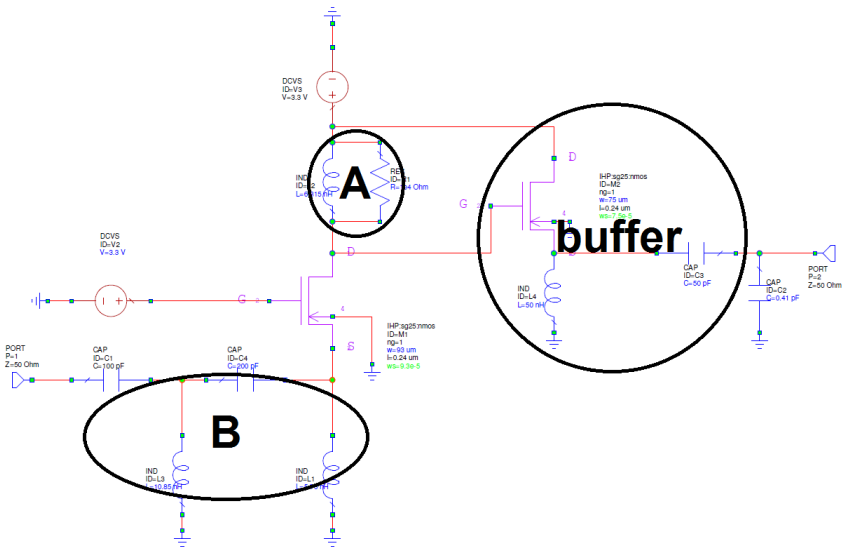


Figure 3.1: CG-LNA circuit.

3.1 Common-Gate Low Noise amplifier (CG LNA)

The CG LNA was designed for a 5 GHZ Wi-Fi receiver application. The circuit schematic is shown in Fig . The input signal is applied at the source of the transistor and the output is taken from the drain. The gate was maintained at fixed bias voltage and it is common to both the input and the output part of the circuit. An input matching circuit was required to achieve good S11. The buffer stage was added at the output of the drain for better matching at the output port. The load and the output capacitor values were tuned to get the gain at 5 GHz.

3.2 Common-Source Low Noise amplifier (CS LNA)

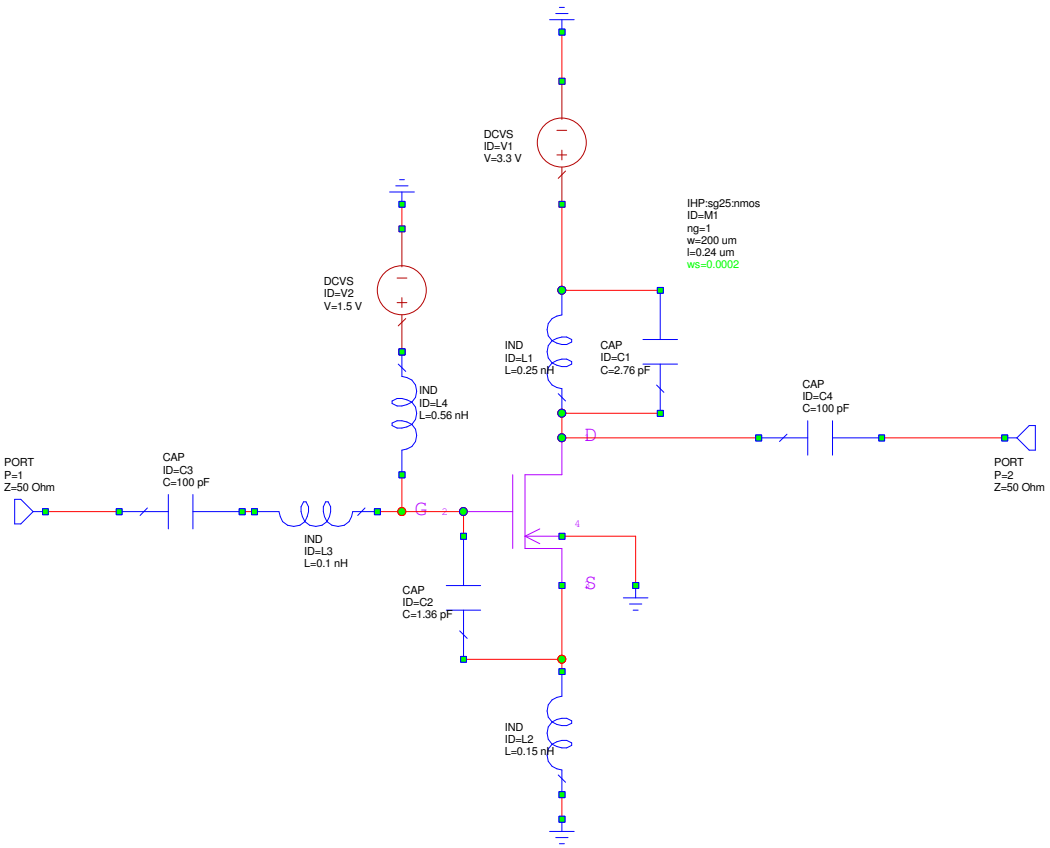


Figure 3.2: Common-Source LNA.

The CS LNA was also designed for a 5 GHZ Wi-Fi receiver application. The circuit schematic is shown in Fig 3.2. The input signal is connected to the gate of the transistor

and the source is connected to the ground by an inductor. The output is taken from the drain. The load inductor and the output capacitor values were tuned to get the gain at 5 GHz.
It was found that the CS LNA is difficult to match with the 50 Ohms port as the input impedance seen at the gate is quite high. But it was easy to obtain the gain above 15 dB. The noise figure was 0.69 which is significantly lower than the CG LNA.

3.3 Cascode

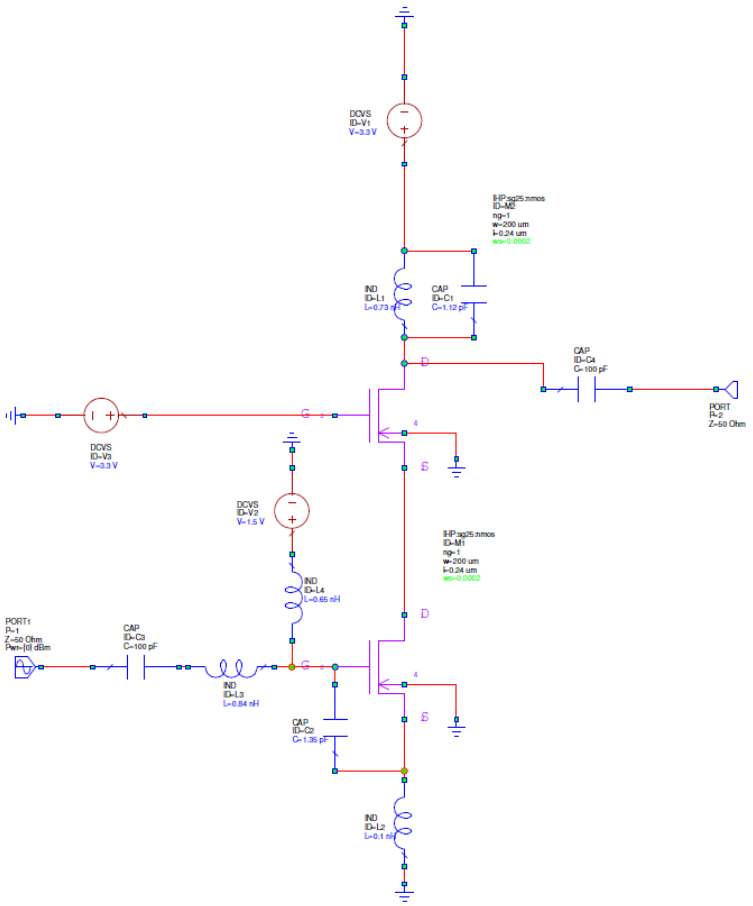


Figure 3.3: Cascode circuit.

From the literature review and the results of the CS LNA and CG LNA, a cascode LNA was explored for the same 5 GHz Wi-Fi receiver application. It consists of two transistors as shown in fig 3.3. This cascode topology consists of a common source transistor at the bottom and common gate transistor stacked on the top. The input signal is applied at the gate of the common source transistor and the output is taken from the drain of the common gate transistor. An input matching network was used at the input of the

common source transistor to improve the S11.

3.4 Summary of the Preliminary work

From the CG LNA design, it was found that the input could be matched easily, it has wide bandwidth but the noise figure was poor. For the CS LNA design, high gain could be achieved easily, the noise figure was very good but the band width was narrow and also it was difficult to match at the input. From the cascode topology high gain was obtained over comparatively wide bandwidth. The noise figure was better than CG LNA but not as good as CS LNA. From this learning, the cascode topology was selected for the LNA design of the project work.

Chapter 4

Project design

4.1 Design Flow

The design process for any microwave circuits can be divided into several steps that form the design flow. At first the specifications of the design are estimated based on the system requirements. Then the circuit topology is decided according to the information collected from the literature review. The ideal circuit elements are used in the initial design phase of the circuit. The required simulations are carried out using the circuit simulator. This provides a rough estimate of the designed circuit. Then the ideal circuit elements are gradually replaced by the circuit elements from the available process design kit step by step. The performance of the circuit would change compared to the simulation results of the circuit using ideal circuit elements. The circuit elements are tuned to get back the desired simulation results. The electromagnetic simulation of the passive structures are necessary for high frequency design. This even changes the overall performance of the circuit. The tuning of the circuit elements and the simulation of the overall circuit performance are carried out iteratively few times until good performance is achieved. This concludes the design phase of the circuit.
After the circuit design phase, the next phases of the design flow are Layout and verification. These are out of scope of this project work. The design of the LNA will be discussed in the subsequent sections.

4.2 Circuit Design

Although in the preliminary work MOSFETs were used as the active device, three different topologies CS LNA, CG-LNA and cascode were explored to estimate the performance of a single stage LNA. Based on the simulation results and literature review, cascode topology is adopted for the LNA design in this project work. As mentioned in [8], different devices can be used for the LNA design. In IHP SG25H1 library, high performance Hetero junction Bipolar Transistor (HBT) are available. Therefore these HBTs are used for the circuit design.

4.3 Design Specifications

From the literature review, the design specifications of the LNA were estimated. From the requirements of the receiver system, it is found that the LNA should have high gain, high bandwidth and low noise figure. The following specifications of the LNA were targeted for this project

Table 4.1: Specification

Parameters	Specifications
Gain	>=15 dB
Bandwidth	20 GHz (over Ku- Ka band range)
Noise Figure	<=5 dB
OIP3	>=0 dBm
S11	<-10 dB (over desired band)
S22	<-10 dB (over desired band)

4.4 Circuit Implementation

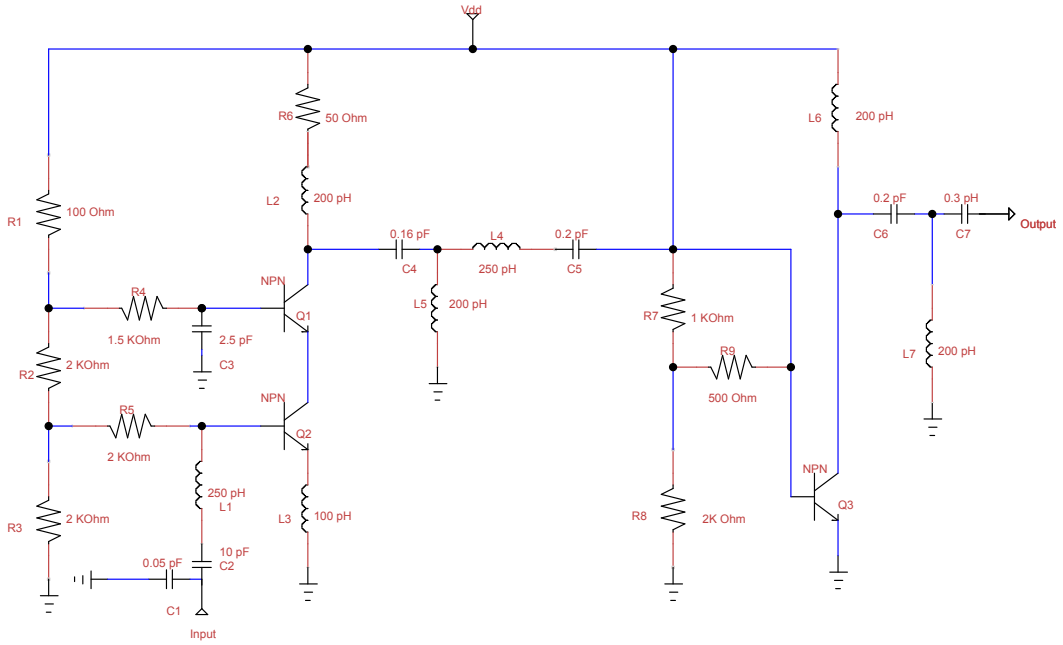


Figure 4.1: Circuit schematic of the designed LNA.

The circuit topology is shown in fig 4.1. As seen from the circuit schematic, the designed LNA consists of two stages. A 2V power supply is used. At first a single stage circuit using cascode topology is designed with the transistors Q1 and Q2. Q1 is the

common base stage and Q2 is the common emitter stage. Resistive divider (R1, R2, R3) is used to provide the required bias to the transistors Q1 and Q2. The base emitter voltages for the transistors Q1 and Q2 are 0.85 V. The inductor L2, at the load was tuned to get the bandwidth over the Ku-Ka band range. Simulation results of this cascode stage provided gain but it did not meet the required specification. Also the bandwidth of the LNA was not satisfactory and the noise figure did not meet the required specification. The input matching was also poor.

In order to improve the noise figure of the LNA, the inductor L3 was added. Then dif-

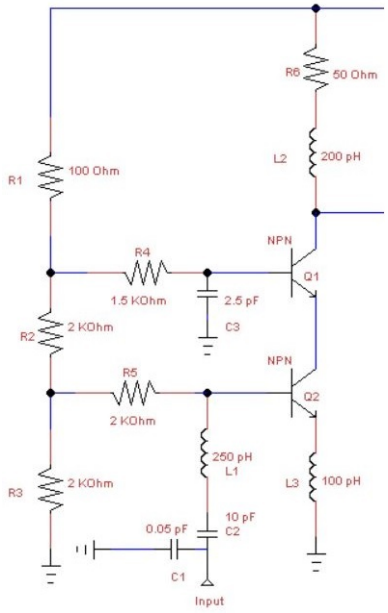


Figure 4.2: Stage 1 of the circuit.

ferent matching circuits were tested at the input of the LNA. Finally, a L-type matching network was connected to the base of the transistor Q2. The input matching network consists of L1, C1 and C2. This improved the S11 of the circuit. The circuit components were tuned and the transistor sizes were also changed but it did not improve the performance further. Only a peak was observed in S21 plot and the bandwidth was low.

Then a second stage using Q3 in common emitter configuration was added. This stage was biased with the resistor divider formed with R7 and R8. It helped to improve the OIP3.The inductor L6 acts as the load of this stage. The capacitor C6 and L6 were tuned together to set the bandwidth. After adding the second stage the gain was increased and also another peak was observed in S21 plot. A small resistance R6 is then added in series with L2. R6, L2 and L6, C6 values affected the bandwidth.

An inter-stage matching was necessary between the two stages to ensure wide bandwidth. A T-type network consisting of C4, L4, L5, C5 is used. Finally a matching circuit was needed to improve the S22 of the circuit. The T-type network formed with C6, C7, L7 helped to improve the S22 of the circuit.

After the initial design of the circuit, the simulation results could meet the desired spec-

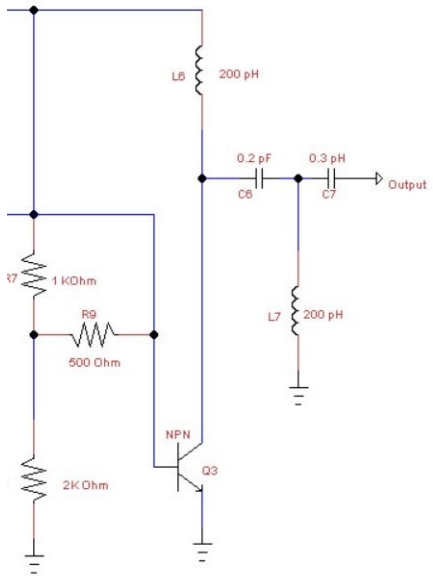


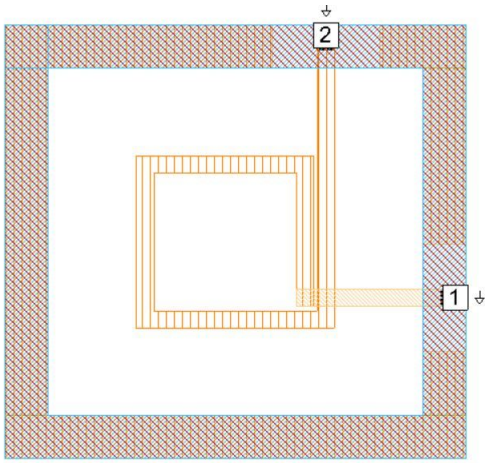
Figure 4.3: Stage 2 of the circuit.

ifications. But to be more realistic, the ideal circuit elements resistors, capacitors and inductors used from the AWR library were replaced. The resistors (rsil, rpnd) and capacitors (cmim) is used from the SG25H1 library. The simulation results almost remained unchanged. It was challenging to replace the ideal inductors. The inductors were drawn as the EM structures in Axiem. One by one, all of the ideal inductors were replaced by the designed inductors drawn as EM structures. This varied the simulation results significantly. As mentioned in the design flow section, the different circuit elements were adjusted to get back the desired simulation results. This iteration was carried out multiple times.

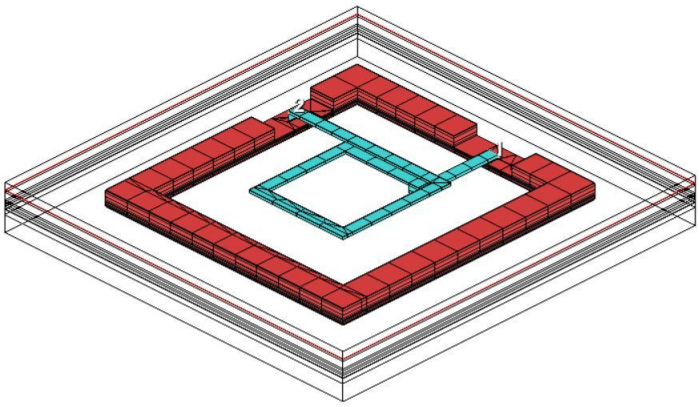
4.4.1 Inductor design

In the initial design phase, ideal inductors are used from the AWR library. There is no layout for the inductors in the SG25H1 library. Hence layouts for each of the inductors were drawn in Axiem. Electromagnetic simulations for the passive structures are necessary in order to determine how the layout of these structures affect the overall performance of the circuit [1]. These electromagnetic simulations capture the effects of the conducting lines and their mutual coupling over the swept frequency range. As these EM structures were used in the circuit, the simulation results changed. Layout of these structures required redrawing several times.
In the SG25H1 process, five metal layers are available. Top metal2, Top metal1, Metal 3, Metal 2 and Metal 1, with Top metal 2 being the top metal layer. The layout for these

inductors were drawn using Top metal 2 and Top metal 1. A via was used to connect the two metal layers at the region of intersections of the metal lines.
The width of these metal lines were 6 m. The spacing between the two metal lines were 2 m. A ground ring was used surrounding the inductor. It protects the inductor from the interference from other parts of the circuit. A gap of 40 m was maintained between the inductor and the ground ring. The inductance value was simulated over a frequency range of 1 GHz to 70 GHz. The 2-D view and 3-D view of one of the inductors are shown in Fig 4.2a and Fig 4.2b. The simulation result for the inductor is demonstrated in Fig



(a) 2D view



(b) 3D view

Figure 4.4: Structures of the inductor

4.5 . As seen from the graph, the inductance value is plotted over 1 to 70 GHz. The inductance value is 250 pH at 21.53 GHz.

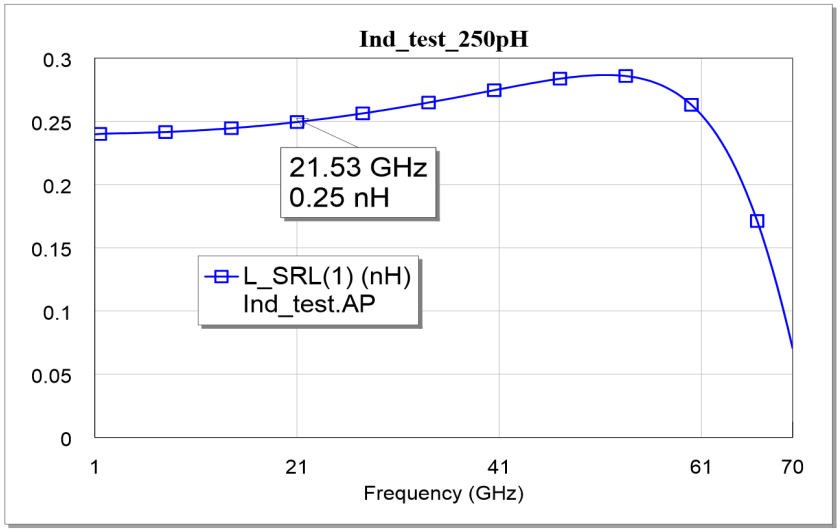
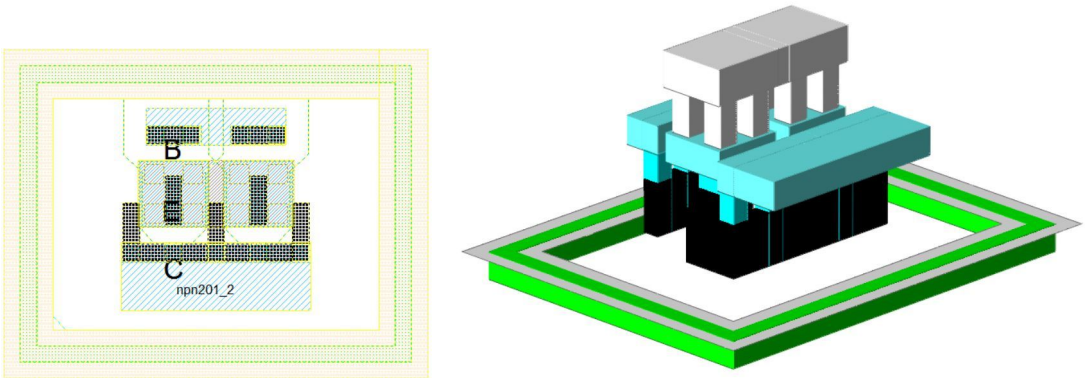


Figure 4.5: Simulation result for the inductor.

4.4.2 Transistor layout



(a) 2D view (b) 3D view

Figure 4.6: (a)2D view, (b)3D view of a single transistor layout

In the SG25H1 library, the HBT has two fixed fingers. It was required to increase the size of the transistor to get the desired gain and the bandwidth. Therefore multiple instances of the transistor was arranged in parallel. The structure of transistor the layout and the schematic are shown in Fig4.6 and Fig 4.7. respectively.

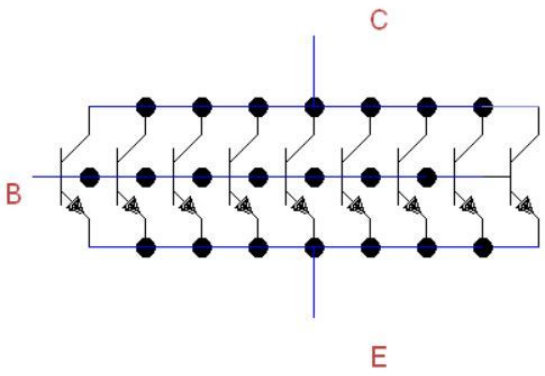


Figure 4.7: Transistor sub-circuit.

4.5 Simulation results of the LNA

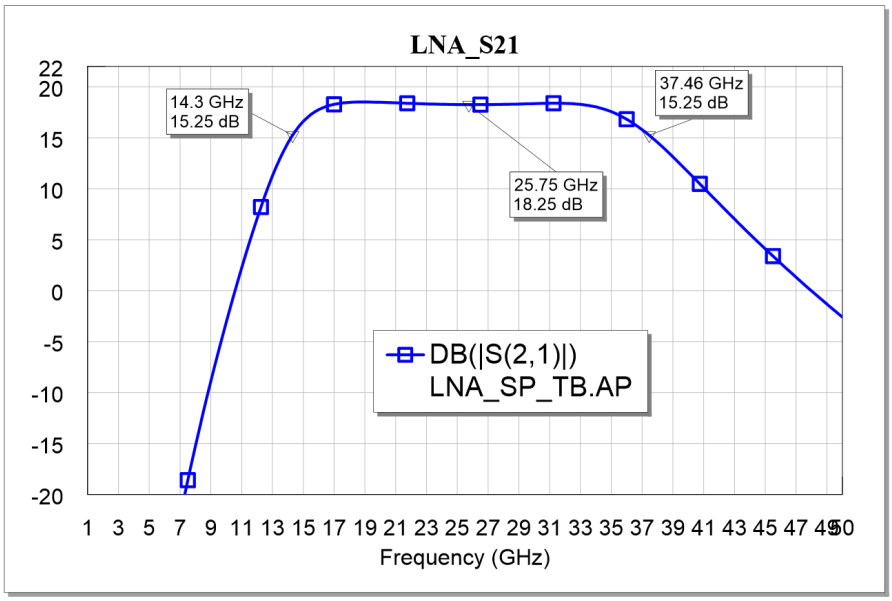


Figure 4.8: Small signal gain with 3dB bandwidth.

Fig 4.8 shows a plot of S21 of the LNA. A 3-dB bandwidth of 23.16 GHz is obtained from 14.3 GHz to 37.46 GHz. Approximately 18.25 dB gain is obtained at the mid frequency band.
The stability for the LNA can be explained from the plot shown in Fig 4.9. The two stability factors, K and B1 are plotted over 1 GHz to 50 GHz. As discussed in Chapter 2, the value of K should be greater than 1 and B1 greater than zero for unconditional stability. B1 refers to left hand axis and K to the right hand axis of the graph. Clearly

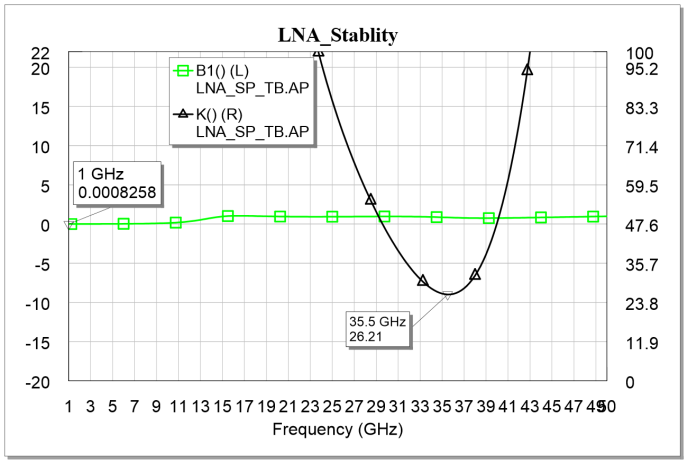


Figure 4.9: Stability of the amplifier.

B1 is greater than zero over 11 GHz and K is greater than unity for the entire frequency range of simulation.

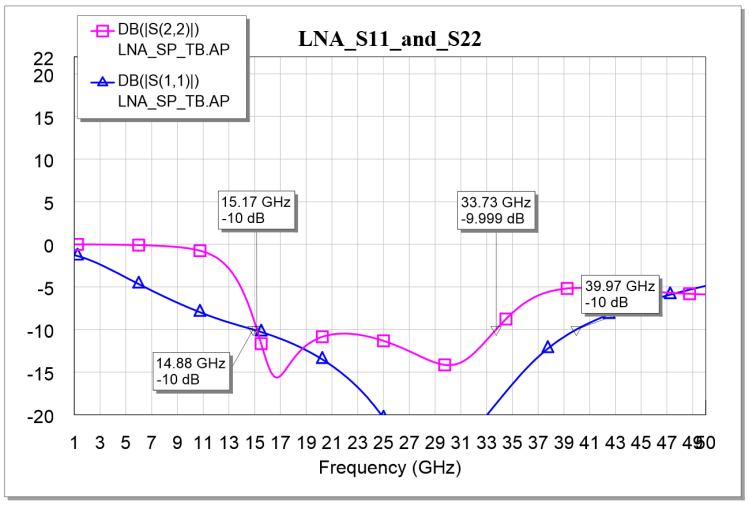


Figure 4.10: S11 and S22 for the amplifier.

S-parameters are shown in Fig 4.10. The S11 is below -10 dB between 14.88 GHz to 40 GHz, which shows a good input matching. The S22 is below -10 dB from 15.17 GHz to 33.73 GHz. The S22 could be improved at the high frequency end.

The noise figure is plotted in Fig 4.11 . As seen the from the two plots for the Noise figure (in brown) and Minimum Noise Figure (in black), they match fairly closely between 15 GHz and 33 GHz. The Noise figure is also below 5 dB over this frequency range. After 33 GHz, the noise figure increases over 5 dB. Therefore there is a scope of improvement of the Noise figure above this frequency range to fully meet the desired specification.

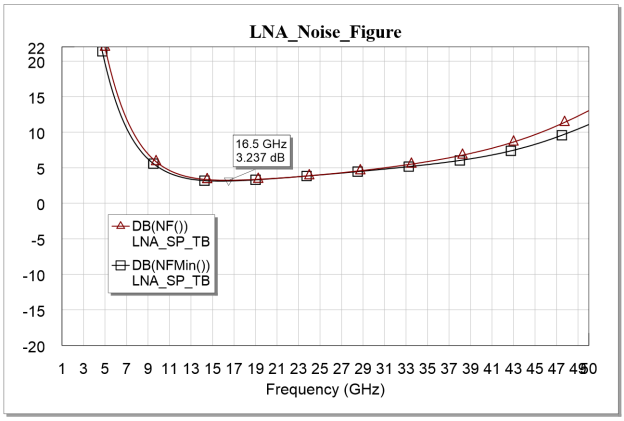


Figure 4.11: Noise figure.

Fig 4.12 is showing the OIP3 for the amplifier. As illustrated in fig 4.12, the output IP3 is given with a swept frequency range, from 14 to 34 GHz. The OIP3 is varied from 16 dBm to 21 dBm within the frequency range, which indicates that the input IP3 of the designed LNA better than 0dBm.

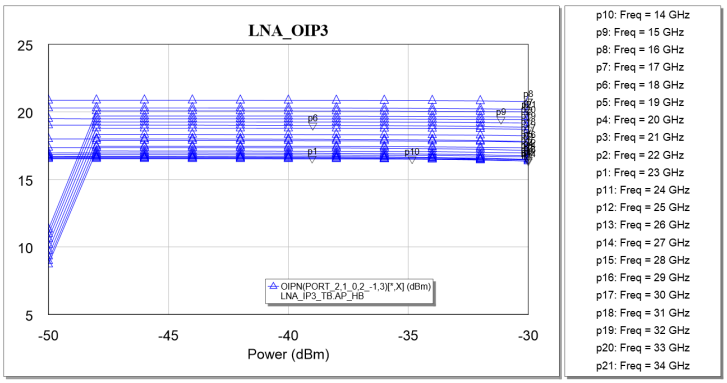


Figure 4.12: OIP3.

4.6 Summary of the result

Table 4.2: Summary of the result

Parameters	Specifications
Gain	**=15.5 dB, (From 14.3 GHz to 37.46 GHz, midband gain is 18.25 dB)**
Bandwidth	**23.16 GHz (From 14.3 GHz to 37.46 GHz, covering Ku- Ka band range)**
Noise Figure	**5 dB (over 9 GHz to 33 GHz, it can be improved above 33 GHz)**
OIP3	**>=15 dBm**
S11	**<-10 dB (over 14.88 GHz to 40 GHz which covers the desired band**
S22	**<-10 dB (over 15.17 GHz to 33.73 GHz, it can be improved at the high frequency end of the band)**

Chapter 5

Conclusions and Future Work

5.1 Conclusion

The primary purpose of this research project was to design a Low noise amplifier for a K-Ka band receiver. With the recent advancement in the device technology, a lot of research is carried on the millimeterwave wireless communication receivers. To ensure good performance of the receiver it is important to design an amplifier with high gain, large bandwidth and low noise. Therefore LNA has gained the importance as one of the main building blocks of the receiver. In this project a two stage LNA is presented which consists of the casode topology in the first stage followed by the common emitter topology.

5.1.1 LNA results

Different topologies for the LNA design are reported in the existing literature. Based on the results achieved from the single stage amplifiers that were designed in the preliminary work, the two stage topology for the LNA was adopted. The designed LNA has a broad 3-dB bandwidth of 22.82 GHz from 14.5 GHz to 37.2 GHz. The peak gain of the LNA is 18.5 dB. The noise figure is well below 5dB across the desired band. Typically the lowest value of the noise figure is 3.23 dB.

5.1.2 S-parameter

The S-parameter simulations, S11 and S22 suggest that the designed LNA is matched to the input and output ports over the designed frequency range. Few matching circuits were tried to obtain a good input and output match. Finally a L- network at the input and T- network at the output are used to give the required matching at the input and the output. The values of the circuit elements were tuned to give the best result.

5.1.3 Inter-stage matching

A T-type matching network was used between the two stages. The circuit element values were tuned in AWR to get an overall good performance of the circuit.

5.1.4 Inductor

At first the ideal inductor was used from the AWR library, in the initial design of the LNA. Although the simulation results were good using the ideal inductors, as they were replaced by the real inductors, the performance of the LNA changed. The ideal inductors do not represent the actual inductors that are used in reality. Therefore all the required inductors were drawn as EM structures. In AWR, the EM simulator is called Axiem. All the inductors were simulated using Axiem over a frequency range of 1 to 70 GHz. These inductors (EM structures) were then used as sub-circuits in the LNA design. As the performance of the LNA changed using these inductors, different circuit elements were tuned again to get back the desired performance.

5.1.5 Transistor

In the SG25H1 library, the HBT and CMOS are available. In the LNA design, HBTs were used for their good performance. Each of the HBTs have fixed two fingers In order to increase the gain and linearity, it was necessary to use a large sized transistors. Therefore multiple instances of the transistors were arranged in parallel to increase the overall size of the transistor.

5.1.6 Simulation result

All the necessary simulations were done using AWR. To estimate the performance of the designed LNA, different parameters were plotted. The simulation results for the S-parameters (S11 and S22), gain, noise figure, OIP3 and stability are shown.

5.2 Future Work

For any RF and microwave circuit design, at first the circuit is designed using the ideal circuit elements. The values of the circuit elements are tuned to get the required results. Then these circuit elements are replaced with the realistic circuit elements. For example, all the ideal inductors were replaced using the EM structures, in the design. There are two major steps of the design flow which were out od the scope for this project. These could be included under the future work and are listed below -

5.2.1 Optimization of the circuit elements

Although the simulation results meet the required specification, there is a scope for further improvement. The values for some circuit elements can be tuned for better performance of one or two parameters. The inductors were drawn in Axiem. These drawings could be changed to get the optimized value for the inductors. The frequency range for the simulation can be extended to higher frequency, the step size for the frequency range can be reduced for better accuracy. The EM simulation takes more time than the usual circuit simulation.

5.2.2 Layout

Layout is one of the most important step of the circuit design. If the simulation results are meet the design requirements, then the layout of the circuit can be done. Layout is a vast topic and it has many steps which was clearly out of the scope of this project. The layout of the LNA can be completed.

5.2.3 Post Layout simulation

After the layout is finished, the whole circuit is simulated again to evaluate the performance. Then this LNA can be connected with a mixer to see the overall performance.

Chapter 6

Abbreviations

LNA	Low Noise Amplifier
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CS	Common-Source
CE	Common-Emitter
CG	Common-Gate
CB	Common-Base
CE LNA	Common-Emitter Low Noise Amplifier
CS LNA	Common-Source Low Noise Amplifier
CG LNA	Common-Gate Low Noise Amplifier

Appendix A

SG25H1 Process metal Stack-up

A.1 General information

SG25 is the basic 0.25m CMOS process. It provides Nmos, Pmos, isolated Nmos and passive components such as poly resistors and MIM capacitors. In addition to the basic CMOS process 3 front-end options and 2 backend options are offered. The back-end option offers 3 thin metal layers, two thick metal layers (2 and 3m thick) and a MIM layer. Together with a high dielectric stack this enables increased RF passive component performance.
SG25H1 technology is a high performance BiCMOS technology. The bipolar module H1 is based on SiGe:C npn-HBT's with up to 190GHz transient frequencies and up to 220GHz oscillation frequencies.

A.2 Cross-section schematic for Metal Stack-up

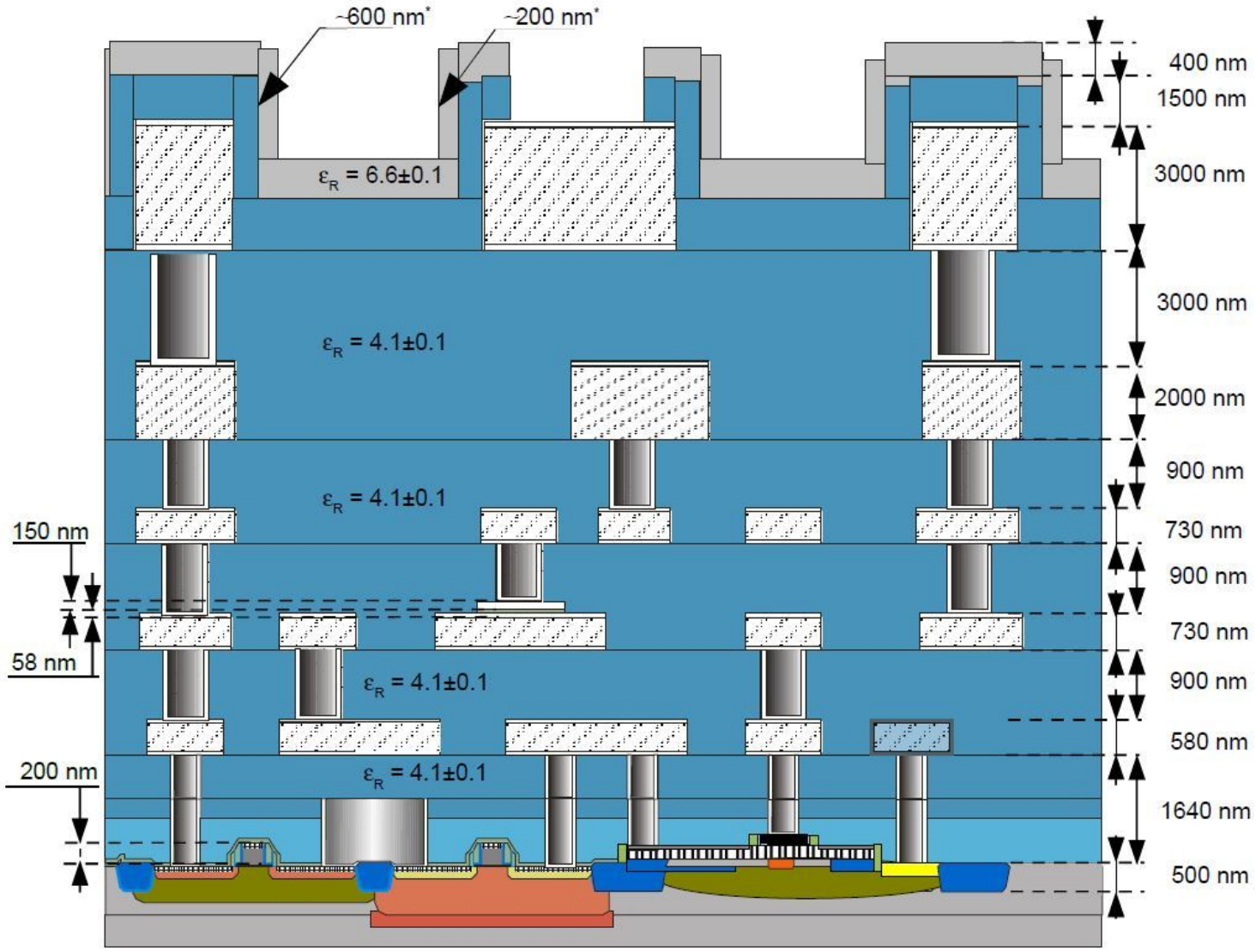


Figure A.1: SG25H1 process cross-section.

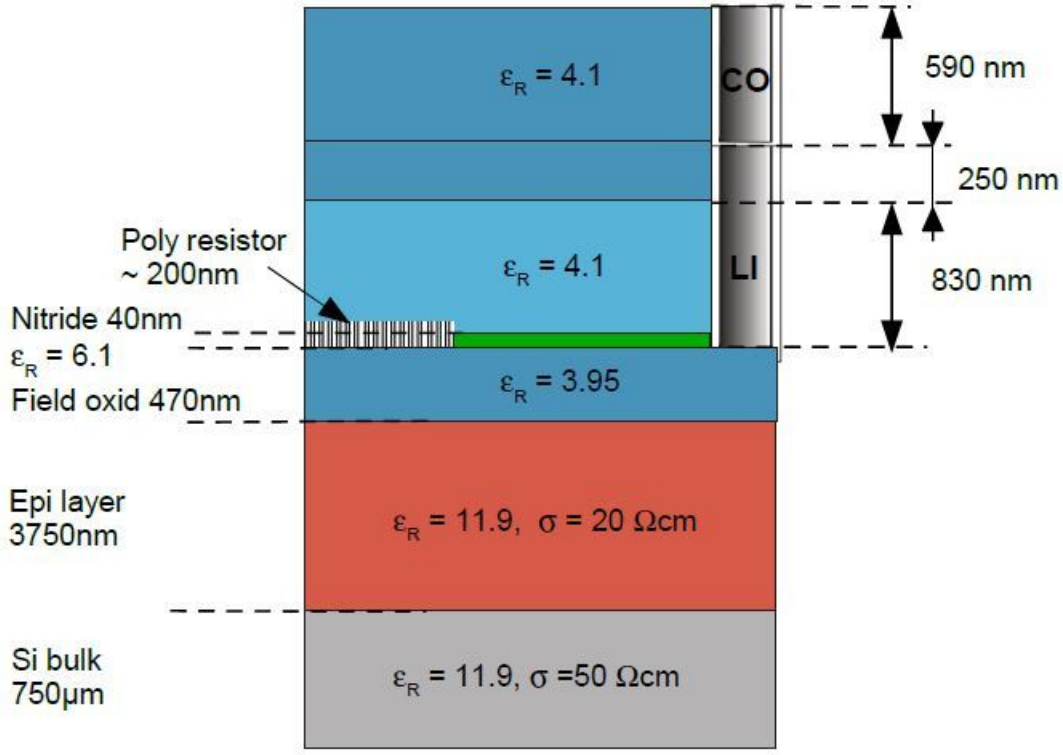


Figure A.2: BEOL detail cross-section below Metal1 for passive modeling.

Appendix B

Description of circuit elements used from SG25H1 library

B.1 Rsil

Table B.1: Rsil

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Sheet Resistance	RSNRSIL	Ω	6	6, 9	7.8	A.i	W= 2.8m; L= 230 mN= 10
Line Width Delta	DWNRSIL	nm	0	60	120	A.i	W= 2.8m; L= 230 mN= 10
Temperature Coefficients	TC1NRSIL TC2NRSIL	ppm/K ppm/K^2		2980 0.2		A.af	
Voltage Coefficient	VC1RSIL VC2RSIL	1/V 1/V^2		0.26 0.55			W= 0.48m; L= 4m
Matching Coefficient	MATRSIL1 MATRSIL1	nm		5.5 1.8			

B.2 Rpnd

Table B.2: Rpnd

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Sheet Resistance	RSNRSIL	ohm	90	6, 9	230	A.i	W= 2.8m; L= 230 mN= 10
Line Width Delta	DWNRSIL	nm	-70	-40	-10	A.i	W= 2.8m; L= 230 mN= 10
Temperature Coefficients	TC1NRSIL TC2NRSIL	ppm/K ppm/K^2	-536 0.98	2980 0.2		A.af	valid for width >1.5m
Voltage Coefficient	VC1RSIL VC2RSIL	1/V 1/V^2	0.0013 -0.013	0.26 0.55			W= 0.48m; L= 4m
Matching Coefficient	MATRSIL1 MATRSIL1	nm	32	5.5 1.8		A.ac	
Contact Resistor	RC2POLY1	Ω*m	48	55	62	A.ae	Salicided contact length is 0.7m

B.3 Cmin

Table B.3: MIM Capacitor

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Specific Area Capacitance	CMIMA	fF/m	0.9	1.0	1.1	A.k	A= 1271 x 140m^2
Specific Capacitance MIM Perimeter	CMIMP	aF/m		50		A.l	A= 2457x10x10m^2
Breakdown Voltage	BVMIM	V	20	>30		A.y	A= 1271 x 140m^2
Applicable Circuit Bias	V_{DDMIM}	V			10.0		10-years life extra polation@ 125C
Voltage Coefficients	VCMIM1 VCMIM2	ppm/V ppm/V^2		-11 1.5		A.ah	-10V <VMIM <+10V
Temperature Coefficient	TCMIM1 TCMIM2	ppm/K ppm/K		0 -0.03		A.ad	-40C <T <125C
Matching Coefficient	KCMIM	nm		7		A.aj	

B.4 Transistor specification

Table B.4: npn201

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Current Gain	NPN201_BETA		140	260	350	A.N	AE=0.18x0.84 m
Early Voltage	NPN201_VA	v	27			A.o	AE=0.18x0.84 m
Breakdown Voltage Emitter Collector	NPN201_BVCEO	V	1.85	1.9		A.p	AE=0.18x0.84 m
Breakdown Voltage Collector - Base	NPN201_BVCBO	V	3	4.5		A.q	AE=0.18x0.84 m
Max. Transit Frequency	NPN201_FT	GHz	150	180		A.s	AE=2x (0.18x0.84 m)
Max. Oszillation Frequency	NPN201_FMAX	GHz	190	220		A.s	
Collector Current	NPN201_IC07	A	TBD			A.ai	AE=0.18x0.84 m
Collector Current for max. Transit Frequ	VS_ICFT	mA		1.8		A.s	AE=0.18x0.84 m
max. Collector Current	VS_ICMAX	mA			1.8		AE=0.18x0.84 m

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