Circuit-Based Monitoring of High-Performance Semiconductor Manufacturing Processes

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Abstract

The conventional process control of semiconductor manufacturing is done by testing the electrical properties of the structures and devices which comprise the process control monitor, or PCM. Being useful at spotting process fluctuations over long periods of time, the PCM poorly predicts the nonlinear behaviour of the real circuits. This means that good PCM measurement results do not guarantee the expected performance of the functional circuits.

An augmented PCM is proposed which uses a simple circuit to relate process variation to nonlinear circuit performance. The suggested circuit control monitor, or CCM, is a nonlinear circuit whose signals can be related to the state of the manufacturing process. It is expected that the correlation between the CCMs' and functional nonlinear circuits' performance would be stronger.

A chaotic Chua's oscillator-based CCM is designed. It is implemented using the GaAs pHEMT manufacturing process which required developing a new version of the circuit's nonlinear element. The circuit equations suggested that the individual oscillator signals contain the features in the form of equilibrium levels which can indicate the state of the process. A computer algorithm is implemented as an analysis tool to retrieve the chaotic features of the measured circuit data. It is found that equilibrium levels fluctuate across the wafer and are closely correlated with both, the PCM parameters and the nonlinear parameters of the functional circuits. Overall, the results are regarded as satisfactory and the viability of the CCM approach is demonstrated.

Acknowledgements

I would like to acknowledge the great help I have received from my academic supervisors Michael Heimlich and Anthony Parker. I would like to thank people from Sydney's Macom design office, namely Simon Mahon, Anna Dadello, Tony Fattorini, Gerry McCulloch and others who assisted me with mastering circuit design and layout, and also measurements. Furthermore, without the contribution of WIN Semiconductors employees Wen-Kai Wang and Richard Kuo, this project would not have been implemented at all.

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Statement of Originality

The project was completed at Macquarie University between December 2011 and December 2014.

The original circuit-based monitoring concept was proposed jointly by Macom Tech. Solutions and WIN Semiconductors.

The Matlab code of Chua's circuit mathematical model included parts developed by V. Sidersky. The code for bifurcation diagram was developed by M. Audet. The remaining Matlab algorithms were developed by the author.

The operational-amplifier-based Chua's circuit schematic for board-level implementation was taken from V. Sidersky's website. The second board-level concept was suggested by the author.

The GaAs pHEMT Chua's circuit implementation was developed by the author employing the saturated-buffer FET logic patented by A.E. Parker and D.J. Skellern. The circuit layouts were developed with the assistance of Macom Sydney Design Centre's employees A. Dadello and A.P. Fattorini. Advice on the layout design was also received from Dr F. Zhu, at time Department of Electronics research fellow.

The integrated circuits were manufactured on WIN Semiconductor foundry, Taiwan. Assistance with interpreting the PCM data was given by R. Kuo.

On-wafer measurements of the designed circuits were prepared with the assistance of Dr O. Sevimli, at time Department of Electronics research fellow and G. McCulloch from Macom. Measurements were performed by the author.

The work of others is acknowledged and referenced, except in cases where the results

are widely known.

This work has not been submitted in whole or part towards another degree at Macquarie University or any other university.

Evgeny Kuxa _____

List of Publications

- E. Kuxa, A. E. Parker, S. J. Mahon, A. Dadello, W.-K. Wang, M. C. Heimlich, *Process control in GaAs manufacturing using Chuas circuit.* CS MANTECH Conference, May 2014
- E. Kuxa, A. E. Parker, S. J. Mahon, A. P. Fattorini, W.-K. Wang, R. Kuo, M. C. Heimlich, *Chua's Chaotic Oscillator as the GaAs Manufacturing Process State Indicator.* APMC 2014, November 2014

List of Acronyms

PCM: process control monitor

CCM: circuit control monitor

pHEMT: pseudomorphic high electron mobility transistor

FET: field effect transistor

LNA: low-noise amplifier

RF: radio frequency

MMIC: monolithic microwave integrated circuit

MESFET: metal-semiconductor FET

PECVD: plasma-enhanced chemical vapour deposition

CPW: coplanar waveguide

RFIC: radio frequency integrated circuit

EM: electromagnetic

HBT: heterojunction bipolar transistor

VSAT: very small aperture terminal

CATV: cable television

BJT: bipolar junction transistor

MBE: molecular beam epitaxy

MOCVD: metal-organic chemical vapour deposition

2-DEG: two-dimensional electron gas

SPC: statistical process control

UCL: upper control limit

LCL: lower control limit

MOSFET: metal-oxide-semiconductor FET

DC: direct current

NR: nonlinear resistor

CAD: computer aided design

SPICE: simulation program with integrated circuit emphasis

FFT: fast Fourier transform

NMOS: n-type MOSFET

PMOS: p-type MOSFET

PCB: printed circuit board

PDK: process design kit

TFR: thin-film resistor

MIM: metal-insulator-metal

LVS: layout versus schematic

DRC: design rules check

UGW: unit gate width

NOF: number of fingers

PC: personal computer

PDF: probability distribution function

P1dB: 1 dB compression point

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If you wish to make an apple pie from scratch, you must first invent the universe.

Carl Sagan

1 Introduction

1.1 Motivation

Manufacturing integrated circuits is a complicated process as it involves multiple operations and processes. There are many stages in the process when things can go wrong and therefore a thorough control is needed.

The manufacturing process includes such operations as material deposition, etching and polishing, patterning using lithography, chemical treatment, epitaxy, etc. After most of these operations a control measurement is performed, such as layer thickness or sheet resistance measurement. These measurements help to monitor the equipment state and should it be necessary, the wafer can be scrapped or restored without going through all the process stages. Nevertheless such frequent testing is normally used only in experimental runs or when using novel processes or equipment. In production runs,

however, such extensive control is not economically viable and normally major testing is performed at critical stages and at the end of the manufacturing cycle when process control monitors (PCM) are measured.

Process control monitors provide the possibility of measuring electrical characteristics of the devices and layers of the integrated circuit. Electrical measurements include, but are not limited to, measuring sheet resistance of layers, such parameters of FETs as transconductance, saturation drain current, leakage currents, threshold and breakdown voltages, etc. Often PCMs are placed in the scribe line in order to maximise the useful area of the wafer. Consequently, it is desired to have PCMs compact and small in size.

Testing of the PCM helps to identify process deviations and predict faulty circuits, as each of the measured parameters has certain control limits. Long-term observation of PCM data assists in tracking the equipment state and forecasting a process going out of control. However when we want to apply the PCM measured data to predict the functionality of the circuits on the wafer it often produces false results. Namely, good PCM measurements may not necessarily guarantee proper performance of the actual circuits, and the opposite event is possible as well.

Such a discrepancy may be caused by the devices in the PCM being biased in a different way than those inside the actual circuit, or possibly the density of the elements can also be a concern when different proximity effects come into play in the real circuit. Regardless of the actual cause, which we will leave for others to investigate, a more reliable monitor is needed in order to improve the yield by not scrapping good wafers and by timely scrapping of faulty reticles.

The problem has been raised by monolithic microwave integrated circuit (MMIC) designers when it was found that the simulation results do not accurately predict the performance of the physical circuit. Basically that means that the device models that designers use are not accurate over the whole range of operational conditions. It was understood that the performance of a MMIC can be predicted by scaling of the model parameters for a MESFET only in the cases when biases and operating conditions are similar [13].

In order to improve the predictability strength of the PCM, its successor, a circuit control monitor (CCM) is proposed. The main idea of a circuit control monitor is to restore the link between the manufacturing process state and circuit performance. A basic CCM is a simple, small circuit which can produce some measurable output. For high sensitivity to the manufacturing process, the circuit has to be nonlinear. Thus candidates for a CCM include low-noise amplifiers (LNAs), mixers and oscillators and possibly other highly nonlinear circuits. It is supposed that a CCM would be application specific, meaning that a radio-frequency integrated-circuit CCM would not be suitable for a digital to analogue converter testing, for example.

In our study on process monitoring improvement we propose a chaotic circuit for the role of a CCM. The main idea is to take advantage of such a chaotic-system property as severe sensitivity to initial conductions. Chua's chaotic oscillator was chosen for its simplicity and due to a extensive amount of information available about this chaotic system. It is hypothesised that inclusion of Chua's circuit in the PCM of a gallium arsenide pseudomorphic high-electron-mobility-transistor process can provide a predictive link between the PCM and nonlinear circuit performance data.

In order to test the hypothesis we firstly have to understand how GaAs processing influences circuit elements' electrical performance. It is important to recognise a relationship between device parameters and circuit performance. Mathematical modelling and computer aided design electrical simulation tools can greatly assist us with establishing this link. Before starting an integrated-circuit CCM design process, the circuit has to be prototyped on a board level for estimating the feasibility of the design.

Thereafter a functional GaAs pHEMT design of the CCM has to be developed. Application of pHEMT technology to Chua's circuit implies the redesign of the circuit without employing complementary devices, that can be manufactured in silicon process, but which are unavailable in most GaAs process. The manufactured devices have to be tested and measured. The obtained measurement results are to be analysed and processed in order to characterise individual oscillators. Then, finally, we can test our hypothesis by contrasting the obtained CCM characteristics and other devices' small-signal and large-signal parameters.

1.2 Synopsis

Chapter 2 of this thesis provides an overview of modern compound semiconductor manufacturing processes. A particular emphasis is given on pseudomorphic high electron mobility gallium arsenide integrated-circuit manufacturing. Principles of pHEMT operation are explained along with the manufacturing process sequence examples. This is followed by explanation of semiconductor manufacturing quality control approaches and particularly methods of monitoring the electrical performance of the active devices by the means of process control monitor. It is shown that the PCM parameters are not directly linked to the nonlinear performance of functional circuits and hence the motivation for the current project is addressed. Consequently a new control method is described. It is proposed that an example of chaotic systems, which are inherently very sensitive systems, could make a good candidate for the role of a CCM. An introduction to the chaos theory is accordingly presented followed by the explanation of the selected candidate's, Chua's chaotic oscillator's, operation.

Chapter 3 provides the results of performed analysis of Chua's circuit. The chaotic system's mathematical properties are studied in detail. The performed analysis made a foundation for the following work. It is identified that chaotic signals contain certain features that could be linked to the circuit components.

Chapter 4 includes the theoretical work needed for the preparation of Chua's circuit for the role of a CCM. The circuit's mathematical model constructed in Matlab is presented. The behaviour of the circuit in different configurations and with variable parameter values is investigated. That is followed by presentation of the initial design of the electrical circuit in AWR Design Environment assembled for circuit simulations. A comparison between the mathematical and circuit simulations is performed and all the similarities and discrepancies are pointed out. Two circuit implementations as board-level prototypes are presented along with their measurement results.

Chapter 5 describes the integrated-circuit CCM design. Two versions of Chua's circuit prepared for two similar GaAs pHEMT manufacturing processes are presented. The background information about the employed processes is given. The design of

the circuit schematic is followed by presenting the prepared circuit layouts. A new version of nonlinear resistor implementation is discussed. Results of the simulations demonstrating chaotic behaviour are presented.

Chapter 6 provides the results of initial measurements performed on the two produced circuits. The measurement setup and procedure are described along with the method of signal analysis. The results show the variation of the output signal characteristics among the circuits in different locations of the wafer. The fluctuation of suggested CCM circuit characteristics suggests sensitivity of the designed monitors to different manufacturing process parameters. The advantage of one design over the other is shown. The study of chaotic signal's characteristics variation across the wafer is discussed in the following paper:

> E. Kuxa, A. E. Parker, S. J. Mahon, A. Dadello, W.-K. Wang, M. C. Heimlich, *Process control in GaAs manufacturing using Chuas circuit.* CS MANTECH Conference, May 2014

Chapter 7 discusses the CCM's characteristics correlation with various PCM parameters. The CCM measurement results are plotted to graphically present the variation across the wafer. The same process is performed for the PCM parameters which are subsequently correlated with the CCM data. The results of the correlation procedure are presented in the following paper:

> E. Kuxa, A. E. Parker, S. J. Mahon, A. P. Fattorini, W.-K. Wang, R. Kuo, M. C. Heimlich, *Chua's Chaotic Oscillator as the GaAs Manufacturing Process State Indicator.* APMC 2014, November 2014

Chapter 8 addresses the established link between the CCM performance and performance of real nonlinear circuits. Two driver amplifier circuits are measured to obtain their nonlinear characteristics. The circuit measurement procedure is discussed and the results are presented. The variation of the drivers' measured characteristics is presented along with the variation of the CCM indicator. The measured data are correlated and confirm the existence of the link between the nonlinear performance of real circuits and performance of circuit monitors.

The *Chapter 9* finalises the work by listing the outcomes and suggesting topics for the future work on the subject.

Appendix A contains the listings of all developed Matlab scripts.

1.3 Scope of the Work

The main goal of the work is to develop a procedure for monitoring a GaAs pHEMT manufacturing process. Numerous ways of process monitoring with the help of circuits are discussed, however the focus of this project is on applying chaotic systems for the role of process monitoring. Particular class of these systems, namely chaotic oscillators, are chosen for the study; Chua's circuit, as a most simple representative of chaotic oscillators, was scrutinised. Other kinds of nonlinear circuits and their application to process monitoring lie beyond the scope of this work.

It is examined how chaotic signals can be interpreted and which of their features can be related to the manufacturing process state. It is expected to find a correlation between the features of chaotic signals and manufactured devices linear and nonlinear characteristics. The project is not aimed on obtaining significant statistical data on the performance of the proposed circuit monitor, while it is required to prove the concept of chaotic-circuit-based process monitoring.

Everyone is stupid except me.

Homer Simpson

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Overview

2.1 Gallium Arsenide Manufacturing

The evolution of the wireless technologies over the past couple of decades pushed forward the development of compound semiconductors. The industry of III-V semiconductors including GaAs HBT amplifiers and pHEMT switches has seen a significant growth [14]. A fundamental driver of the compound-semiconductor manufacturing are the developments in cellular networks of the 4th [15], [16] and 5th generations which require GaAs amplifiers and switches in the mobile handsets as well as in the base stations. Other areas of GaAs MMICs wireless applications include automotive radar [17], aerospace [18] and defence [19], VSAT [20] and also wired networks such as CATV and broadband [21].

The field effect transistors (FETs) implemented in gallium arsenide which used

Schottky barrier for the gate were first introduced in 1967 [22] and they provided good amplification and low-noise performance at frequencies higher than in conventional bipolar junction transistor (BJT) amplifiers. The advances in molecular beam epitaxy and metal-organic chemical vapour deposition processes allowed thin layers of various semiconductor to be laid down on the GaAs substrate. That development led to creation of high electron mobility transistor (HEMT) [23].

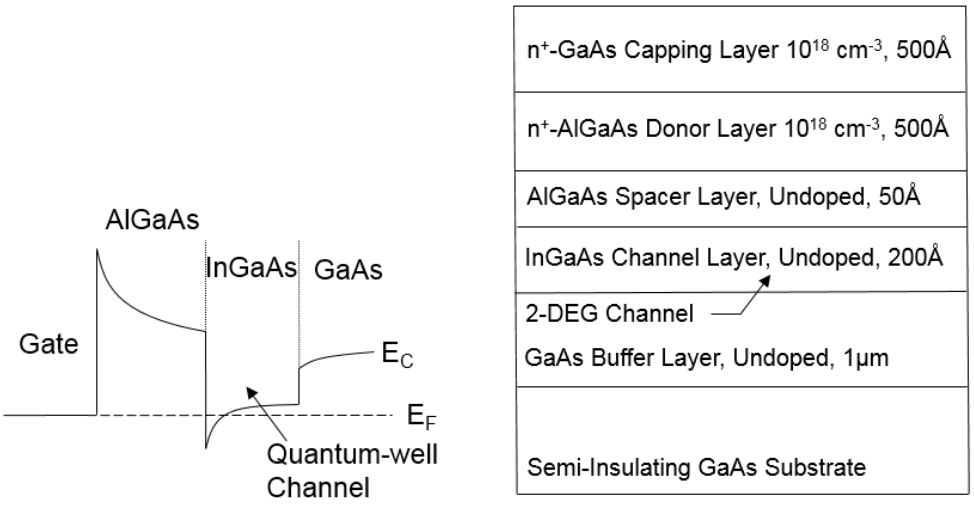
2.1.1 pHEMT Manufacturing Process

High electron mobility transistors are the group of devices which in their operation rely on heterojunctions often built using III-V semiconductors. The heterojunctions are formed between semiconductors of different compositions and band gaps, such as GaAs/AlGaAs. In a HEMT free electrons are physically separated from the ionised donors due to a specially designed epitaxial layer structure, thus the electron mobility is increased [24]. Conventionally, the epitaxial layers are grown employing molecular beam epitaxy (MBE) [25] or metal-organic chemical vapour deposition (MOCVD) [26] and may be doped or undoped depending on the requirements.

The HEMT active layer is composed of GaAs and AlGaAs layers. The most important heterojunction is that between the Si-doped AlGaAs and the undoped GaAs. The band gap of AlGaAs is higher than the band gap of the adjacent GaAs, which results in the diffusion of free electrons from AlGaAs into GaAs thus forming a two-dimensional electron gas (2-DEG) at the heterointerface. There are no ionised donors in the channel, therefore the 2-DEG does not suffer from Coulomb scattering and exhibits very high mobility.

HEMT performance can be improved if InGaAs is used as the 2-DEG channel instead of GaAs. Pseudomorphic high electron mobility transistor's layer structure and energy-band diagram are shown in Fig. 2.1. The InGaAs channel is called pseudomorphic because its lattice unnaturally compresses to mirror the structure of GaAs. The pseudomorphic device, or pHEMT, is based on the AlGaAs/InGaAs/GaAs structure, and the electrons flow in the strained quantum-well InGaAs channel. The benefits include enhanced electron transport, improved confinement of carriers in the quantum

well along with a higher current density and transconductance than that of a conventional HEMT [27]. For example, Mishra et al [28] compared two HEMT devices of their fabrication and pseudomorphic structure exhibited 11.6 % better transconductance performance comparing to a similar HEMT device. At the same time, the cut-off frequency was increased from 175 GHz up to more than 200 GHz in a pHEMT.



(a) Energy-band diagram (b) Device layer structure

Figure 2.1: GaAs pseudomorphic HEMT [1].

It is desirable to use a higher InAs mole fraction because then the energy band gap increases, enhancing the carrier transport properties. However in this case the lattice mismatch strain between InGaAs and GaAs rises and the quantum-well thickness is required to be very small, which is challenging to achieve. The solution to that can be the use of a thin strained supperlatice structure (Fig. 2.2) when thin GaAs layers are included in the InGaAs channel to smooth the surface of the InGaAs [1].

At a foundry it is very important to have a well-controlled and stable material growth process, or epitaxy. For example, layer growth rate in a MOCVD process will depend on temperature, flow rate of precursors, pressure, etc. In a MBE process, where an additional wafer preparation chamber is normally used, substrate surface preparation by chemical treatment is also important [29]. The properties of the grown

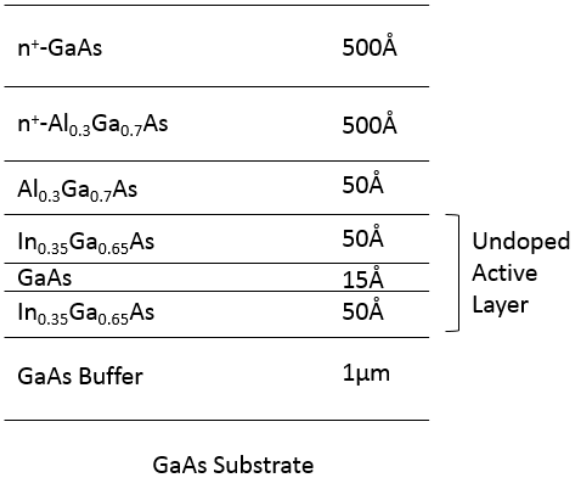


FIGURE 2.2: Thin strained superlattice pseudomorphic active layer structure [1].

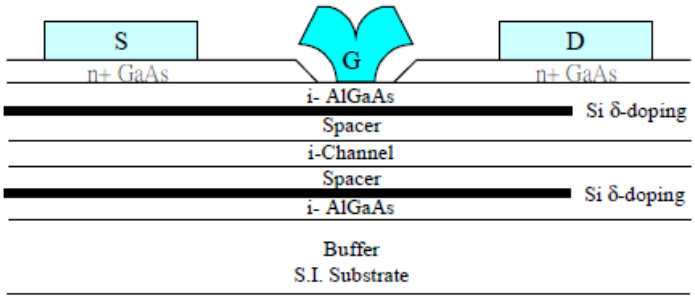


FIGURE 2.3: The 0.15 μm optical-gate pHEMT device [2].

layers affect the performance of manufactured devices. Fluctuations of doping and thickness of a capping layer will result in irregularity of transconductance, g_m and cut-off frequency, f_t. The same effects are observed for AlGaAs donor layer doping level fluctuation. Lithography process, which is critical in gate formation, needs precise control. Variation of gate width across the wafer will result in variation of device speed of operation [1].

WIN Semiconductors is a GaAs foundry which has developed numerous technologies employing HBTs, BiFETs and pHEMTs [30]. It is worth describing WIN's GaAs pHEMT manufacturing process, as this work leverages circuits manufactured by WIN Semiconductor's fabrication plant.

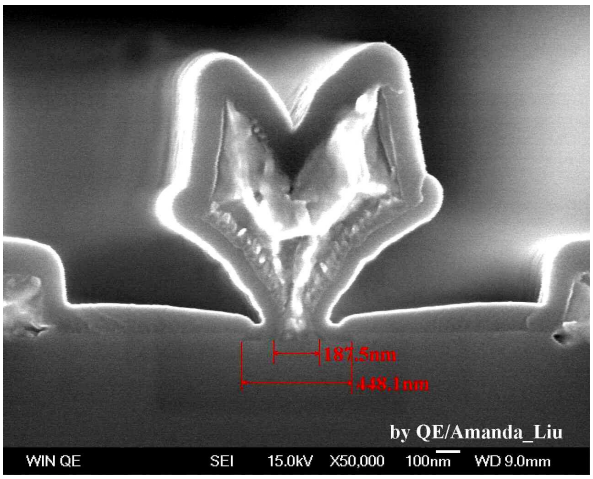


Figure 2.4: Scanning electron microscope cross-section of the 0.15 μm optical gate [2].

The present 0.15 μm pHEMT process utilises molecular beam epitaxy (MBE) material growth and an i-line (λ_i = 365 nm) stepper for formation of the gates. The epitaxial structure consists of a high In concentration undoped InGaAs channel layer and double δ-doped layers, that provide the carriers to the channel. There are AlGaAs spacer layers grown between the channel layer and Si layers, and on top of the upper spacer layer an AlGaAs Schottky layer is placed. The final layer structure is presented in Fig. 2.3. The gate is formed using so-called optical-gate flow. The gate photo-lithography is usually the most critical and yield-limiting process step. For the shown process, 99.2 % of the devices on the wafer showed normal performance, indicating that the gate photo-lithography is very well controlled. The cross-section of the optical gate is displayed in Fig. 2.4 [2].

Another high-performance developed process employed electron-beam, or e-beam, lithography [31] in the process of gate formation. The result is that the gate, with width of 100 nm at the bottom and 500 nm at the top is placed in the 2 μm drain-source region thus achieving ultra-low resistance of the channel [11].

Both the aforementioned processes, codenamed PL-15 and PP-10 correspondingly, were utilised within the course of this project. The key parameters of these processes are listed in Table 2.1. Both processes employ two-level metallisation, similar thin film

Manufacturing Process Parameter	PP-10 Value	PL-15 Value
Peak transconductance, G_{Mpeak}	725 mS/mm	550 mS/mm
Maximal drain current, I_{Dmax}	760 mA/mm	500 mA/mm
f_t	130 GHz	95 GHz
f_{max}	180 GHz	–
Pinch-off voltage, V_{to}	-0.95 V	-0.7 V
MIM Capacitance	400 pF/mm^2	400 pF/mm^2
TRF Resistance	50 Ω/□	50 Ω/□

TABLE 2.1: Key parameters of WIN's PP-10 and PL-15 manufacturing processes [11], [12].

resistor structures and silicon nitride PECVD for standard MIM capacitors.

According to [11], measurements of the PP-10 two-finger 75 μm gatewidth devices suggest that average value of g_m is 728.4 mS/mm with a 4.5 mS/mm standard deviation, average pinch-off voltage is -0.95 V with a 0.03 V standard deviation and f_t is 134 GHz with a 3.3 GHz standard deviation. Average breakdown voltage measured on a 25-finger 75 μm gatewidth pHEMT is 9.5 V with a 0.12 V standard deviation.

2.2 Semiconductor Manufacturing Process Control

For every industry it is important to have a reliable and repeatable manufacturing process. Semiconductor production, being utterly complicated, also greatly relies on process control as a means of achieving high-yield manufacturing. A specific feature of the semiconductor manufacturing process is that it has hundreds of sequential steps, with potential yield loss occurring at every step [32].

Yield is often divided into mechanical and parametric. Mechanical yield loss can happen due to a wafer breakage or other sort of damage. Parametric yield in its turn is based on the electrical tests.

Statistical Process Control (SPC) has been widely adopted since the beginning of the commercialisation of IC manufacturing [33]. The original aim of SPC was to

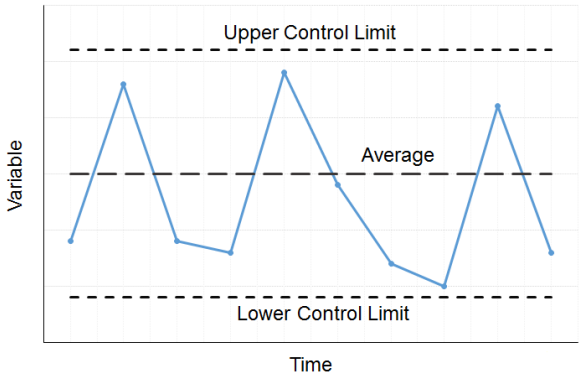


Figure 2.5: Typical control chart.

summarise the process and, should in the future the performance deviate from the norm, an alarm is raised and measures are taken to correct the root causes of the problem. The process is claimed to be in statistical control when it shows only routine run-by-run variations, which happen due to natural process fluctuation and systematic measurement errors. On the other hand, departures from those variations indicate that the process is out of statistical control. For every large deviation from the norm an assignable cause may be defined. As opposed to chronic or routine sources of variation, which are usually present due to inherent measurement errors or unavoidable inaccuracies of equipment sensors or control equipment, an assignable cause implies that something can be found and corrected or avoided such as equipment failure or operator mistake.

The fundamental tool of SPC is a control chart which can aid in detection and elimination of sources of unnecessary variations. This chart graphically displays how some sample quality characteristic changes with time. A typical control chart is presented in Fig. 2.5. Upper control limit (UCL) and lower control limit (LCL) are selected such that if a process is under statistical control mostly all of the points will fall between them. Should a point fall outside of the control limits it is going to indicate that a process is out of control. An average, or centre, line corresponds to an in-control state [32].

Control charts can help prevent a process from going out of control. For example,

when a trend, or run, is seen on the chart, suggesting that soon points will start falling outside of control limits, appropriate actions of eliminating a root cause should be taken, thus maintaining the process in-control. For example, it may happen that in a dielectric chemical vapour deposition chamber, a dielectric film is growing on an RF electrode due to degrading chamber cleaning process. This results in decreased deposition rate and deposited layers getting thinner from run to run. An experienced process engineer would be able to point that cause and take measures like increasing a cleaning step time or manual chamber cleaning.

Any process engineer wants to have some tools to control the process inside the chamber where the wafer processing is taking place in real time. Unfortunately, many critical wafer parameters, such as sheet resistance and layer thickness, can only be obtained after the contact measurements, procedures which can destroy the wafer surface. As opposed to contact measurements, real-time control is often performed by utilising the in-chamber parameters, such as temperature, pressure, RF power, etc. measured by various sensors. These parameters affect the critical wafer parameters (layer thickness, resistivity, etc.) indirectly. Moreover, the manufacturing processes suffer from a high level of system nonlinearity and often corrupted by slow drift due to maintenance operations, for example. Therefore models, which relate process variables to in-situ variables can be utterly complicated and computationally intensive [34].

The process control monitor (or module) normally contains such test structures as transistors (MOSFETs, HBTs, HEMTs, etc.), different functional layers, such as metal layers, resistive layers and, depending on the technology, capacitive structures too. This monitor is placed somewhere on the chip along with the production circuits, or can be placed in the scribe line region to save functional space. Test structures can include short circuit check units and open circuit check units. Normally these objects are represented by comb or meandering lines [35]. Certain PCM parameters, for example, metal sheet resistance or dielectric thickness can be measured straight after the corresponding process step by four-point probe testing [36] or spectroscopy [37]. At the same time, electrical properties of active devices can be tested only after all process steps are finished and before the wafers are prepared for slicing.

The measured *electrical* data is called parametric data and usually includes such semiconductor device parameters as threshold voltage, forward, reverse and leakage currents, resistivity of the layers, etc. The parametric data itself can not indicate a failure. Diagnosing steps are needed to be taken by a qualified engineer in order to find the root cause of the failure. Usually, there exists a many-to-many relationship between the PCM parameter and process factors, making it virtually impossible to define a faulty process step from the deviation of certain PCM parameter away from the mean value [38].

Electrical testing of circuits is done to ensure the correct operation of the final product and also to guarantee stable operation of the fabrication process. The PCM is tested by the fabrication plant on finished wafers, at both DC and RF, and based on the results wafer is accepted or rejected. Additional tests may be carried on finished dice or packaged parts, which is usually done at the customer site. The speed of testing is of vital importance, thus wafers are often tested employing a combination of probes and automated parametric testers [39].

Quality PCM tests are required for maintaining high yield or verifying improvements made to the process. DC wafer probe tests are fast and reliable, however wafer-level DC measurements do not necessarily guarantee acceptable RF module performance. RF measurements can be incorporated in the wafer-level tests for a faster feedback. The results can also be used for device modelling such that the extracted parameters can be used by circuit designers [40].

The RF part of PCM measurements firstly peruses the purpose of providing information on key manufacturing parameters to process and device engineers. Simultaneously, such device figures of merit as RF gain, transit time, f_t are reported and used in device models, such as hybrid-π. RF test measurements can be done in-line, i.e. similarly to PCM DC tests, however require calibration structures integrated on wafer (e.g. open circuit, short circuit, load and through line) [41].

Normally, circuit designers use empirical FET models which may not accurately represent the FET under all circumstances. Typically this model is developed from a device under specific bias conditions, while in production the circuit may not be using

the FET under nominal conditions and thus the empirical model does not match the 'true' FET model [42]. Therefore, yields can be lower than expected and it would be hard to define whether the reason for that are the tests themselves or poor-quality wafers, for example. Moreover, it is possible that the devices in the PCM operate differently from those in the circuit because of the element density. Densely packed FETs may suffer from various proximity effects from nearby devices, metal lines, or multiple gate fingers [43]. The PCM device normally stands alone and is not a subject to electromagnetic effects and thus, even though the in-circuit devices may still be operating under normal bias conditions, their performance nevertheless varies.

Usually a PCM test of pHEMT will include measuring drain current I_d as a function of source-to-drain voltage V_{ds}. Measuring a family of this characteristics for a range of gate-to-source voltages V_{gs} helps identifying the drain saturation current I_{dss} and extrinsic transconductance g_m. The threshold voltage V_{th} is defined by linear extrapolation of the square root of the drain current versus gate voltage to zero current. Pinch-off characteristic can be obtained from measuring gate current as a function of gate voltage. A network analyser can be engaged into measuring the pHEMT's scattering parameters, such as current gain, $\mid h_{21} \mid$. The cut-off frequency f_t can be found by extrapolating current gain versus frequency function to unity using a -6 dB/octave slope [44].

It was found by Baumberger in his work [45] that main performance parameters of a GaAs MESFET, such as g_m, f_t and V_{th} are strongly correlated with drain current I_d measured at fixed bias voltages V_{gs} and V_{gs}. That is taken as an indication that observed process variations are one-dimensional in nature and thus can be represented by a single parameter, X_S, which can be incorporated into the device SPICE model. This factor was included in empirical formulas for V_{to}, β, C_{gs0} and C_{gd0}. During the simulations X_S can be swept (0.9–1.1) representing the expected process extremes.

As opposed to small-signal parameters of linear models (e.g. hybrid-π), large-signal excitations, when device operation is nonlinear, depend on the device's size, especially when the highest harmonic frequency is comparable with this size. Circuit envelope is a simulation technique commonly used in microwave communication systems analysis for

transient and steady state simulations. Device parasitics and active parameters can be used for this model to simulate the nonlinear behaviour of the circuits. This method's results are close to the results of the lumped model simulation yet the difference is noticeable. It is stated that the distributed model, that is circuit envelope, is supposed to have a better correspondence with the measurements [46]. However the mismatch indicates that the models have limited applications and linear device parameters are hard to utilize in the models, predicting RFIC's nonlinear behaviour.

As a result, circuit designers use models that have limited validity – a model is not reality. When process fluctuations occur, PCM can indicate that, but the deviation may be considered insignificant; however it could result in a change of the FETs biasing regime to one where the device model is not suitable. Thus the circuit behaves in an unexpected manner and the yields appear to be low. That creates a niche in the process control actions that needs to be filled. There is a requirement for a monitor that can perform as a PCM but is at the same time suitable for the RF tests, and which additionally has a better correlation with the nonlinear performance of the circuits.

It would be naïve to assume that the problem of mismatch between small-signal device model predictions and real nonlinear performance is not being investigated. On the contrary, a lot of effort is put towards improving the wafer tests. Engineers try to make tests simpler, faster to perform and at the same time more reliable. Analytical fault models help to improve the test accuracy keeping the test variables at minimum [47]. One of the analogue circuit testing methods, referred to as signature testing, involves applying a short transient stimulus to the circuit under test and analysing the response in order to predict the circuit specifications [48]. The transient testing focuses on the circuit response to an arbitrary periodic or aperiodic waveform. The goal of the test process is to design a signature test stimulus that is constrained by the performance of the wafer in such a way that signature test response would contain information about the specifications of a bare die. That is followed by developing a model which includes the package parasitics and predicts the specifications of the circuit as seen from the package terminals.

The faults of analogue circuits can be subdivided into catastrophic faults, which are

caused by short or open circuits or due to dust particles, and parametric faults which happen due to the fluctuations in the manufacturing environment. Among the former faults are the faults caused by process gradients which can result in device mismatch. In their work [49], L. Milor and V. Visvanathan propose an algorithm of generating tests to be implemented before wafer probe measurements to filter out faulty reticles early in order to save time and resources. Therefore the first step of the algorithm is to determine a tolerance box of process parameters (e.g. layers thickness, doping levels), defined by process engineers. Secondly, map the tolerance box by the sensitivity matrix of the good circuit into the measurement space axis of which correspond to a measurement to be introduced before specification testing in wafer probe. The approach of simulation-before-test was taken. The idea is to compare the test result with one from the simulated database and define the fault by determining the closest simulated fault signature.

2.3 Circuit Control Monitor

The approach to process monitoring investigated here involves including simple nonlinear circuits in the process control monitor area and consequently referred to as circuit control monitor, CCM. Although the effective area on the wafer may thus be compromised, the benefits of better monitor sensitivity could outweigh this drawback.

It is expected that the correlation between the performance of transistors in a CCM with the devices in the actual circuit will be stronger. The output of a CCM is affected not only by the linear transistor characteristics but also by the influence of conductive lines. The superposition of these effects may not be linear therefore not properly simulated by the model circuits.

A proper CCM candidate has to be chosen for having a strong correlation between its performance and that of real circuits. The candidates for the CCM should produce some measurable signals from which the state of the process can be estimated. The possible list of candidates includes, but is not limited to, low-noise amplifiers, mixers and oscillators. LNAs can be subjects to gain measurements, measurements

of third-order intercept point, 1 dB compression, etc. Mixers can be characterised by their conversion loss or gain, noise figure or isolation. Oscillator measurements can include their output power, frequency and phase noise. At the same time, to make the CCM measurements effective, the procedures for circuit testing should be as simple as possible and preferably not use complicated measuring equipment which needs careful calibration. Otherwise, measurements of CCMs would require efforts similar to measuring real functional circuits.

We can now briefly review the existing circuits from the aforementioned classes. The comparison of viable CCM candidates is given in Table. 2.2. The sizes of the listed circuits vary from 0.336 mm^2 up to 3.6 mm^2. All of the presented examples utilise GaAs pHEMT process and thus can be applied for the CCM role with little or no modification. It can be seen from the table that different figures of merit can be measured depending on the circuit class.

Low-noise amplifier's S-parameters including the gain are normally measured employing a network analyser, while noise figure analysers can be employed for noise parameter measurements. Similar setups are used in power amplifier testing. Mixer measurements usually use spectrum analysers to monitor a mixer performance connected to an LO. Oscillators can be measured using signal source analysers or spectrum analysers can be employed as well.

Low-noise amplifiers can be designed in a very compact way as shown by the comparison. Measurements of LNAs are also relatively simple. However, amplifiers from this class are normally designed to provide operation that is highly linear, therefore being still affected by process variation, these circuits may not be sensitive enough for the purposes of monitoring. More or less the same statements apply to the power amplifiers. Mixers, on the other hand, take advantage of active device nonlinear characteristics and tend to operate in the knee region of drain-to-source current versus drain-to-source voltage characteristic. On the other hand, mixers usually contain planar coupled-line baluns or CPW structures, which define the mixer operation, but not sensitive to process variations. Therefore for the purpose of a CCM, the area will

Circuit	Size, mm^2	Specifications	Reference
Two-Stage **LNA** and SP2T Switch RFIC FEM for WLAN 802.11a Application	0.916 x 0.95	f = 5.4 GHz; G = 16 dB; NF = 2.1 dB	[50]
Ultra Low-Power Q-Band **LNA**	2 x 1	f = 27–45 GHz; G = 25 dB; $NF <$ 3.1 dB	[51]
Ultrawideband 3–10 GHz **LNA** MMIC	1.5 x 1.4	f = 3–10 GHz; G = 4 dB; $NF < 5$ dB	[52]
Compact **LNA**	0.73 x 0.46	f = 50–60 GHz; G = 15.5 dB; $NF <$ 3.3	[53]
23-37 GHz Miniature MMIC Sub-harmonic **Mixer**	0.85 x 0.85	f = 23–37 GHz; CL = 9.4–12 dB; LO = 13 dBm; $P1dB$ = 6 dBm	[54]
26–38 GHz Monolithic Doubly Balanced **Mixer**	1 x 2.1	f = 26–38 GHz; CL = 5.4–10.7 dB; LO = 12 dBm; $P1dB$ = 13 dBm	[55]
Novel 60-GHz Monolithic Star **Mixer**	1.5 x 1.5	f = 50–75 GHz; C = 13–18 dB; LO = 13 dBm; $P1dB$ = 3 dBm	[56]
5.25 GHz **PA** for 802.11a Application	1.5 x 1.0	f = 5.25 GHz; G = 25.6 dB; $P1dB$ = 24.8 dBm	[57]
Compact K-Band **PA** MMIC with Integrated ESD Protection	2.23 x 1.33	f = 17–24 GHz; G = 20 dB; $P1dB$ = 28 dBm	[58]
C-Band MMIC Low Phase Noise **VCO** for Space Applications	2.4 x 1.5	f = 7.3 GHz; P_{OUT} = 14 dBm; PN = -86 dBc/Hz	[59]
Fully Integrated 2.4-GHz High Efficiency Class-E **VCO**	2 x 2	f = 2.4 GHz; P_{OUT} = 27 dBm; PN= -118.33 dBc/Hz	[60]
Low Phase Noise Ka-Band **VCO**	1.3 x 0.8	f = 30.9 GHz; P_{OUT} = 14 dBm; PN = -116.36 dBc/Hz	[61]

LNA: Low-Noise Amplifier, PA: Power Amplifier, VCO: Voltage-Controlled Oscillator
G: Gain, NF: Noise Figure, CL: Conversion Loss, LO: Local Oscillator, PN: Phase Noise

TABLE 2.2: Comparison of possible CCM candidates

be used inefficiently. Furthermore, both amplifiers and mixers need external signal sources for testing. Therefore their figures of merit will be defined not only by the device parameters but also by the measuring equipment.

Functional amplifiers are designed to be stable. A power amplifier can be stable

during a small-signal operation, but as the input power increases, unexpected oscillations, frequency divisions or continuous spectrum of high power may be observed. It was shown in [62] that a class-E power amplifier operated linearly at low powers. However with the input power increase the spectrum became continuous suggesting chaotic behaviour. Further power increase resulted in observation of normal spectrum. When the power was decreased chaotic performance was observed with no hysteresis, but with the further power decrease amplifier exhibited mixer-like spectrum. Amplifier instability can be utilised in the CCM. We know that chaotic systems are highly nonlinear and sensitive, therefore it is possible to design a PA or an LNA making it deliberately unstable.

Voltage-controlled oscillators are naturally nonlinear circuits. Their advantage over the aforementioned candidates is that they do not rely on any inputs during measurements apart from a DC bias or control voltage – oscillators are autonomous circuits. The disadvantage these circuits is that they contain resonators which can occupy a lot of space on the reticle, but do not contribute to the circuit's sensitivity.

As was mentioned, chaotic systems are very sensitive to initial conditions and values of their components. Chaotically behaving power amplifier can be a good candidate for a CCM, however rather complicated amplifier testing procedure makes this type of circuit less attractive. At the same time, there exists a class of oscillators, which are capable of generating chaotic signals. Oscillators do not need external signal sources during testing and only an oscilloscope can be used to measure their output.

Chaotic signals can not be characterised in terms of a 3 dB bandwidth or phase noise. Chaotic oscillators generate oscillations with a wide and continuous spectrum. As any chaotic system, chaotic oscillators are highly nonlinear and very sensitive circuits and that makes them good candidates for the role of a CCM. Besides, we trust, that a chaotic oscillator can be designed to be very compact.

2.4 Chaos Theory

In our daily life when we say 'chaos' we mean something that does not follow any laws and completely lacks order. From the *mathematical* point of view, chaos is not completely random and can be described in formal terms. The main difference between a random behaviour and a chaotic system is that the latter follows some deterministic equations [63].

Many have heard the term 'butterfly effect'. It refers to the idea that a butterfly flapping its wings somewhere in Brazil and thus creating a small turbulence can cause a hurricane, say, in the Philippines. That idea was formulated by Edward Lorenz, the father of modern chaos theory.

Edward Lorenz, a meteorologist, had been developing a computer program simulating some weather patterns. The output of the program could be seen as a line graph. When Lorenz wanted to repeat some part of the simulations, he used a generated variable and rounded it. The printout indicated three decimal places in numbers instead of six, as computer had been storing them. He observed that the simulated results started to deviate quickly from previously obtained data. The tiny change transformed the whole pattern his program produced. Lorenz put his findings into a seminal paper which was titled "Deterministic Nonperiodic Flows" [64], published in 1963, where he elaborated on the sensitive dependence on initial conditions. Although, it was not instantly recognised, many researchers from the 1980s accepted that Lorenz's work challenged the classical understanding of nature [65].

Edward Lorenz is often called the father of modern chaos theory while emphasis on *modern* is given because he was not the first to describe a chaotic phenomena. French mathematician Henri Poincaré (1854-1912) discovered a chaotic deterministic system during his study of a three-body problem. He found that an evolution of a three-body system in space strongly depends on initial conditions, their positions and velocities. If we do not know the initial coordinates and velocities of the bodies to a very high precision we can not make accurate predictions about the final state. Thus Poincaré showed that determinism and predictability are two distinct problems [66].

Chaos theory works with nonlinear dynamical systems. A dynamical system is a system that changes over time, in other words, these systems evolve. In a linear system small perturbation in input results in small perturbation in the output. We can compare linear and nonlinear systems following the analysis performed in [67]. For example, let us take Newton's Second Law of Motion:

$$F_x(x,t) = ma = m\frac{d^2x}{dt^2} \tag{2.1}$$

We also know that for a point mass subject the force from an ideal spring is given by

$$F_x(x) = -kx \tag{2.2}$$

where k is the spring constant and x is the displacement. We can combine these two equations to find the evolution equation for the position of a particle:

$$\frac{d^2x}{dt^2} = -\frac{k}{m}x \tag{2.3}$$

This equation is linear relative to x hence the described system is linear. If we displace the mass from the equilibrium position, it will oscillate around the equilibrium sinusoidally with an angular frequency

$$\omega = \sqrt{k/m} \tag{2.4}$$

If we take the case where spring's force depends on the square of the displacement, for example $F = bx^2$, then the evolution will be described by the following equation:

$$\frac{d^2x}{dt^2} = \frac{b}{m}x^2 \tag{2.5}$$

Here, x position appears in the equation squared, therefore the system is nonlinear.

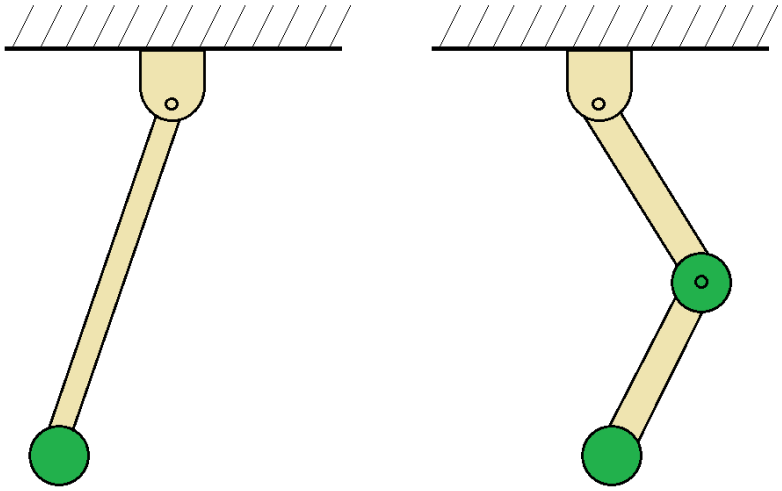
We refer to a system as linear if, and only if, the following condition is true: if $g(x,t)$ and $h(x,t)$ are linearly independent solutions of the time-evolution equation; then $cg(x,t) + dh(x,t)$ is also a solution, where c and d are any numbers. Also suppose $h(x,t)$ gives response of the system to a stimulus $S(t)$. If $S(t)$ is changed to $2S(t)$, a

linear system will give response $2h(x,t)$, while for a nonlinear system in general case response will be larger or smaller than $2h(x,t)$.

If a parameter of a linear system, such as spring constant k from Equation 2.2 is changed, then the frequency and amplitude of the oscillations will change but the qualitative behaviour stays the same. For a nonlinear system it is not the case and small change of a control parameter can result in sudden and significant change in the qualitative and quantitative behaviour of the system. For some value of the control parameter, the behaviour can become completely aperiodic (i.e. never exactly repeating itself); such behaviour is called chaos. The spectrum of chaotic oscillations may have spikes but always has a broad-band noise-like component [68].

In practice engineers may want to study chaos to understand the sources of random-like noise and develop tools for identifying chaotic vibrations in physical systems. Generally, chaotic vibrations occur when a strong nonlinearity is present. Physical examples may include nonlinear elastic or spring elements, nonlinear damping (friction), electric and magnetic forces, nonlinear resistive, inductive or capacitive circuit elements, diodes, transistors, etc.[69]. The list of chaotic phenomena in physical systems is still extending and the following systems can be included: certain chemical reactions [70], vibrations of elastic structures [71], systems with sliding friction [72], nonlinear acoustic systems [73], lasers and nonlinear optical systems [74], electronic circuits with nonlinear capacitance and inductance elements [75], etc.

Sometimes chaos is referred to as dynamical instability or a severe dependence on initial conditions. This high dependence on initial conditions results in the fact that the behaviour of two identical chaotic systems, initial conditions of which differ only slightly, will become different very quickly. A common example of such behaviour is a double pendulum (Fig. 2.6(b)), a pendulum swinging on the end of another pendulum. It is quite intuitive that if we incline this pendulum to a certain degree and let it swing, at the same time recording its motion, it would be incredibly hard to repeat this behaviour no matter how hard we try to incline the pendulum to the same degree. It is obvious that, with a normal pendulum (Fig. 2.6(a)) it is not the case and



(a) Single (normal) pendulum (b) Double pendulum

Figure 2.6: Two types of pendulums.

two identical pendulums started at the same time can go in synch with each other for rather a long time, unlike the situation with their more complex counterparts.

Systems studied by the chaos theory can evolve with time continuously or in a discrete fashion. Most commonly, continually evolving physical systems are described by ordinary differential equations (ODE); e.g. $dx/dx = ax + bx^2$ or partial differential equations (PDE); e.g. $(\partial u/\partial t) + u(\partial u/\partial x) + (\partial^3 u/\partial x^3) = 0$. Discrete evolution can be described by difference equations (DE), or Maps, e.g. $x(t+1) = ax(t) + bx^2(t)(t = 0, 1 \dots)$ [76].

An n-th order autonomous continuous-time dynamical system can be defined by the state equation

$$\dot{x} = f(x), \quad x(t_0) = x_0 \tag{2.6}$$

where $\dot{x} = dx/dt$, $x(t) \in \mathbb{R}^n$ is the state a time t, and $f : \mathbb{R}^n \to \mathbb{R}^n$ is called the vector field. The set of points traversed by $f(x)$ over all time is called trajectory [68].

For example, Lorenz's equations can be written down as

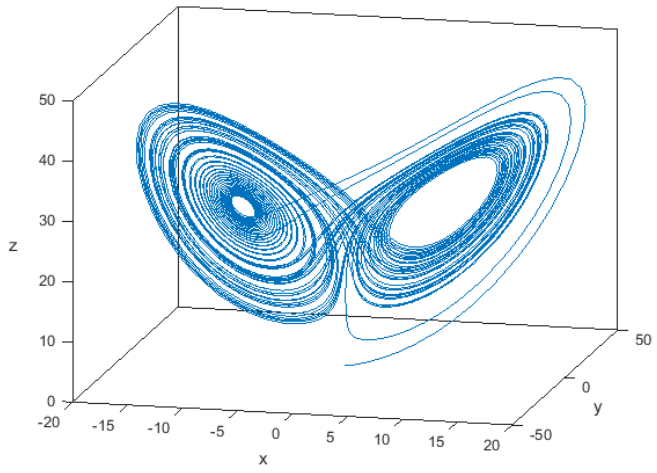


FIGURE 2.7: Matlab-generated Lorenz's two-lobed attractor.

$$\begin{aligned} \dot{x} &= \sigma(y - x) \\ \dot{y} &= rx - y - xz \\ \dot{z} &= xy - bz \end{aligned} \tag{2.7}$$

where σ, r and b are control parameters, and with the values of $\sigma = 10$, $b = 8/3$ and $r = 28$ the Lorenz's system exhibits a complex chaotic two-lobed trajectory (Fig. 2.7) [77].

In practice, when the model of the system's evolution is not known, it can be quite hard to distinguish chaotic behaviour. Chaos can be easily confused with randomness. Chaos theory possesses a large number of instruments for identifying and quantising chaos. The most useful techniques include studying time series, constructing phase portraits, generating power spectrum, calculating Lyapunov exponents and plotting bifurcation diagrams [78].

The easiest way to study a system is to record the evolutions of its state variables. The recorded data series can be presented graphically, when a variable is plotted versus time. In recording the time-series it is important to maintain an appropriate and fixed sampling rate. In most cases, the studied system will be evolving continuously, therefore

the recording rate of the system's state variables has to be sufficient to capture the dynamics of the system's evolution. Most analysis techniques rely on the measurements taken at equally spaced time intervals. If measurements at such a constant pace are not available, then data can be modified by finding the interval values using interpolation or by simply ignoring the irregularity and assuming the time intervals to be equal. From observation of the time series, nonchaotic behaviour (such as fixed point, periodic and quasi-periodic) can be distinguished from irregular or unpredictable behaviour.

Another useful and widely used method of graphically presenting the data series involves building phase portraits of the system. The space in which the phase portraits are constructed is called a phase space or a state space. A state space is an abstract mathematical space with its axis being the variables needed to specify the state of the system. In such a way, time is not presented explicitly on the phase plot and can be seen as a sequence of points [79].

In some cases, it is only possible to measure only one signal of the system. That signal can contain information about the other unobserved state variables and reconstruction of the state space can help to predict the present state. A scalar data series $s(t)$ can be used to construct a vector time series equivalent to the original dynamics. In order to capture the structure of the orbits in state space one can use lagged variables. If we possess a measured signal in the form of $s(n), n = 1, 2, 3, \ldots, N$, where $t_n = t_0 + (n-1)\Delta t$, we can create a vector in a D_e-dimensional space using a collection of time delays. The vector time series $u(t)$ takes the following form [80]:

$$u(t) = \{s(t), s(t+\tau), \ldots, s(t+(D_e-1)\tau)\}^T \tag{2.8}$$

This method is widely used for dynamic reconstruction, however the time delay τ and the embedding dimension D_e has to be chosen ad hoc for every system.

Arguably, the easiest way of distinguishing the chaotic time-series is finding of the power spectrum of the time series. Chaotic signals have broad and continuous spectra, therefore taking a Fast Fourier Transform of the data series is often suggested as the initial step of the system analysis.

Another test for chaotic behaviour involves the change of one (or several) control

parameters. The reason for this procedure is to find out whether the system can exhibit steady or periodic behaviour in some range of the parameter space. If it does, then we can confidently say that the system is deterministic and there are no hidden sources of random noise [69]. The transition between orderly and chaotic motion in a dynamic system can happen in several ways. Three routes to chaos worth mentioning: period-doubling, intermittency and quasiperiodicity. Period-doubling is said to occur when a new cycle emerges with period twice of the original cycle. Intermittency is the occurrence of a signal that randomly oscillated between regular phases and irregular bursts. In quasiperiodicity a second oscillation is added into the original cycle [81]. However it should be stated that all possible ways to chaos have not been discovered yet.

The most studied route to chaos is period-doubling, a systematic cascading progression to chaos. Period-doublings occur with some intervals between critical values of the control parameter at which new periods appear on the route to chaos. In other words, critical parameter values can be called bifurcation points and events of period-doublings, bifurcations (bifurcation means splitting in two parts). Sometimes bifurcation is referred to as a parameter value from which precisely two branches emerge [79]. Critical parameter (λ) values for each new periodicity come at an approximately constant rate. The interval between critical parameter values decreases exponentially and the ratio between two intervals, current and preceding is close to constant and known as the Feigenbaum number (δ):

$$\frac{\lambda_n - \lambda_{n-1}}{\lambda_{n+1} - \lambda_n} \to \delta = 4.6692016\ldots \tag{2.9}$$

Another type of transition, intermittency, involves bursts of chaos or noise in orderly periodic oscillations at irregular intervals when no period-doublings occur. A third route to chaos is called quasiperiodicity, a motion caused by two or more periodicities with independent frequencies and phases; as a result, motion never repeats itself, however it can resemble periodicity hence the name quasiperiodicity [79].

The bifurcation diagram is a technique used for studying the chaotic system's

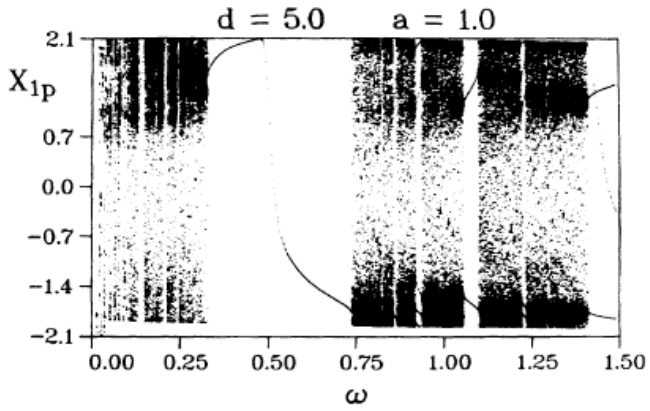


Figure 2.8: Bifurcation diagram showing coordinate X_{1p} of the attractor in the Poincaré cross section versus the excitation frequency ω [3].

prechaotic or postchaotic changes. A typical bifurcation diagram will show some measure of the motion (e.g. maximum amplitude) as a function of some control parameter. Thus, observing period-doubling bifurcations becomes an easy task [69].

For example, Fig. 2.8 displays the bifurcation diagram as plotted by Parlitz and Lauterborn in [3]. This diagram shows the strobed amplitude of the oscillations versus the excitation frequency ω in the driven Van der Pol oscillator [82]. A two-dimensional oriented surface, called a Poincaré cross section, is constructed in the phase space. Projections of the attractors in the Poincaré cross section onto the coordinate X_{1p} are made for each ω in the range from 0.0 to 1.5. One can see quasiperiodic and periodic oscillations occurring. All trajectories lie on an invariant torus within the three-dimensional phase space.

Dynamical systems can exhibit the following states of motion: equilibrium or fixed point, periodic motion or limit cycle, and quasiperiodic motion. These are classic attractors and they are associated with geometric objects: a point for equilibrium, a closed curve for a limit cycle and a surface in a three-dimensional phase space for quasiperiodic motion. The chaotic class of motion is associated with the strange, or chaotic, attractor, a new geometric object called a fractal set. It is a geometrical object in state space to which chaotic trajectories are attracted. In a three-dimensional phase space this object looks like a collection of an infinite set of sheets of parallel surfaces,

some of which are separated by infinitesimal distances [69].

The equilibrium solution of a dynamical system is the solution which does not change with time. A trajectory originating from the equilibrium point will remain indefinitely at that point. The stability of an equilibrium point, its nature, is defined by the characteristic values, or eigenvalues of the Jacobian matrix of partial derivatives, evaluated at the studied equilibrium point.

Consider a third-order continuous-time dynamical system with the state variables x_1, x_2 and x_3 which depend on time:

$$\begin{aligned} \dot{x}_1 &= f_1(x_1, x_2, x_3) \\ \dot{x}_2 &= f_2(x_1, x_2, x_3) \\ \dot{x}_3 &= f_3(x_1, x_2, x_3) \end{aligned} \tag{2.10}$$

where $\dot{x}_n$ indicates the time derivative.

The Jacobian matrix for this system can be written down in the following way:

$$\mathbf{J} = \begin{pmatrix} \dfrac{\partial f_1}{\partial x_1} & \dfrac{\partial f_1}{\partial x_2} & \dfrac{\partial f_1}{\partial x_3} \\ \dfrac{\partial f_2}{\partial x_1} & \dfrac{\partial f_2}{\partial x_2} & \dfrac{\partial f_2}{\partial x_3} \\ \dfrac{\partial f_3}{\partial x_1} & \dfrac{\partial f_3}{\partial x_2} & \dfrac{\partial f_3}{\partial x_3} \end{pmatrix} \tag{2.11}$$

In the general case, the characteristic equation of this Jacobian will have a cubic form, therefore will have three solutions, or eigenvalues. The real eigenvalues are usually represented by γ and the complex ones as $\sigma \pm j\omega$. If an equilibrium point has a pair of stable complex conjugate eigenvalues, which have negative σ ($\sigma < 0$) and non-zero ω ($\omega \neq 0$) and an unstable real eigenvalue γ ($|\sigma| < |\gamma|$) then there exists what is known as a transversal homoclinic orbit. The presence of this orbit implies that there exists infinitely many unstable periodic orbits of arbitrarily long period and also non-periodic solutions called chaotic trajectories [83].

There are two definitions of the stability of the equilibrium points. A fixed point is said to be *Lyapunov stable* if, given $\epsilon > 0$, there exists a $\delta = \delta(\epsilon) > 0$ such that, for any

solution $y(t)$, satisfying $|x_q(t_0) - y(t_0)| < \delta$, then $|x_q(t_0) - y(t_0)| < \epsilon$ for $t > t_0$, $t_0 \in \mathbb{R}$. A fixed point is called *asymptotically stable* if it is Lyapunov stable and if there exists a constant $b > 0$ such that if $|x_q(t_0) - y(t_0)| < b$ then $\lim_{t\to\infty} |x_1(t) - y(t)| = 0$.

Chaotic systems can be quantified by how strongly they depend on initial conditions. The qualitative measure of the system's sensitivity to the initial conditions can be given in terms of Lyapunov exponents, in such a way a chaotic attractor can be characterised. Lyapunov exponents quantify the rate of convergence or divergence of nearby trajectories. The signs of the exponents tell us whether the two trajectories would diverge from each other or converge. A positive exponent means that the two trajectories would diverge, and the more positive the exponent the faster they move apart. A zero value of the exponent implies a temporary continuous nature of the flow [84]. Calculating Lyapunov exponents from the equations of a system is a rather trivial task; the difficulty arises when we try to retrieve the exponents from the time series. The data series have to be prepared, noise should be filtered out and a proper embedding dimension has to be chosen. Lyapunov exponents describe the growth and shrinkage rates of small perturbations in different directions of the state space. An attractor can be defined as chaotic when at least one of the Lyapunov exponents is positive [85].

Now, we can investigate the Lyapunov exponents of a one-dimensional state space. The time-development equation of such a system is:

$$\dot{x}(t) = f(x) \tag{2.12}$$

Let $x(t)$ and $x_0(t)$ be two trajectories originating from nearby points. Then the distance between the two trajectories can be defined as $s(t) = x(t) - x_0(t)$ and that distance exponentially increases or decreases with time.

It is assumed that x is close to x_0 therefore a Taylor series expansion can be used:

$$f(x) = f(x_0) + \left.\frac{df(x)}{dx}\right|_{x_0} (x - x_0) + \dots \tag{2.13}$$

Now, keeping only the first-derivative term in the expansion of $f(x)$, the rate of change of distance can be written down:

$$\begin{aligned}\dot{s} &= \dot{x} - \dot{x_0} \\ &= f(x) - f(x_0) \\ &= \left.\frac{df}{dx}\right|_{x_0} (x - x_0)\end{aligned} \tag{2.14}$$

It is expected that the distance changes exponentially with time and therefore Lyapunov exponent λ that satisfies the following equation is introduced:

$$s(t) = s(t = 0)e^{\lambda t} \tag{2.15}$$

The time derivative of (2.15) is taken in order to find:

$$\dot{s} = \lambda s(t = 0)e^{\lambda t} \tag{2.16}$$

$$= \lambda s \tag{2.17}$$

Now, knowing Equations 2.14 and 2.15, the expression for λ can be found:

$$\lambda = \left.\frac{df(x)}{dx}\right|_{x_0} \tag{2.18}$$

Thus it is evident that, if λ is positive, then the two trajectories diverge and if it is negative they converge. However, in practice the time derivative of the time-evolution function changes significantly with x. Consequently, an average of λ over the history of trajectory has to be found. If the time evolution function is known, the derivative of the function along the trajectory can be evaluated to find the average value. In order to be defined as chaotic, a dynamical system has to have at least one positive Lyapunov exponent [67].

The most important numerical task in the simulation of dynamical systems is the calculation of trajectories. The time-evolution of the state variables is obtained by the integration of the differential equations using some integration algorithm. The goal of such algorithm is to approximate the behaviour of the system on a digital computer. An important point here is that computers are discrete-time in nature, therefore it is not

the actual system being simulated, but a complex discrete-time system. Integration algorithms are different in a way that they map the same differential equation into different discrete-time systems. In [68] there are presented several standard algorithms for approximating the solution to continuous-time system

$$\dot{x} = f(x,t) \quad x(t_0) = x_0 \tag{2.19}$$

The derivative of the state a time t_k can be approximated by

$$\dot{x}(t_k) \approx \frac{x_{k+1} - x_k}{h} \tag{2.20}$$

With this approximation (2.19) becomes

$$x_{k+1} = x_k + hf(x_k, t_k) \tag{2.21}$$

This formula is known as forward Euler algorithm and it is evident that with smaller step-size h integration becomes more accurate.

Backward Euler formula is written as

$$x_{k+1} = x_k + hf(x_{k+1}, t_{k+1}) \tag{2.22}$$

when we approximate the time derivative as

$$\dot{x}(t_k) \approx \frac{x_k - x_{k-1}}{h} \tag{2.23}$$

This is an implicit integration algorithm because x_{k+1} is a function of itself. Therefore, additional computation to solve for x_{k+1} is required. The term x_{k+1} on the right-hand side can be seen as a form of feedback, implicit algorithms have better stability properties and exhibit increased accuracy over explicit algorithms, such as forward Euler.

Trapezoidal algorithm is another implicit algorithm which can be seen as a merging of forward and backward Euler algorithms:

$$x_{k+1} = x_k + \frac{h}{2}\{f(x_k, t_k) + f(x_{k+1}, t_{k+1})\} \tag{2.24}$$

The family of Runge-Kutta algorithms originate from the idea that the solution can be approximated by its Taylor series expansion. The order of this algorithm tells which number of terms of the Taylor expansion are used in the approximation. The terms for most common fourth-order Runge-Kutta explicit algorithm are

$$\begin{aligned} k_1 &= f(x_k, t_k) \\ k_2 &= f(x_k + \frac{h}{2}k_1, t_k + \frac{h}{2}) \\ k_3 &= f(x_k + \frac{h}{2}k_2, t_k + \frac{h}{2}) \\ k_4 &= f(x_k + hk_3, t_k + h) \\ x_{k+1} &= x_k + \frac{h}{6}(k_1 + 2k_2 + 2k_3 + k_4) \end{aligned} \tag{2.25}$$

All of the values $k_1 - k_4$ are averaged together to give the approximation to the vector field which is used to predict x_{k+1}.

Inevitably, there are certain errors associated with all numerical algorithms. Local errors are introduced by a single step of integration algorithm, while global error is the total error caused by iterative application of the integration formula. Each type consists of round-off errors, which result from performing arithmetics on a digital computer and depend on the hardware used, and truncation errors that occur assuming there is no round-off error. The global round-off error is the product of number of steps and the local round-off error. The global truncation error is the accumulation of the local truncation errors, which depend on the step-size.

2.5 Chua's Circuit

Professor Leon Chua first came up with this circuit during his visit of Professor Matsumoto's laboratory in Waseda University in 1983. The goal of the ongoing research was to show that chaos can exist in electronic systems. It was required to build an electronic circuit which was capable of behaving chaotically. The specifications for the physically realisable circuit were the following: an autonomous circuit having exactly two or three unstable equilibrium points. It should contain as few as possible 2-terminal

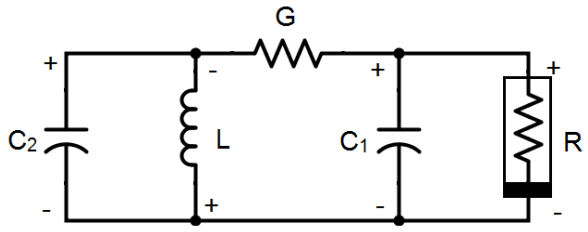


Figure 2.9: Chua's circuit schematic diagram.

linear passive resistors, inductors, and capacitors, and exactly one 2-terminal nonlinear resistor with a piecewise-linear voltage controlled current-voltage characteristic which is eventually passive.

From the eight candidates that met the requirements, one was chosen and then simulated in a computer program. The mathematical simulations resulted in an appearance of a chaotic attractor. Numerous simulations were performed in order to investigate the operation of the circuit and to ensure that the chaotic behaviour was not an artefact of a somewhat simple computer program [86].

Takashi Matsumoto presented the results of his computer simulations in a paper [4]. The dynamics of the circuit (Fig. 2.9) are described by the following equations:

$$\begin{aligned} C_1\frac{dv_{C_1}}{dt} &= G(v_{C_2} - v_{C_1}) - g(v_{C_1}) \\ C_2\frac{dv_{C_2}}{dt} &= G(v_{C_1} - v_{C_2}) + i_L \\ L\frac{di_L}{dt} &= -v_{C_2} \end{aligned} \tag{2.26}$$

In Equations 2.26 v_{C_1} and v_{C_2} denote the voltages across capacitors C_1 and C_2 and i_L is the current through the inductor L. The current-voltage relation for the nonlinear resistor, $g(v_{C_1})$, is shown in Fig. 2.10. The attractor observed by Matsumoto is presented in Fig. 2.11. The fourth-order Runge-Kutta method was used to solve Equations 2.26 with the following set of the parameters:

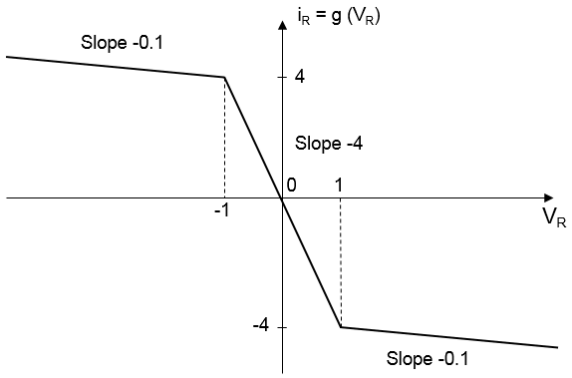


FIGURE 2.10: Nonlinear resistor's current-voltage function [4].

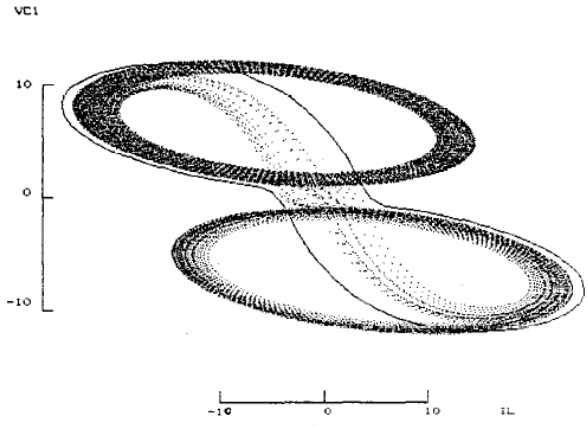


FIGURE 2.11: (i_L, v_{C_1})-plane of the chaotic attractor [4].

$$1/C_1 = 10,\ 1/C_2 = 0.5,\ 1/L = 7,\ G = 0.7 \tag{2.27}$$

The chaotic nature of the proposed circuit required experimental confirmation. Members of Leon Chua's Nonlinear Electronics Laboratory in Berkeley, Guo Qin Zhong and Farhad Ayrom fabricated the circuit and were able to observe the chaotic behaviour [5]. The circuit realisation is presented in Fig. 2.12 and the schematic of the operational-amplifier nonlinear resistor is shown in Fig. 2.13. As a result, a chaotic attractor was observed in the measured circuit signals (Fig. 2.14). That work proved that Chua's circuit is a genuine example of the electronic chaotic circuit.

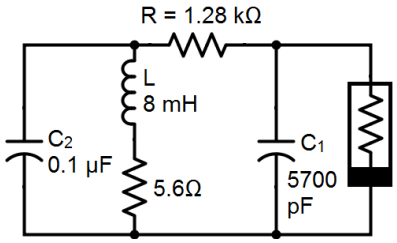


Figure 2.12: The circuit designed by Zhong and Ayrom [5].

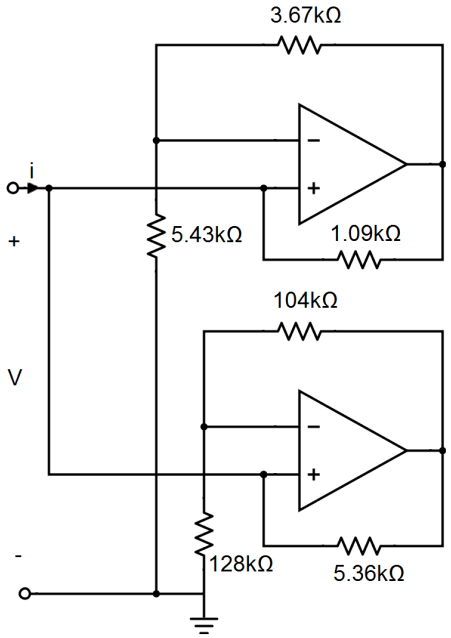


Figure 2.13: Operational-amplifier nonlinear resistor realisation [5].

The implementation of the nonlinear resistor, or Chua's diode as it is also named, has been reconsidered multiple times and several approaches have been taken. The implementations include tunnel diode, operational transconductance amplifiers and CMOS inverter circuit [87].

A realisation of Chua's circuit employing CMOS transconductance amplifiers is discussed in [6]. This approach combined quasi-linear voltage controlled current sources (VCCS), piecewise-linear voltage controlled current sources and capacitors. A VCCS-based gyrator configuration was chosen for inductor and resistor implementation. The circuit concept is shown in 2.15. Figure 2.16 shows the schematics of transconductance amplifiers and the nonlinear resistor used for building this CMOS Chua's circuit. The

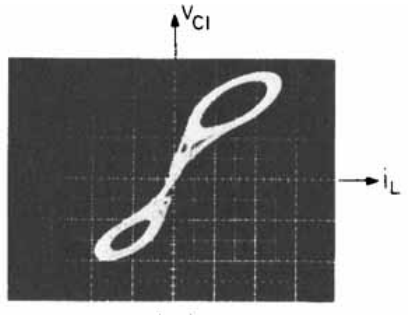


FIGURE 2.14: The chaotic attractor observed by Zhong and Ayrom [5].

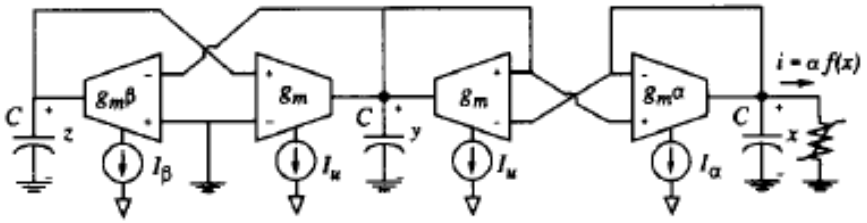


FIGURE 2.15: Conceptual transconductance amplifier Chua's circuit [6].

prototype of this circuit was fabricated using a 2.4 μm CMOS process and was able to generate Chua's double scroll attractor [6].

Another integrated CMOS realisation of Chua's circuit is described in [7]. Two operational transconductance amplifiers, in a positive feedback configuration, comprise the Chua's diode and two back-to-back transconductance amplifiers implement the gyrator. The circuit was produced using a 2 μm double-metal double-poly CMOS process and the diagram of the resultant integrated circuit is show in Fig. 2.17.

As can be seen from the previously described implementations, they employ a large number of MOSFETs in the transconductance operational amplifiers. A piecewise-linear current-voltage characteristic of the NR requires a significant amount of circuitry and also limits the speed of circuit operation (to approximately 10 kHz) due to compensation capacitors in the operational amplifiers. The four-transistor realisation of Chua's diode which can be visualised as a pair of cross-coupled inverters (Fig. 2.18), helped to minimise the number of components in the NR and advance the operational

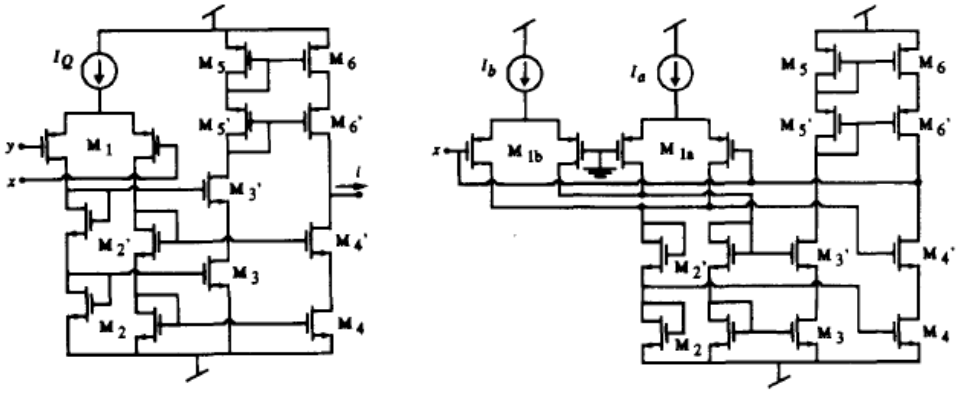


Figure 2.16: CMOS schematics for the transconductance amplifiers (left) and CMOS Chua's diode (right) [6].

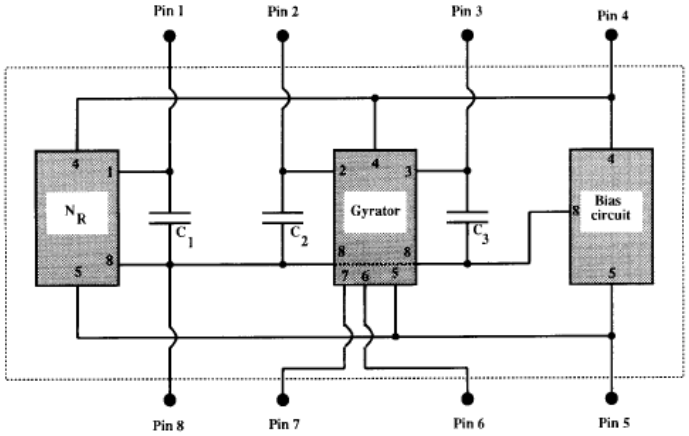


Figure 2.17: Network schematics of the CMOS IC Chua's circuit including the bias [7].

frequency to the megahertz range [8].

The current-voltage characteristic of this circuit can be written as a cubic function:

$$g(V) = G_a V - \frac{G_a}{V_{max}^2} V^3 \tag{2.28}$$

In this equation G_a denotes the slope of the characteristic at the origin and $\pm V_{max}$ are the outer zeroes, non-zero voltages at which the current is zero. The given implementation of Chua's diode results in a smooth characteristic rather than a piecewise one. It still allows the circuit to exhibit various chaotic phenomena.

However, as pointed at by Ginestar et al in [9], the shape of the cubic-like function

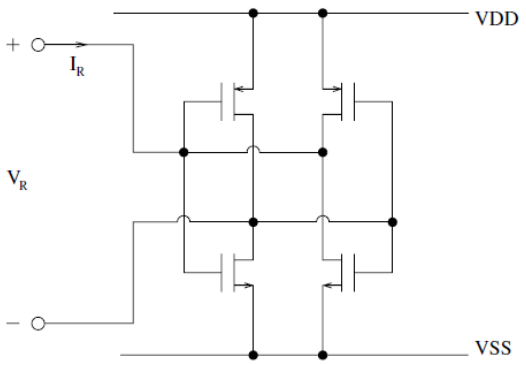


FIGURE 2.18: Four-transistor cubic-like Chua's diode [8].

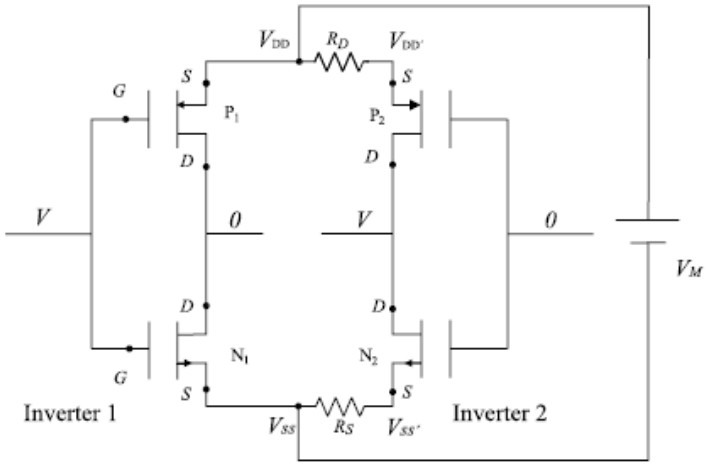


FIGURE 2.19: Variable cubic-like Chua's nonlinear resistor [9].

is defined by the characteristics of the transistors in a selected chip and it can be difficult to find realistic values of the resistor, the inductor and the capacitors to obtain the characteristic attractor of the Chua's circuit. Therefore a modified realisation of cubic-like nonlinearity, that allows changing the shape of the characteristic function, is proposed. The modified NR utilises two matched enhancement-type MOSFET complementary pairs with added drain (R_D) and source (R_S) resistors. The schematic is presented in Fig. 2.19. It was shown that changing the values of R_D and R_S results in modifying the shape of NR's current-voltage function.

An approach where Chua's diode is replaced with a tunnel diode is described in

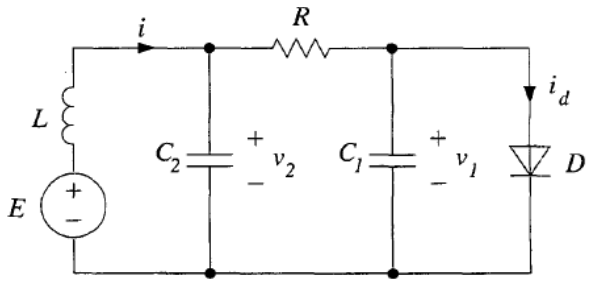


Figure 2.20: Implementation of Chua's circuit with a biased tunnel diode [10].

[10]. The authors use an appropriately biased tunnel diode, one of the fastest electronic components, in place of Chua's diode. This implementation (shown in Fig. 2.20) significantly increases the 1-orbit frequency, the frequency of the simplest unstable periodic orbit. Low frequency (kilohertz range) of operation of the op-amp based Chua's circuit implementations impede using spectrum analyser for revealing the details of the strange attractor topology. With using a 1N3720 tunnel diode, the authors were able to observe periodic components in the spectrum of v_1 at the frequency about 30 MHz with the orbits' harmonics noticeable at as high as 150 MHz.

Similar investigation of tunnel diode-based Chua's circuit was performed by Shi and Ran in [88]. In their work they show that global dynamics of Chua's circuit with NR's piecewise-linear function can be determined by combining together the behaviour of three regions. At the same time, current-voltage function of a tunnel-diode is highly nonlinear, thus the circuit can not be analysed as a three-region piecewise-affine system. The authors suggest another approach – splitting the state space in six different regions according to C_1 capacitor voltage V_{C1}. From the analysis it is seen, that the total dynamic behaviour can be determined by the dynamics in three regions of six. These could be mapped onto the three regions corresponding to piecewise-linear case. Investigation showed the existence of a double scroll which was obtained by simulations. Same procedure can be applied for the analysis of other Chua's circuit implementations with smooth NR's current-voltage functions, such as cross-coupled inverter realisation.

Chua's circuit found its application in such areas as image processing and trajectory recognition [89], secure communications [90] and even music composing [91].

Simulating a chaotic oscillator in CAD is not a trivial task and a suitable tool is required. Circuit simulation methods can be subdivided into analytical and numerical.

- *Analytical methods* such as Volterra series are normally well-suited for circuit design. This method assumes a sinusoidal steady-state solution of the nonlinear circuit. However, when it is required to obtain waveforms and spectra, iterative numerical methods are preferred. In numerical time-domain integration, circuit is described by differential algebraic equations. The nonlinear circuit is simulated by discretising time variable and applying some integration algorithm (e.g. forward and backward Euler, Runge-Kutta and Gear algorithms, trapezoidal approximation, etc.) to the original differential equations.

- *Harmonic balance* method transforms the set of differential algebraic equations into a set of algebraic equations in the frequency domain. The application of harmonic balance is limited to somewhat mild nonlinear operations because only periodic and quasiperiodic steady-state solutions can be obtained. High-quality oscillators or circuits operating near a bifurcation normally have long transients and transient, generally, require long simulation time.

- *Fast time-domain* techniques address steady-state solutions directly. This method would suit the simulation of highly nonlinear periodic regimes. Both of the aforementioned methods have limited application for chaotic system simulations because chaotic circuits have long transients which should be the focus of the simulations.

- The *envelope transient* method is normally applied for circuits with modulated signals and gives accurate results in intermodulation distortion. It can also be applied for the simulations of autonomous circuits – voltage controlled oscillators and injection-locked oscillators, but it generally requires complementary techniques for avoiding convergence toward nonoscillatory solution.

For simulating transients, when actual oscillation frequency undergoes variations, small time-integration step is necessary, otherwise the simulator can converge to the unstable

DC solution [92].

A small error in the former will produce an enormous error in the latter.

Henri Poincaré

3

Chua's Circuit Analysis

On the basis of sensitivity, simplicity and size, Chua's circuit was selected as a candidate for the CCM. Its analysis begins with the study of mathematical properties of this chaotic system.

3.1 Mathematical Properties

In this analysis a canonical six-component circuit was considered, with its elements being two capacitors, one resistor, one inductor, with its passive series resistance simulated by a separate resistor, and finally a non-linear active element, NR. A circuit diagram is shown in Fig. 3.1, however one should note that NR is an active element, therefore it needs some bias which is not shown for this small-signal model. As the first step in understanding how this circuit functions, the Kirchhoff's equations have

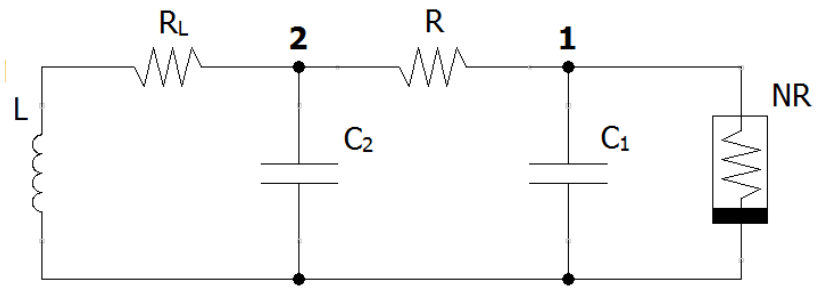


FIGURE 3.1: Chua's circuit schematic diagram.

to be written down for each node. These equations will help us to develop a set of differential equations which describe the behaviour of the circuit in the time domain.

3.1.1 Circuit Equations

As seen from Fig. 3.1, there are two nodes for which we want to write down the Kirchhoff's laws:

$$\mathbf{1}: \quad 0 = -i_{C1} + i_R - g(V_{C1}) \tag{3.1}$$

$$\mathbf{2}: \quad 0 = i_L - i_R - i_{C2} \tag{3.2}$$

where $g(V_{C1})$ is the current-voltage characteristic of the non-linear resistor (NR).

We want to analyse the signals of three reactive circuit-elements. Namely these are the voltages across the two capacitors and the current through the inductor. As it is known from the capacitor current-voltage relation:

$$I_C(t) = C\frac{dV_C(t)}{dt} \tag{3.3}$$

At the same time, the voltage across the inductor can be expressed in the following way:

$$V_L(t) = L\frac{dI_L(t)}{dt} \tag{3.4}$$

Therefore by putting i_{C1} and i_{C2} in the left-hand side of Equations 3.1 and 3.2 and using Equation 3.3 the following expressions are obtained:

$$C_1 \frac{dV_{C1}}{dt} = i_R - g(V_{C1}) \tag{3.5}$$

$$C_2 \frac{dV_{C2}}{dt} = i_L - i_R \tag{3.6}$$

The current flowing through the resistor can be simply expressed by:

$$i_R = \frac{V_{C2} - V_{C1}}{R} \tag{3.7}$$

From the schematics it is quite obvious that $V_L = -V_{C2} - i_L R_L$ and if Equation 3.4 is applied to this relation and also using Equation 3.7 we can write down three differential equations that fully describe the behaviour of the circuit.

$$\begin{aligned} C_1 \frac{dV_{C1}}{dt} &= \frac{V_{C2} - V_{C1}}{R} - g(V_{C1}) \\ C_2 \frac{dV_{C2}}{dt} &= \frac{V_{C1} - V_{C2}}{R} + i_L \\ L \frac{di_L}{dt} &= -V_{C2} - i_L R_L \end{aligned} \tag{3.8}$$

For simplicity of the further analysis it is possible to bring these equations to a dimensionless form by performing the following change of variables:

$$x = V_{C1} \tag{3.9}$$

$$y = V_{C2} \tag{3.10}$$

$$z = R i_L \tag{3.11}$$

Also the following dimensionless coefficients are introduced:

$$\alpha = \frac{C_2}{C_1} \tag{3.12}$$

$$\beta = \frac{R^2 C_2}{L} \tag{3.13}$$

$$\gamma = \frac{R R_L C_2}{L} \tag{3.14}$$

Now if we apply Equations 3.9–3.11 and 3.12-3.14 to the system of Equations 3.8 and also denote the time derivatives with $\dot{x}$, $\dot{y}$ and $\dot{z}$ we acquire the following system:

$$\begin{aligned} \dot{x} &= \alpha(y - x - g(x)) \\ \dot{y} &= x - y + z \\ \dot{z} &= -\beta y - \gamma z \end{aligned} \tag{3.15}$$

3.1.2 Nonlinear Resistor

The current-voltage characteristic of the nonlinear resistor, $g(V)$, depends on its implementation. The function of the original operational-amplifier realisation of the nonlinear element can be written down in the following way [93]:

$$g(V) = \begin{cases} G_b V + (G_b - G_a)E, & if\ V < -E \\ G_a V, & if\ -E \leq V \leq E \\ G_b V + (G_a - G_b)E, & if\ V > E \end{cases} \tag{3.16}$$

The graphical representation of the piecewise-linear current-voltage characteristic is displayed in Fig. 3.2. As can be seen, G_a is the conductance in the region between the breakpoints, defined as $\pm E$; G_b is the conductance when the applied voltage is beyond $\pm E$. It is understandable that the element can not have negative conductance in the whole range of voltages, therefore at high input voltage the circuit becomes passive, having a positive conductance. Another widely discussed implementation of the nonlinear element has a smooth nonlinearity which resembles a cubic function as shown in Fig. 3.3. This nonlinearity can be characterised by its slope at the origin G_a and 'outer zeros' V_{MAX} (see Equation 2.28).

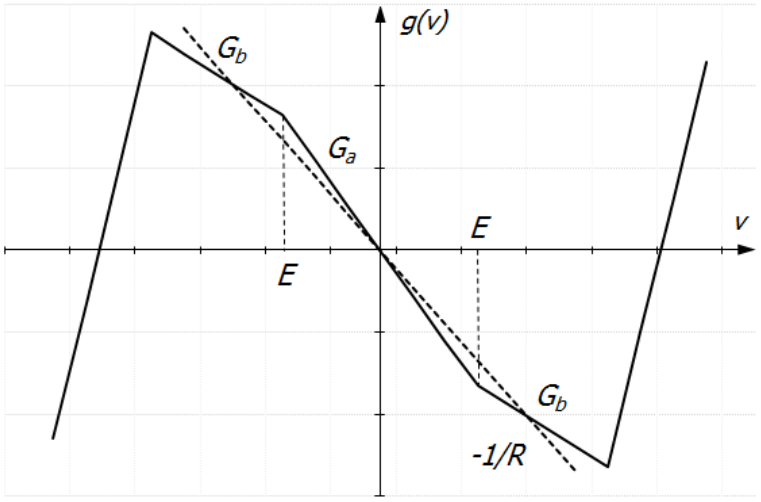


Figure 3.2: Piecewise-linear current-voltage characteristic of the NR (solid) and load line (dashed).

The load, which the NR "sees" is the resonator resistance which is equal to the value of the linear resistor, R (ignoring small inductor series resistance). From simple oscillator analysis [94] it is known that the resonator's resistance has to be small enough so that the resonator losses do not quench the oscillations but at the same time there are no other restrictions on what resonator resistance R should be. In the chaotic oscillator class, however, it is required that the current-voltage function of the NR intersects the load line, that is $-1/R$, in three points: at the origin, and twice in the regions of negative conductivity. In such a way the circuit will have unstable equilibrium points thus being able to oscillate chaotically [95]. The piecewise-linear and cubic-like characteristic intersections with the load line are shown in Fig. 3.2 and Fig. 3.3 respectively.

3.1.3 Equilibrium Points

Thus now we should go a little bit deeper into the details and study the concept of equilibrium points. Equilibrium solution (or point) is a solution which does not change in time. Firstly, a general three-dimensional dynamical system can be described by the following set of equations:

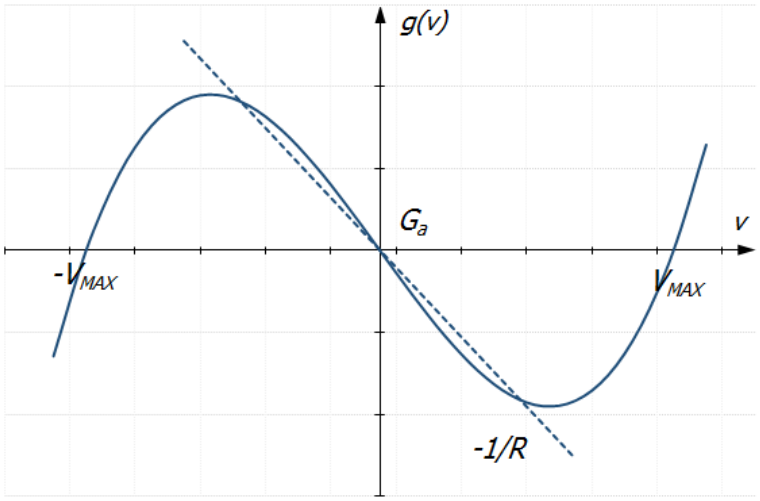


FIGURE 3.3: Cubic-like current-voltage characteristic of the NR (solid) and load line (dashed).

$$\begin{aligned} \dot{x} &= f_1(x, y, z) \\ \dot{y} &= f_2(x, y, x) \\ \dot{z} &= f_3(x, y, z) \end{aligned} \tag{3.17}$$

The stationary solutions of Equations 3.17, when the time derivatives are equal to zero, represent the equilibrium points. An equilibrium point with the coordinates (x_q, y_q, z_q) satisfies the following equation: $f_n(x_q, y_q, z_q) = 0$. Many other names are used for such solutions, such as fixed points, stationary points, rest points, critical points, etc. In this work, the terms equilibrium points or fixed points will be mainly used.

Equilibrium points of this system can be found by simply setting the time derivatives equal to zero.

$$\alpha(y - x) - g(x) = 0 \tag{3.18}$$

$$x - y + z = 0 \tag{3.19}$$

$$-\beta y - \gamma z = 0 \tag{3.20}$$

In order to solve this simple system, z in Equation 3.20 can be expressed in terms of y, placed in Equation 3.19 and the expression of x in terms of y can thus be found. Finally, y in Equation 3.18 is substituted with the y expression and the obtained equation is solved.

$$z = -\frac{\beta y}{\gamma} \tag{3.21}$$

$$y = x\frac{\gamma}{\beta + \gamma} \tag{3.22}$$

$$-x\frac{\beta}{\beta + \gamma} - g(x) = 0 \tag{3.23}$$

Equation 3.23 shows that all of the system's equilibrium points mainly depend on the current-voltage function of the nonlinear resistor, $g(x)$. Coefficient γ is usually much smaller than β, therefore the coefficient associated with x is close to 1 and is exactly 1 in the case of no inductor resistance. This suggests that small perturbations of circuit parameters which define β and γ do not significantly affect location of the equilibria.

3.2 Loading Effects

It is expected that in order to characterise the circuit's performance, its signals will be measured with the laboratory equipment. As it will be discussed in the subsequent chapters, the measurements will include taking samples of capacitor voltages connecting the voltage probe either relative to the ground or across the capacitor of interest. This kind of measurements will inevitably load the circuit to a certain extent, meaning that the resonator conductance will be affected. It is thus possible that the load line will change its slope and intersect the NR's current-voltage characteristic in a different region therefore changing the coordinates of the equilibrium points. In the extreme

case the circuit can become dissipative thus not meeting the conditions for oscillation at all.

When connecting a measuring device with a certain input impedance (load resistance R_{load}) to a capacitor, it effectively creates a path for a current which is parallel to i_R. In other words, Chua's equations (3.8) obtain the following form:

$$\begin{aligned} C_1\frac{dV_{C1}}{dt} &= \frac{V_{C2}-V_{C1}}{R||R_{load}} - g(V_{C1}) \\ C_2\frac{dV_{C2}}{dt} &= \frac{V_{C1}-V_{C2}}{R||R_{load}} + i_L \\ L\frac{di_L}{dt} &= -V_{C2} - i_L R_L \end{aligned} \tag{3.24}$$

The shown modification of the circuit equations predicts relocation of the equilibrium points. However if the input impedance of the connected device (that is R_load) is considerably higher than the value of R, this relocation will be practically unnoticeable. Nevertheless it is important to consider the loading effects during the circuit design phase because theoretically-functional oscillator may not operate under the load of measuring equipment, thus becoming non-characterisable.

It doesn't matter how beautiful your theory is, it doesn't matter how smart you are. If it doesn't agree with experiment, it's wrong.

Richard Feynman

4

Chua's Circuit Prototyping

Necessary theoretical knowledge about Chua's circuit operation was obtained and now it is required to experimentally confirm the expected sensitivity of the circuit. We need to perform circuit simulations to find which component parameters affect the output signals and in which way. Besides it is required to build a circuit prototype to acquire real-life examples of chaotic oscillations.

4.1 Matlab Simulations

Chua's circuit can be thoroughly investigated with the help of mathematical software such as Matlab. The Matlab package allows the solution of differential equations, plotting attractors, finding equilibrium points and defining their stability.

4.1.1 Piecewise Nonlinearity

We begin the study with the simulation of the canonical version of Chua's circuit with piecewise nonlinearity. Empirically the following circuit parameters (Fig. 3.1) were chosen for the simulation:

$$C_1 = 1\,\text{nF}$$
$$C_2 = 10\,\text{nF}$$
$$L = 220\,\mu\text{H}$$
$$R = 550\,\Omega$$
$$R_L = 1\,\Omega$$

The parameters of the piecewise-linear function (Equation 3.16) are as follows:

$$G_a = -1.16\,\text{mS}$$
$$G_b = -0.45\,\text{mS}$$
$$E = 1\,\text{V}$$

The Matlab script calculates the α, β and γ coefficients of the system:

$$\alpha = 10$$
$$\beta = 13.75$$
$$\gamma = 0.025$$

The script then finds the coordinates of the equilibrium points using Equations 3.21-3.23. The simulated system has three such points: one at the origin and two symmetric points with non-zero coordinates:

$$\mathbf{P}^+ = \quad (1.2952, 0.0024, -1.2928)$$
$$\mathbf{P^0} = \quad (0, 0, 0)$$
$$\mathbf{P}^- = \quad (-1.2952, -0.0024, 1.2928)$$

The aforementioned notation will be used for the equilibrium points, where $\mathbf{P}^+$ indicates the equilibrium point with positive x (or V_{C1}) coordinate, $\mathbf{P}^-$ the point with negative x coordinate and $\mathbf{P^0}$ indicates the equilibrium point at the origin. The coordinates of the fixed points are given in terms of (x, y, z), or in other words (V_{C1}, V_{C2}, i_L).

The next step would be to define the stability of the equilibrium points, following M.P. Kennedy in [83]. In order to do that, the points' eigenvalues have to be calculated. The Jacobian matrix is constructed and evaluated at the origin equilibrium point and also at $\mathbf{P}^+$ and $\mathbf{P}^-$, which will have same eigenvalues. The Jacobian matrices for the origin eigenvalue, $\mathbf{M_0}$, and for the nontrivial equilibria, $\mathbf{M_1}$, take the following form:

$$\mathbf{M_0} = \begin{pmatrix} -\alpha\left(1 + G_a - \dfrac{\gamma}{\gamma+\beta}\right) & \alpha & 0 \\ 1 & -1 & 1 \\ 0 & -\beta & -\gamma \end{pmatrix} \tag{4.1}$$

The eigenvalues of this matrix are the following:

$$\gamma_0 = 2.769$$
$$\sigma_0 \pm j\omega_0 = -1.088 \pm j2.638$$

$$\mathbf{M_1} = \begin{pmatrix} -\alpha\left(1 + G_b - \dfrac{\gamma}{\gamma+\beta}\right) & \alpha & 0 \\ 1 & -1 & 1 \\ 0 & -\beta & -\gamma \end{pmatrix} \tag{4.2}$$

The associated eigenvalues are:

$$\gamma_1 = -6.763$$
$$\sigma_1 \pm j\omega_1 = 0.128 \pm j3.33$$

With the help of Matlab the investigation of the circuit can be taken a bit further by studying the geometry of the chaotic attractor. There are eigenspaces associated with the eigenvalues of the equilibrium points. The real eigenvalue of the origin fixed point has the eigenvector $E^r(0)$ and the complex conjugate pair's eigenvector spans the

plane $E^c(0)$. Non-trivial equilibrium points $\mathbf{P}^+$ and $\mathbf{P}^-$ have eigenvectors $E^r(\mathbf{P}^+)$ and $E^r(\mathbf{P}^-)$ corresponding to the real eigenvalues and complex eigenvalues span the planes $E^c(\mathbf{P}^+)$ and $E^c(\mathbf{P}^-)$. The trajectory can not cross planes E_c therefore, trajectories originating above the plane will stay indefinitely above the plane and trajectories originating below the plain will stay below. Therefore defining these planes is important for finding the boundaries of the attractor.

Eigenvector $E^r(0)$ can be defined by:

$$M_0 E^r(0) = \gamma_0 E^r(0) \tag{4.3}$$

We can denote the eigenvector as $E^r(0) = (x, y, z)^T$ and thus obtain:

$$\begin{pmatrix} -\alpha\Big(1 + G_a - \dfrac{\gamma}{\gamma+\beta}\Big) - \gamma_0 & \alpha & 0 \\ 1 & -1-\gamma_0 & 1 \\ 0 & -\beta & -\gamma-\gamma_0 \end{pmatrix} \begin{pmatrix} x \\ y \\ z \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix} \tag{4.4}$$

After solving this matrix equation, the eigenvector subsequently can be written like this:

$$E^r(0) = \begin{pmatrix} x \\ y \\ z \end{pmatrix} = \begin{pmatrix} (1+\gamma_0)(\gamma+\gamma_0)+\beta \\ \gamma+\gamma_0 \\ -\beta \end{pmatrix} \tag{4.5}$$

Therefore the equation for the eigenvector corresponding to the real eigenvalue of the origin equilibrium point:

$$\frac{x}{(1+\gamma_0)(\gamma+\gamma_0)+\beta} = \frac{y}{\gamma+\gamma_0} = \frac{z}{-\beta} \tag{4.6}$$

The equation for the surface span by the complex conjugate eigenvalues of the origin equilibrium point is as follows:

$$((1+\gamma_0)(\gamma+\gamma_0)+\beta)x + \alpha(\gamma+\gamma_0)y + \alpha z = 0 \tag{4.7}$$

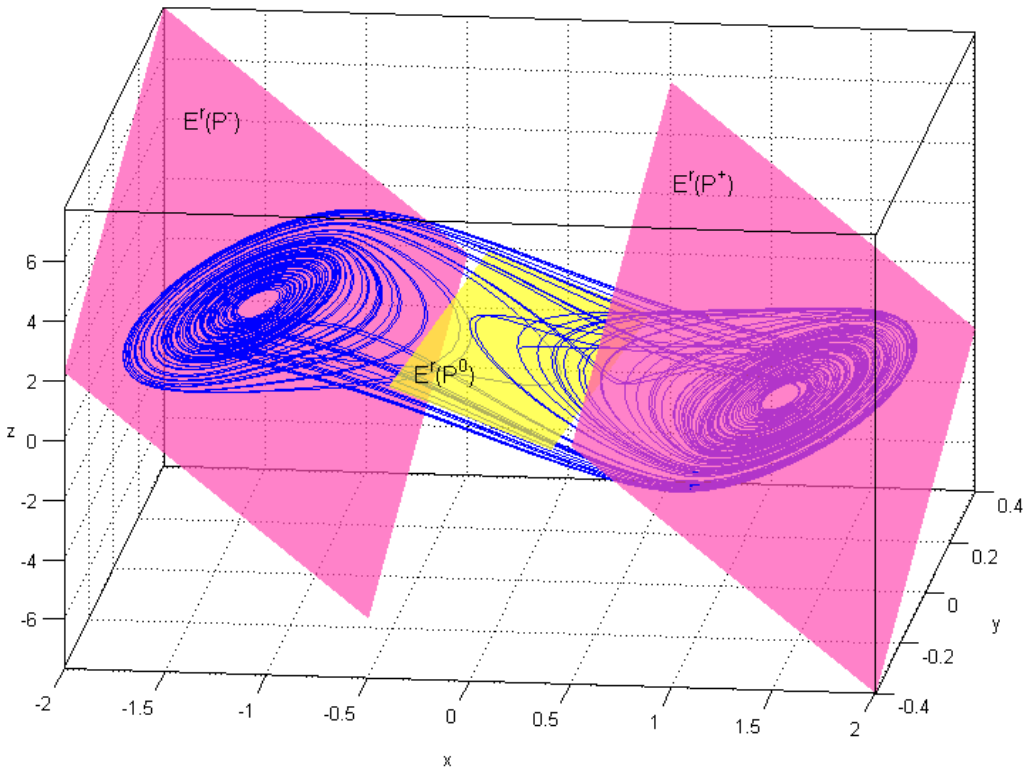


FIGURE 4.1: The geometry of the chaotic attractor from a circuit with piecewise nonlinearity.

Similarly it is possible to obtain the surface equations for the eigenplanes associated with the nontrivial equilibrium points $\mathbf{P}^+$ and $\mathbf{P}^-$. The vector corresponding to the real eigenvalues is written down like this:

$$\frac{x \pm x_e}{(1+\gamma_1)(\gamma+\gamma_1)} = \frac{(y \pm y_e)}{(\gamma+\gamma_1)} = \frac{(z \mp z_e)}{-\beta} \tag{4.8}$$

The plane span by the complex eigenvalues:

$$(1+\gamma_1)(\gamma+\gamma_1)(x \pm x_e) + \alpha(\gamma+\gamma_1)(y \pm y_e) + \alpha(z \mp z_e) = 0 \tag{4.9}$$

where x_e, y_e and z_e are the equilibrium point coordinates. Note that circuit coefficient γ should not be confused with real eigenvalues γ_0 and γ_1 of the zero and nonzero equilibrium points, respectively, all being conventional notations.

System equations for the circuit with piecewise nonlinearity are solved using a solver

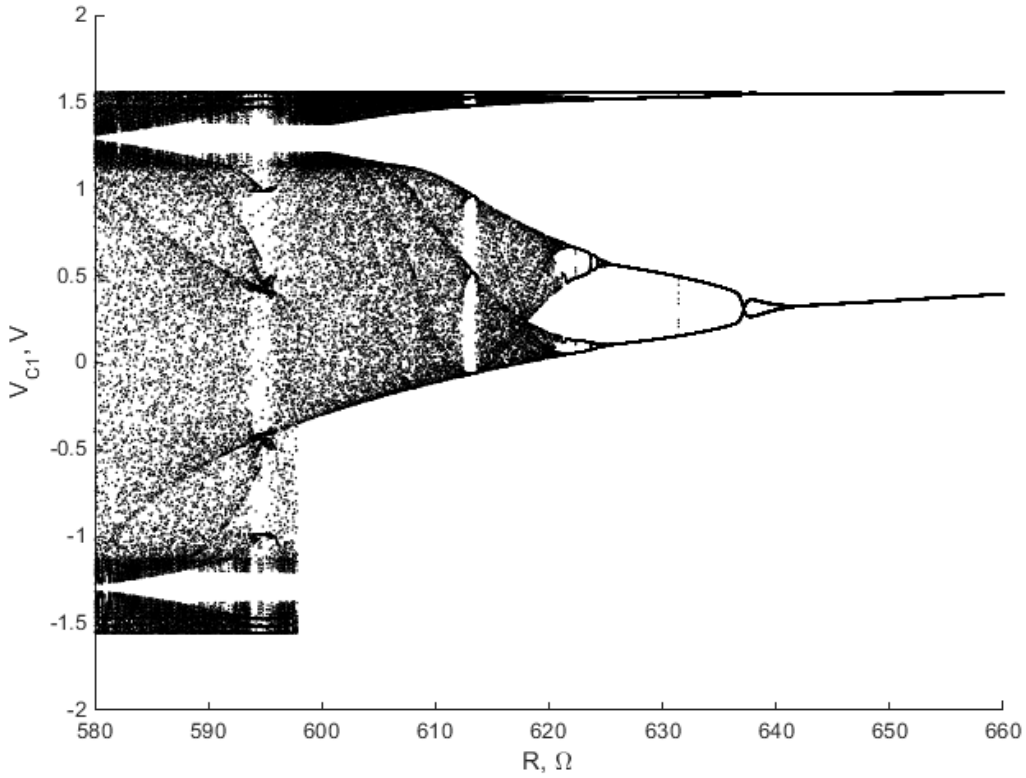


FIGURE 4.2: The bifurcation diagram of the circuit with piecewise-linear nonlinearity generated by Matlab algorithm.

based on the 4^{th} order Runge-Kutta formula. The double-scroll attractor obtained from the simulations is shown in Fig. 4.1. The planes defining its geometry are shown too.

Matlab can also help in the bifurcation analysis. It is possible to observe how the bifurcations occur when we change certain circuit parameters. In this case, the bifurcation diagram is plotted as a series of dots which represent the trajectory crossing the equilibrium plane. The result of the bifurcation diagram for a varying R can be observed in Fig. 4.2. It is evident that for higher R values the trajectory is a limit cycle, which is indicated by the two lines. Then at a value of R of approximately 640 Ω a pitchfork bifurcation can be observed; a period doubling took place. With the further increase the period-doublings start occurring at ever decreasing intervals until the chaotic attractor emerges at R close to 598 Ω. This represents the period-doubling route to chaos.

R, Ω	x_e	G_a, mS	x_e
540	1.2953	-1.158	1.2915
545	1.2952	-1.159	1.2934
550	1.2952	-1.160	1.2952
555	1.2951	-1.161	1.2970
560	1.2951	-1.162	1.2988

Table 4.1: Simulation of linear resistor and piecewise-linear current-voltage function effect on x_e coordinate of equilibrium point

The analysis of Chua's equations suggested that equilibrium points depend mainly on the current-voltage function $g(x)$ of the NR. We can simulate the circuit with different values of its components and with different coefficients of the current-voltage function to investigate their effect on equilibrium-point coordinates. First, we check the effect of linear resistor on x_e by varying R in the range from 540 Ω to 560 Ω with 5 Ω steps therefore varying it by approximately ±2 %. To find the $g(x)$ effect on x_e we change G_a from -1.158 mS to -1.162 mS thus varying it by less than ±0.2 %. The results are summarised in Table 4.1. One can see from this table that larger variation of R comparing to the one of G_a leads to smaller change in x_e thus proving our assumption that the influence of R is much less than that of $g(x)$.

4.1.2 Smooth nonlinearity

The simulations can be repeated for the circuit with the same parameters but with a smooth nonlinearity, described by a cubic function. The same circuit parameters are to be used:

$$C_1 = 1\,\text{nF}$$
$$C_2 = 10\,\text{nF}$$
$$L = 220\,\mu\text{H}$$
$$R = 550\,\Omega$$
$$R_L = 1\,\Omega$$

However, in this case the nonlinearity will be described by the cubic function $g(x) = ax^3 + cx$. The parameters of this cubic nonlinearity, which were defined empirically, are the following:

$$a = 0.297$$
$$c = -1.257$$

The values of α, β and γ stay unchanged, although the coordinates of the equilibrium points are now different. The implementation of the code results in the following equilibria:

$$\begin{aligned} \mathbf{P^+} &= (0.9335, 0.0017 - 0.9318) \\ \mathbf{P^0} &= (0, 0, 0) \\ \mathbf{P^-} &= (-0.9335, -0.0017, 0.9318) \end{aligned}$$

The change in the nonlinear function will alter the Jacobian matrices of the system and the eigenvalues assigned to the fixed points correspondingly. The system matrix for the origin equilibrium point will have the following entries:

$$\mathbf{M_0} = \begin{pmatrix} -\alpha - \alpha c & \alpha & 0 \\ 1 & -1 & 1 \\ 0 & -\beta & -\gamma \end{pmatrix} \tag{4.10}$$

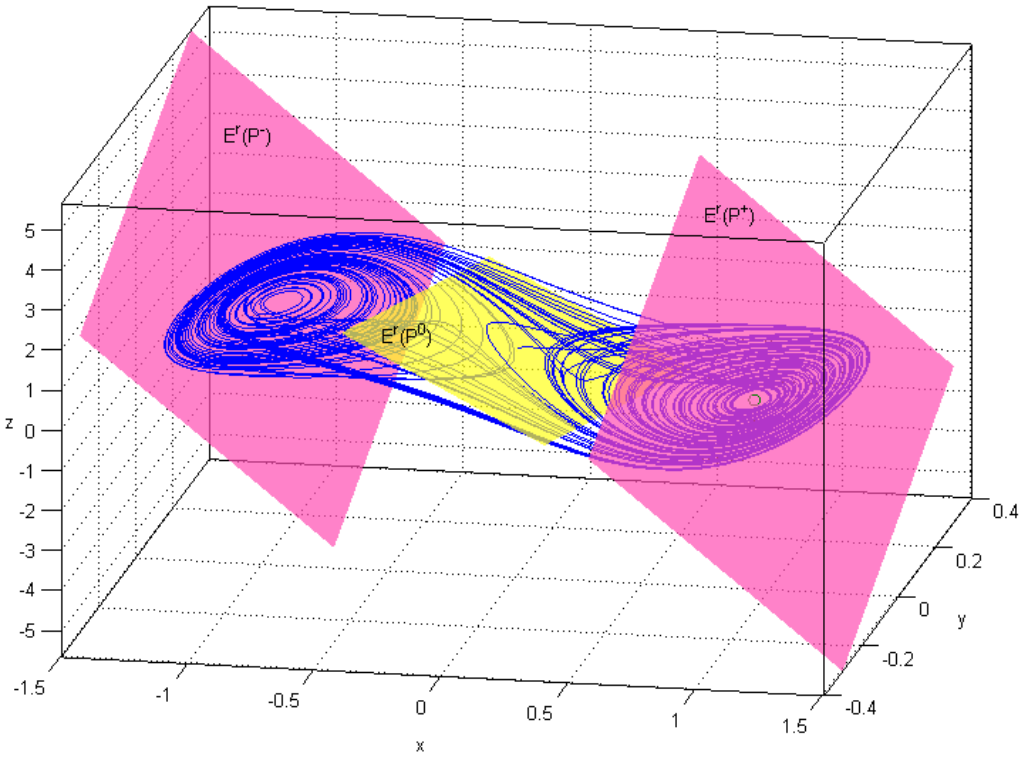


FIGURE 4.3: The geometry of the chaotic attractor from a circuit with cubic nonlinearity.

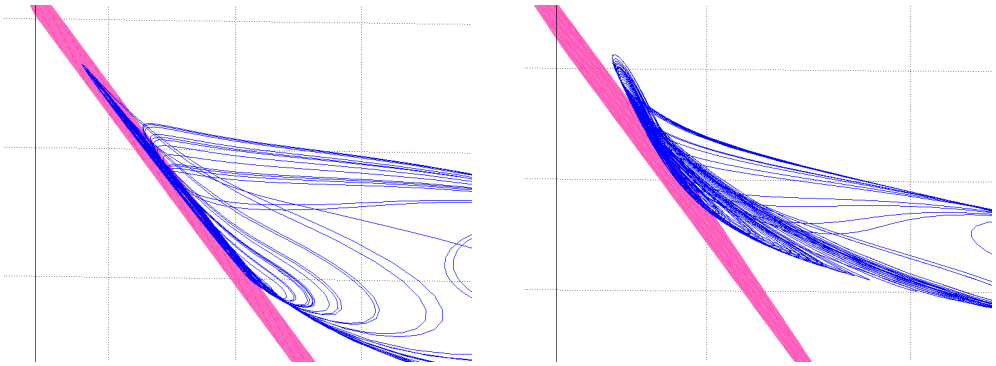
The eigenvalues of this matrix turn out to be the following:

$$\gamma_0 = 3.7546$$
$$\sigma_0 \pm j\omega_0 = -1.0798 \pm j2.857$$

The Jacobian matrix for the non-zero equilibria appears like this:

$$\mathbf{M_1} = \begin{pmatrix} -\alpha(1 + 3ax^2 + c) & \alpha & 0 \\ 1 & -1 & 1 \\ 0 & -\beta & -\gamma \end{pmatrix} \tag{4.11}$$

with the eigenvalues being the following:



(a) Piecewise-linear (b) Cubic

FIGURE 4.4: Zoom in on the P^- equilibrium point for the two attractors.

$$\gamma_1 = -6.508$$

$$\sigma_1 \pm j\omega_1 = 0.169 \pm j3.311$$

In can be seen that the eigenvalues did not significantly change from the piecewise case; their signs remained the same, meaning that the stability of the equilibrium points was basically not altered.

As can be verified from Fig. 4.3, the geometry of the attractor did not significantly change. The eigenplane equations were not affected by the change of the nonlinear element function and remained the same as in the piecewise-linear case. However, after taking a closer look, the planes in which the trajectory rotates appear to be different for the two kinds of nonlinearities.

Scrutinizing the trajectories in the vicinity of the equilibrium points, as displayed in Fig. 4.4, can show that the trajectory of the attractor corresponding to the piecewise function (Fig. 4.4(a)) rotates around the equilibrium point lying in the E^r plane, while in the case of the cubic nonlinearity (Fig. 4.4(b)) the trajectory becomes curved. For the case of cubic nonlinearity the eigenvalues of the system matrix (4.11) are changing continuously with x, thus E_r becomes not a line but a curve and E_c becomes not a plane but a curved surface [88]. Although in this Matlab script, for the sake of simplicity, we only evaluated eigenvectors and eigenplanes at the equilibrium points $x = x_e$, thus

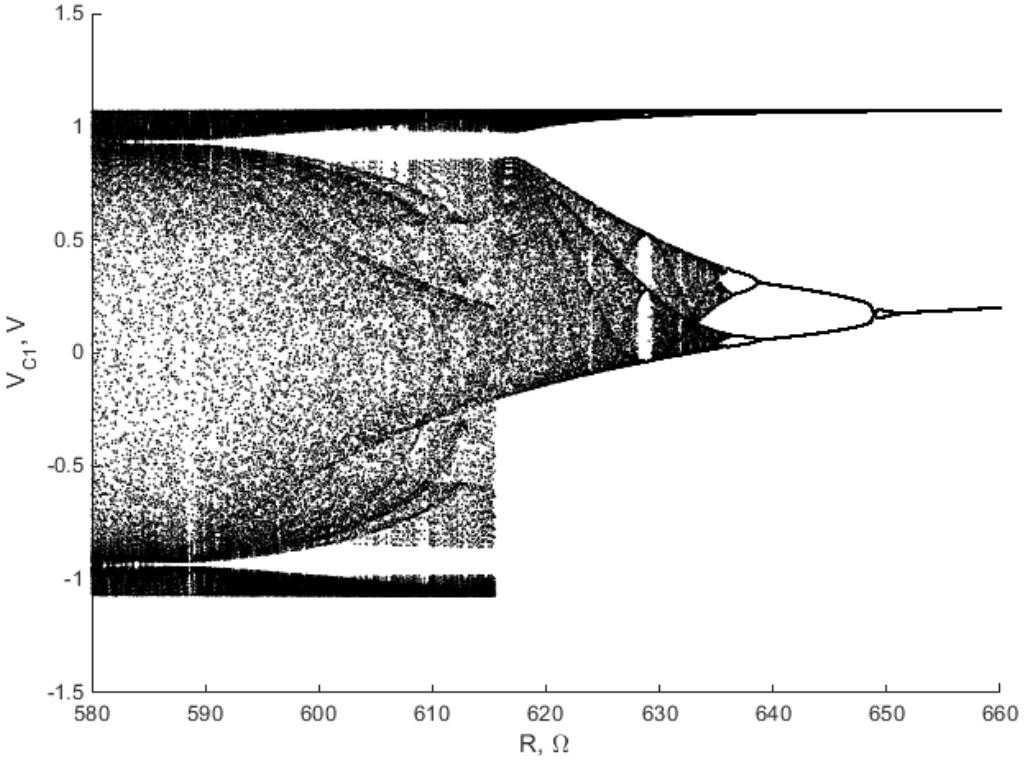


Figure 4.5: The bifurcation diagram of the circuit with piecewise-linear nonlinearity generated by Matlab algorithm.

obtaining flat planes.

The bifurcation diagram of a cubic-nonlinearity system is very similar to the piecewise-linear one. The obtained diagram is presented in Fig. 4.5. The values at which bifurcations are taking place changed. First period-doubling occurs at the value R of approximately 650 Ω and the chaotic attractor appears at R close to 615 Ω. Qualitatively both diagrams are equivalent.

We can repeat the circuit sensitivity simulation with the cubic nonlinearity. In this case we can change the $g(x)$ coefficient a in the range of 0.295 to 0.299 with 0.001 step, thus varying it by approximately ±0.7 %. Range for linear resistor value R was carried over from the previous simulation. In can be seen from Table 4.2 that results qualitatively the same as in the case with the piecewise-linear function.

It was also attempted to see the capacitance change effect but it was found even

R, Ω	x_e	a, mS	x_e
540	0.9336	0.295	0.9367
545	0.9335	0.296	0.9351
550	0.9335	0.297	0.9335
555	0.9335	0.298	0.9319
560	0.9334	0.299	0.9304

TABLE 4.2: Simulation of linear resistor and cubic current-voltage function effect on x_e coordinate of equilibrium point

less noticeable than the effect of linear resistor value.

4.2 CAD Circuit Simulations

The electronic circuit that corresponded to the mathematically simulated circuit equations, is designed using AWR Design Environment (Microwave Office) [96]. The first attempted approach is to construct a circuit with a cubic-like smooth nonlinearity rather then a piecewise-linear type. The reason for this is that the piecewise function usually requires much more complicated schematics than a smooth nonlinear characteristic does. Also following the CCM's requirement for a simple circuit we favoured this implementation over the op-amp NR.

The first circuit is designed using generic SPICE level-1 MOSFET models with the default parameters available from the AWR component library. The usage of simple models (as opposed to more complicated ones of the pHEMT devices) in the investigation of circuit operation can significantly contribute to the overall understanding of Chua's circuit in terms of its applicability for the process control. It is expected that the nonlinear resistor comprised of MOS and HEMT devices will produce qualitatively similar current-voltage characteristics.

The configuration of the nonlinear resistor employs two cross-coupled MOS inverters. Each inverter is represented as an ideal complementary pair of MOSFETs. The schematic of the nonlinear element is shown in Fig. 4.6. The circuit simulation is

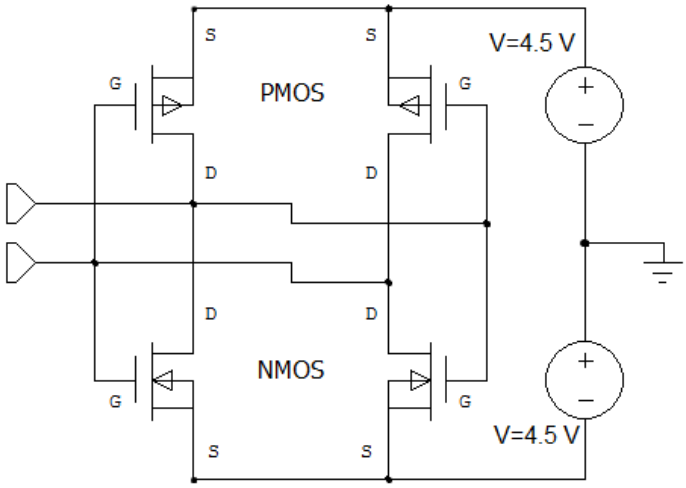


Figure 4.6: Nonlinear element with two cross-coupled CMOS inverters as simulated in AWR.

performed using the harmonic balance (HB) simulator. The obtained current-voltage characteristic of this element (Fig. 4.7) is a smooth function and can be described by a cubic polynomial as a good approximation, however a higher-order polynomial is required for a more precise representation. In order to obtain the mathematical function describing the simulated current-voltage characteristic a special curve-fitting software, Eureqa [97], [98] was used. This program can generate mathematical functions from a data series with a good fit. It is possible to approximate the data using polynomials, and in this case we obtain a 7^{th}-order polynomial describing the simulated curve with a very good fit:

$$g(x) = 6.223 \times 10^{-7}x^7 - 0.0001495x^5 + 0.01781x^3 - 0.7961x \tag{4.12}$$

It also should be stated that this function represents the current in milliamperes (mA) when the input is in volts (V).

The schematic of the passive part of the circuit is shown in Fig. 4.8, where the nonlinear resistor shown in 4.6 is indicated as NR. The values of the passive circuit components are the following:

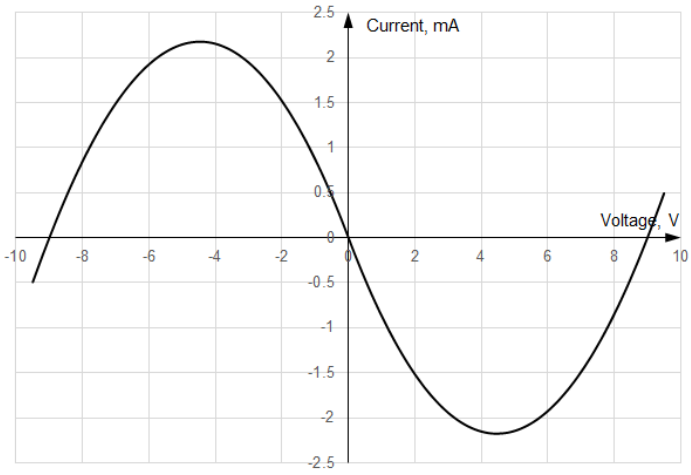


FIGURE 4.7: Current-voltage characteristic of the MOSFET nonlinear element.

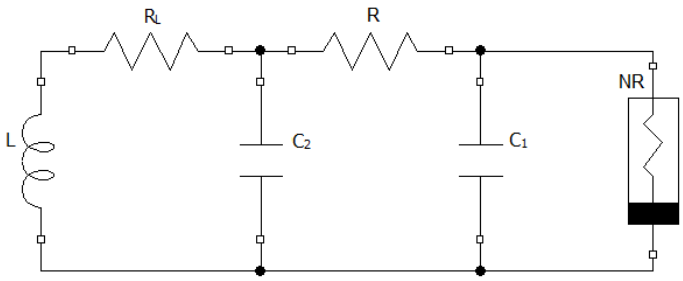


FIGURE 4.8: AWR schematic of the designed MOSFET Chua's circuit.

$$C_1 = 1\,pF$$

$$C_2 = 10\,pF$$

$$L = 2\,\mu H$$

$$R = 1650\,\Omega$$

$$R_L = 5\,\Omega$$

With this set of parameters, the circuit is capable of generating chaotic oscillations, as shown after constructing the phase plot.

Voltage-meter components are placed in parallel with the capacitors C_1 and C_2. Voltage as seen by these voltmeters is simulated in time domain using the APLAC transient simulator [99], [100]. Empirically it was shown that this simulator is the only

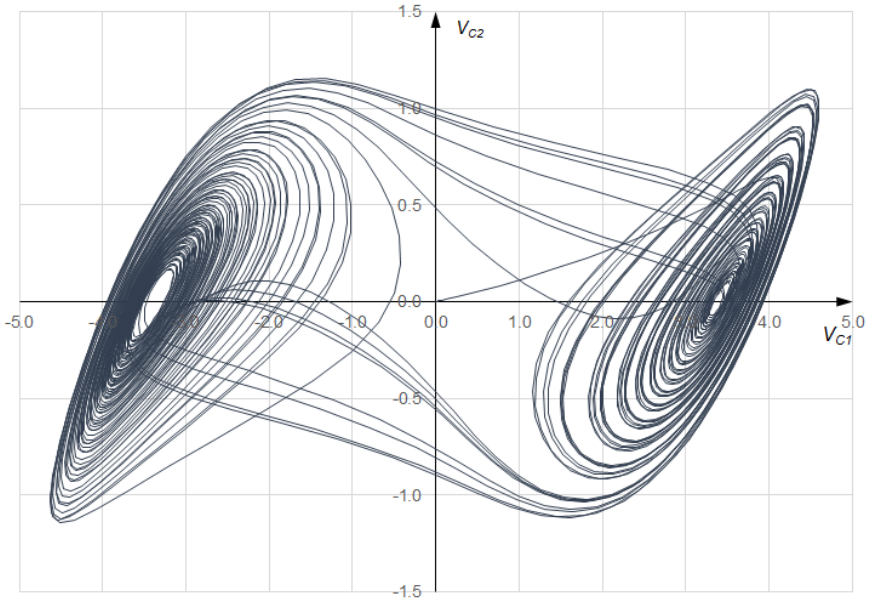


Figure 4.9: Attractor for CMOS circuit generated from AWR simulation.

one among available simulators, including, harmonic balance, AC harmonic balance, APLAC harmonic balance and APLAC AC harmonic balance, which is capable of correctly simulating long transients.

APLAC employed trapezoidal method for solving the circuit differential equations. Simulation was performed for 10 μs with 1 ns step. It was observed that after increasing the step size to 5 ns the solution converges to an unstable DC solution. Euler and Gear algorithms were tried as well. Gear algorithm showed results which were very similar to the ones obtained with the trapezoidal method while Euler's algorithm's result was slightly different as seen in the transient.

Generated time-series for $V_{C1}(t)$ and $V_{C2}(t)$ with no post-processing are used to plot the attractor. The C_1 capacitor voltage is plotted on the x-axis and the C_2 capacitor voltage on the y-axis. The resultant phase portrait is shown in Fig. 4.9 where one can observe the chaotic attractor, thus establishing chaotic behaviour for the circuit.

Now, the Matlab model can be tested to see if its results are consistent with the AWR circuit simulations. The formula 4.12 obtained from the curve fitting was incorporated in the equations of the Matlab code.

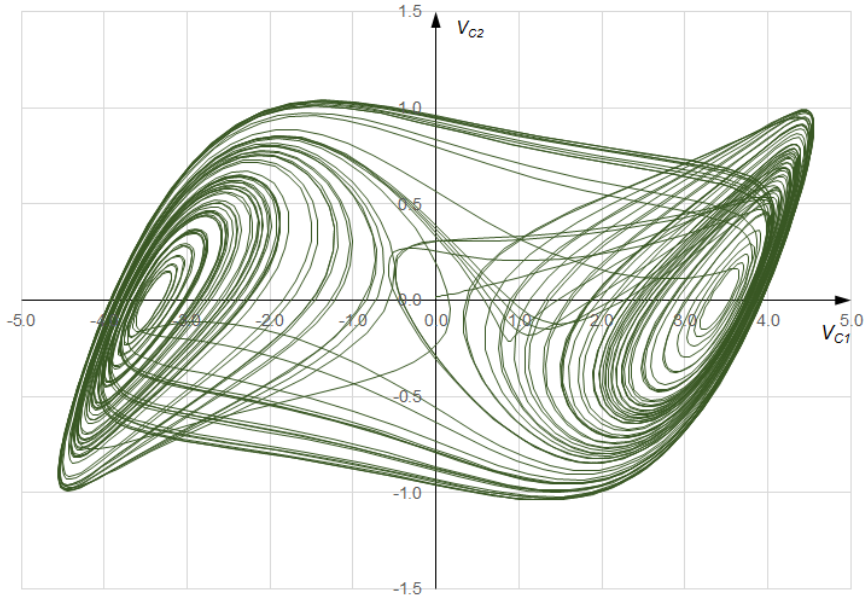


FIGURE 4.10: Attractor for CMOS circuit generated by the Matlab script.

Running the Matlab code to simulate the equations resulted in the attractor as shown in Fig. 4.10. It can be seen that this attractor very closely matches the one obtained from the AWR circuit simulation as presented in Fig. 4.11. The equilibrium points, which can be seen as the centres of the holes around which the trajectory rotates, are almost identical. The mismatch between the two results may arise from slightly inaccurate description of simulated nonlinearity by the mathematical function obtained from curve-fitting. Another possible reason could be the fact that the two simulators use different methods for numerical solution of the differential equations.

According to the Matlab solution, the equilibrium points of the simulated circuit have the following coordinates:

$$\begin{aligned} \mathbf{P}^{+} &= \quad (3.45, 0.0104, -3.44) \\ \mathbf{P}^{\mathbf{0}} &= \quad (0, 0, 0) \\ \mathbf{P}^{-} &= (-3.45, -0.0104, 3.44) \end{aligned}$$

These coordinates are consistent with the simulated data. That can be easily seen from the figure comparing the attractors (Fig. 4.11).

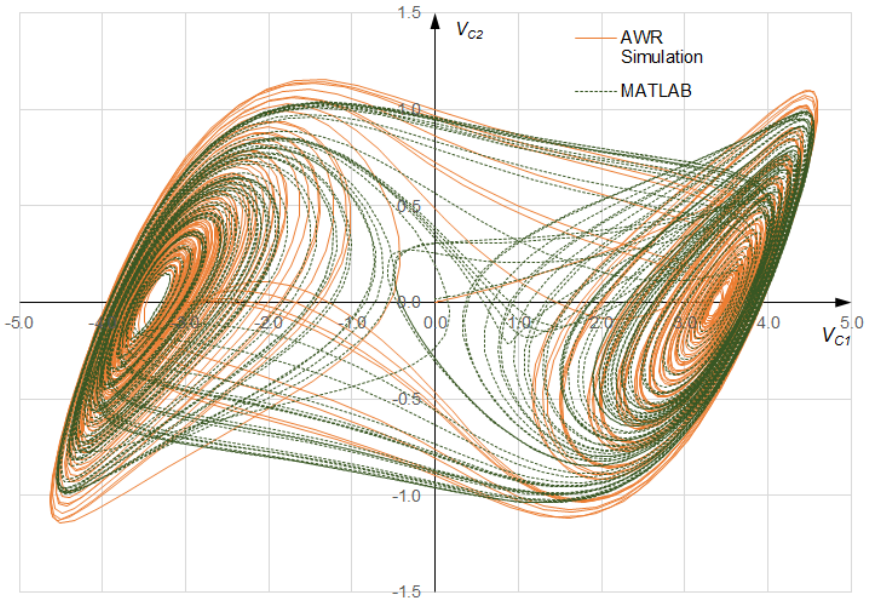


Figure 4.11: Comparison of the MOSFET circuit attractors generated in AWR and by Matlab script.

The performed comparison confirms that the developed Matlab model is capable of making rather accurate predictions of the real circuit behaviour, given that the current-voltage characteristic of the nonlinear element is known in the form of a mathematical equation.

In this circuit investigation an APLAC transient simulator was used for obtaining the signals in the time domain. This simulator has shown consistency of its results with the mathematical model prediction however it is considered that various time-domain simulators may not be useful in simulating chaotic responses due to their long transients. On the other hand, frequency-domain simulators, such as Harmonic Balance (HB) can not simulate steady chaotic solutions due to the spectrum continuity. However, we can employ the HB simulator in locating the equilibrium points of the system.

In order to find the equilibrium points, constant (or DC) solutions have to be found. We can place a variable DC source in parallel with the NR and then sweep the voltage. HB simulations result in the current-voltage graph as shown in Fig. 4.12. The x-coordinates (or V_{C1}) of the equilibrium points can be seen on this graph as the

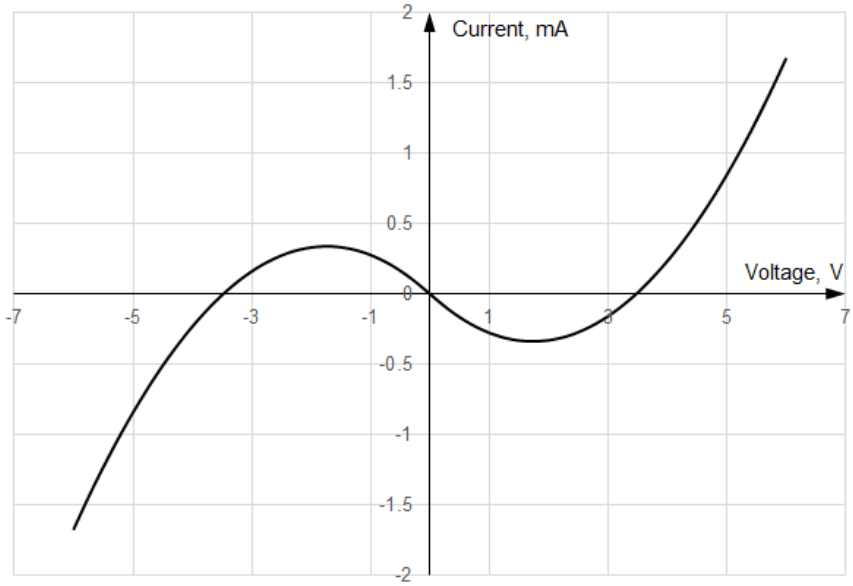


FIGURE 4.12: Steady state Harmonic Balance circuit simulation.

characteristic's intersections with the voltage axis or, in other words, voltage values when the DC current is zero [101]. It can be seen from the graph and is confirmed by the dataset that points of intersection are -3.48 V, 0 V and 3.48 V. These numbers are very close to the ones predicted by the Matlab simulations and can be visually confirmed by observing the time-domain signals and phase space portraits.

4.3 Analysis of the Circuit's Signals

When referring to a chaotic system, one would always emphasise its high dependence on the initial conditions. It is true that real chaotic systems are highly dependent on some parameters while not so sensitive to others [102]. As the purpose of this work is to investigate the applicability of a chaotic oscillator for the role of manufacturing process control, we positively want to investigate how sensitive Chua's circuit is to fluctuations of the manufacturing process.

In order to become a usable CCM, a candidate has to be small in size, contain as few components as possible and, most importantly, be able to predict the functionality of the other circuits located on the same reticle. Consequently, the measurable output

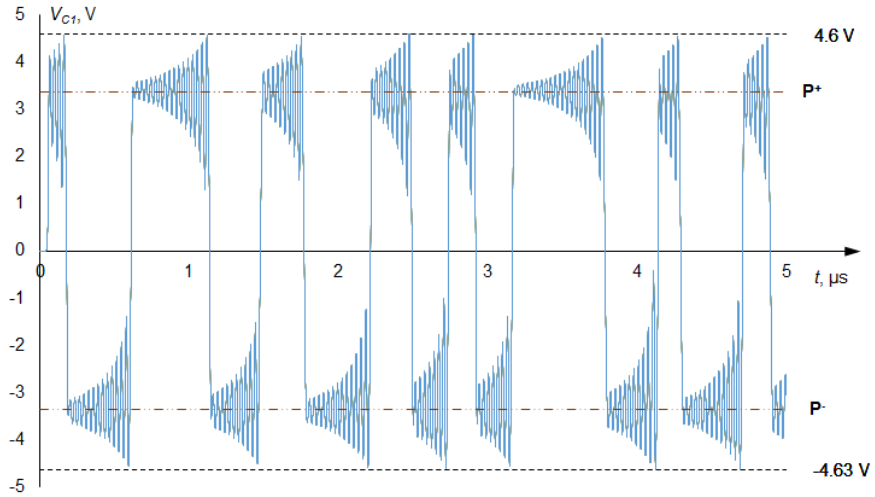


Figure 4.13: V_{C1} of the MOSFET Chua's circuit simulated in time domain by AWR.

signals of the CCM should contain some distinct features which can be attributed to its nonlinear performance.

In reality it is desired to make the measurements as simple as possible. Therefore we would prefer to measure just a voltage across one of the capacitors. As the simulations have shown, the more interesting signal to look at would be the voltage across capacitor C_1 which has far more distinct equilibrium levels then that of C_2 voltage. Current is normally much harder to observe in the time domain, therefore we do not consider doing measurements of inductor current.

The first and most obvious characteristic of the signal one can estimate is its peak-to-peak voltage. As seen from Fig. 4.13, the maximum voltage level is 4.6 V and the minimum value is -4.63 V, thus making the peak-to-peak voltage equal to 9.23 V. Measurements of this kind can be easily performed by almost any oscilloscope and do not require much preparation.

Next, this signal can be analysed in the frequency domain to obtain its spectrum. The chaotic signals generated by Chua's circuit are non-periodic, therefore it is expected that their spectrum is broad with almost no distinct peaks. To evaluate the spectrum of the simulated signal one can use the Fast Fourier Transform in a Matlab algorithm. The result of the FFT signal transform is shown in Fig. 4.14. Note that the amplitude

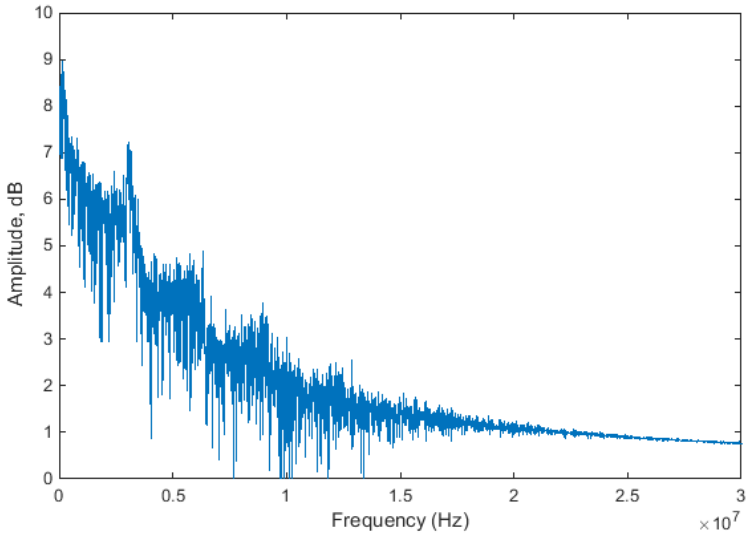


FIGURE 4.14: C_1 voltage of the AWR-simulated MOSFET circuit in the frequency domain.

Signal parameter	Measurement Technique
Amplitude	Oscilloscope
Frequency Spectrum	Spectrum analyser / Oscilloscope + FFT
Equilibrium Levels	Oscilloscope and post-processing

TABLE 4.3: Characteristics of chaotic signals and how they could be measured.

has not been normalised, therefore the units are relative.

Another feature of the signals which becomes obvious in the time domain is the position of the equilibrium points. The equilibria coordinates can be seen on the graph as the voltage levels around which the higher-frequency oscillations occur (shown in Fig. 4.14 as $\mathbf{P}^+$ and $\mathbf{P}^-$). The summary of chaotic signal's characteristics and how we can measure them is presented in Table. 4.3.

On the other hand, finding the equilibrium levels from the recorded time-series (when the nonlinear resistor's terminals are inaccessible, as in the case of integrated circuits) is a non-trivial procedure and can not be done by means of conventional measurement equipment (additional signal processing will be required). However it is possible to recover the levels corresponding to the equilibrium-point coordinates from

sufficiently long time series. The fixed points are not explicitly present in the time series and can only be estimated. In fact, the accuracy of this estimation depends on how noisy the time-series data is. For *low-noise* simulated signals the following algorithm is used:

1. Split the data into above-zero and below-zero oscillations to look for positive and negative equilibrium points separately.

2. For each of the two $\mathbf{P}^+$ and $\mathbf{P}^-$ sub-series we create an inverted copy of itself. This is needed for finding the local maxima and minima in the sub-series.

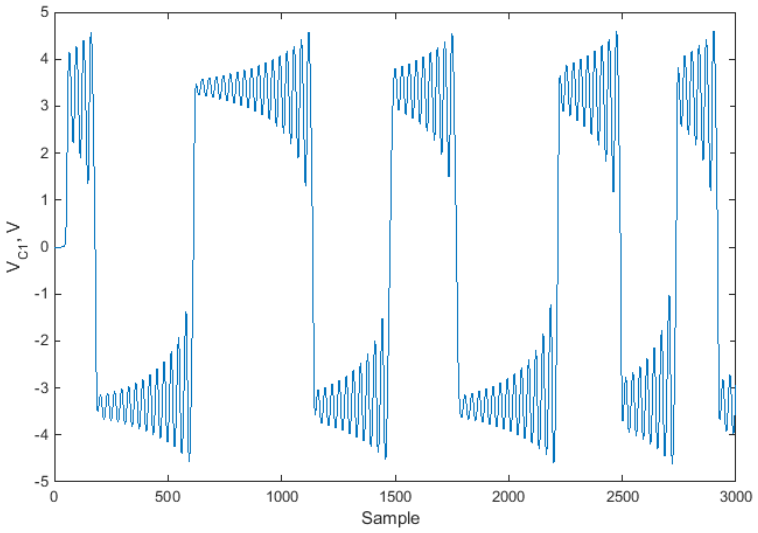
3. The *findpeaks* Matlab function is used to find the local maxima. Application of this function to the non-inverted copy of each of the sub-series corresponds to finding the local maxima, hence when this function is applied to the inverted copy local minima is obtained. That complication is required because there is no built-in Matlab function for finding the negative peaks.

4. The two equilibrium points, $\mathbf{P}^+$ and $\mathbf{P}^-$, are found as the median distance between the minimum peak-up and the maximum peak-down.

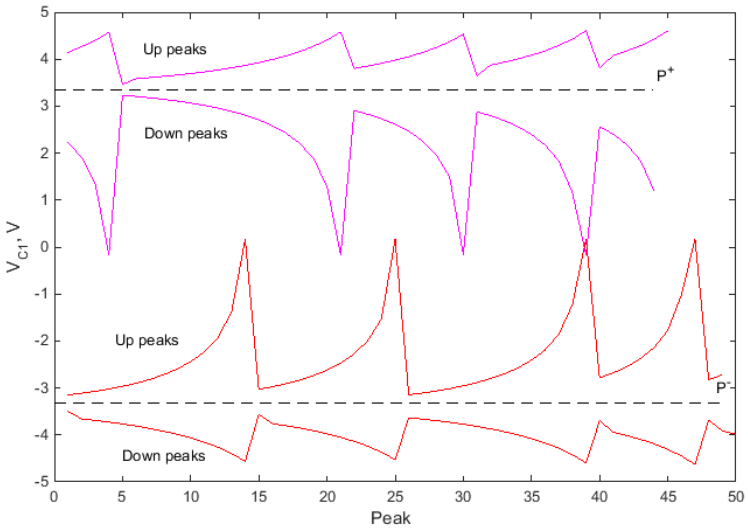
   See Fig. 4.15 for the algorithm graphic output.

It has been previously shown during the mathematical analysis of the circuit in Chapter 2 that, the location of the equilibrium points depends on the current-voltage function of the nonlinear element, however the linear resistor also affects the equilibria. On the other hand, the nonlinear resistor is the only circuit element which contains nonlinear devices.

In the fulfilled circuit simulations, the transistors are the devices whose performance we want to monitor. In the context of integrated-circuit manufacturing, estimating the resistance of the resistive components is a relatively simple task which involves measuring the resistive layer sheet resistance. The linear resistance can then be calculated based on the sizes of the resistive circuit elements. The resistors inside the PCM and the ones inside of the functional circuit, because of their linear nature, operate in the



(a) Analysed time-series data



(b) Plotted peak data and equilibrium levels (dotted lines)

FIGURE 4.15: The output of the Matlab equilibrium-level estimation algorithm.

same way, regardless of the bias conditions of the circuit. At the same time, transistors of the PCM can be biased differently than the transistors of the functional circuits. The performance predicted by the PCM can not be simply extrapolated to every possible bias value, specifically because of the nonlinear effects present in these semiconductor devices. That said, however, in determining the Chua's circuit's equilibrium levels,

the linear resistor's variations can be eliminated when the actual resistive layer sheet resistance variation is known.

4.4 Circuit Sensitivity

As the measurable signal characteristics have been defined, we can try to monitor them while changing certain circuit parameters to scrutinise the oscillator's sensitivity. The same MOSFET design from Section 4.2 is to be used in the simulations. The parameters of some linear and nonlinear elements are planned to be modified in order to determine their influence on the circuit's output signals.

The effect of transistor transconductance (KP in the AWR MOSFET SPICE model) on the attractors and especially on the location of their equilibrium points is investigated firstly. In order to vary the transconductance, parameter KP of the transistor models, the gate oxide thickness TOX was altered. It enters the formula for KP calculation in the following way:

$$KP = UO\frac{3.8 \cdot \varepsilon_0}{TOX} \tag{4.13}$$

where UO is the mobility (600 cm^2/Vs for NMOS, 250 cm^2/Vs for PMOS) and $\varepsilon_0 = 8.85 \cdot 10^{-14}$ F/cm is the vacuum permittivity. KP in its turn affects the characteristic of the MOSFET transistors, particularly the drain current function $I_d(V_{ds})$. The effect of TOX change on the transistor characteristic is shown in Fig. 4.16. The default value for the oxide thickness is 100 nm. The graph depicts the effect of a variation of this parameter by ±2 %. The transistor's drain current in the MOS model is linearly dependent on the transconductance, therefore the change in saturation drain current I_{DSAT} can be seen as being very close to the same ±2 %.

The circuit was simulated with TOX values in the range from 94 nm to 104 nm with 2 nm steps. In each case mathematical expression of $g(V)$ was generated using Eureqa and simulated V_{C1} was analysed for equilibrium points in Matlab. Fixed points of the attractor were obtained from both the solution of the equation and from the data series.

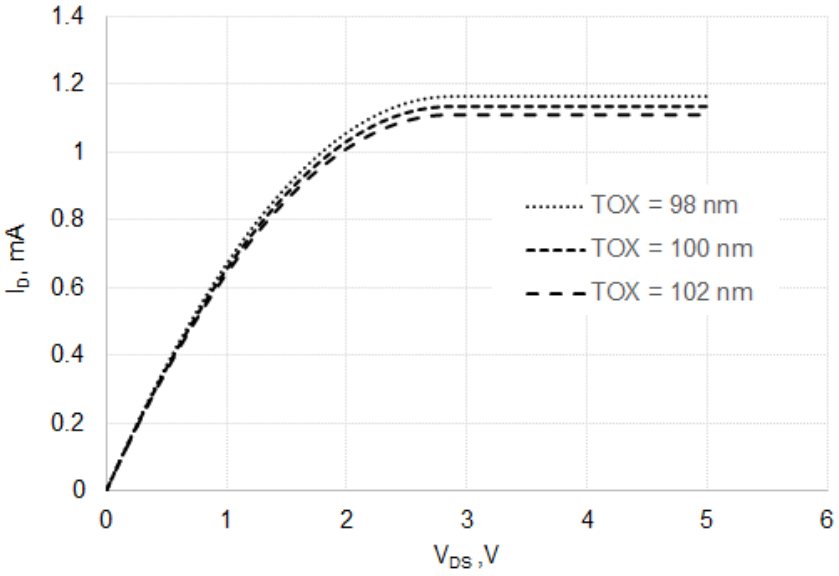


FIGURE 4.16: NMOS output characteristic for three TOX values.

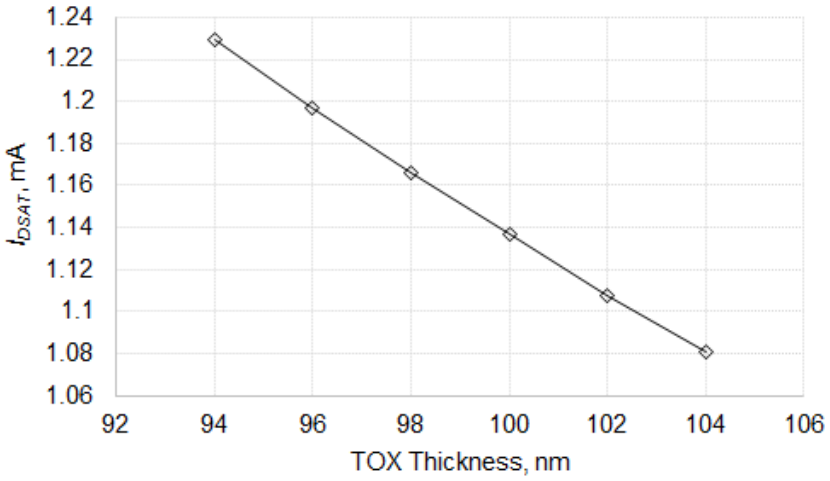


FIGURE 4.17: Drain saturation current I_{DSAT} as the function of gate oxide TOX thickness

It should be noted that the TOX parameter which indicates the MOSFET gate oxide thickness is not directly applicable to a pHEMT technology which this study is aimed at. However the effect of TOX can be seen in shifts of gate capacitance and threshold voltage which do have analogies in GaAs pHEMT devices.

The variation of the drain saturation current I_{DSAT} with change of the thermal gate oxide thickness (TOX) can be seen in Fig. 4.17. This figure extends the TOX

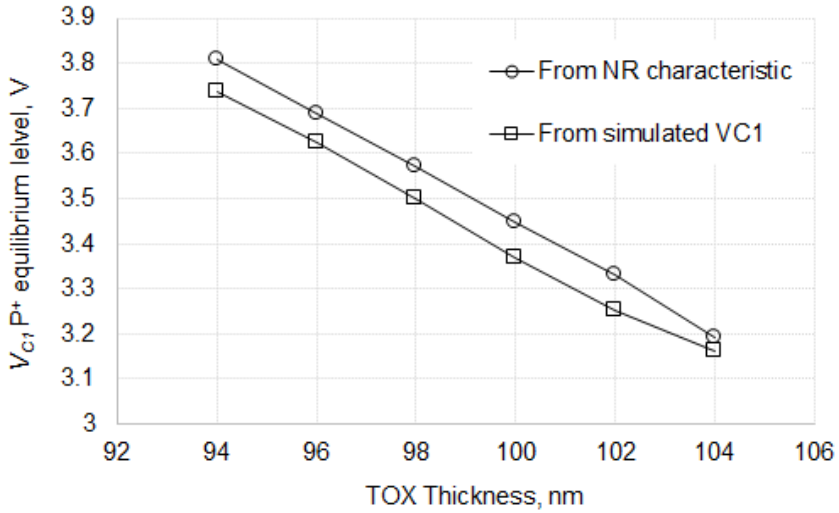


Figure 4.18: Effect of gate oxide TOX thickness change of the V_{C1} P^+ equilibrium level.

variation effect on the drain current shown in Fig. 4.16. At the same time, the effect of a TOX change on the V_{C1} positive equilibrium level $\mathbf{P}^+$ can be seen in Fig. 4.18. The two traces indicate the V_{C1} $\mathbf{P}^+$ level obtained from the solution of Chua's equations with the estimated $g(V)$ function and the data generated by the algorithm retrieving the equilibrium levels from the simulated time series. Firstly, one can notice a close correspondence between the outcomes of the two approaches (the convergence of lines is accidental). Secondly, the declining trend of the $\mathbf{P}^+$ equilibrium level with the increase of TOX thickness can be easily seen. The comparison of the figures mentioned above indicates that the effect of TOX thickness influences the shift of equilibrium points in a stronger way then it does with the transistor saturation current. The standard deviation of I_{DSAT} is approximately 4.8 %, while the standard deviation in the datasets of the equilibrium coordinates from the equation solution and from the locating algorithm is over 6.5 %. This finding suggests that the circuit's nonlinear signals are able to somewhat magnify the effect of the transistor parameter change comparing to the results of the linear characteristic measurements.

We can also check how the change in linear resistance R affects the equilibrium voltage level. In the simulation we vary R in the range from 1630 Ω to 1680 Ω with step of 15 Ω, in other words, ±2 % from the initial value of 1650 Ω. Signals simulated

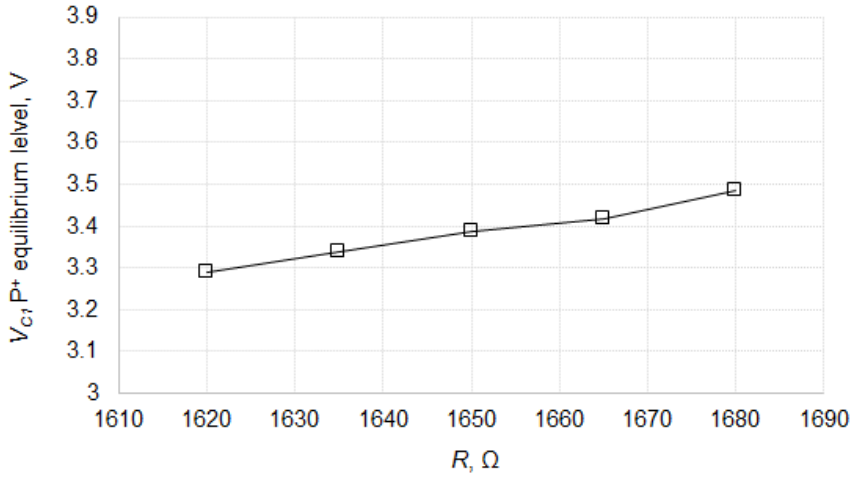


FIGURE 4.19: Effect of linear resistor R change of the V_{C1} P^+ equilibrium level.

in AWR were treated to the Matlab equilibrium-level locating algorithm to obtain $\mathbf{P}^+$. The results are presented in Fig. 4.19 and as can be seen, the effect is quite noticeable. However the standard deviation of positive equilibrium voltage is approximately 2.2 % which is less than in the case of TOX variation.

Apart from equilibrium point level, peak-to-peak voltage of capacitor C_1 was also recorded during the variation of R and TOX values. The results are presented in Table 4.4. We can note that peak-to-peak voltages change significantly during the variation of both parameters. However we can see that standard deviation of signal characteristics for R variation is higher for peak-to-peak voltage, while the opposite is observed in the case of TOX change. This finding suggests that the change of linear circuit parameters affects linear characteristics of signal (such as peak-to-peak voltage) more, while nonlinear signal characteristics in the form of equilibrium levels are more strongly affected by nonlinear parameters.

Many parameters affect the performance of the transistors and if some, for example, increase the saturation drain current, others can decrease it independently. Consequently, there is a possibility that a pair of parameters varying simultaneously can give no net effect on the transistor current-voltage characteristics. This means that such variations of the manufacturing process might not be captured during linear

R, Ω	Peak-to-peak, V	V_{C1} P^+, V	*TOX*, nm	Peak-to-peak, V	V_{C1} P^+, V
1620	9.0613	3.2891	96	9.8108	3.6250
1635	9.1814	3.3379	98	9.5517	3.4985
1650	9.2690	3.3873	100	9.2875	3.3696
1665	9.4012	3.4165	102	9.0260	3.2502
1680	9.8048	3.4845	104	8.7614	3.1632
STD, %	**3.063**	**2.207**	**STD, %**	**4.468**	**5.493**

Table 4.4: Peak-to-peak voltage and $\mathbf{P}^+$ equilibrium level of V_{C1} for varied R and *TOX* values.

MOS Type	W, μm	*NSUB*, cm^{-3}	I_{DSAT}, mA
P	60	1E15	0.710365
P	60.9	1.1E15	0.709099
P	60	1.1E15	0.69862
P	60.9	1E15	0.721021
N	40	1E15	1.13658
N	40.5	1.1E15	1.13176
N	40	1.1E15	1.11779
N	40.5	1E15	1.15079

Table 4.5: Effect of W and *NSUB* change on the saturation drain current.

PCM testing. The sensitivity of Chua's circuit is investigated for one such scenario.

The explored case involved changing the substrate doping concentration, *NSUB*, and the MOSFET gate width, W, together. An increase of *NSUB* decreases the saturation current while an increase of W does the opposite. New values of *NSUB* and W were chosen for NMOS and PMOS transistors in such a way that their output characteristics remained very close to those corresponding to the default values for a range of gate voltages, V_g.

Table 4.5 describes the saturation current shift due to a change of channel width, W, and substrate doping, *NSUB*. One can notice that the change of each of the parameters

W_N, μm	W_P, μm	*NSUB*, cm^{-3}	P^+, V	P^-, V
40	60	1E15	3.3873	-3.3243
40.5	60.9	1.1E15	3.4650	-3.4772

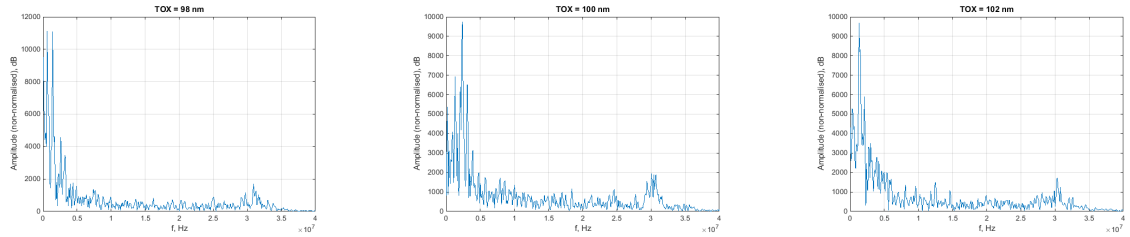
TABLE 4.6: Effect of W and *NSUB* changes on the coordinates of the V_{C1} equilibrium levels.

separately noticeably affects the saturation drain current for both types of transistor. The change expressed in percent varies from 1.25 % up to 1.65 % which can easily be measured. At the same time, a simultaneous increase of W and *NSUB* has very little effect on the saturation currents, resulting in their shift by ≈0.42 % for NMOS transistors and ≈0.18 % for PMOS. That change can be noticed at the time of transistor tests, but the change is comparable to the measurement error.

In the latter case the output characteristics remained the same, however the effect of parameter fluctuations was noticed on the nonlinear element's characteristic, which in turn changed the location of the equilibrium points.

As can be seen from Table 4.6, the effect of W and *NSUB* changes is much more noticeable when observing the equilibrium-point coordinates. The two simulated time series were processed by the Matlab algorithm to recover the equilibrium levels of the C_1 capacitor voltage.

We can also perform the FFT transformation of the simulated signals to obtain their spectrum. Three spectra of V_{C1} are shown in Fig. 4.20 corresponding to different *TOX* values. We can see that the spectra are wideband and continuous, which makes it hard to quantify it. The changes in the spectra are noticeable, however no pattern during *TOX* varying was observed. This means that spectra can presumably work as an indicator of Chua's circuit performance, however we do not have a theoretical link between signal's spectrum and circuit parameters. Thus, with the current knowledge, we can not utilise the frequency spectrum for the purposes of process monitoring.



(a) $TOX = 98$ nm (b) $TOX = 100$ nm (c) $TOX = 102$ nm

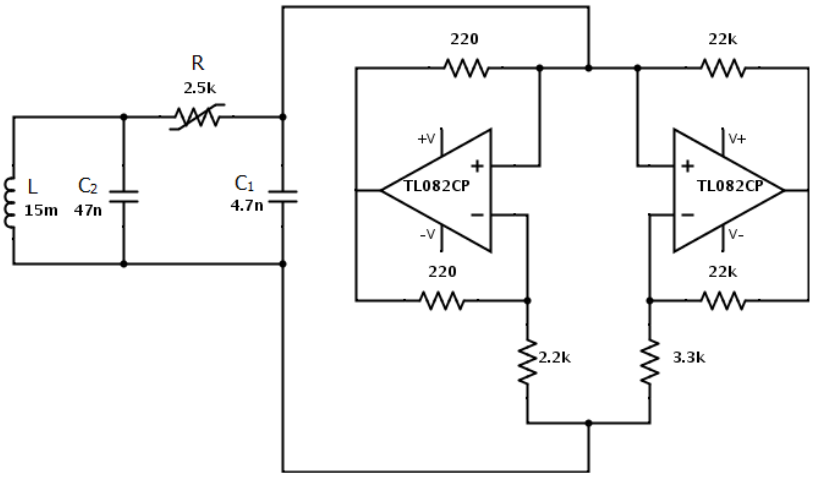
FIGURE 4.20: Spectra of the AWR-simulated V_{C1}, with MOSFET TOX varied, obtained after Matlab FFT transformation.

4.5 Board-level CCM Concept

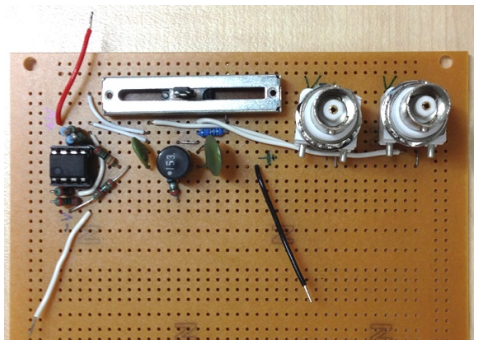
After all the circuit simulation procedures were complete, it was decided to try construction of the CCM candidate, Chua's circuit, from discrete components. The hands-on experience with the real circuit's behaviour was assumed to be necessary for better understanding the circuit prior to attempting the IC design. The CMOS IC op-amp and inverter realisations of the NR were chosen for their wide availability and ready solutions, as opposed to compound-semiconductor devices. At this stage of the project it was important to find appropriate ratios of the passive component values and gain experience with the signal analysis. It is expected from a CMOS-based NR to generate a similar current-voltage function as a pHEMT-based one would. Therefore CMOS prototyping of Chua's circuit can be used for developing methods for chaotic-circuit design, its signal analysis and can be easily scaled to the compound-semiconductor realisation.

As was mentioned before, the classical Chua's circuit employs operational amplifiers for the generation of a piecewise-linear current-voltage characteristic. The suggested implementation ([103]) utilises two operational amplifiers, thus a TL082CP integrated circuit can be used as it is essentially a dual op-amp. The schematic is shown in Fig. 4.21(a) and the PCB with the assembled circuit is presented in Fig. 4.21(b). This implementation requires six resistors and a dual voltage supply of ± 9 V.

The constructed circuit required almost no tuning and chaotic signals were observed on the screen of the oscilloscope. The measured signals, the voltages across the two



(a) Schematic of the op-amp Chua's circuit prototype



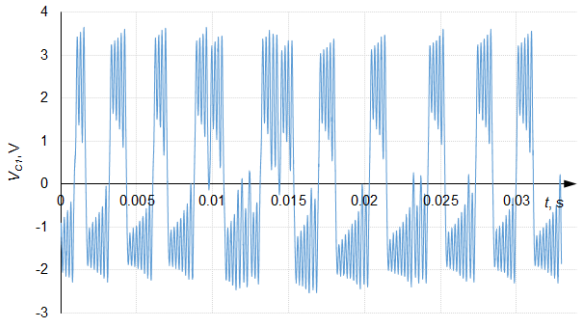
(b) Photo of the PCB containing the constructed Chua's circuit

FIGURE 4.21: The op-amp realisation of the Chua's circuit.

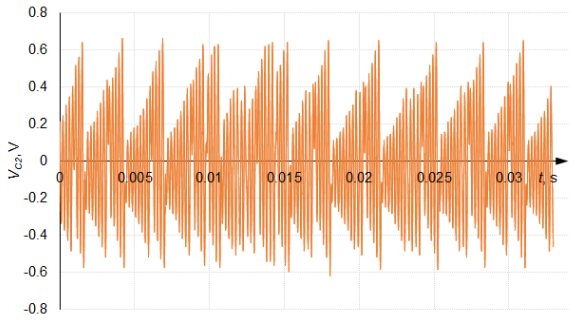
capacitors, are presented in Fig. 4.22. The chaotic nature of the signals is apparent and it matches the shape of the previously simulated signals very well.

The circuit was able to demonstrate period-adding bifurcations with change of potentiometer resistance R. The observed bifurcations are presented in Fig. 4.23. This experiment clearly indicates the circuit's ability to generate chaotic signals.

Another implementation of Chua's circuit involves a cross-coupled-inverter configuration of the nonlinear resistor. The authors of [8] used a 4007-series integrated circuit with CMOS inverters. The HCF4007UBE integrated circuit is a dual complementary pair plus inverter. The IC contains two CMOS pairs and one extra pair connected in



(a) C_1 capacitor voltage

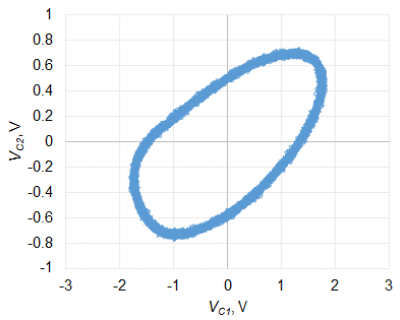


(b) C_2 capacitor voltage

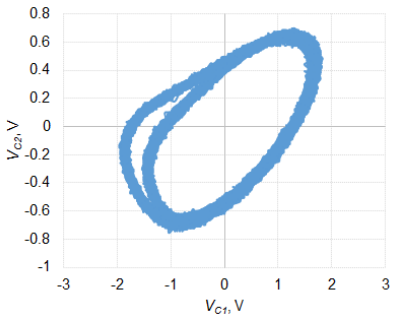
Figure 4.22: Measured signals generated by the op-amp Chua's circuit realisation.

inverter configuration. The outputs of the IC were interconnected to form two cross-coupled inverters from the two available complementary pairs. The schematic can be seen in Fig. 4.24 along with the PCB photograph. The variable resistor was a removable component and was placed in the IC holder. The circuit was biased using a bipolar ±4.5 V power supply.

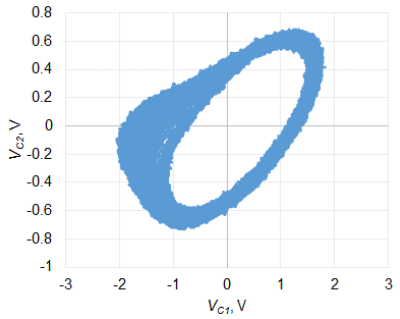
Depending on the R value, the circuit was able to generate harmonic or chaotic oscillations. The CMOS implementation of the NR allowed the circuit to operate at approximately 165 kHz while the op-amp circuit was tuned to around 5.7 kHz. The constructed oscillator demonstrated chaotic behaviour, however for a relatively narrow range of resistance R. This time the voltage on capacitor C_1 was measured relative to ground because measuring the voltage across the capacitors showed no result for a reason which was not investigated. The results of the measurements are displayed in Fig. 4.25 and the appearance of the signal is chaotic.



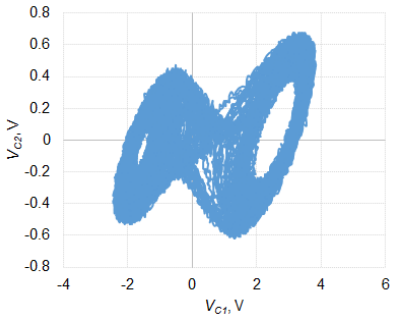
(a) Limit cycle



(b) Period-2 orbit

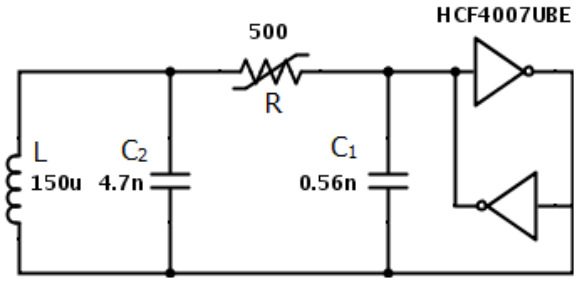


(c) Period-4 orbit

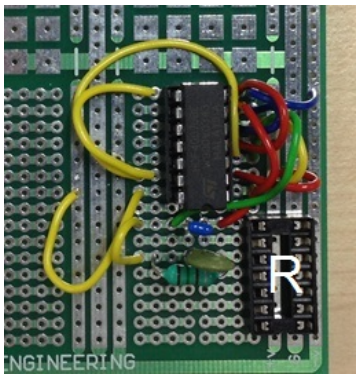


(d) Chaotic attractor

FIGURE 4.23: Bifurcations occurring in the op-amp Chua's circuit with changing R.



(a) Schematic of the inverter Chua's circuit prototype



(b) The photo of the PCB containing the constructed Chua's circuit

FIGURE 4.24: The CMOS inverter realisation of Chua's circuit.

It was also attempted to evaluate the circuit's sensitivity to the active component parameters. Namely, 3 different 4007-series ICs were tried, and the samples of C_1 capacitor voltages were recorded while keeping the rest of the circuit parameters fixed.

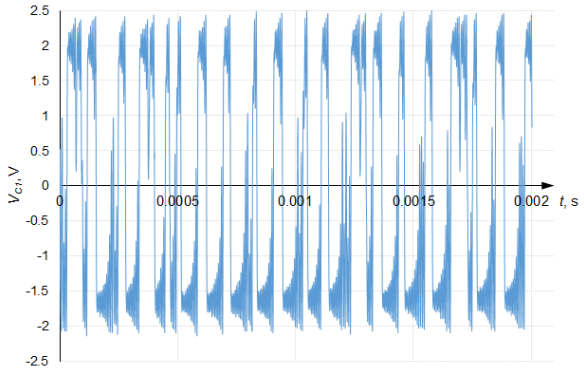


FIGURE 4.25: Measured capacitor C_1 voltage in time domain.

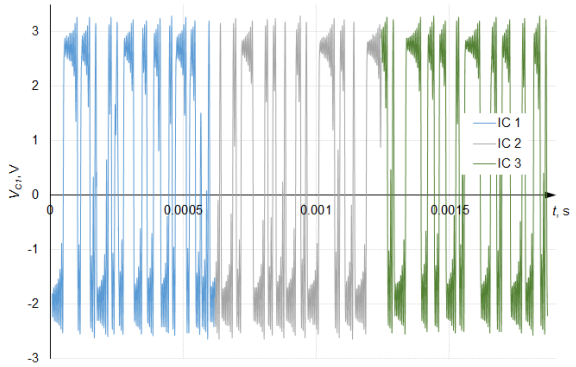


FIGURE 4.26: Signals generated by the Chua's oscillator with three different 4007-series integrated circuits.

It was found that the oscillator behaves in a very similar manner with each of the ICs. The overlaid signals can be seen in Fig. 4.26.

The equilibrium levels were scrutinised but no significant difference was observed. It should be mentioned that the equilibrium levels did appear to be different for each of the tested integrated circuits, but the slight shifts could have been caused by the distortions due to the lengthy wiring and other interference. The computer algorithm for locating the equilibria gave diverse results for each of the data series but we will refrain from claiming that this was due to fluctuations in the CMOS manufacturing process. A more careful experiment is required with prior measurements of the IC's individual FET characteristics. Nevertheless, the sensitivity of the circuit was regarded as a sign of the suitability of this candidate for the role of a CCM.

4.6 Conclusions

Performed mathematical modelling and circuit simulations helped to gain a good understanding on Chua's circuit operation and effect of its component values on the output signals. The difference in geometry of attractors for two different types of NR was pointed out.

The ideal MOSFET realisation of Chua's circuit was simulated in CAD software AWR and results of the simulation were matched by the circuit mathematical modelling done in Matlab. This showed that the developed Matlab model is valid and both ways are suitable for simulating chaotic systems. It was verified by the mathematical model that location of the equilibrium points mainly depend of the shape of NR's current-voltage characteristic.

The sensitivity of the MOSFET Chua's circuit was proven during the simulations in which linear and nonlinear parameters of the circuit's elements were varied. It was demonstrated that small changes of MOSFET parameters are noticeable in the output signals. Furthermore, comparing with the linear parameter measurements, the circuit's nonlinear signals are capable of somewhat magnifying the observable change of the circuit's device parameters. In addition, the shift of the parameters which might not be noticed during linear PCM measurements can be captured from the Chua's circuit's nonlinear signals. In conclusion it can be stated that this simulation study gives a good motivation for further investigation of the circuit's applicability for manufacturing process monitoring. It was also shown that equilibrium-voltage level is probably the most suitable characteristic of circuit's output signals for monitoring the active components' state.

Board-level prototypes of Chua's circuit allowed obtaining real-life chaotic signals which were subsequently analysed. Comparison of signals produced by the circuit with three different ICs demonstrated that circuit can be sensitive to NR's characteristic.

You'll have to forgive the crudeness of this model. I didn't have time to paint it or build it to scale

Dr Emmett Brown

5

Integrated-Circuit Design of the CCM

The proposed control method requires designing an integrated-circuit version of Chua's circuit. The idea of a CCM is that it is placed on each reticle for prediction of the performance of neighbouring circuits. Therefore it is required to come up with a design of Chua's circuit specifically for the manufacturing process in need of the control. In other words, Chua's circuit CCM has to be individually designed for a particular process the same way as normal circuits would.

The CCM circuits are to be manufactured employing two different gallium arsenide pHEMT processes. The main difference between the used processes is the gate length of the pHEMTs which is 0.10 μm and 0.15 μm. The latter process is specified as 'low-noise' with particular emphasis on LNA application.

5.1 Manufacturing Processes Overview

5.1.1 PP-10 GaAs pHEMT Process

It is essential to get familiar with the manufacturing process before attempting an integrated circuit design. Circuit designer utilises the transistor models provided in a process design kit (PDK) by the manufacturer . A PDK would also normally include models of passive structures such as resistors, capacitors and inductors. The described design utilised PDKs provided by WIN Semiconductors, as the fabrication was to take place on their facilities.

The development of the circuit is carried out in AWR Environment as in the previous simulation studies. The PDKs are imported in the CAD and scalable transistor models are simulated to obtain their current-voltage characteristics.

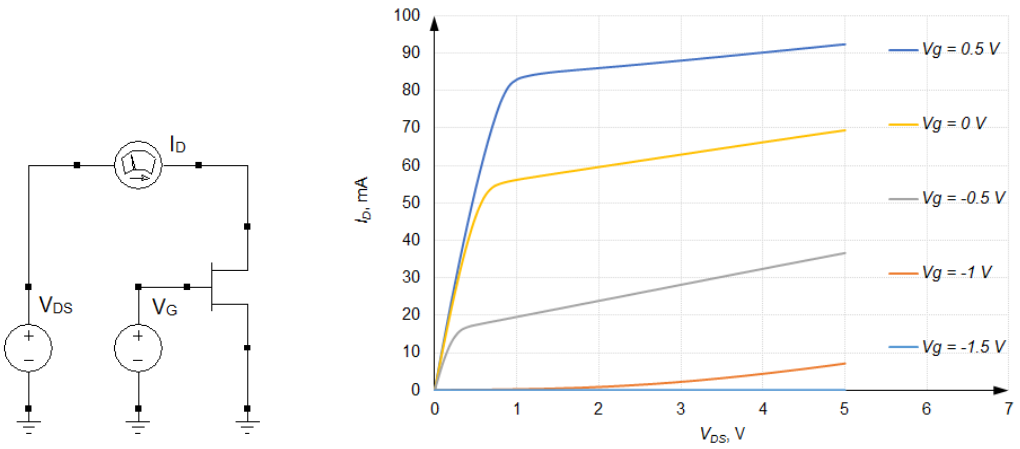
One of the features of pHEMTs, distinguishing them from regular silicon MOS devices, is that they have non-zero drain current when the gate voltage is not applied (see Fig. 5.1). It can also be seen that the transconductance of these transistors is very high.

The PDK of the process, coded as PP-10, included the scalable transistor models. The devices produced are 0.10 μm AlGaAs/InGaAs depletion-mode (D-mode) pHEMT transistors with f_t of 135 GHz, transconductance of 725 mS/mm and breakdown at 9 V.

The amount of current carried by a pHEMT device at fixed bias depends on their unit gate width UGW. It is evident that a device with a greater gate width can carry more current as seen in Fig. 5.2.

5.1.2 PL-15 GaAs pHEMT Process

The second design is to be implemented employing WIN's 0.15 μm low-noise InGaAs pHEMT manufacturing process, PL-15. The difference between the PP-10 and PL-15 processes can be confirmed from the characteristics of the pHEMTs. The lower



(a) Simulation setup

(b) Family of pHEMT output characteristics for a 50 μm UGW pHEMT

Figure 5.1: The simulation of the PP-10 pHEMT output characteristics.

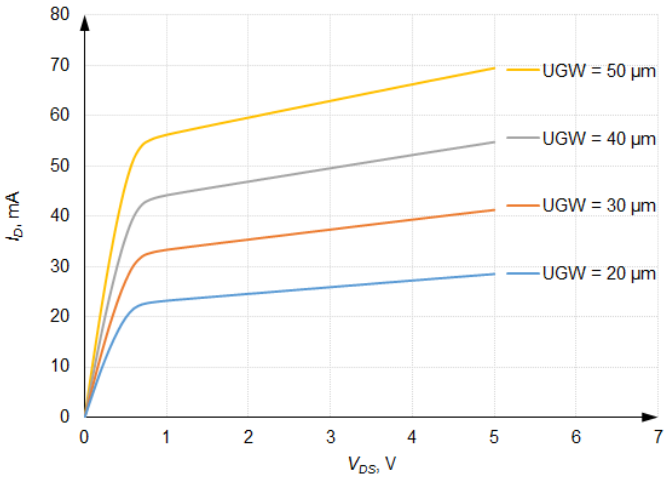


Figure 5.2: The simulation of the PP-10 pHEMT output characteristics with variable unit gate widths (UGW) with $V_G = 0$ V.

transconductance and higher pinch-off voltage of the PL-15 pHEMTs can be seen from the simulated characteristics shown in Fig. 5.3.

The PL-15 process design kit (PDK) allows modifying the width of the pHEMT channel by changing the unit gate width (UGW) and by changing the number of fingers (NOF). The multifinger design involves dividing a large transistor into a number of smaller ones connected in parallel, which helps to use the area more efficiently. By

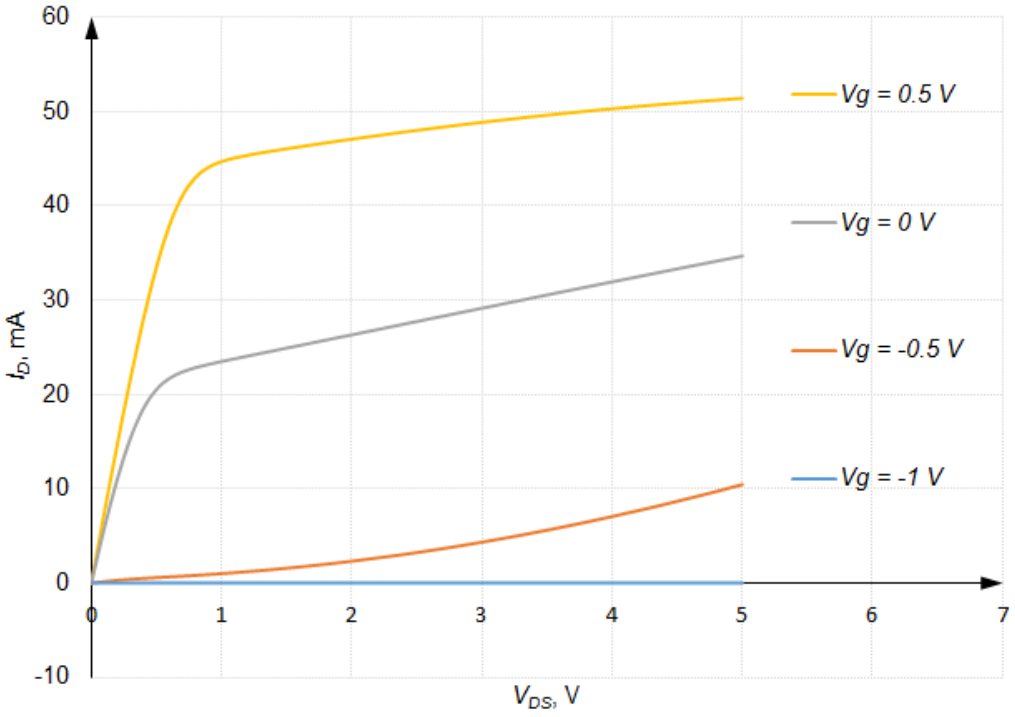


FIGURE 5.3: The simulation of the PL-15 pHEMT output characteristics for a 50 μm UGW.

choosing the number of fingers and the gate width appropriately, an overall transistor width and height can be specified to better fit the layout. The comparison between the layouts of two equivalent pHEMTs with 400μm gate width is shown in Fig. 5.4.

5.2 Circuit Design

The development of the CCM for the both described processes is discussed in the following sections.

5.2.1 Nonlinear Resistor

The first and main challenge of designing Chua's circuit using pHEMTs is the selection of the nonlinear resistor implementation. In the previously simulated circuit the NR was constructed using CMOS transistors connected in a way to form two cross-coupled

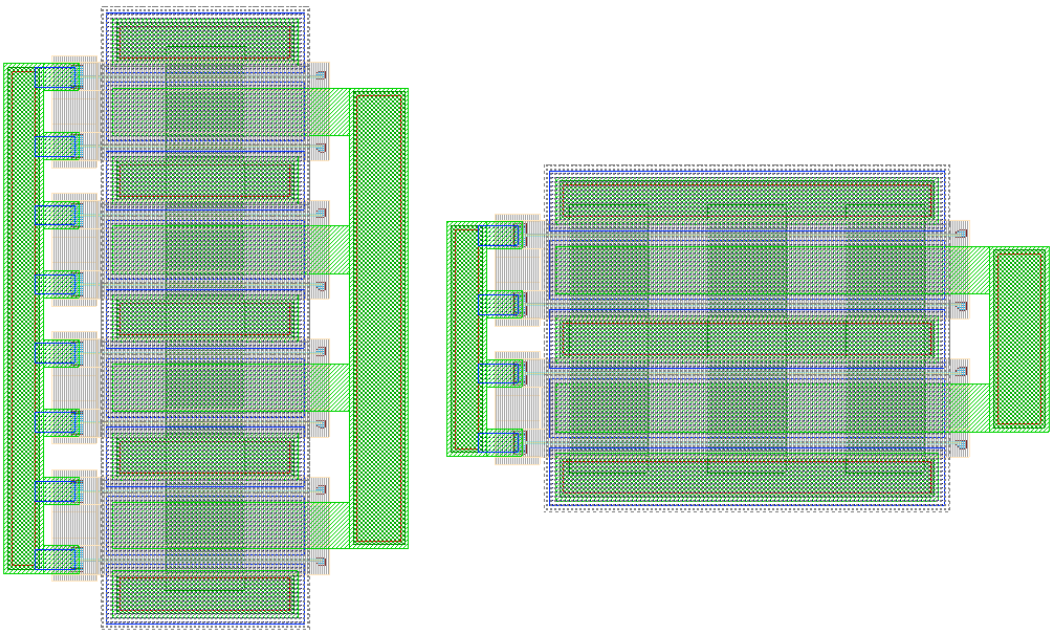


Figure 5.4: The layouts (same scale) of two equivalent PL-15 pHEMTs: 8 finger by 50 μm (left) and 4 finger by 100 μm (right).

inverters. However pHEMTs can not be manufactured as complementary pairs, therefore the design of the inverters has to be reconsidered.

The first step in constructing the nonlinear resistor using pHEMTs is to evaluate the available inverter implementations which employ transistors of only one conductivity type. Secondly, the cross-coupling of these inverters has to result in a current-voltage characteristic which has a negative slope at the origin. At the same time, the slope has to be comparable to the slope of the load line, that is $-1/R$.

After careful selection, we choose to use the saturated-buffer FET logic inverter approach [104]. The schematic of a generic pHEMT saturated-buffer inverter is shown in Fig. 5.5. During the inverter operation, the input signal arrives at the gate of the switch transistor, and the pull-up transistor acts as an active load. The inverted signal appears on the switch's drain, however it becomes shifted into the positive voltage region and therefore needs to be downshifted. That action is performed by the source follower with a pull-down transistor being an active load and the diode acting as a level shifter.

The nonlinear resistor contains two identical inverters. The goal of the inverter

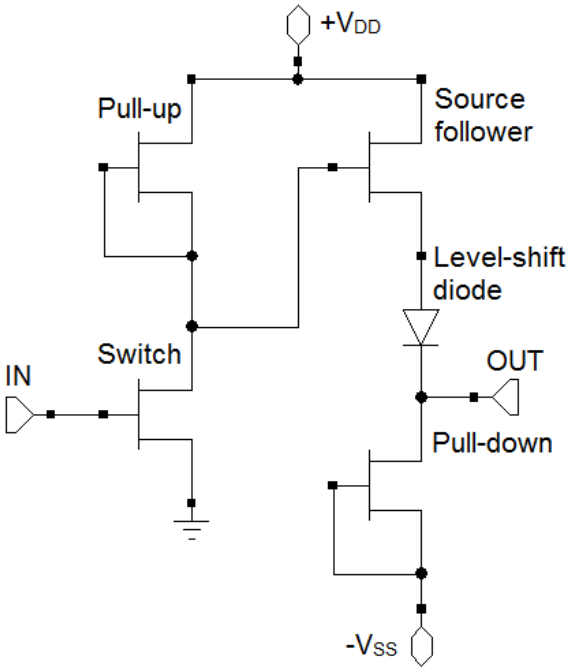
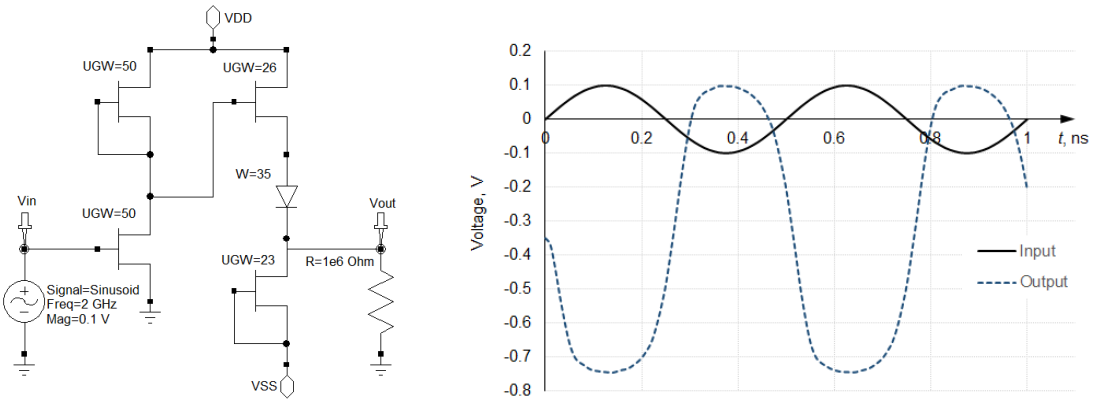


FIGURE 5.5: Schematic diagram of the saturated-buffer logic inverter.

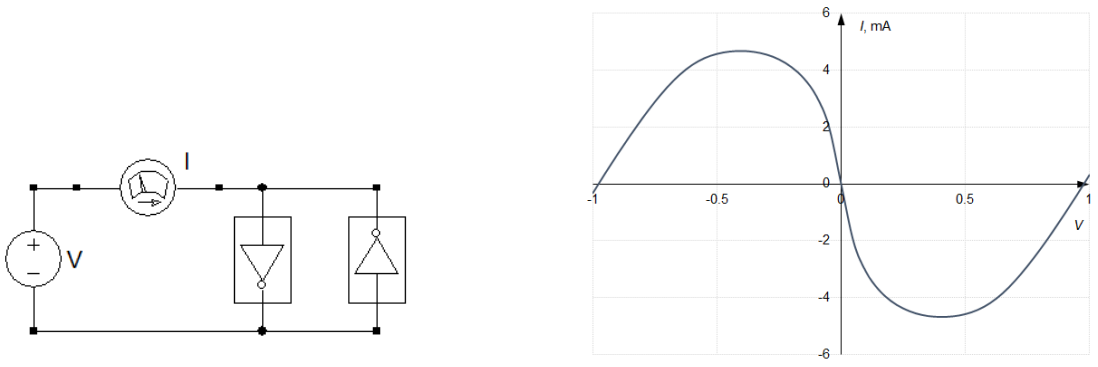
design is to generate a circuit which inverts the input signal and shifts its level in such a way that, in a cross-coupled configuration, when the output of the first inverter is connected to the input of the second, the resulting current-voltage characteristic has a negative conductance region with an acceptable incline. This incline, as discussed before, is defined by the value of the linear resistor R. It is desirable to keep this value high enough because small resistors are more vulnerable to the TFR size and sheet-resistance fluctuations. Our goal is to minimise the influence of R variation on the circuit's performance.

The inverter designed in PP-10 is shown in Fig. 5.6 with the gate widths of the devices included. The response of this inverter to a sinusoidal signal of 2 GHz frequency and 0.1 V amplitude, measured on a 1MΩ load resistor, is shown in Fig. 5.6(b). In this simulation the bias conditions were the following: $V_{DD} = 2.2$ V and $V_{SS} = -2.2$ V. It can be seen that the output signal is shifted down relative to the input. If we connect the output of one inverter to the input of the second and the output of the second to the input of the first, as shown in Fig. 5.7(a), and use these connections as



(a) Inverter schemtic (b) Family of pHEMT output characteristics

Figure 5.6: Time-domain simulation of the inverter for the PP-10 process.



(a) Cross-coupled-inverter simulation setup (b) Current-voltage characteristic

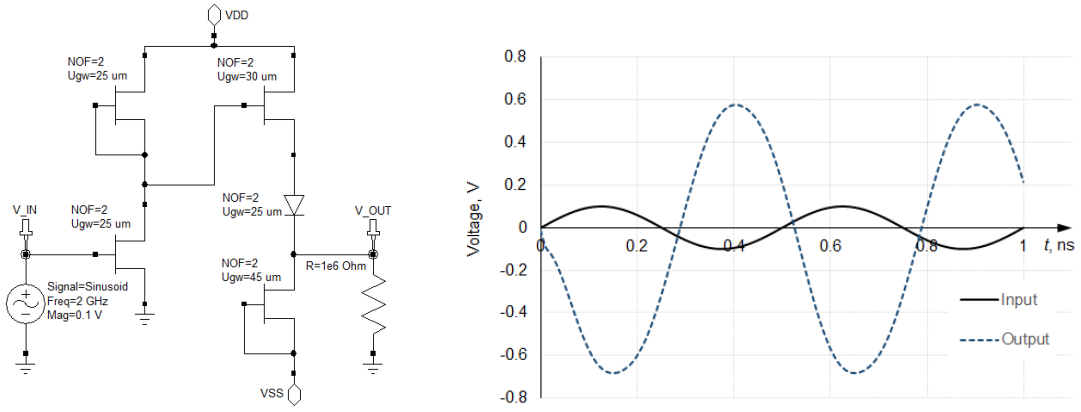
Figure 5.7: Simulation of the PP-10 cross-coupled-inverters nonlinear resistor configuration.

the terminals of the NR we can perform its simulation. The resultant current-voltage characteristic for the same V_{DD} and V_{SS} of 2.2 V is displayed in Fig. 5.7(b).

It can be seen that the obtained characteristic of the developed nonlinear element is smooth, however polynomial functions describe this curve quite poorly. The Eureqa software generated the following function:

$$g(V) = 5.46 \times 10^3 (V^2)^{(0.00119V)} - 5.46 \times 10^3 \text{ [mA]} \tag{5.1}$$

The incline of this characteristic at the origin equals approximately –21.8 Ω and sets the lower limit (ignoring the '–' sign) on the circuit's linear resistor R. We remember



(a) Inverter schemtics

(b) Inverter input and output voltages

FIGURE 5.8: Time-domain simulation of the inverter for the PL-15 process.

referring to section 3.1.2 that the load, $-1/R$, has to intersect the current-voltage characteristic of the NR somewhere in its negative-conductance region. Therefore the highest R value corresponds to the load line crossing the $g(V)$ function at its maximum which occurs at ≈ -0.4 V. This conductivity correspond to the R value of 85.7 Ω. Thus we have a range of 21.8 Ω to 85.7 Ω to choose the R value from. However it should be stated that this range can be adjusted by the change of the bias voltages. Now, as the proposed design of the inverter has proven its viability, the development of the passive part of Chua's circuit can take place.

The PP-10 inverter design can not be considered fully successful as the shape of the output is not linear relative to the input. And although cross-coupling resulted in a good shape of current-voltage characteristic the issue of inverter nonlinearity is addressed in the PL-15 design. The schematic of the inverter implemented for the PL-15 process is shown in Fig. 5.8(a) and the simulated performance of this inverter is shown in Fig. 5.8(b). It can be seen that the designed circuit has a more linear performance than the one from the first circuit implementation.

The PL-15 nonlinear resistor is also constructed by cross-coupling two identical inverters. Both bias voltages, V_{DD} and V_{SS}, were increased to 3 V. The resultant current-voltage characteristic is shown in Fig. 5.9. It can be seen that the shape has changed. The mathematical formula describing this current-voltage relationship was

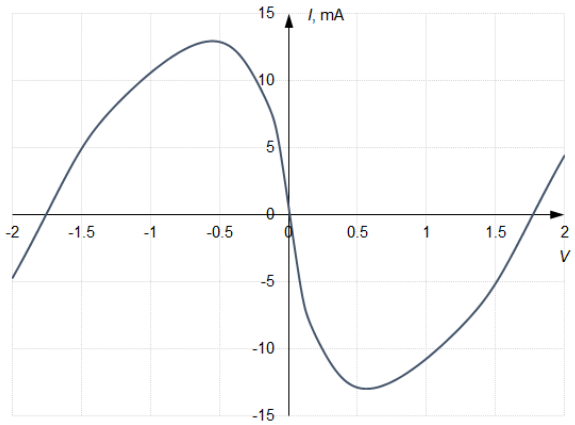


Figure 5.9: Current-voltage characteristic of the PL-15 cross-coupled inverters.

obtained through Eureqa curve-fitting function:

$$g(V) = 1.67V^3 + \frac{0.0649V + V^3}{-0.000847 - 0.0318V^2 - 0.0487V^4} - 0.0828\ [\text{mA}] \tag{5.2}$$

The conductivity of NR at the origin is approximately $-14\ \Omega$ and incline of the load line when it intersects the maximum and minimum of the current-voltage function is $-42.8\ \Omega$. Thus the range of values for the linear resistor R spans from $14\ \Omega$ up to $42.8\ \Omega$. It is again worth mentioning that the incline of current-voltage characteristics can be modified in a certain range by changing the bias voltage.

5.2.2 Resonator Design

Both, the PP-10 and PL-15 process design kits include spiral and square inductors of fixed inductance values, metal-insulator-metal (MIM) capacitors and thin-film resistors (TFR), the values of which are defined by their dimensions. The resistivity of the TFR layer is given as $50\ \Omega/\square$, and the capacitance density of the MIM structure is given as $400\ \text{pF/mm}^2$ for the both processes. The necessary values of resistors and capacitors are obtained by selecting proper sizes of the TFR or MIM elements.

The first step in the resonator design involves the choice of linear resistor's R value. According to the previously stated PP-10 limitations, the value of $29.43\ \Omega$ was

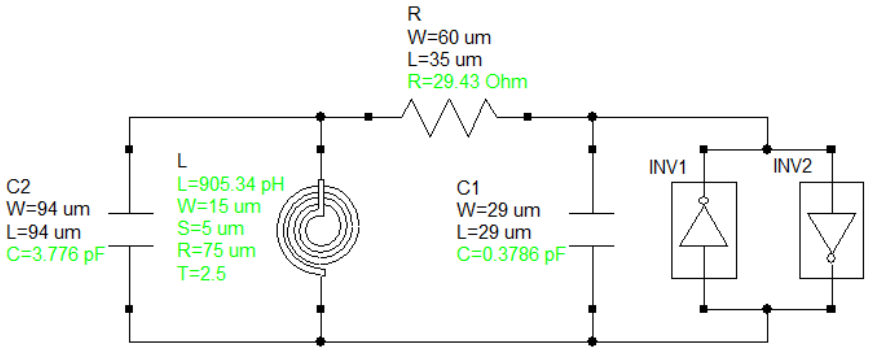


FIGURE 5.10: Schematic diagram of Chua's circuit for the PP-10 GaAs process.

chosen, which corresponds to 35 μm long and 60 μm wide TFR structure. It is known, that certain ratios have to be maintained between the values of the Chua's circuit components to ensure the chaotic behaviour. The value of the coefficient β (3.13) is normally supposed to be in the region of 2-20, while the standard value of α (3.12) is close to 10. Based on these restrictions it is possible to choose appropriate inductor and capacitor values. One should note that the choice of L and C define the frequency of operation of Chua's circuit in the same way as in a harmonic oscillator case.

We aim to use smaller-value reactive components for two reasons. First, and most obvious, is that the size of the circuit has to be minimised in order to meet the CCM requirements. Secondly, smaller C and L values correspond to higher resonant frequencies and we presume that a high-frequency oscillator, having a higher degree of nonlinearity, would be more sensitive to the process fluctuations.

The capacitive MIM structures used in this design has a square shape with the sides for the C_1 capacitor equal to 29 μm and for C_2 equal to 94 μm. The resultant capacitances are 0.3786 pF and 3.776 pF respectively. The spiral inductor is selected from the available designs in the PDK and its value is 905.34 pH. Therefore the dimensionless coefficients of the circuit were calculated to have the following values:

$$\alpha = 9.974 \tag{5.3}$$

$$\beta = 3.613$$

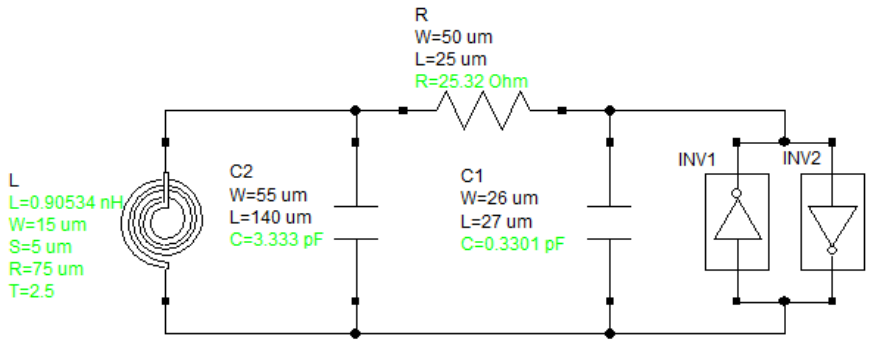


Figure 5.11: The schematic diagram of Chua's circuit for the PL-15 GaAs process.

The schematic of the PP-10 Chua's circuit with the values of its components is presented in Fig. 5.10.

Similarly, in the case of PL-15 design, the linear resistor is chosen from the range specified by the shape of the NR current-voltage characteristic. The inductor is selected from the cells available in the PDK and the capacitor values are specified to maintain the necessary ratios. The linear resistor is 50 μm by 25 μm in size resulting in 25.32 Ω resistance. The capacitors have dimensions of 26 μm by 27 μm and 55 μm by 140 μm giving the capacitance of 0.3301 pF and 3.333 pF respectively. The spiral inductor value did not change and remained 905.34 pH. The dimensionless coefficients of this Chua's circuit are the following:

$$\alpha = 10.097 \tag{5.4}$$
$$\beta = 2.36$$

The schematic of the PL-15 version of Chua's circuit is shown in Fig. 5.11. One can find that the schematic of the circuit did not change significantly. However a more careful selection of the transistor gate widths resulted in a more linear response of the inverter, which did not distort the input sinusoidal wave considerably and produced almost no level shift. Presumably, a better performance of the inverters resulted in improved functioning of the NR leading to a more stable overall operation.

Both circuits are simulated in AWR to check their functionality. Time-domain simulations of the capacitor voltages are done employing the APLAC transient simulator. Same as in the case of MOSFET circuit, trapezoidal method of solving differential equations was employed, signals were simulated for 10 ns with 0.02 ns step.

These simulations showed that the designed Chua's oscillators are capable of generating chaotic signals for a range of bias voltages. In addition, the circuits are tested for the ability to operate in chaotic mode for a range of the passive resistor's R values.

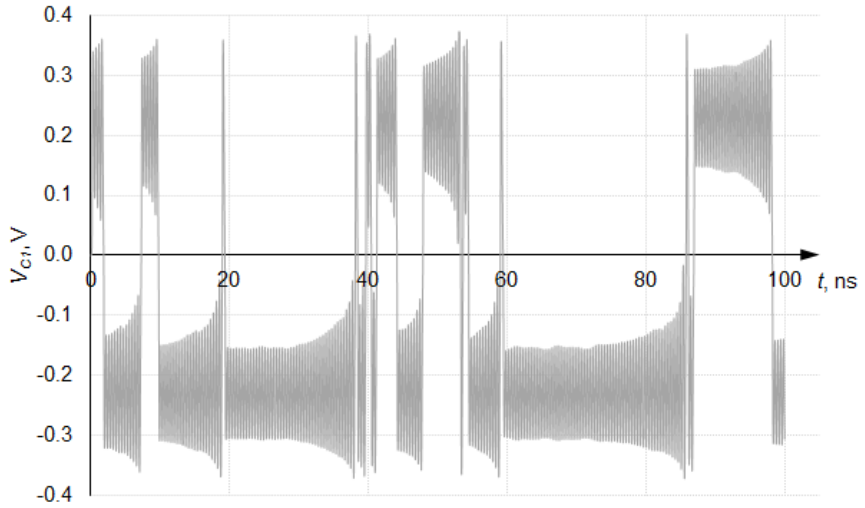
For the PP-10 implementation the capacitor-voltage oscillations in the time domain are shown in Fig. 5.12. We can clearly see the chaotic-type oscillations of the voltages and if we embed them in a phase space, i.e. plot them one versus the other (Fig. 5.13), we can observe the chaotic attractor, a telltale sign of chaos.

The PL-15 implementation is simulated as well and the results of the capacitor-voltage simulations are shown in Fig. 5.14. When these signals are embedded into a phase space the chaotic attractor could be observed, as shown in Fig. 5.15. Thus both designs were shown to be operational and capable of producing chaotic signals.

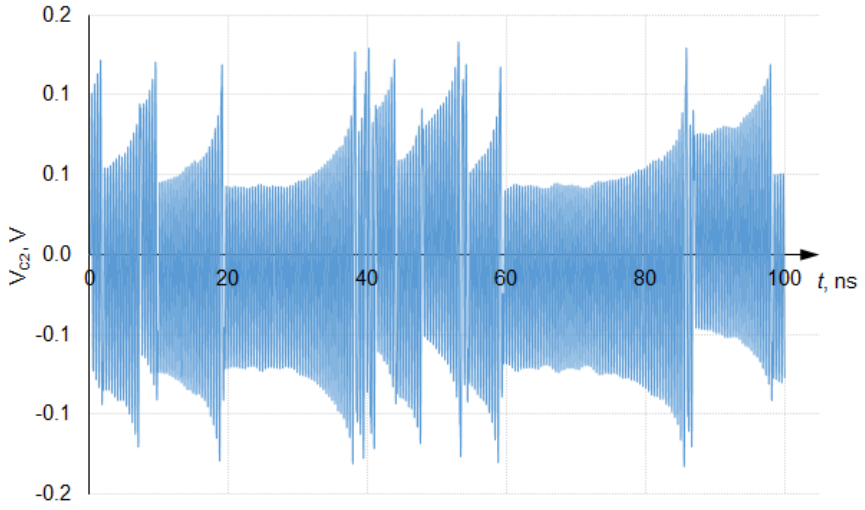
5.2.3 Circuit Layout

The next step in preparing the circuit for fabrication is the generation of the layout: how components and the interconnections between them are actually going to look on the semiconductor substrate. AWR Design Environment offers the layout tool which is used in this project.

The main goal of the layout generation is the development of a working circuit, that occupies as little area as possible, but at the same time does not violate the process design rules. The design rules for a particular process define the minimum sizes of the elements for each layer. For example, there exists a minimum width of a metal line and minimum distance between adjacent metal lines. The minimal dimensions are usually limited by the lithography process.



(a) C_1 voltage in the time domain



(b) C_2 voltage in the time domain

Figure 5.12: Simulation of the PP-10 circuit's signals in the time domain.

Keeping in mind all the limitations during the layout procedure is important; fortunately, a design rule file for a process can be imported into AWR for an automated search for errors. Another feature that helps to avoid mistakes in the layout is the 'layout versus schematics' (LVS) check. This option helps in finding mismatches between the schematic file and the layout by locating missed or extra, unnecessary electrical connections.

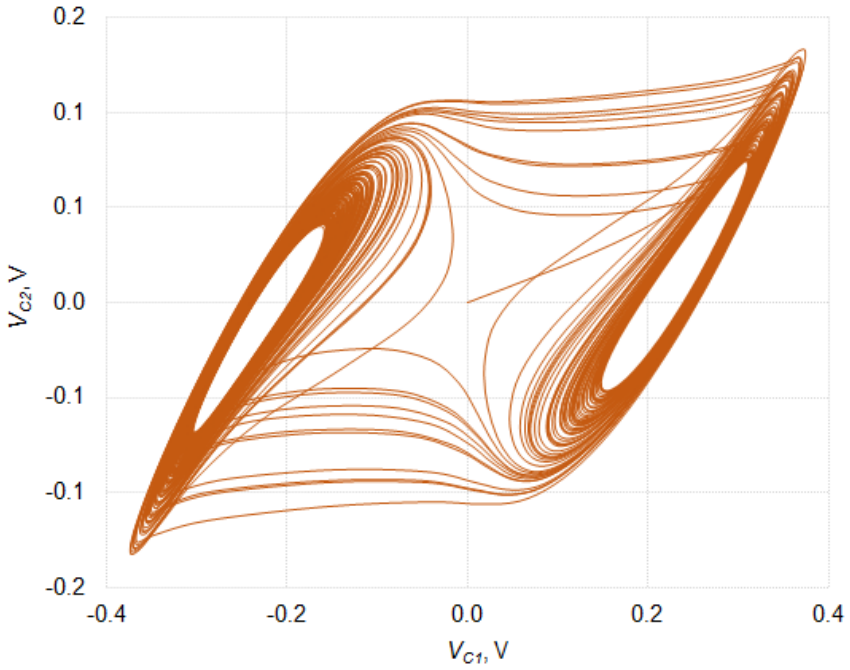
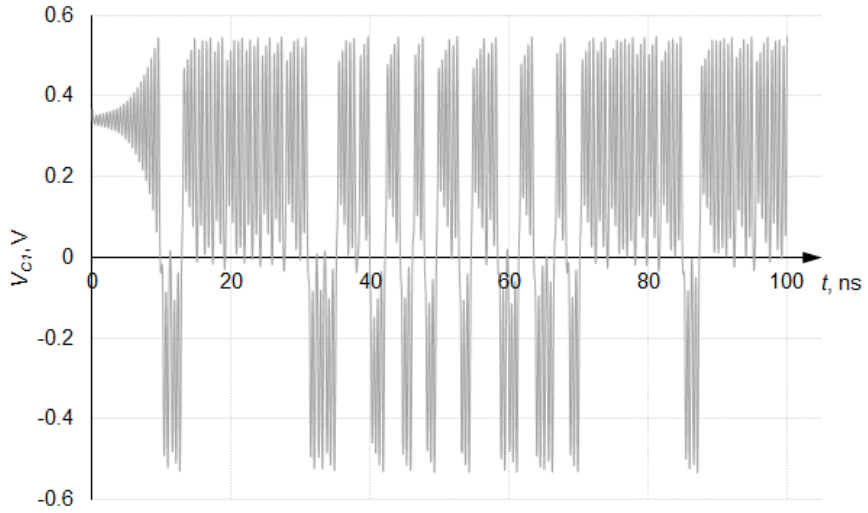


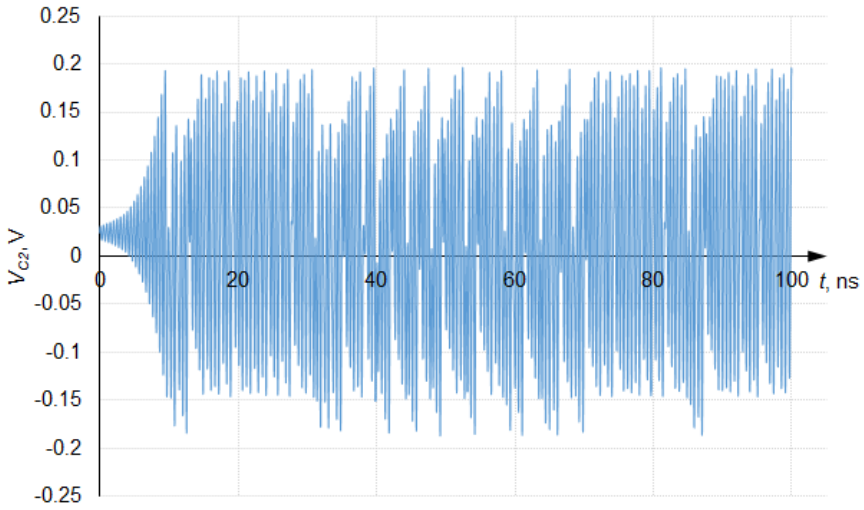
FIGURE 5.13: The chaotic attractor observed during the PP-10 design simulations.

Circuit layout design is an iterative process when the desired performance is achieved by multiple modifications and improvements of the drafts. The final version of the PP-10 layout is shown in Fig. 5.16. There are two pairs of DC pads for bias-voltage application and two RF pads connected to capacitors C_1 and C_2 for monitoring their voltage. On the left-hand side of the layout we can see the circuit's passive part: two MIM capacitors, the spiral inductor and the TFR resistor. The right-hand side of the layout contains the nonlinear resistor made of eight pHEMTs and two pHEMT diodes.

The PDK allows using two metal layers for the interconnections. They can be used separately or as a stack. However it is important to keep in mind the maximum allowed current densities for every line. The widths of the metal lines have to be adjusted according to the maximum expected current. The data on sheet resistivity and current limits of selected layers are shown in Table 5.2.3. Obviously, a stacked metal line is capable of conducting more current per unit width than each of the metal layers separately. Thus, in most cases, stacked metal 1 and metal 2 were used for the interconnection. It was also necessary to use the metals separately to construct the so-called air bridges when the crossing of two lines was inevitable. The air bridge



(a) C_1 voltage in the time domain



(b) C_2 voltage in the time domain

Figure 5.14: Simulation of the PL-15 circuit's signals in the time domain.

construction involves laying one metal (metal 2) line on top of the other (metal 1), separating them by the so-called span layer. The challenge of the layout design is to avoid intersections if possible and if it is not, the air bridges have to be constructed in a way to ensure as less parasitic influence as possible. One should keep in mind that an air bridge effectively adds certain amount of parasitic capacitance between the crossing conducting lines.

The final design occupies a rectangular area on the wafer with the sides 1050 μm by

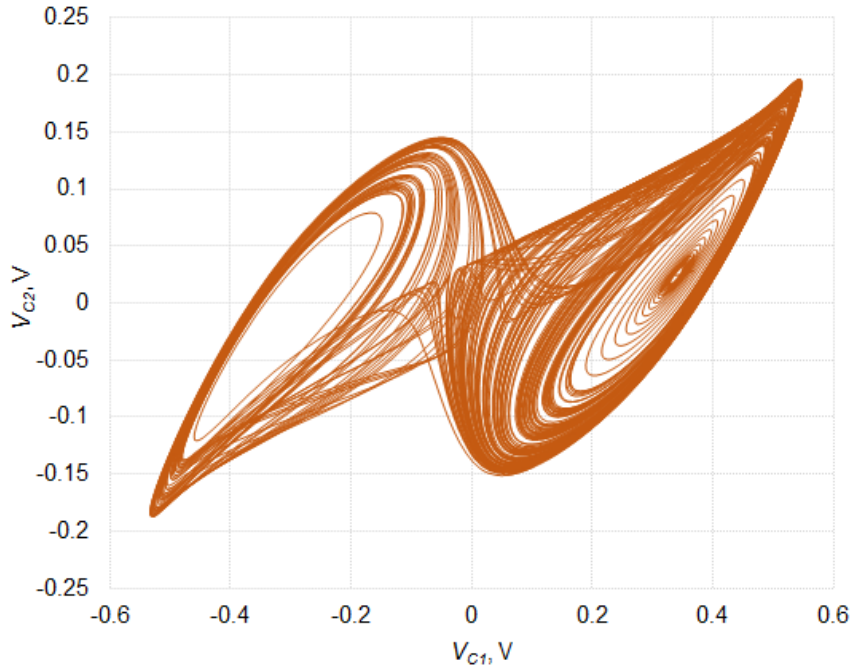


FIGURE 5.15: The chaotic attractor observed during the PL-15 design simulations.

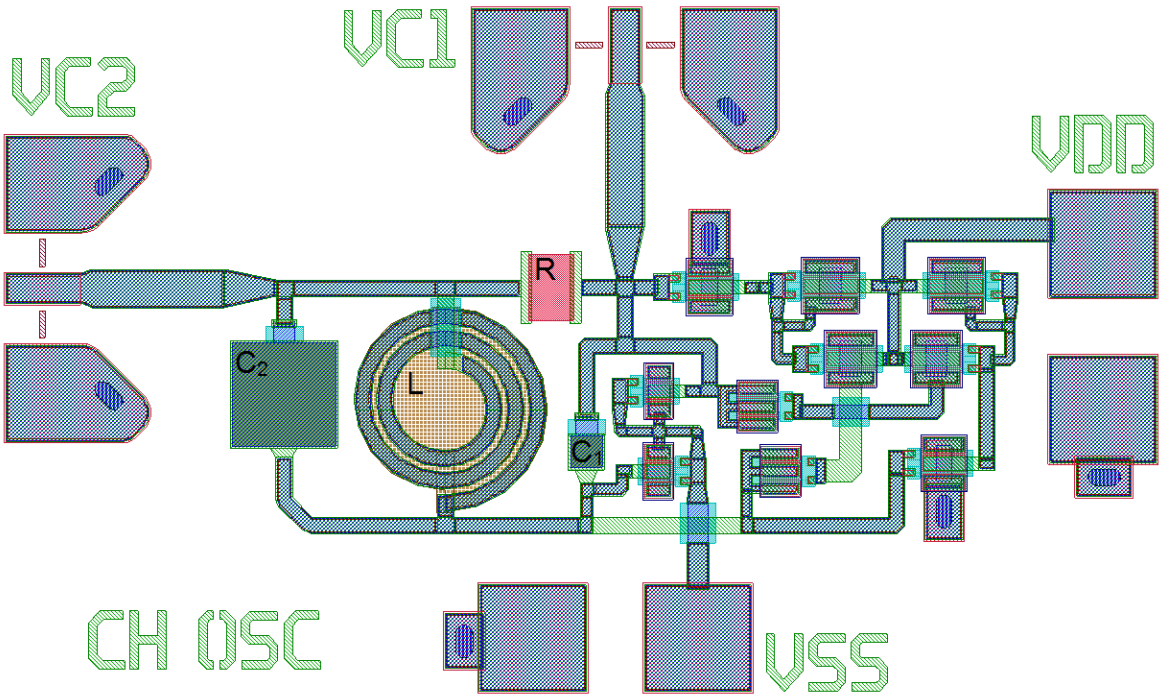


FIGURE 5.16: The layout of Chua's circuit designed for the PP-10 manufacturing.

Layer	Resistivity ($\Omega/\square$)	Current density limits (mA/μm)
Thin film resistor (TFR)	50	1.0
Metal 1	0.03	4.0
Metal 2	0.02	6.0

Table 5.1: PP-10 process conductive layer characteristics.

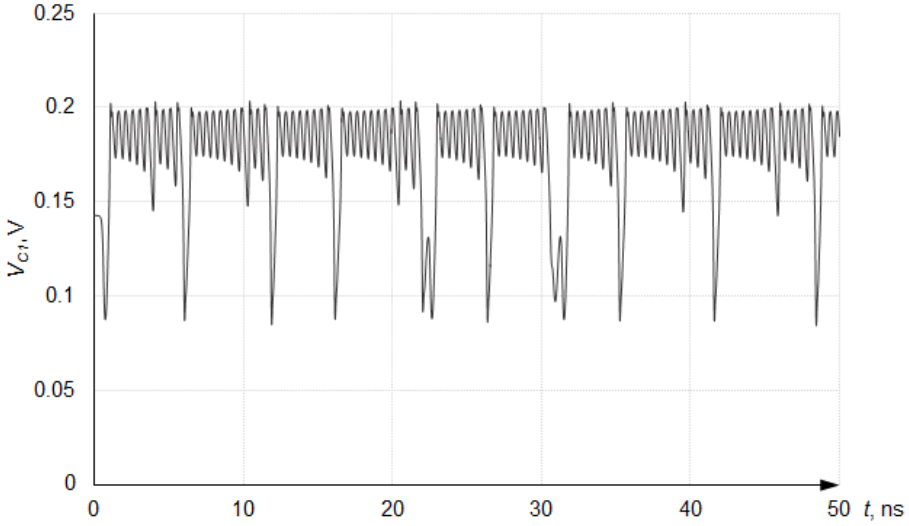


Figure 5.17: Simulated C_1 voltage of PP-10 circuit with inclusion of the EM effects.

625 μm. However the dimensions of the circuit excluding the pads are approximately 720 μm by 300 μm.

After all the circuit elements were laid out and interconnected, the circuit is subject to electro-magnetic simulation (EM simulation). The purpose of this procedure is to include all the effects of the metal conducting lines and their couplings to ensure the circuit's functionality when it is produced. Thus all the metal lines, extracted with an EXTRACT element, are to be simulated in the EM simulator for inclusion of their effect in the circuit's performance as the EM document is reintegrated back into the schematic. AXIEM simulator was used in this procedure. This simulator produces 3D planar full-wave solutions to Maxwell's equations [105].

The results of this simulation for the PP-10 circuit in terms of the C_1 voltage are

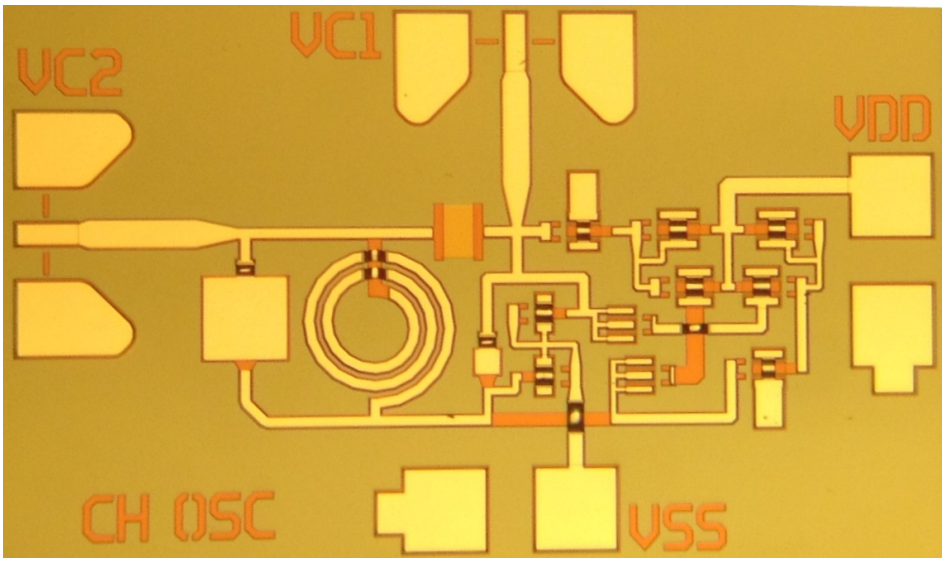


FIGURE 5.18: Microphotograph of the manufactured Chua's circuit layout on the PP-10 wafer.

presented in Fig. 5.17. As can be seen, the signal appears to be chaotic; however it is different from the circuit simulation results, shown before. The first reason for the difference is that different measurement component was used. The previous results were obtained from the AWR measurement component V_METER. The two voltage meters were connected in parallel with capacitors C_1 and C_2 to obtain the voltage across them. However, in the EM simulations, a 'Measurement Probe' M_PROBE was used. This component presents the voltage at the point of its placement relative to the ground potential. The capacitors were not connected to ground, therefore the results of the two measurements are different, yet qualitatively the same. Here it should be mentioned that the RF pads connected to the capacitors also allow voltage measurements only relative to ground. This means that the M_PROBE measurements indicate the results that are expected in the measurements.

The layout was included on the mask-set to be subsequently manufactured at the WIN Semiconductors' facilities. The production results were provided as three quarter-wafers. The outcomes of the fabrication can be seen in Fig. 5.18.

Based on the PP-10 layout experience, a layout of the PL-15 implementation is generated. The improved Chua's circuit CCM design is depicted in Fig. 5.19. A

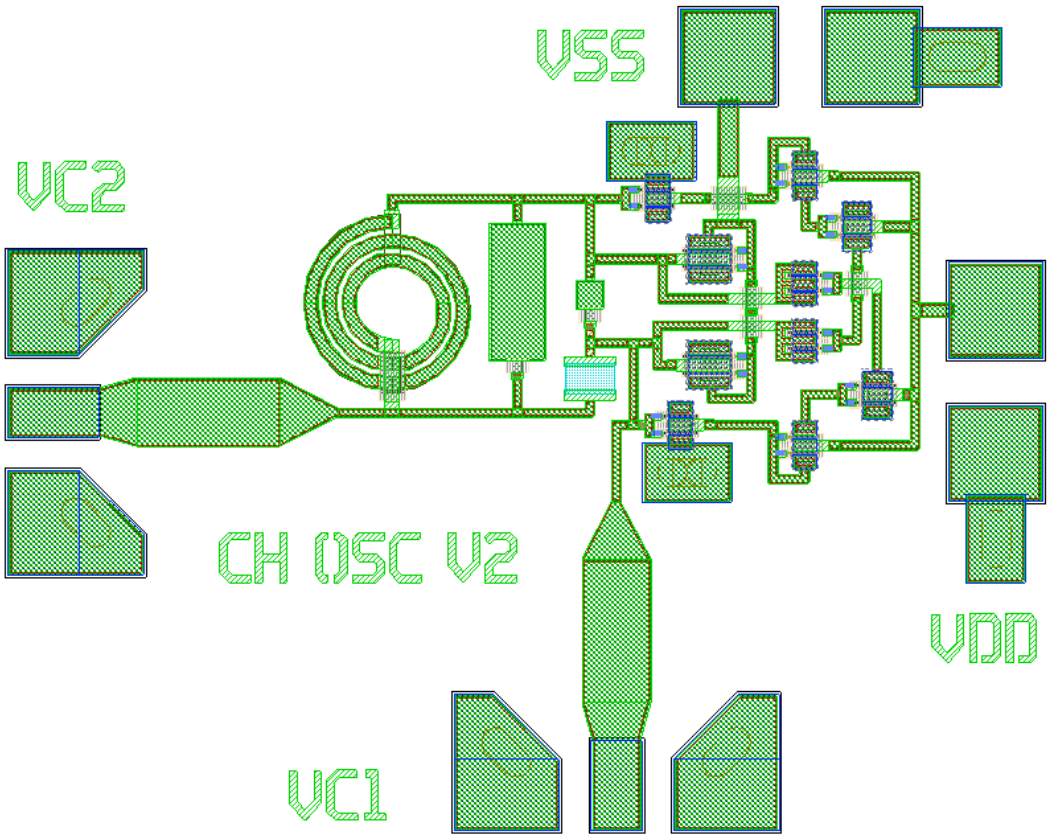


Figure 5.19: The layout of Chua's circuit designed for the PL-15 manufacturing.

number of modifications are made to this layout. The shape of the MIM capacitors was changed from square to rectangular for a more efficient area utilisation. At the same time, the layout of the nonlinear resistor was completely revised to make the inverters look like a mirror image of one another for the purpose of achieving a better symmetry. The developed layout passed all the LVS and DRC checks.

The presented layout also was subject to EM simulations, the C_1 capacitor voltage is simulated using the M_PROBE component thus finding the potential relative to ground. The simulation results are depicted in Fig. 5.20. The capacitor voltage is presented in the time domain and the signal's chaotic nature is evident. The outcomes of the EM simulation were considered acceptable for the layout to be included in the PL-15 tapeout. The final design had the dimensions of 1090 μm by 865 μm, with the actual circuit excluding the pads being approximately 645 μm by 400 μm in size.

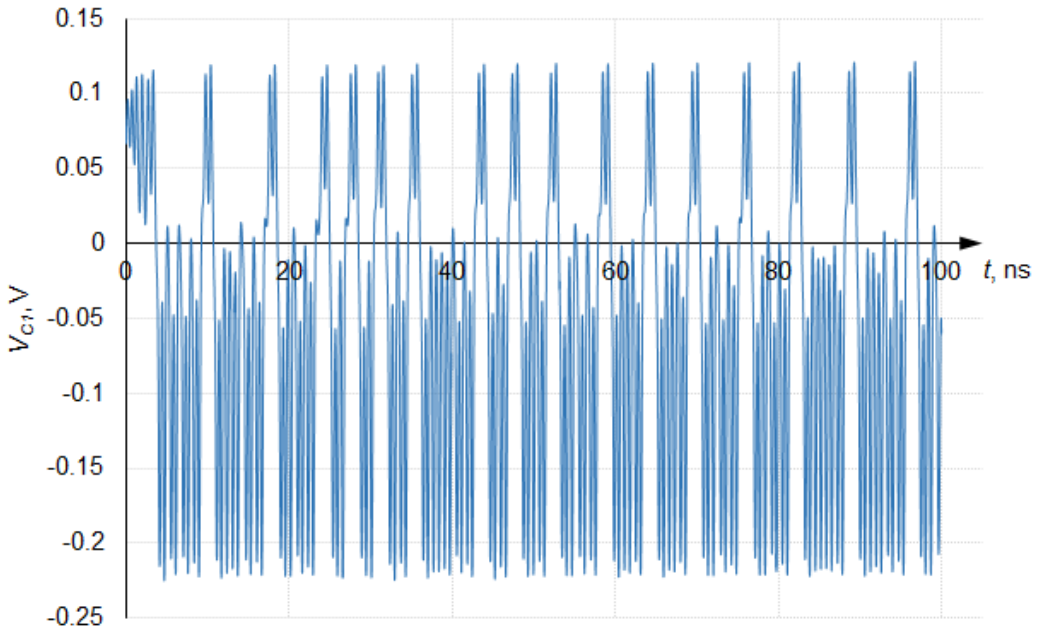


FIGURE 5.20: Simulated C_1 voltage of PL-15 circuit with inclusion of the EM effects.

Here it should be noted that, by the end of the project the author has realised the strong points of measuring the voltage across the capacitors as opposed to measuring the capacitor potentials relative to the ground. Should another version of this CCM candidate be required, this issue will be taken care of. This would involve a redesign of the RF pads because conventional RF pads have connections to ground.

The circuit was manufactured on WIN Semiconductor's foundry employing the low-noise pHEMT gallium arsenide PL-15 manufacturing process. The photograph of the manufactured second version of Chua's circuit is shown in Fig. 5.21.

The manufactured wafers were treated by three different kinds of wafer-level packaging materials. The applied compounds were Polybenzoxazol (PBO), Benzocyclobuten (BCB) and partial EMR adhesive [106]. In what follows, the 3 quarter-wafers were available for the measurements, one with each wafer-level packaging material. Later in the text, the wafers will be referred to by the denominations of the polymers, namely BCB, PBO and EMR.

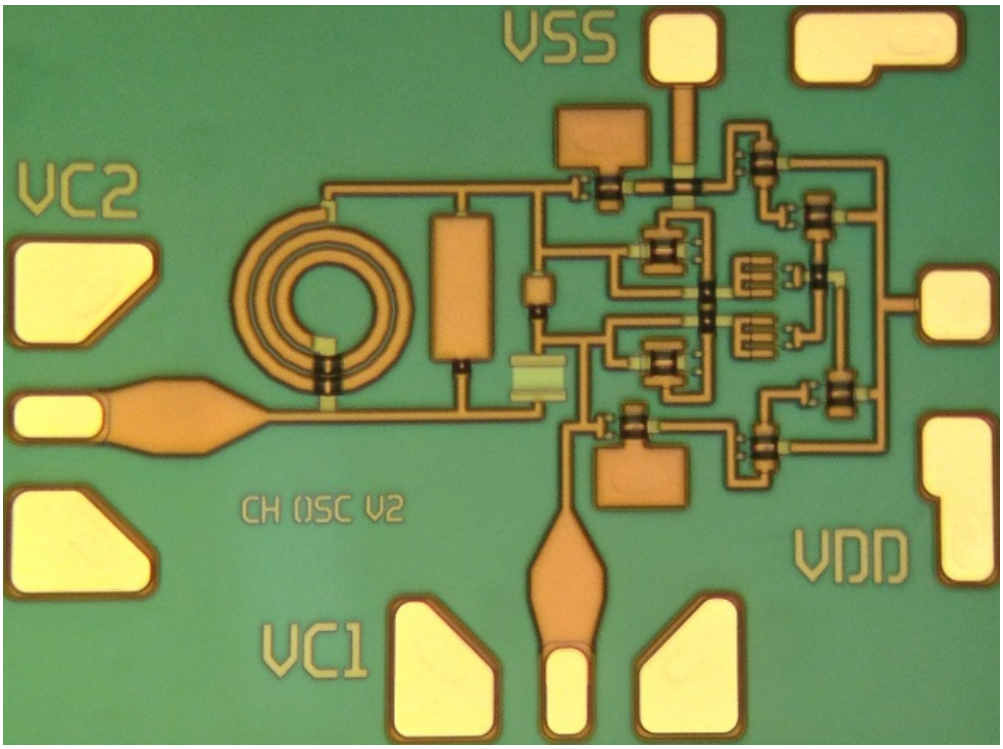


Figure 5.21: Microphotograph of the manufactured Chua's circuit layout on the PL-15 wafer.

5.3 Conclusions

Two versions of Chua's circuit were designed for implementation in two different GaAs pHEMT processes. A new realisation of the NR employing saturated-buffer-logic cross coupled inverters was designed which was motivated by the lack of complimentary logic in pHEMT. Circuit simulations proved the functionality of both designs – chaotic oscillations were observed in both cases.

The main challenge of the NR design was to overcome high transconductance of PP-10 and PL-15 pHEMTs. Normally an advantage, for the purpose of nonlinear element design, this fact impeded obtaining the NR's current-voltage function with an incline at the origin, corresponding to a realistic and high enough value of linear resistor.

Both circuits were fabricated by WIN Semiconductors and were available for the measurements as quarter-wafers.

Measure what is measurable, and make measurable what is not so.

Galileo Galilei

6

CCM Testing

The manufactured circuits were provided for the measurements as quarter sections of the produced wafers. Thus it was possible to explore the variation of circuit's performance not only from reticle to reticle but also from wafer to wafer.

6.1 PP-10 Measurements

The manufactured circuits are measured on-wafer. The testing setup involves a probe station (Fig. 6.1) consisting of a vacuum chuck for holding the wafer, four probe holders and a microscope for correct placement of the probes. One Instek PST-3202 programmable power supply (Fig. 6.2) is used for biasing the oscillators. An Agilent Technologies DSO9104A oscilloscope is used for taking the time-series data.

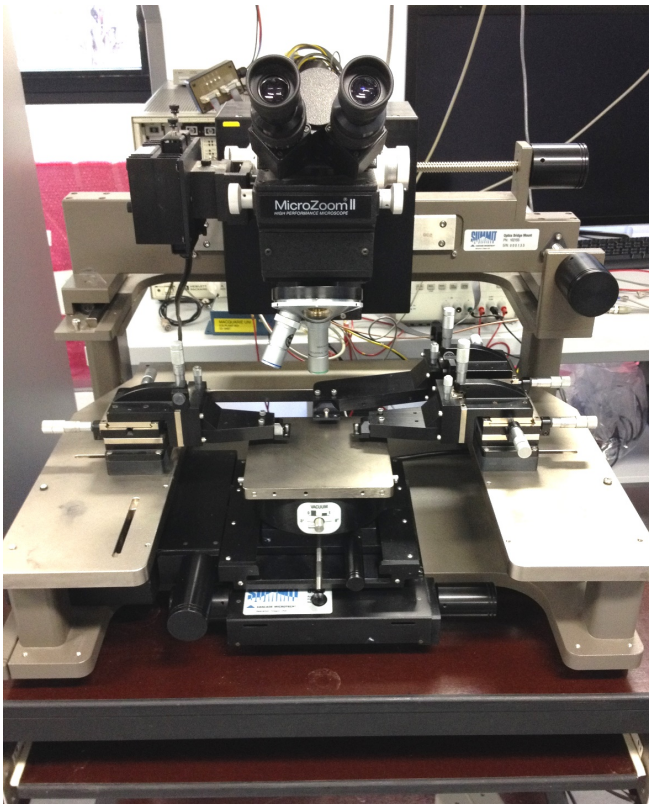


Figure 6.1: The probe station with three probe holders mounted.

Figure 6.2: Instek DC voltage source

A pair of DC probes is used to connect the circuit to a DC power supply, and one RF probe is used to read the capacitor voltage. The initial tests showed that the circuit performs differently from what was expected after the simulations. The signals generated by the circuit did not match the simulated ones for any value of the positive

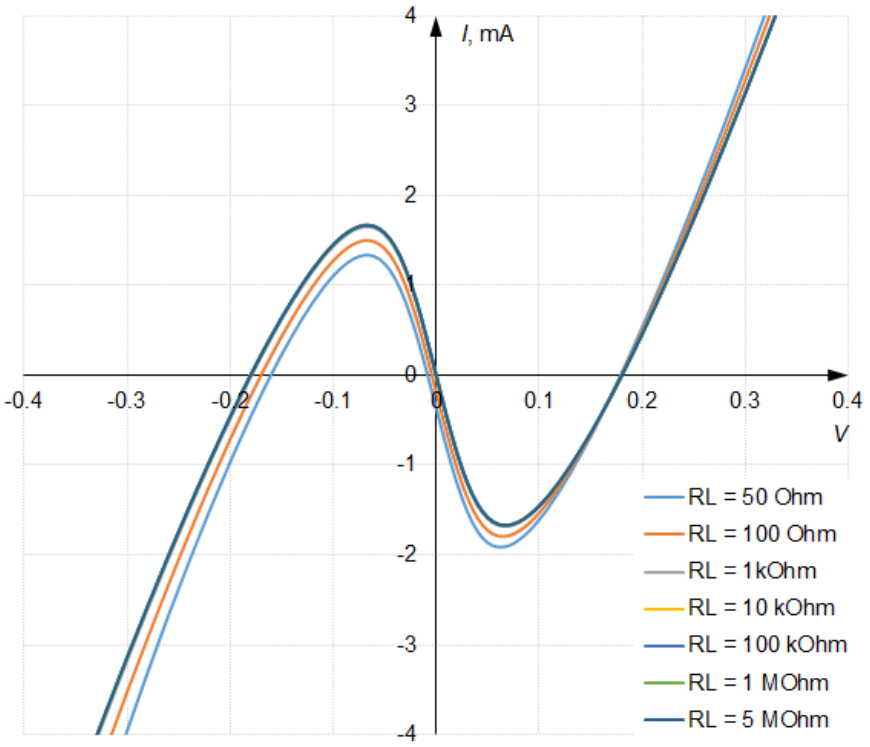
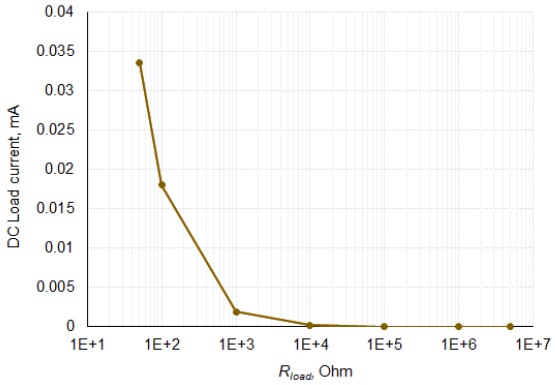


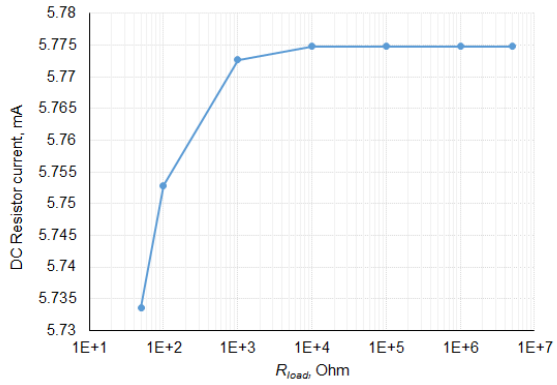
Figure 6.3: Effective circuit current-voltage characteristics plotted for various loads connected to C_1.

and negative bias voltages, V_{DD} and V_{SS}. Moreover the circuit showed a sensitivity to the load connected to it. The capacitor voltages were different when measured simultaneously and individually.

The observed sensitivity to the loading was motivational to go back to the simulations and investigate the influence of measuring equipment on the circuit performance. In order to find how the loading changes the oscillation pattern, earlier discussed Harmonic Balance-based method of locating equilibrium points was used. This involves a variable DC source to be connected to the NR while the DC current flowing through it is measured. The results of the simulations can be seen in Fig. 6.3, where trace intersection with the x-axis indicates the coordinates of the equilibrium points. Simulations are performed for a wide range of R_{load} starting from 50 Ω (typical spectrum analyser input resistance) and ending with 5 MΩ, including 1 MΩ (typical oscilloscope input resistance). One can see that as the load increases above 1 kΩ no changes in



(a) DC current flowing into the load versus the load resistance R_{load}.



(b) DC current flowing through resistor R versus the load resistance R_{load}.

FIGURE 6.4: Effect of load resistance R_{load} on the circuit DC currents.

the current-voltage characteristic is observed (all traces become practically indistinguishable from each other). This simulations suggest that if the C_1 pad is used to connect measuring equipment, its input resistance has to be higher than 1 kΩ. On the other hand if a spectrum analyser is connected to the V_{C1} pad, the circuit will be expected to perform differently than it was performing under the same bias conditions but measured with an oscilloscope.

The same loading sensitivity is confirmed by further DC simulations. As can be seen from Fig. 6.4, load current (Fig. 6.4(a)) and resistor current (Fig. 6.4(b)) reach some saturation value when R_{load} is 10 kΩ or higher. It can therefore deduced, that

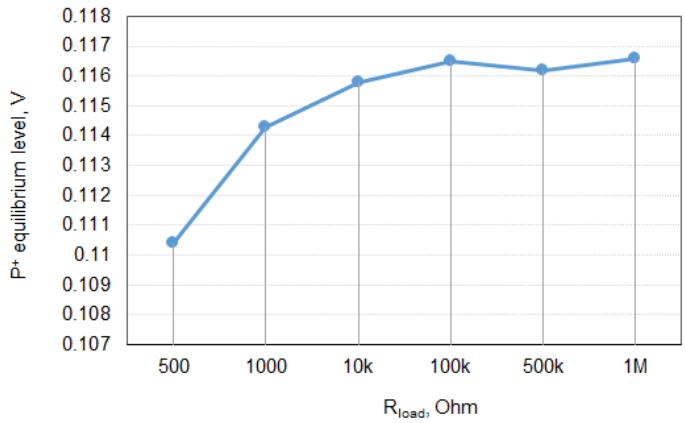
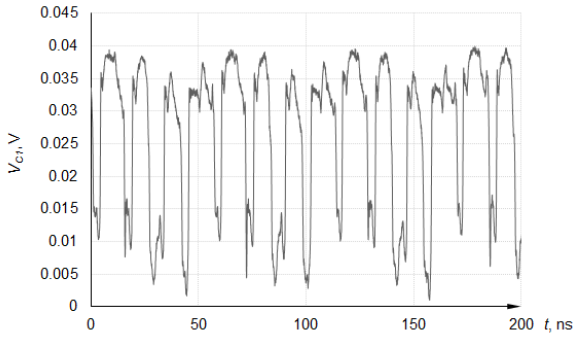


Figure 6.5: Relocation of the P^+ of V_{C1} with the change of load resistance R_{load}.

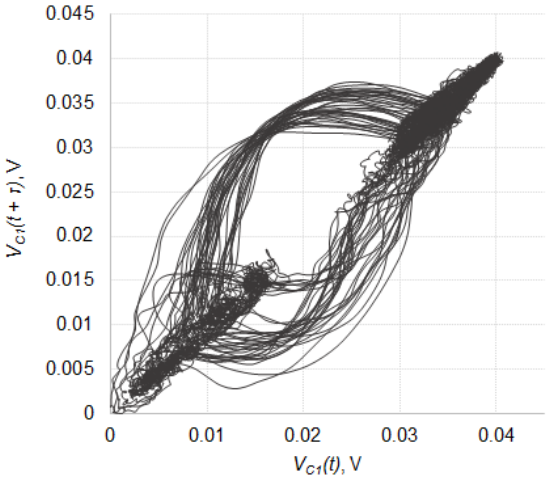
when load resistance is high, it has no influence on the measured signal. Time-domain simulations of V_{C1} also support this assumption. As can be seen in Fig. 6.5, positive equilibrium level gradually increases but reaches a saturated value for R_{load} above 10 kΩ, after which the fluctuations are due to inaccuracies of the statistical equilibrium-location algorithm. As a conclusion, it can be said that using an oscilloscope when taking voltage samples will not distort the circuit performance.

In all the measurements performed on-chip, the oscilloscope resistance was set to 1 MΩ in order to minimise the loading. However the loading sensitivity was observed as difference in performance during one-channel (V_{C1} only) and two-channel (V_{C1} and V_{C2}) measurements. When two voltage probes are connected, the load resistance seen by the resonator is half that of one-channel resistance. Simulations suggest that 500 kΩ is a value sufficiently large to ignore the loading effects. Nevertheless the real current-voltage characteristic of the NR could be different from the one simulated in the software and the range of R for which chaotic oscillations can be achieved is very narrow. Thus even a small deviation from the fixed R leads to a different performance under a given bias voltage.

The circuits located on all the three quarter-wafers were measured in order to test for the variation in their performance, should one exist. The observed signals resembled chaotic behaviour but nevertheless generally appeared as periodic. The circuits



(a) V_{C1} in time domain

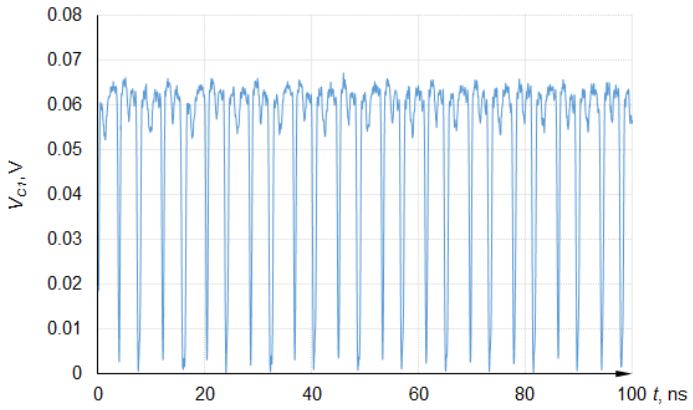


(b) V_{C1} embedded in pseudo phase space

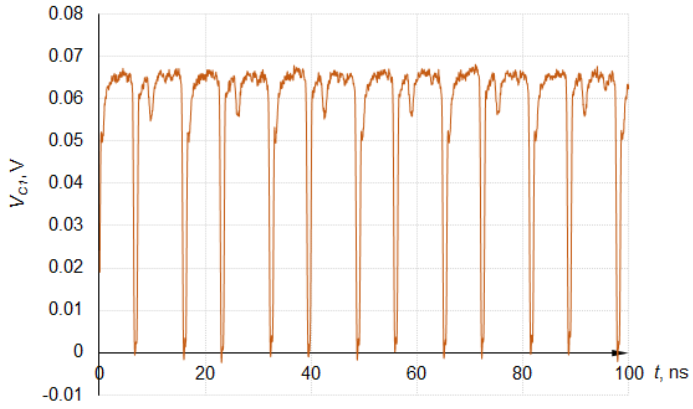
Figure 6.6: Chaotic-like C_1 capacitor voltage oscillations from the PP-10 circuit.

exhibited a wide range of different types of oscillations depending on the bias voltage, including the periodic sinusoidal oscillations at the expected frequency of approximately 2 GHz. But, at the same time, the applied bias voltages could not make the circuits generate chaotic signals. Nevertheless a few circuits produced signals, appearing as chaotic (Fig. 6.6(a)).

The chaotic nature becomes more evident if we employ the time-lag method for embedding the variable into a phase space (Fig. 6.6(b)). Only one voltage, specifically V_{C1}, was available for the analysis, and the phase portrait can not be constructed from a single time series. However if we plot voltage at time t versus the voltage from the same time series but with a time lag τ, we can construct a pseudo-phase plot. The



(a) Period-1 oscillations



(b) Period-2 oscillations

Figure 6.7: C_1 capacitor voltages measured on the same reticle at different bias voltages from the PP-10 circuit.

term 'pseudo' comes from the fact that we only plot one variable versus its time-shifted copy, but not two different variables. The obtained orbit resembles a chaotic attractor although in the presence of significant noise.

As a matter of fact, most of the circuits were not able to demonstrate this behaviour, but exhibited periodic oscillations. There existed a type of oscillations which appeared to be most common among the tested circuits.

The results of the oscilloscope measurements can be seen in Fig. 6.7. The two shown time series indicate the oscillations generated by the same circuit but with two different bias voltages applied. It can be seen that both signals are periodic, however

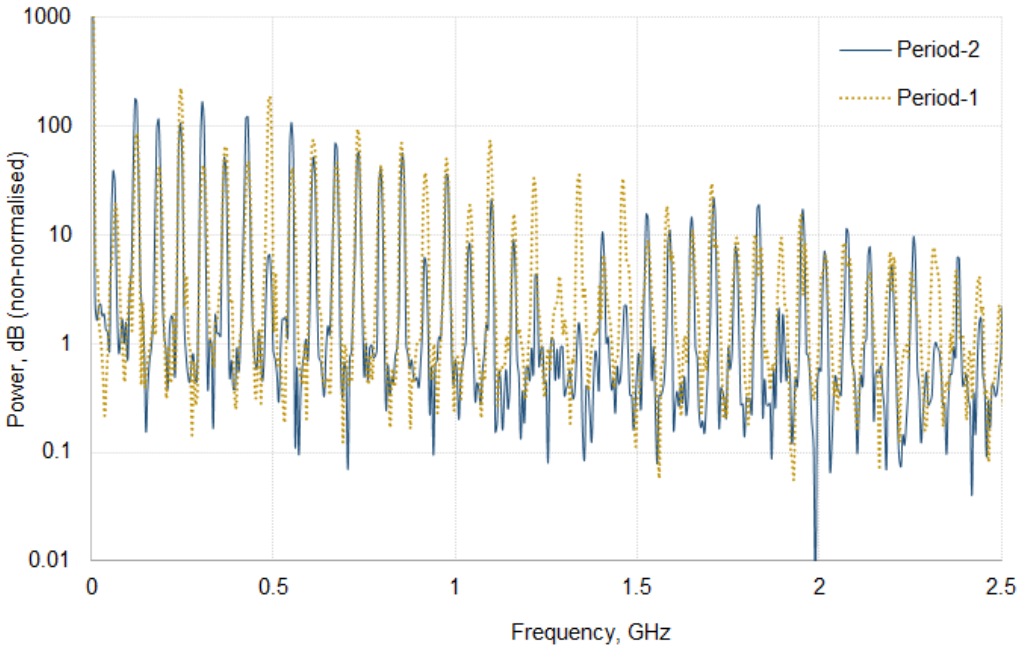


Figure 6.8: The spectra of period-1 and period-2 oscillations from the PP-10 circuit.

the period of the period-2 oscillations is twice that of the period-1 oscillations. The author interprets this change of oscillation period as period-doubling bifurcations on the way to chaotic oscillations which, however, were not distinctly observed. An FFT analysis of the measured signals is executed and the results are presented in Fig. 6.8. Note, that the results are not normalised, therefore the amplitudes should be treated as only relative. It is seen from the graph that the harmonics of the oscillations are located at the same frequencies, however the period-1 signal has harmonics which are not present in period-2 oscillations or have much higher power.

It was also observed that the transitions from period-2 to period-1, which happened with increasing the bias voltage, occurred at approximately the same voltages for every circuit on the available quarter-wafers. However, after recording the voltages at which the transitions occurred, it is concluded that there is a progressive change from the centre of the wafer towards its edges. That observation suggests that the circuit is sensitive to the variation of certain manufacturing parameters. It is quite common that different manufacturing processes, such as material deposition or etching and

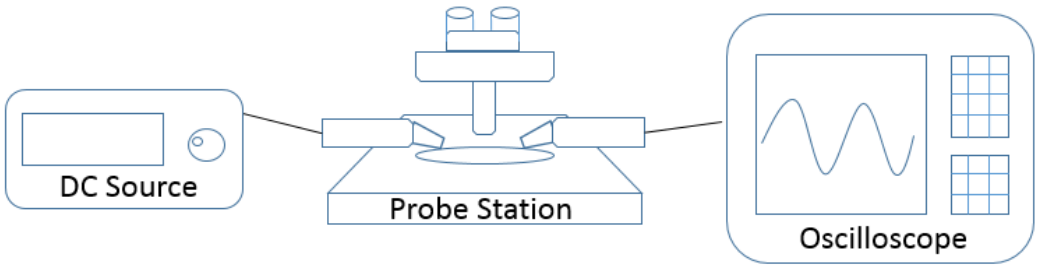


Figure 6.9: The time-domain voltage measurement setup.

polishing, result in a final layer profile that may be concave or convex. At this stage of the experiment it was proposed that the circuit is sensitive to that kind of process variation.

The measurement results did not fully meet the expectations: a chaotic mode of operation was not achieved, which indicates a poor quality of the developed design. However it can also be attributed to the pHEMT models which were not suited for the oscillator application. On the other hand, some of the chaotic system features were observed, and furthermore the circuit's sensitivity has been noticed in terms of a gradual change in the performance from the centre of the wafer towards its edges. And, although a quantitative approach to the process quality estimation has not been developed, the measurement results gave motivation for the work to continue and switching to the PL-15 implementation of the CCM.

6.2 PL-15 Measurements

The PL-15 realisation is measured following the same procedures as described above, including the on-wafer measurements on the probe station. The first stage of the circuit measurements uses an Agilent Technologies DSO9104A oscilloscope for recording the signals in the time domain. Two channels of a DC PST-3202 programmable power supply are used for biasing the oscillators. The diagram describing the test-bench setup is shown in Fig. 6.9.

The measurement procedure began with finding an appropriate bias voltage for

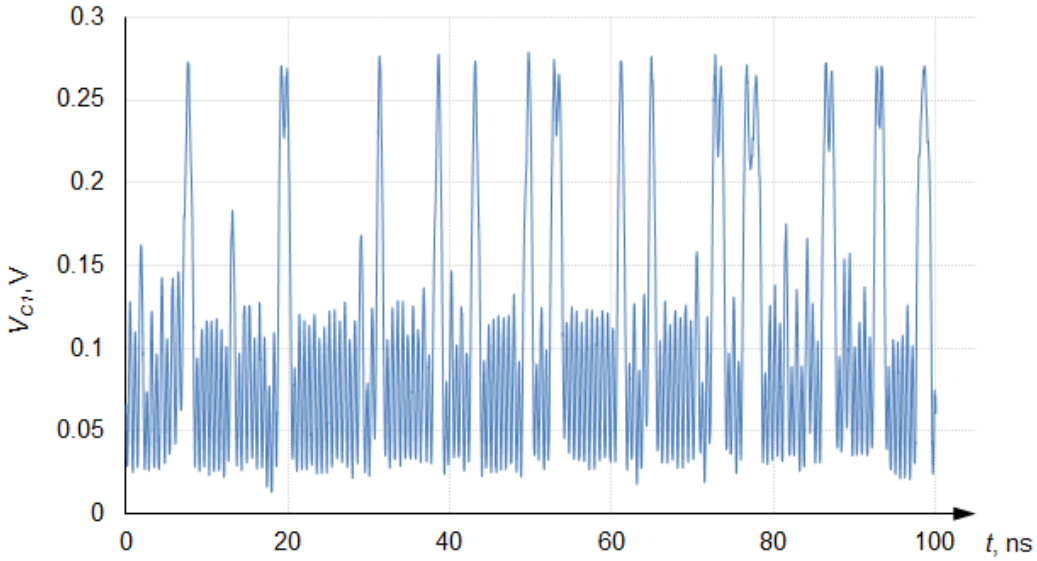


Figure 6.10: The capacitor C_1 voltage from the PL-15 circuit as measured by the oscilloscope.

the circuits to operate in a chaotic regime. The bias voltage at which the chaotic-like oscillations are observed was slightly different from what was expected from the simulations. The average voltage at which the circuits are generating non-periodic oscillations are $V_{SS} = -3$ V and $V_{DD} = 6$ V. The typical non-periodic signal that is observed is shown in Fig. 6.10.

The obtained signal closely resembles the simulated voltage and appears to be chaotic. Fast Fourier Transform are performed on the time-series and spectrum of the capacitor voltages can be seen in Fig. 6.11. As can be seen, the spectrum is continuous and has no distinct peaks. Such spectrum is a certain attribute of a chaotic signal.

These primary measurements are considered encouraging and further analysis is undertaken. In order to prove that the circuit really is capable of operating in chaotic mode, we have to explore its performance at different bias voltages. Bias voltage effectively changes the shape of the NR's current-voltage function. This function (or the polynomial coefficients of thereof) can be referred to as a control parameter under the change of which period-adding bifurcations are observed.

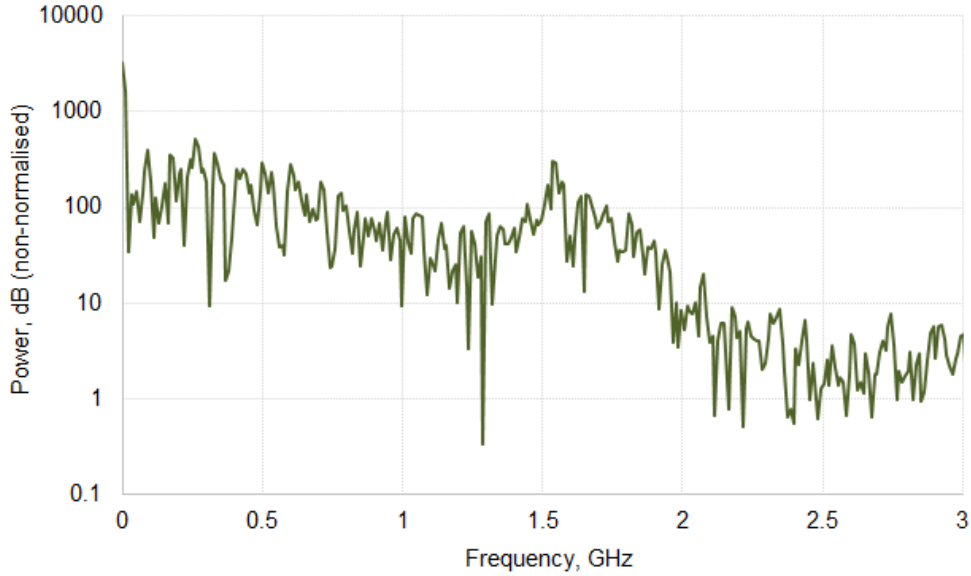
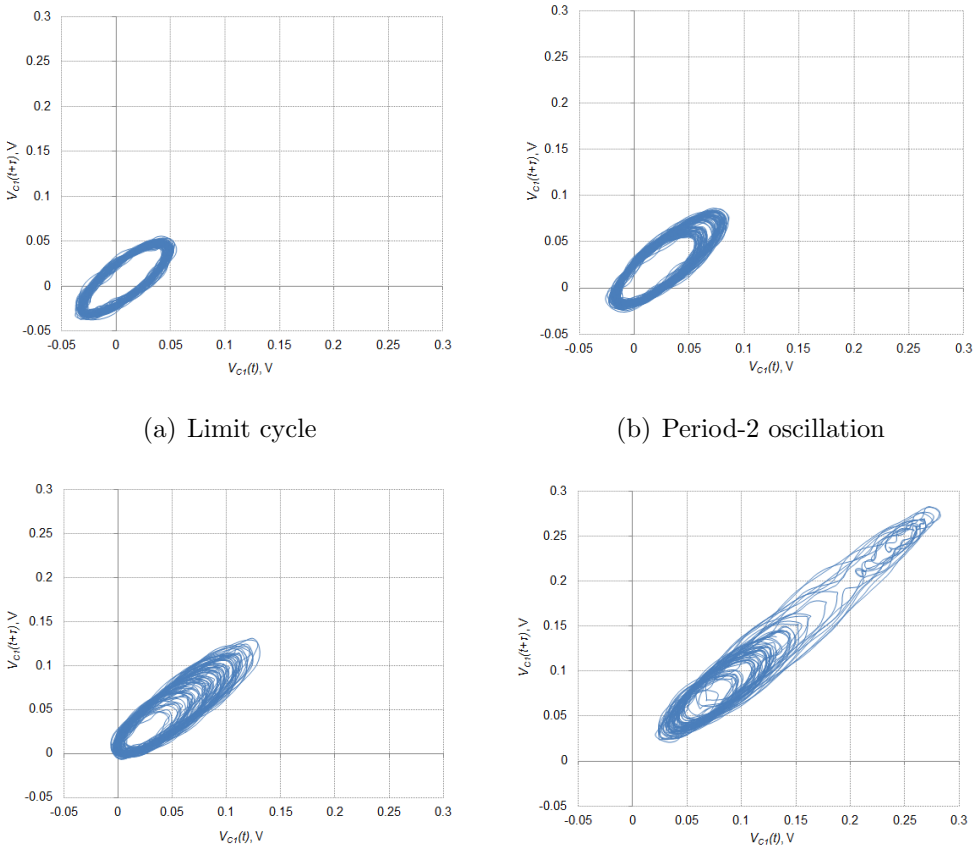


Figure 6.11: Spectrum of the measured capacitor C_1 voltage from the PL-15 circuit obtained after Matlab FFT processing.

The witnessed bifurcations are presented in Fig. 6.12. The technique used to plot the results is the time-lag method discussed earlier. The figure shows the period bifurcations which happened with the increase of V_{DD} bias voltage with V_{SS} being kept constant. The oscillations begin as a limit cycle (Fig. 6.12(a)), then we can see the period doubling (Fig. 6.12(b)) and another one which follows (Fig. 6.12(c)), and finally the chaotic attractor appears (Fig. 6.12(d)), indicating the onset of the chaotic regime of the circuit operation.

The signals can be analysed in the frequency domain if we take an FFT transformation of each type of oscillations. The results of a Matlab FFT algorithm processing are depicted in Fig. 6.13. It can be seen that a period-1 oscillations have a single harmonic approximately of 1.68 GHz, two extra harmonics at approximately 0.8 GHz and 0.88 GHz arise in the period-2 oscillations and multiple harmonics appear in the case of period-4 oscillations. Oscillations corresponding to the chaotic attractor have a broad and continuous spectrum, as expected. Frequency analysis confirms that the designed system is capable of orderly behaviour and chaos appears only in a certain range of a control parameter, that is V_{DD} in the studied case. Therefore it can be stated with



(a) Limit cycle

(b) Period-2 oscillation

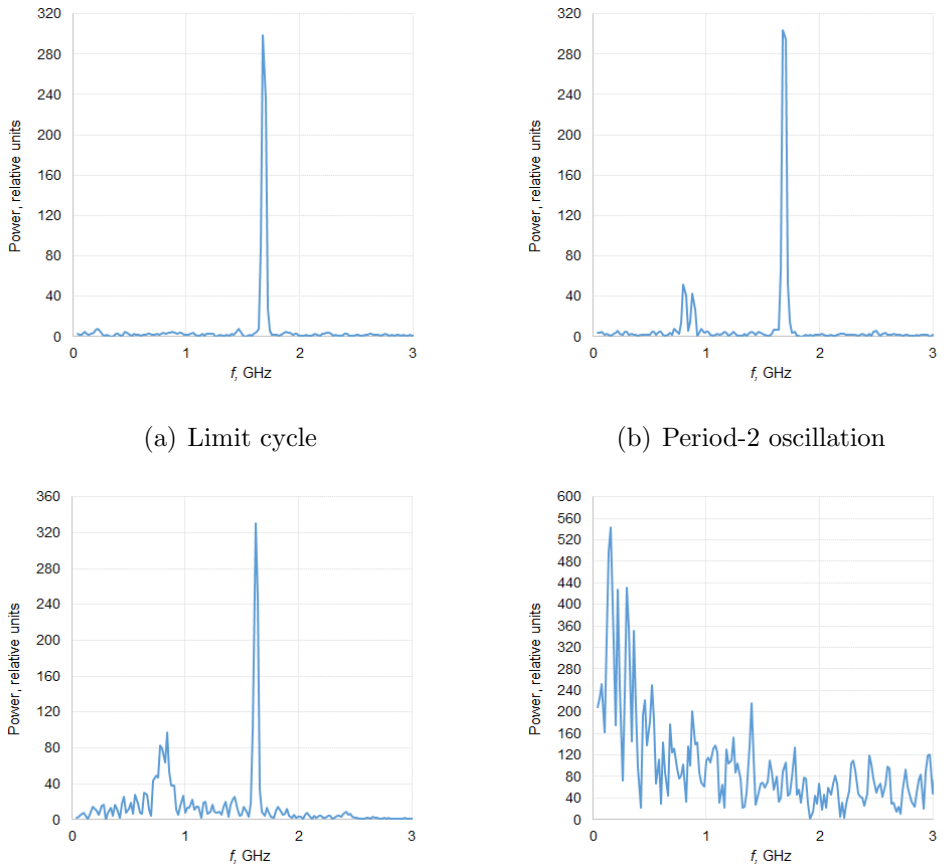
(c) Period-4 oscillation

(d) Chaotic attractor

FIGURE 6.12: Period bifurcations observed in the PL-15 Chua's circuit.

confidence that observed non-periodic signals are not noise but chaotic oscillations.

After conceptually proving the designed circuit's ability to generate chaotic signals all the circuits on the available quarter-wafers are measured. The idea of those measurements is to investigate how the circuit output varies from one reticle to another. In order to observe the differences, the bias voltage applied to the measured circuits had to be kept constant within the framework of one quarter-wafer. The bias voltage defines the shape of the current-voltage function of the nonlinear resistor which in its turn changes the characteristics of the output signals. It can be seen from the bifurcations demonstration (Fig. 6.12) where the centre of the hole around which the trajectory rotates is moving in the direction of higher voltage as the bias voltage is increased. Thus identical bias voltage has to be applied to all the circuits located on the subject quarter-wafer as long as we want to focus on the location of the equilibrium



(a) Limit cycle

(b) Period-2 oscillation

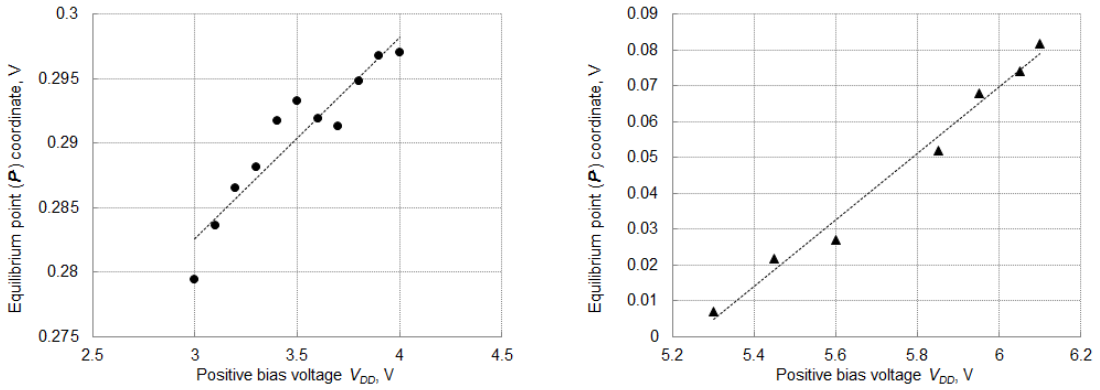
(c) Period-4 oscillation

(d) Chaotic attractor

Figure 6.13: FFT transformation of the bifurcating signals in the PL-15 circuit.

levels.

It is decided to employ the voltage level that corresponds to the V_{C1} coordinate of the P^- equilibrium point as the circuit's individual characteristic. In other words it is the lower voltage level around which the most of the oscillations occur, as can be seen from Fig. 6.10. At this point, the equilibrium levels are estimated manually as the mean distance between the local peaks of the lower oscillations. This method appeared to be acceptable as it gives quite an accurate quantitative result, however it is realised that a computer algorithm has to be developed for automation of the measurements, bringing higher accuracy and shorter analysis time. As the previously described simulations have shown, the equilibrium points should be reasonable indicators of the NR performance and consequently of the transistor characteristics defined by the manufacturing process.



(a) The simulation of the bias voltage effect on the equilibrium level

(b) The measurement of the equilibrium level with the bias voltage change

Figure 6.14: Effect of the bias voltage on the equilibrium levels in the PL-15 circuit.

It is expected from the simulations that a change of bias voltage would effectively relocate the equilibrium points of the voltages as a result of the current-voltage characteristic reshape. The outcome of these simulations can be seen in Fig. 6.14(a). The experiment is performed under conditions similar to that in the simulations. The bias voltage is gradually increased and the V_{C1} samples are recorded with the oscilloscope. We can see from Fig. 6.14(b) that the trend is the same as in the simulated dataset, however one should note the difference in scale. The cause of the different sensitivity in the simulated circuit and the real one is still under investigation. The first obvious difference is in the bias voltages, which are higher for the real circuit and perhaps slightly exceed the drain-source voltage recommended for the PL-15 pHEMTs. Therefore, it is possible that the operation of the pHEMTs under high bias voltage is quantitatively different from normal operation and this results in a more rapid change of the NR current-voltage characteristic. Nevertheless, another experimental confirmation of the simulation study encourages the continuation of the circuit measurements.

In the follow-up experimental study of the circuits, it is decided to take the voltage samples of all available circuits on the quarter-wafers. Thus, in the preparation of the measurements, several circuits across the quarter-wafer are probed for their regime under proposed bias conditions before taking the samples. However, during the first stages of the experiment, constant chaotic performance throughout the wafer was not

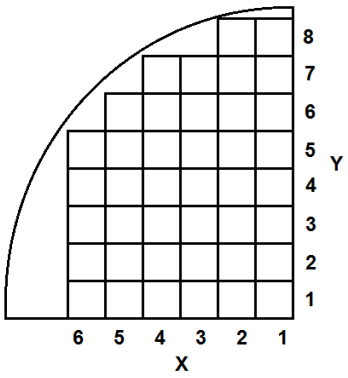


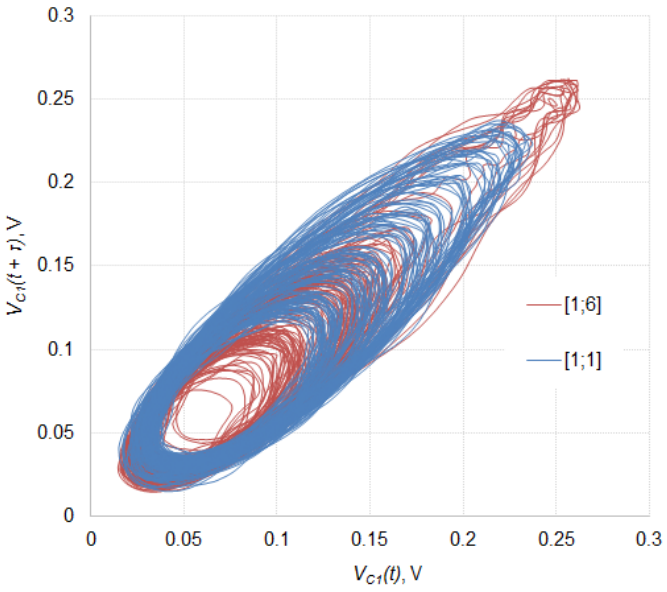
Figure 6.15: The reticle map of the PL-15 quarter-wafer.

maintained. Nevertheless the initial measurements showed that the equilibrium-point coordinates of the circuits change gradually going from the centre of the wafer towards its edges. More careful measurements are planned to quantify this variation.

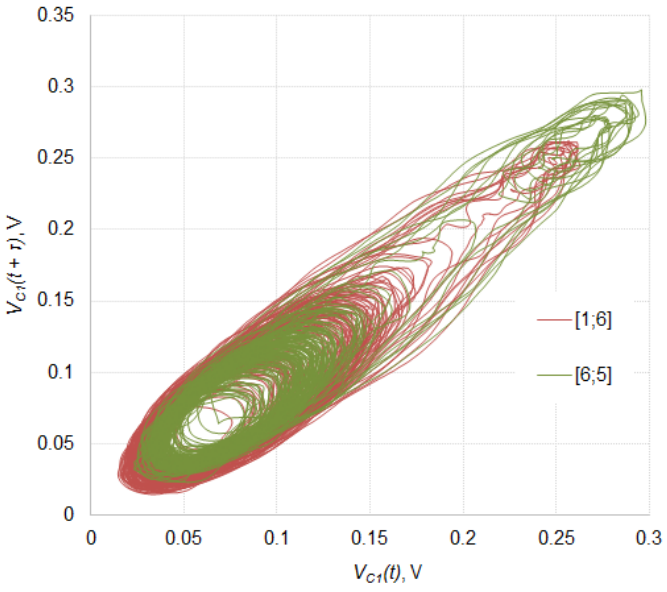
The adopted reticle coordinate grid can be seen in Fig. 6.15. The coordinates are chosen to increase from the centre of the wafer towards its edges. At the same time, the orientation of the quarter-wafer was changed: this quarter in reality represents the 1^{st} quadrant of the full wafer. It is rotated to match the pads with the correct probes due to inability to replace the probe holders replacement at the time of the experiment. The following experiment is done on the quarter-wafer with the PBO wafer-level packaging.

It is observed that the coordinates of the equilibrium points change rather steadily from the circuits in the centre of the wafer moving towards its edges. That can be seen from Fig. 6.16 where two pairs of attractors are plotted on top of each other. If we focus on the lower equilibrium point, which is the centre of the hole that is closer to the origin, we can observe it relocating. It is worth mentioning that the attractor, corresponding to the [1;1] reticle is not chaotic: the chosen bias voltage did not allow chaotic operation of the circuit located on that reticle. Nevertheless the lower equilibrium point is still located at the same level as it would have been, should the operation be chaotic. That means we can still compare these attractors confidently.

The coordinates of the lower equilibrium point are estimated for most of the circuits



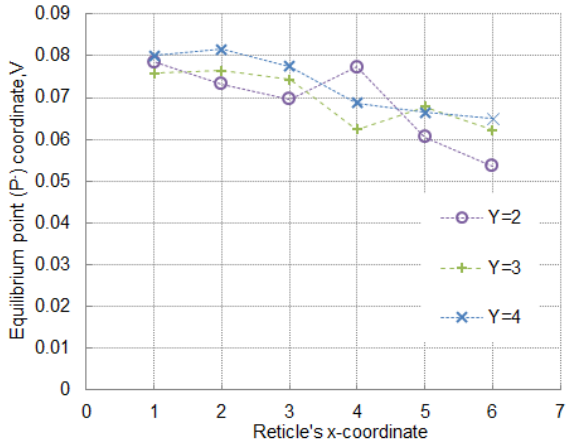
(a) Attractors from (1;1) and (1;6) reticles



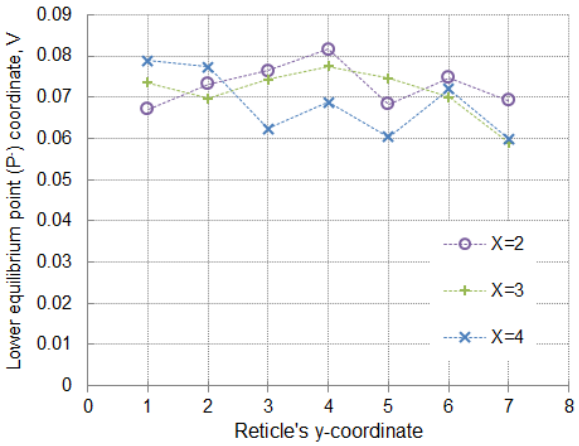
(b) Attractors from (1;6) and (6;5) reticles

Figure 6.16: Comparison of the attractors corresponding to the signals of the circuits at different locations on the PL-15 wafer.

on the wafer. These coordinates are utilised to make a plot depicting the change of equilibrium levels for circuits located at different sites of the quarter-wafer. Two plots shown in Fig. 6.17 demonstrate how the lower equilibrium varies from circuit to circuit as we go along the x-axis (Fig. 6.17(a)) and as we go along the y-axis (Fig. 6.17(b)).



(a) Equilibrium level shift for circuits along the x-coordinate



(b) Equilibrium level shift for circuit along the y-coordinate

Figure 6.17: The observed shift of the lower equilibrium level for the circuits at various locations on the PL-15 wafer.

Each graph presents the data for three rows/columns of reticles. The declining trend is clearly noticeable when we look at the change across the x-direction. Similar, yet more noisy, data are observed for the y-coordinate equilibria variation. Furthermore for both cases we can see good correlations between the three lines presented on each graph, which suggests that the change in equilibrium coordinates is not random, but rather depends on the location of the circuit on the wafer.

6.3 Conclusions

The measurements of the two designed GaAs pHEMT Chua's circuit were performed on the wafers. Samples of capacitor voltages of all circuits on the available quarter-wafers were taken with the help of oscilloscopes. An algorithm for automated location of equilibrium levels was developed to shorten the analysis time. The results of initial measurements suggested that there exists a variation of equilibrium-voltage levels among the circuits in different locations on the wafer. The examination of the measured data suggested that this variation is not random but gradual with a trend going from the centre of the wafer towards its edges.

As has been mentioned before, it is quite common that certain manufacturing wafer-parameters change linearly from the centre of the wafer towards its edges. For example, it may happen that the deposited layer of metal or dielectric has a larger thickness in the centre of the wafer than at the edges due to the nature of the deposition process and processing chamber configuration. Thus the results obtained from the described experiment gave a motivation to correlate the equilibrium-point coordinate with different parameters available from the process control monitor (PCM) measurements.

Tell me how it feels knowing chaos will never end.

Slayer

7

CCM correlation with PCM

We confirmed that the distribution of equilibrium levels for the circuits on the wafer appears to be related to certain manufacturing parameters. Consequently it was decided to correlate the CCM characteristic in the form of equilibrium-voltage levels with all of the available PCM parametric data. Since it was found that the PL-15 implementation of Chua's circuit appears to perform appropriately for a CCM, the second, extended, measurement procedure was carried out to obtain more precise data to be used in the oscillator's analysis for the equilibrium-point levels. Hence, all measurement and test data in this chapter refers to the PL-15 implementation of Chua's circuit.

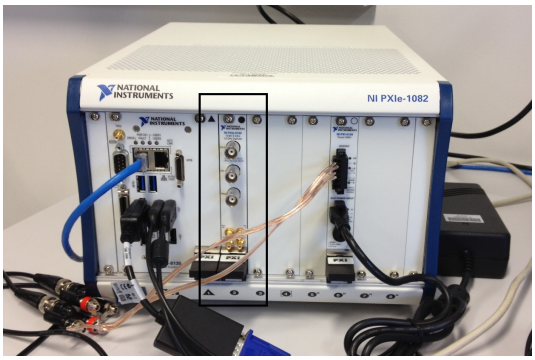


Figure 7.1: National Instruments PXI chassis with the digitiser.

7.1 Measurement Setup

A National Instruments PXIe-5162 Digitiser/Oscilloscope (Fig. 7.1) is used for measurement of time series. This oscilloscope, of 1.5 GHz bandwidth and 5 GSa/s sample rate, was fitted in the NI chassis which had an on-board PC, making the data series acquisition easier. Apart from a different tool for signal recording, the laboratory setup is fundamentally the same as in the previous measurements. At the same time, a new Matlab script is developed for automated locating of equilibrium-points coordinates. This algorithm is statistical in nature but allows a quite accurate estimation of the equilibrium levels. The steps of the algorithm are as follows:

1. The function *findpeaks* is used to find the local maxima and minima.
2. The function *ksdensity* is employed in the generating of the probability density functions (PDF) for both, the local maxima and minima.
3. The *intersections* function is used for finding the intersections between the PDFs of local minima and maxima.
4. The voltage levels corresponding to the intersections of the PDFs are defined as the equilibrium levels.

The illustration of the described algorithm result is shown in Fig. 7.2. Taking into account the noise present in the data this statistical method appears to be accurate enough for our purposes. It is apparent that a data series of sufficient length has to

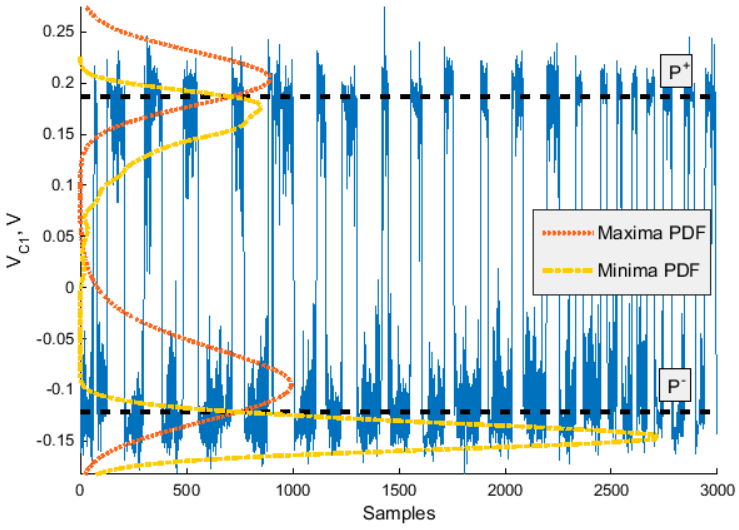


Figure 7.2: The result of the equilibrium-levels estimation algorithm applied to the V_{C1} time series.

be taken in order to estimate the equilibrium levels with enough precision. It should be noted that the time-series data appears to be more noisy than in the measurements done with a Agilent Technologies DSO9104A oscilloscope. This is most probably due to the higher sampling rate of the bench-top oscilloscope, which is 20 GSa/s versus only 5 GSa/s of the PXI digitiser.

At the same time, another automation algorithm is developed in order to make the analysis time shorter. The data series generated by a single oscillator is recorded in a LVM (LabView Measurement) file with a name which included the coordinates of the reticle (e.g. *1_-5.lvm* for $x = 1$, $y = -5$). Then the generated files can be processed by the developed algorithm to find the equilibrium levels for all the circuits and record the obtained data into an array which could later be visualised, or plotted.

Thus each oscillator on the wafer could be characterised by the positive and negative equilibrium levels of its signals. However, it was found that the separation, or difference between these two levels, could be a better indicator. First of all, when the NR current-voltage function changes due to component parameter fluctuations, it relocates the equilibrium points in opposite directions because of the function's symmetrical nature. Secondly, it is decided that a single number would be easier to use in the analysis and

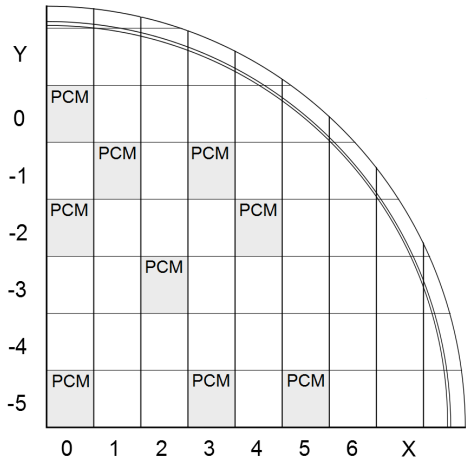


FIGURE 7.3: The map of the quarter-wafer with the adopted reticle coordinate grid and PCM data availability.

correlation procedures rather than two separate values. As a result, it is chosen to characterise each CCM in terms of its C_1 capacitor equilibrium-voltage level difference, or V_{dif}.

At first, the analysis of the PCM data is carried out. The data from 25 monitors, evenly distributed across the wafer, are available for the analysis. However, only 9 sites were measured on the quarter-wafers in our possession. The PCM tests included measurements of maximum transconductance, typical (at $V_{GS} = 0$ V, $V_{DS} = 1.5$ V) and maximum (at $V_{GS} = 0.5$ V, $V_{DS} = 1.5$ V) drain saturation currents, sheet resistances of epitaxial and TFR layers, threshold voltage, pinch-off voltage and other parameters. The measurements were carried out on WIN Semiconductors' facilities and their results provided with the wafers. The parameters included in the PCM tests are summarised in Table 7.1.

The map of the quarter-wafer with the correct reticle coordinate grid is shown in Fig. 7.3. It can be seen that this time the orientation of the wafer corresponds to the 1^{st} quadrant, which is consistent with reality. The new coordinate grid corresponds to the system used at WIN. Moreover, the reticles for which the PCM data was available are clearly identified.

Parameter	ID	Unit
Maximum gm of FET at V_{DS}=1.5 V	GM	mS/mm
Drain Current of FET at V_{GS}=0 V, V_{DS}=1.5 V	IDSS	mA/mm
EPI Isolation Leakage Current at 10 V	ISEP	nA
Drain Current of FET at V_{GS}=0.5 V, V_{DS}=1.5 V	IDMAX	mA/mm
TLM EPI Sheet Resistance	RSEP	Ω / □
TLM TFR Sheet Resistance	RSTR	Ω / □
Breakdown Voltage Between Gate-Drain at 1 mA/mm	VDG	V
V_{GS} at Peak GM	VGMP	V
Threshold Voltage at V_{DS}=1.5 V	VPO	V
Pinch-off Voltage at V_{DS}=1.5 V, I_{DS}=1 mA/mm	VTO	V
Pinch-off Current at V_{GS}=-2 V, V_{DS}=1.5 V	IPO	mA/mm

Table 7.1: Parameters measured during the PCM testing at WIN Semiconductors.

7.2 Correlation Results

The measured PCM parameters were available in the tabled form. However, this method of data presentation is not very visual and the variation of the measured parameters is hard to observe. Nevertheless, tabled data becomes quite useful if we want to find the correlation coefficients between the parameters.

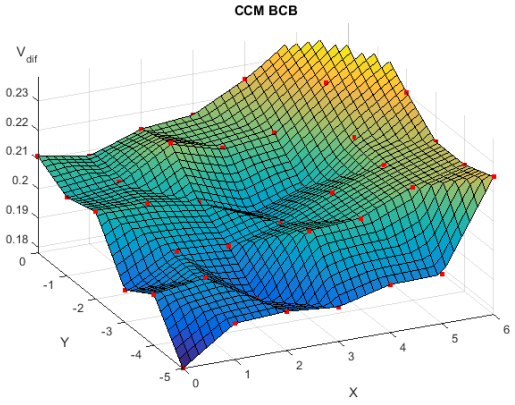
The CCM Chua's oscillators are measured on all the reticles of the 3 available quarter-wafers. The measured data are processed to obtain these circuit characteristics in terms of the equilibrium-voltage level difference V_{dif}. Firstly, this data are correlated with the PCM measurements done on the same reticles with the CCM candidates. The correlation is done employing Microsoft Excel's function *correl*, which outputs the correlation coefficient of two arrays. The CCM's V_{dif} was correlated with the PCM parameters and the result of this correlation in the form of the correlation coefficient ρ is presented in Table 7.2.

Correlation coefficient, ρ			
		V_{dif}	
Parameter ID	BCB	PBO	EMR
GM	-0.1005	0.322387	0.571457
IDSS	-0.73131	-0.56307	-0.87133
ISEP	-0.22559	0.371085	0.132097
IDMAX	-0.48449	-0.53837	-0.82031
RSEP	0.026862	-0.227597	0.145449
RSTR	0.860103	0.227597	0.892723
VDG	-0.05168	0.085876	0.921771
VGMP	0.17489	0.867968	0.759058
VPO	0.675119	0.571418	0.877746
VTO	0.637746	0.438752	0.849211
IPO	-0.00215	-0.09771	-0.09649

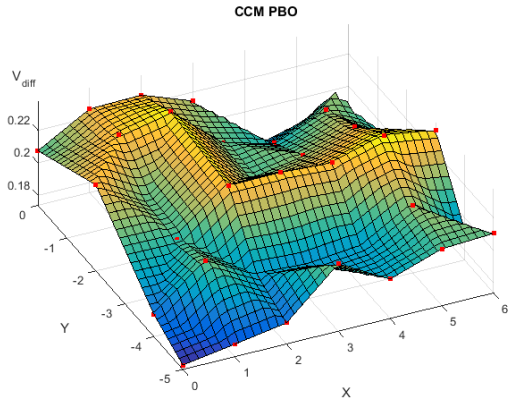
Table 7.2: Correlation coefficients ρ between the CCM characteristic, V_{dif} and PCM parameters for the three quarter-wafers.

It can be seen that the PCM parameters that have perceptible correlation with the CCM's V_{dif} include IDSS, IDMAX, RSTR, VPO and VTO. It is apparent that the TFR sheet resistance would specify the value of the passive resistor of Chua's circuit, which in its turn affects the coordinates of the equilibrium points. However a link between the equilibrium levels and pHEMT transistor parameters, such as saturation drain current and threshold voltage, can also be observed, implying that the circuit is also sensitive to the transistor parameters.

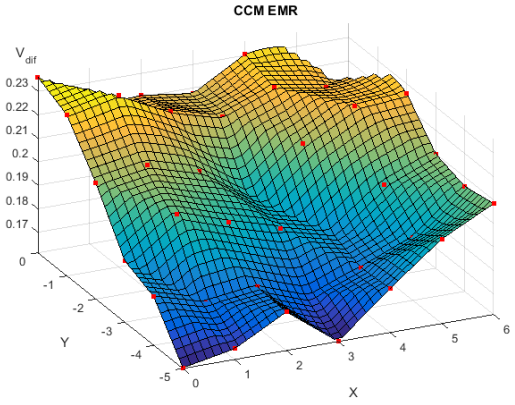
We can also employ Matlab to assist us in the PCM data visualisation. The PCM tables are used to generate maps indicating the values of certain parameters at different locations of the wafer. However, as the number of measured reticles is limited, the parameter values at the unmeasured sites are approximated by interpolation. A similar procedure of generating the maps of the equilibrium-level differences across the wafer allows a visual comparison between the PCM and the CCM measured parameters.



(a) BCB Wafer

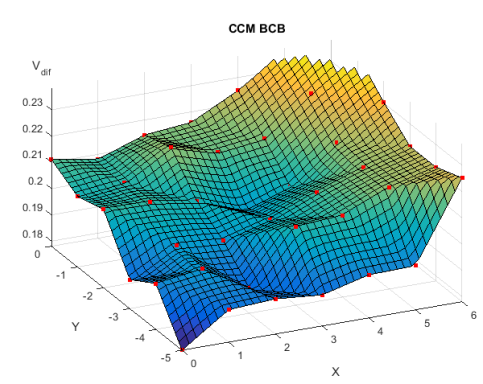


(b) PBO Wafer

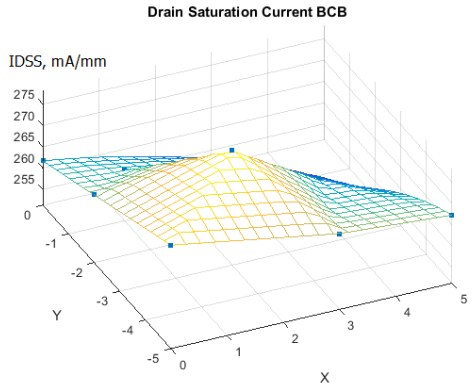


(c) EMR Wafer

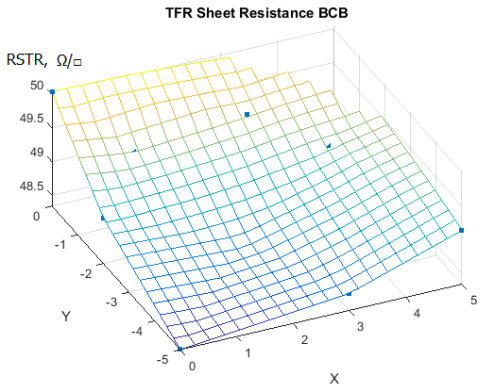
Figure 7.4: The maps of the equilibrium levels separation for the CCMs of three quarter-wafers.



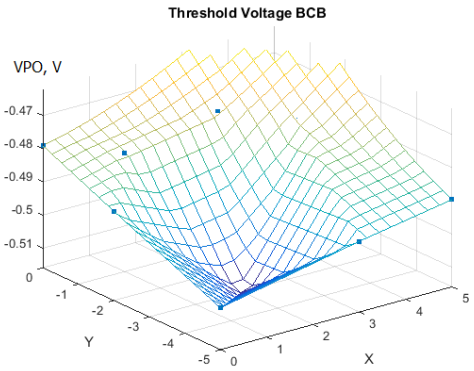
(a) CCM V_{dif}



(b) PCM Drain current



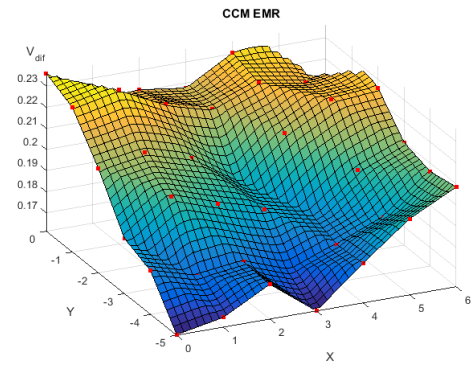
(c) PCM TRF Resistance



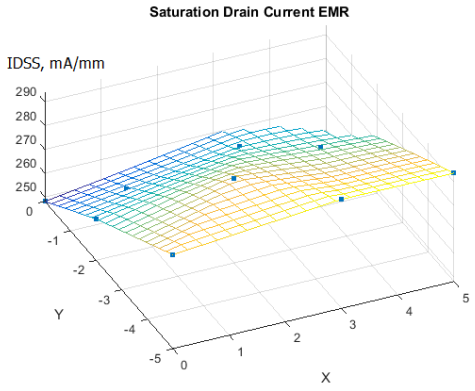
(d) PCM Threshold Voltage

FIGURE 7.5: The comparison between the CCM and PCM parameters for the BCB quarter-wafer.

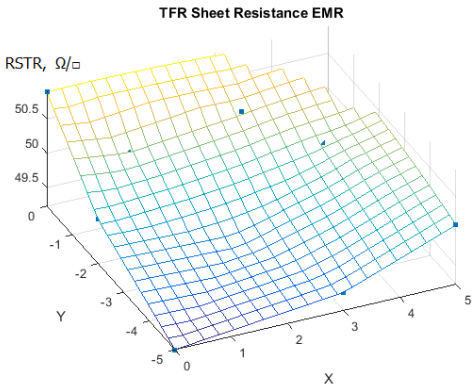
The CCM parameter maps for the three quarter-wafers are shown in Fig. 7.4. Red round markers indicate the measured sites which are specified by the x and y coordinates. It can be seen that the maps shown in Figs 7.4(a) and 7.4(c) demonstrate similar trends, while the map shown in Fig. 7.4(b) has less in common with the former two. There are a few possible explanations for this discrepancy. First, is that this is the actual data, and the PBO polymer affects the circuits' performance in the shown way. The more likely explanation is erroneous measured data. It was observed throughout the measurement process that the oscillations of Chua's circuits on the PBO wafer were less stable and changed from one instance of the measurement to another. The probable cause of this is worn-out RF pads, which had poor connectivity with the probes. This



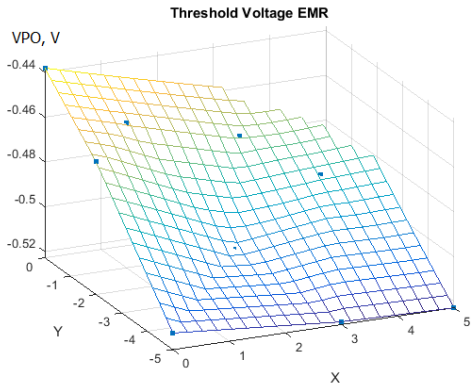
(a) CCM V_{dif}



(b) PCM Drain current



(c) PCM TRF Resistance

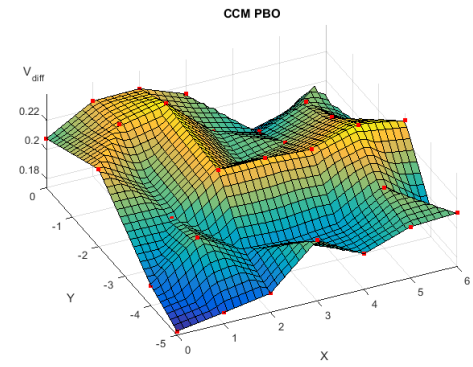


(d) PCM Threshold Voltage

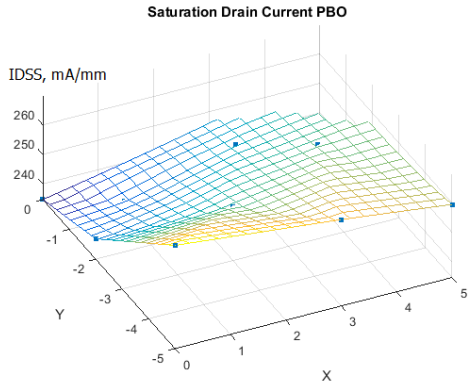
Figure 7.6: The comparison between the CCM and PCM parameters for the EMR quarter-wafer.

consequently led to not very reliable results. Thus it is chosen to utilise only the BCB and EMR wafers in future analysis, displaying the PBO results for reference only. On the other hand, the existent correlation between the PCM parameters and the PBO CCM data indicates that the measured signals are valid at least to a certain extent.

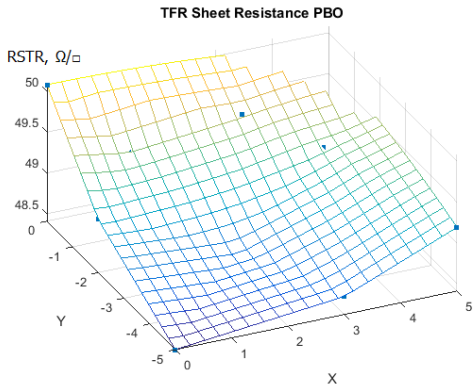
Figs 7.6-7.7 demonstrate the maps of the CCM's V_{dif} and such PCM parameters as saturation current (IDSS), TFR sheet resistance (RSTR) and threshold voltage (VPO) set against each other for BCB, EMR and PBO wafers respectively. The previously demonstrated correlation therefore can be seen from the similarity of the surfaces. As expected, the best correlation is seen between the V_{dif} and PCM's TFR sheet



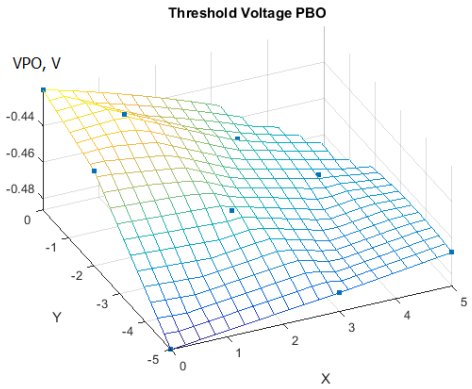
(a) CCM V_{dif}



(b) PCM Drain current



(c) PCM TRF Resistance



(d) PCM Threshold Voltage

Figure 7.7: The comparison between the CCM and PCM parameters for the PBO quarter-wafer.

resistance, although the remaining IDSS and VPO parameter distributions also quite closely match the CCM maps.

7.3 Variations in Correlation

One can notice that certain PCM parameters tend to correlate quite tightly with the measured CCM metric on one wafer and have nearly no correlation on the other. One example would be VGMP parameter which shows high correlation coefficient for the PBO and EMR wafers, but demonstrates nearly no correlation with the CCM on the BCB wafer. Several similar examples can be found in Table 7.2. Deeper investigation of that can lead to a conclusion that this could be purely a statistical artefact.

		Standard deviation, STD		
Parameter ID	Error	BCB	PBO	EMR
GM	0.09%	0.48%	0.79%	0.64%
IDSS	0.04%	2.59%	4.61%	5.87%
ISEP	0.01%	14.88%	11.94%	4.97%
IDMAX	0.02%	1.24%	1.53%	2.22%
RSEP	0.04%	0.52%	0.40%	0.43%
RSTR	0.02%	1.07%	1.06%	1.04%
VDG	1.01%	2.14%	16.59%	1.87%
VGMP	32%	16.67%	56.52%	23.33%
VPO	0.02%	2.78%	5.03%	6.34%
VTO	2.9%	3.01%	3.32%	5.04%
IPO	0.05%	14.99%	11.79%	13.53%

Table 7.3: PCM parameter measurement errors and standard deviation values for BCB, PBO and EMR wafers.

Different PCM parameters are measured with a various accuracy and also have different spread. The parameters, which have the highest meaning for the purposes of correlation with the CCM parameter can be identified if we calculate the standard deviation in the measured population. Table 7.3 summarises the STD values of the PCM parameters. The measurement error is supplied for each parameter as well. It is found from referring the smallest increment in the measured value to the mean value in the parameter population. It can be seen that most of the PCM characteristics are measured with an error of several tenths of a percent. However there are some parameters where measurement accuracy is a few orders of magnitude lower. Among such parameters are VGD, VGMP and VTO. This observation suggests that correlation of these parameters with the CCM metric can produce false results.

At the same time, parameters more suitable for correlation with the CCM performance are the ones which have relatively large deviation and good measurement

accuracy. Such parameters include IDSS, ISEP, IDMAX, RSEP, RSTR, VPO, IPO and, probably, GM. Parameters which are left (VDG, VGMP and VTO) have high measurement errors which would result in random correlation coefficients with the CCM data. Hence these are not recommended for performing the correlation with.

One can see that the transconductance GM distribution does not match the variation of CCM parameter across the wafer. Even though the EMR wafer demonstrates relatively high correlation coefficient (PBO too, but to much less extent) the correlation is non-existent for the BCB wafer. According to [107] high transconductance in a pHEMT can be achieved through high carrier mobility, high carrier sheet concentration of the materials and low gate to source, gate to drain resistance of the device. Electron transfer efficiency from the δ-doped AlGaAs layer to the InGaAs channel is essential for good electron control ability of the gate, which ensures high GM. In the manufacturing this means that recess depth must be thoroughly controlled, which is the case for PL-15 process. The lack of correlation in circuit performance and device GM metric could be coming from the fact that GM is the maximum (peak) transconductance of a pHEMT at $V_{DS} = 1.5$ V. It is possible, that under a different bias, intermediate values of transconductance are varying less than maximum GM. That is, when the pHEMTs in the circuit are not biased to exhibit maximum transconductance, the performance of that circuit becomes much less correlated with the GM parameter.

At the same time, the correlation coefficient for the FET drain current IDSS and the CCM metric appears to be quite high for all the wafers. IDSS measurement is performed at gate-source voltage V_{GS} of 0 V and drain-source voltage V_{DS} of 1.5 V. From reading DC current and voltage annotations, available in the AWR schematic editor, it was confirmed that most of the pHEMTs are biased with approximately the same voltages. Drain current in each device affects the shape of the current-voltage characteristic of the NR and that influence is seen in the CCM metric.

High correlation was also seen for the TFR sheet resistance RSTR parameter. The CCM Chua's circuit contains a thin film resistor which, as it has been shown before (Section 4.4), has its influence on the location of equilibrium points. Therefore, high correlation coefficients for the BCB and EMR wafers is well-supported by the numerical

and circuit simulations.

7.4 Conclusions

In summary of this measurement session it can be said that the correlation between the performance of the Chua's circuit CCM and wafer PCM measurements was established even into backend processing. Relatively tight correlation was shown for such key process indicators as saturation and maximum currents, thin film resistor sheet resistance and threshold voltage. At the same time poor or non-existing correlation of certain PCM metrics can be explained by their coarse measurements. Overall it can be said that the achieved results suggest that the Chua's circuit-based CCM makes predictions that sufficiently closely match the prognosis of the PCM. The next stage of the experiment would be to prove the CCM's ability to predict the nonlinear performance of the real functional circuit.

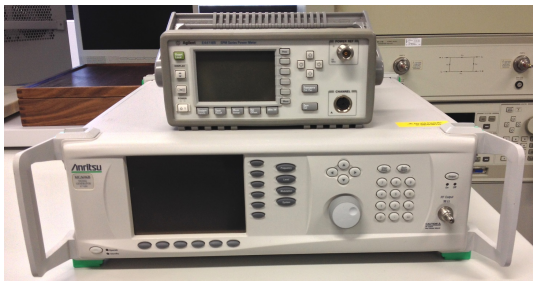
Of the various branches of electrical investigation, perhaps the most interesting and immediately the most promising is that dealing with alternating currents.

Nikola Tesla

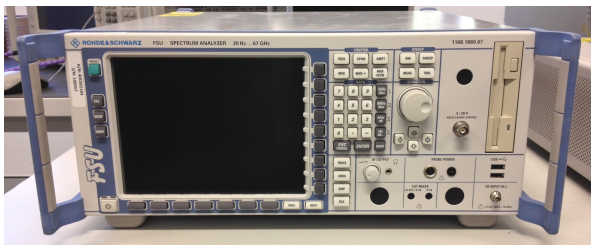
8

CCM and Nonlinear Circuits

The main goal of the CCM is to reliably predict the nonlinear performance of the functional circuits. It has already been shown that the Chua's circuit-based CCM is very sensitive to manufacturing-process parameter variations. Its signal's characteristic, difference between the equilibrium levels, V_{dif} proved itself to perform as an individual circuit's fingerprint. These fingerprints were shown to exhibit variation, which was closely matched by variation of certain PCM parameters. What has been shown proves the viability of the CCM concept, however the main purpose, nonlinear performance prediction, has not been studied hitherto. Consequently another experiment was planned in order to investigate a possible link between the CCM parameter and the nonlinear parameters of the functional circuits.



(a) Agilent Power Meter (top), Anritsu Signal Genrator (bottom)



(b) Rohde & Schwartz Spectrum Analyser

Figure 8.1: The laboratory equipment used in the experiment.

8.1 Nonlinear Circuits Measurements

The mask with the PL-15 version of Chua's circuit also contained functional circuits developed by Macom circuit designers. On the reticle there were two similar driver amplifiers which are coded by numbers 1599 and 1600. It is decided to perform measurements of these drivers' nonlinear characteristic in terms of their 1 dB compression point ($P1dB$). This characteristic gives a fairly good insight into the circuit's nonlinear performance and at the same time is relatively easy to obtain using the available equipment.

The 1 dB compression point indicates the amplifier input power level at which the output level deviates by 1 dB from the extrapolated linear region. The setup for these measurements includes an Anritsu MG3696B 67 GHz signal generator (Fig. 8.1(a)), a Rohde & Schwartz FSU 20 Hz – 67 GHz spectrum analyser (Fig. 8.1(b)), a pair of RF probes for the input and output signals and a DC probe mounted on the probe station. The circuits are powered by the Instek PST-3202 programmable power supply. The test bench is illustrated in Fig. 8.2.

From the specification of the drivers it is found that the centre operational frequency is 28.5 GHz. Therefore the frequency of the signal generator is maintained constant at this value throughout the whole experiment and no frequency-sweeping measurements are performed.

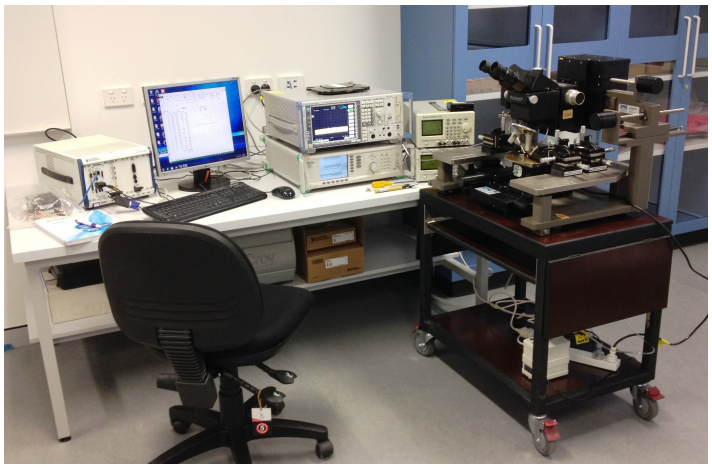


Figure 8.2: The laboratory equipment setup for the *P1dB* measurements.

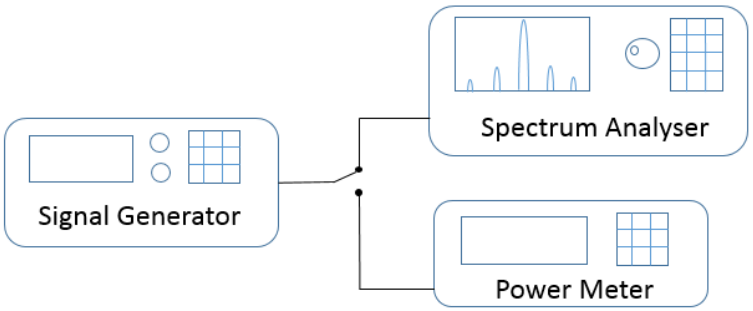


Figure 8.3: Spectrum analyser calibration setup.

Firstly, a calibration of the spectrum analyser is performed, as the drivers' output power is to be measured with its assistance. The signal generator is connected to the power meter with the output power being swept from -5 dBm to 10 dBm and then the power meter is replaced by the spectrum analyser (Fig. 8.3) and the same process repeated. The results are shown in Table 8.1. We can see a slight mismatch between the reading of the power meter and that of the spectrum analyser. Generally the spectrum analyser shows a level which is lower than the power meter measurement by approximately 0.55 dB. Both devices appeared to show good linearity of the measurements. Consequently it is decided that the spectrum analyser can be used for the drivers' output power measurements.

At this point it should be noted that the purpose of the *P1dB* measurements is to

Power out, dBm	Power meter, dBm	Signal generator, dBm
-5	-8.58	-8.04
-4	-7.6	-7.04
-3	-6.58	-6.04
-2	-5.6	-5.04
-1	-4.6	-4.03
0	-3.61	-3.05
1	-2.62	-2.06
2	-1.62	-1.05
3	-0.64	-0.06
4	0.34	0.90
5	1.32	1.90
6	2.29	2.80
7	3.27	3.80
8	4.23	4.80
9	5.2	5.76
10	6.16	6.7

Table 8.1: The results of the spectrum analyser calibration.

obtain the variation of this parameter among the circuits on a quarter-wafer. Therefore absolute, precise values of the 1 dB compression are not compulsory; the major requirement is consistency of the measurement approach during the whole experiment. As a result, the cable and connector losses could be ignored as long as the setup is maintained. The equipment configuration used for the *P1dB* measurements is shown in Fig. 8.4.

The procedure for the 1 dB compression point measurements involves a signal generator power sweep from -18 dBm to 5 dBm with 1 dB increment, which was shown to be a reasonable range to observe the compression on. The driver output power is measured using the spectrum analyser by placing the marker on the peak observed at

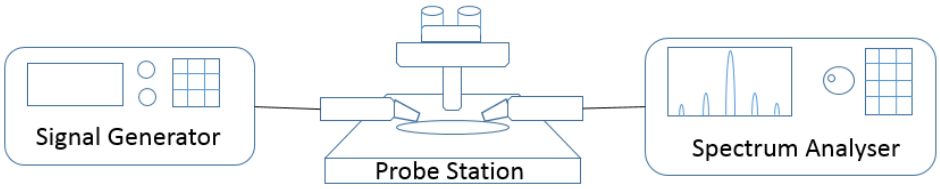


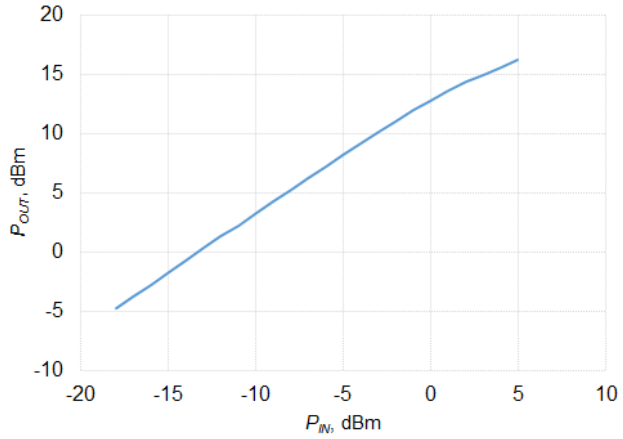
Figure 8.4: The laboratory equipment setup for the *P1dB* measurements.

28.5 GHz. The signal generator is synchronised with the spectrum analyser using the internal reference 10 MHz generator. Every driver circuit (1599 and 1600) is measured on the available three quarter-wafers. The measurement results are presented as tables of output powers recorded for every input power value.

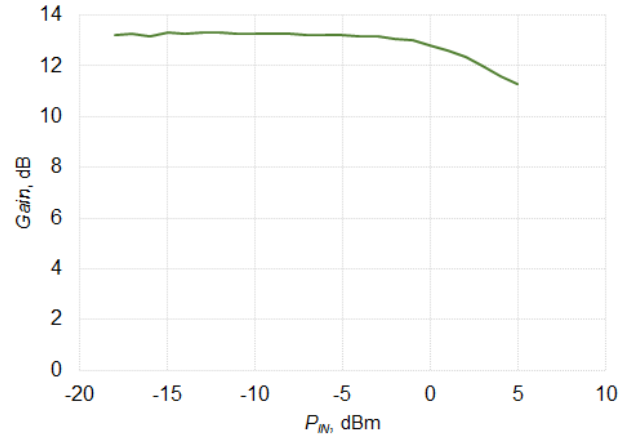
Typical 1599-driver gain-linearity measurement results are presented in Fig. 8.5. Two ways of representing the data are shown. Fig. 8.5(a) shows how output power changes with an increase of input power, while Fig. 8.5(b) demonstrates the change of driver gain for given input powers. Gain is defined simply as input power P_{IN} subtracted from output power P_{OUT}, $Gain = P_{OUT} - P_{IN}$. The second method of data presentation appears to make it easier to get the 1 dB compression point.

However, the *P1dB* of every driver on the wafers is estimated with the help of a Matlab script. The algorithm for the 1 dB compression estimation used the gain data. The stable gain region ($P_{IN} \approx$ -12 dBm – -7 dBm) is used to find the average gain. The 1 dB compression is found as the intersection of the horizontal line 1 dB below the average gain and the experimental curve. The output is given in terms of input power, P_{IN}. When *P1dB* is estimated for all the drivers on the available quarter-wafers it is possible to plot the distribution maps as was done for the CCM's V_{dif} and various PCM parameters.

The results of the measurements are plotted to produce maps for the three quarter-wafers. The distribution of *P1dB* for two drivers are presented on Figs 8.6–8.8. The maps indicate the values of *P1dB* expressed in terms of input power. It is also possible to express *P1dB* in the form of gain, which does not distort the results but makes the



(a) Input power versus output power



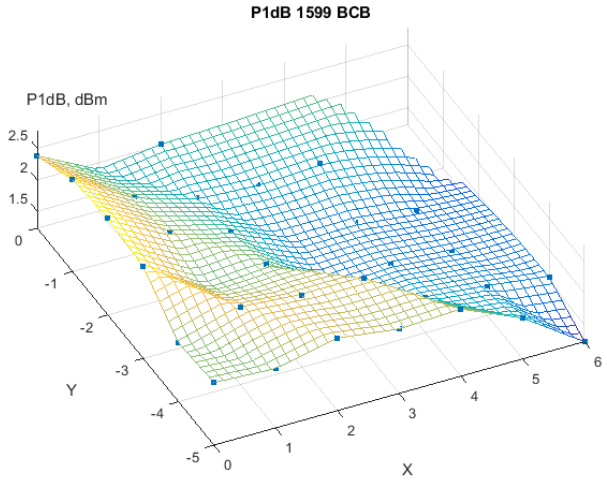
(b) Input power versus gain

Figure 8.5: The 1599 driver measurement results presented in two different ways.

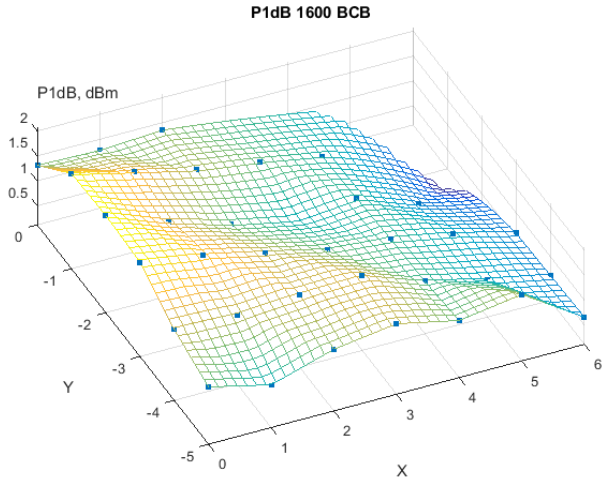
maps somewhat smoother and easier to read.

8.2 Correlation Results

After the circuits' nonlinear parameters in terms of the 1 dB compression point was obtained, it is possible to correlate this data with the parameters of the Chua's circuit CCMs. In order to make the correlation procedure easier it is preferable to normalise the data for correlation. The normalisation procedure brings the values of the parameters to a range between 0 and 1, thus making the comparison and correlation an easier task. The normalisation of a parameter P can be performed employing the following



(a) 1599 Drivers' *P1dB*



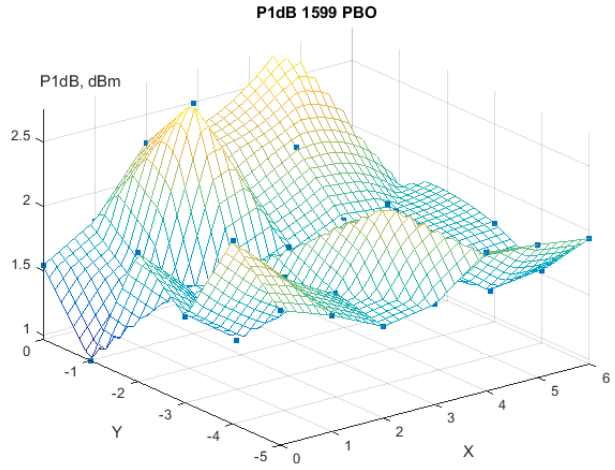
(b) 1599 Drivers' *P1dB*

Figure 8.6: 1 dB compression point of the drivers on the BCB wafer.

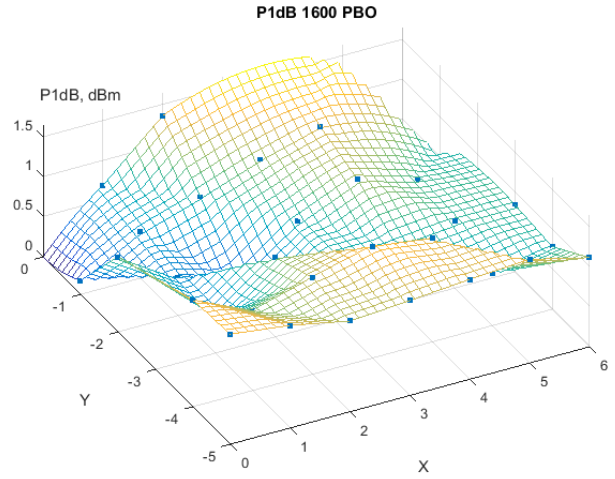
formula:

$$P_{NORM} = \frac{P - P_{MIN}}{P_{MAX} - P_{MIN}} \tag{8.1}$$

For the purposes of comparison, the normalised maps of the CCM and drivers' nonlinear parameters are displayed on Figs 8.9–8.11. We can see a fairly close similarity between the maps for each quarter-wafer. Even the PBO wafer, which did not show



(a) 1599 Drivers' *P1dB*

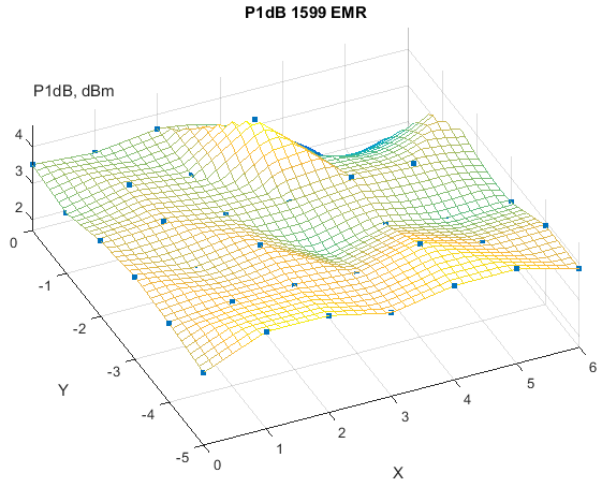


(b) 1599 Drivers' *P1dB*

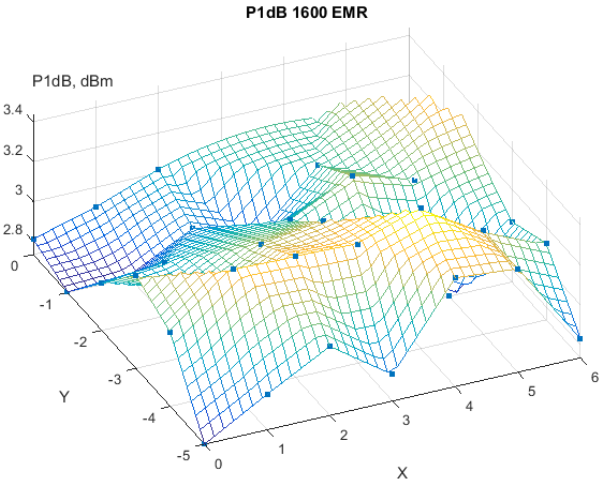
Figure 8.7: 1 dB compression point of the drivers on the PBO wafer.

good results in the case of PCM-parameter correlation, exhibits a good match between the CCM and drivers' parameters, at least visually.

From the map of the reticle (Fig. 8.12), which had been stepped across the available wafers, we can see that the 1599 and 1600 drivers and Chua's circuit are located on the opposite edges. By reference to the wafer map (Fig. 7.3) one can deduce that the drivers located, for example, in the $y = -5$ row, are physically closer to the CCMs of the $y = -4$ row. Therefore it seemed reasonable to correlate the parameters of



(a) 1599 Drivers' *P1dB*

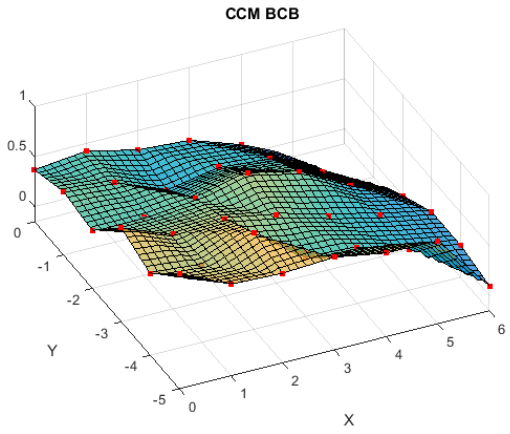


(b) 1599 Drivers' *P1dB*

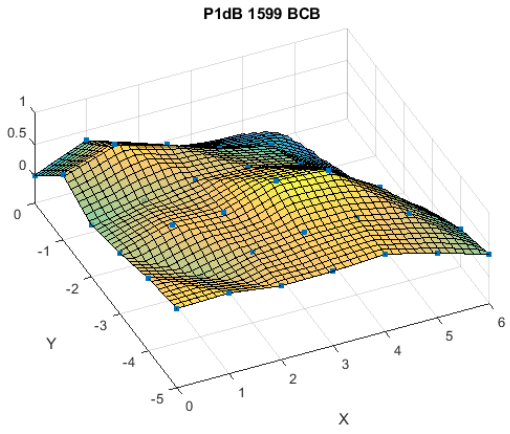
Figure 8.8: 1 dB compression point of the drivers on the EMR wafer.

adjacent circuits rather than those located on the same reticle.

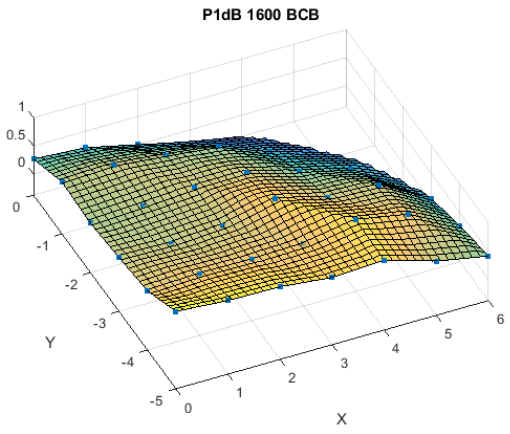
The experimental data are correlated with the help of the Excel *correl* function. The results are presented in Table 8.2. This table displays the values of the correlation coefficient ρ for the normalised CCM's V_{dif} and the normalised drivers' *P1dB* values. As can be seen, correlation between the circuits of the same reticles and adjacent ones was performed. Overall the values of the correlation coefficients for the BCB and



(a) CCM V_{dif}

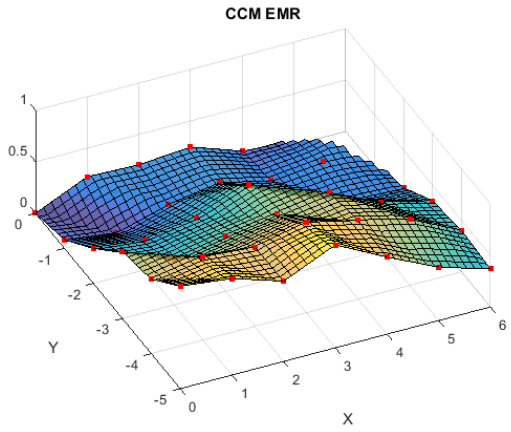


(b) 1599 *P1dB*

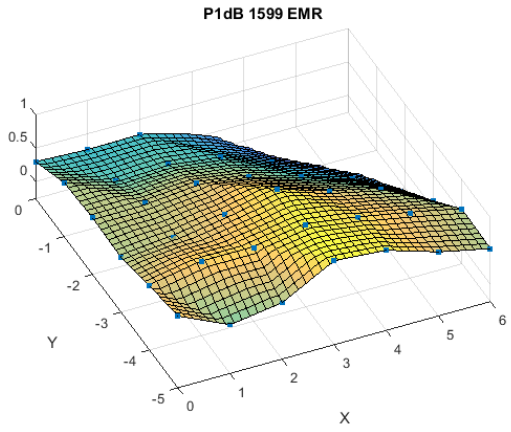


(c) 1600 *P1dB*

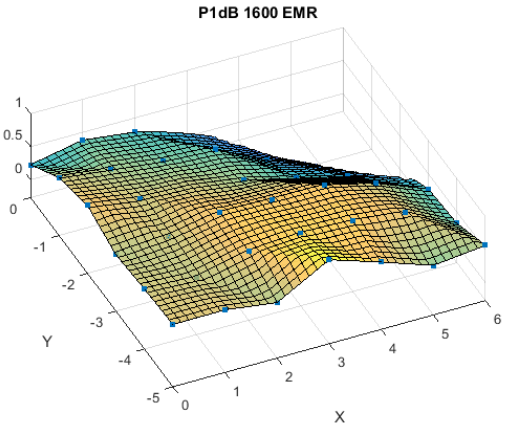
Figure 8.9: Comparison of the normalised parameters of the CCM and drivers on the BCB wafer.



(a) CCM V_{dif}

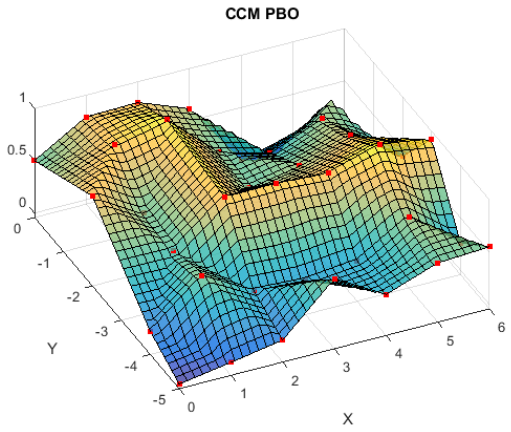


(b) 1599 *P1dB*

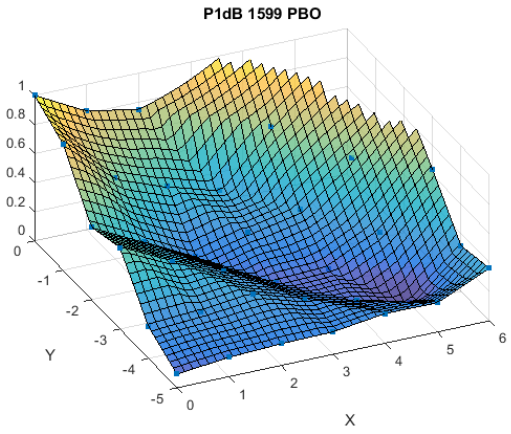


(c) 1600 *P1dB*

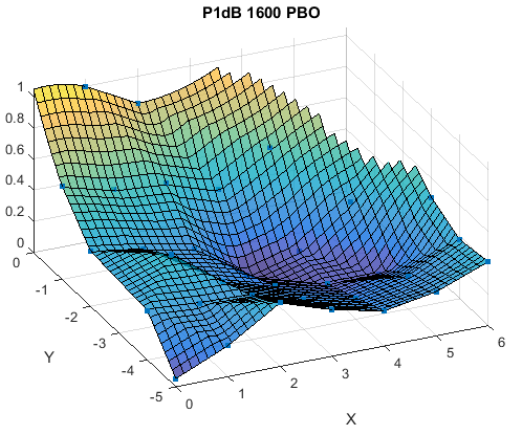
Figure 8.10: Comparison of the normalised parameters of the CCM and drivers on the EMR wafer.



(a) CCM V_{dif}



(b) 1599 *P1dB*



(c) 1600 *P1dB*

Figure 8.11: Comparison of the normalised parameters of the CCM and drivers on the PBO wafer.

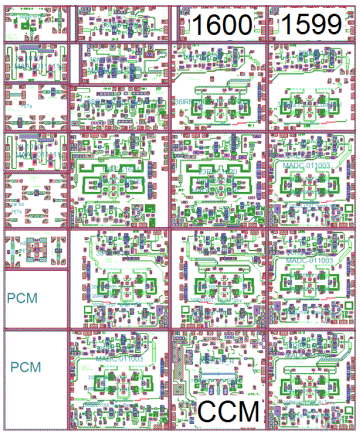


Figure 8.12: The reticle map.

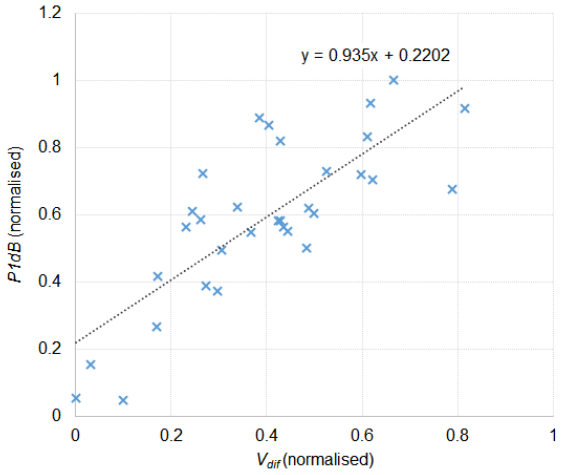
Correlation coefficient ρ

	V_{dif}					
Wafer	BCB		EMR		PBO	
Reticles	Same	Adjacent	Same	Adjacent	Same	Adjacent
1599 *P1dB*	0.55761	0.69117	0.76339	0.6461	0.33656	-0.17976
1600 *P1dB*	0.68907	0.78571	0.71625	0.55916	0.20958	-0.14834

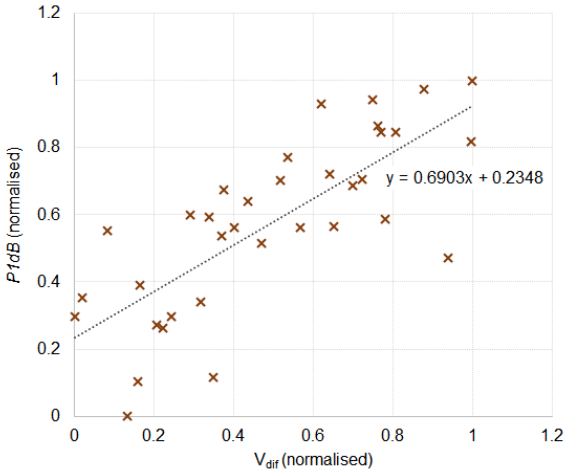
Table 8.2: Correlation coefficients ρ of normalised CCM's V_{dif} and normalised 1599 and 1600 *P1dB*.

EMR wafers appear to be reasonably high, indicating that there exists a link between the performance of Chua's circuit and the driver amplifiers. One can notice that the correlation between adjacent circuits is stronger for the BCB wafer case, while on the EMR wafer circuits of the same reticles were found to have stronger correlation in performance. At the same time, the correlation of the nonlinear performance for the PBO wafer does not look satisfactory and appears to be non-existent. As has already been stated, the reason for that might be inaccurate CCM measurements due to poor probe connectivity.

We can also present data graphically by plotting the CCM's V_{dif} versus driver's *P1dB* for either the same or adjacent reticles. In this case the dispersion of data can be seen. Two graphs for the cases of best correlation coefficients are shown on Fig. 8.13. The trend-line equations are also presented on the plots to indicate the relation



(a) BCB Wafer, same reticles



(b) EMR Wafer, adjacent reticles

Figure 8.13: Plotting CCM's V_{dif} versus driver's *P1dB*.

between V_{dif} and *P1dB*.

8.3 Conclusions

A reasonably strong correlation between Chua's circuit's equilibrium-voltage level difference and the driver amplifier's nonlinear characteristic in terms of the 1 dB compression point was observed. This suggests that the proposed CCM is capable of predicting the nonlinear behaviour of functional circuits. However, it should also be stated, that

additional data on functional circuits' nonlinear performance is needed for statistically more significant results.

Chaos is inherent in all compounded things. Strive on with diligence.

Buddha

9 Conclusions

9.1 Work Scope

The research showed that circuit-based manufacturing process monitoring is a feasible concept and can be done with the help of chaotic Chua's circuit. The results of the experiments allow us to say that CCM performance is closely correlated with the small-signal transistor parameters and large-signal nonlinear circuit parameters as well.

The author realises that process control of the semiconductor manufacturing has a number of drawbacks and approaches that can be taken to address these issues are numerous too. However the scope of this work was to show that signals generated by sensitive chaotic systems have certain featured that can be attributed to the state of the system's components. The main purpose of this project was to prove that chaotic circuits can be applied for the role of semiconductor process monitoring. And it was

shown on the example of the simplest chaotic oscillator, Chua's circuit. Further work in this direction can include the investigation of different chaotic oscillators such as Duffing oscillator or any other circuit developed from nonlinear chaotic equations. Presumably the features of these oscillators would be connected with a manufacturing process state in a different way than in Chua's circuit and a combination of several oscillators in a CCM can give even better insight into the manufacturing process condition and status of other nonlinear circuits.

9.1.1 Project Summary

The purpose of the presented work was to prove the viability of a novel approach to the compound semiconductor process monitoring. The new method is to apply a so-called circuit control monitor (CCM) which involves using simple nonlinear circuits for the purpose of estimating manufacturing process state and predicting the yield.

The motivation of developing a new control mechanism came from the conventional PCM's poor ability of predicting circuit's nonlinear behaviour. Small-signal FET parameters can be extracted during the PCM measurements. These parameters are later incorporated into FET models used by circuit designers. However, models are only valid for a range of bias at which the parameters had been extracted, with only a short extra range to which they could be extrapolated. Therefore, designers use the models which have a limited validity.

It is possible that FETs in functional circuits are biased in a different way then the devices of a PCM. Consequently, when a PCM is measured, results can be acceptable while the actual circuit is working in an unexpected manner. Furthermore, the performance of a nonlinear circuit is not only defined by the active device small-signal parameters – multiple nonlinear effects come into play, making it impossible to predict the behaviour based solely on the linear measurement results.

Therefore, our proposal is to see how nonlinear behaviour is correlated between different circuits. In our proposed concept we want to use a small and simple nonlinear circuit for controlling the functionality of real circuits located alongside with it on a semiconductor wafer.

The work investigated Chua's chaotic oscillator as a candidate for the role of CCM. During the project a careful analysis of the operation of Chua's circuit was carried out. The analysis employed numerical simulations in Matlab and circuit simulations in AWR Design Environment. A study of the literature on chaotic systems and circuits was performed to identify the characteristic features of chaotic signals.

As a result of the literature survey and various simulations it was found that the equilibrium points of such a chaotic system as Chua's circuit can work as a good indicator or fingerprint of individual oscillators. The equations that govern the behaviour of Chua's circuit and therefore specify the coordinates of the equilibrium points suggested that the location of the equilibria strongly depends on the current-voltage function of the nonlinear resistor, or Chua's diode as it is also called. This circuit component contains active devices, whose performance needs an evaluation during the CCM testing; hence the location of the equilibrium points can give a good insight into the transistor performance. Consequently, we have a link between the circuit's measurable nonlinear signals and the state of the manufacturing process.

The functionality of Chua's oscillator was first tested on a circuit-board level using discrete components and then an integrated-circuit realisation was designed. The integrated circuit was manufactured employing a gallium arsenide pHEMT process. Two different designs were suggested, the second being an improved version of the first, addressed the known issues. The challenge in the design of the pHEMT inverter, part of the Chua's diode, was the lack of complementary logic and the high transconductance of the pHEMTs, which are normally not used in this kind of application.

The solid-state electronic circuits were measured on the wafer and the generated signals were analysed. The first implementation of Chua's circuit in GaAs showed the conceptual feasibility of the GaAs oscillator implementation, however it failed to show a fully chaotic behaviour.

The succeeding version of Chua's circuit included a number of improvements, on both schematic and layout levels. As a result, chaotic features were observed in the measured signals. A special algorithm was developed to automatically find the equilibrium levels from the measured time-series data, and it significantly reduced the time

required for the measurement analysis. Moreover it was chosen to characterise each individual oscillator by the separation of the equilibrium capacitor voltage levels, referred to as V_{dif}.

With the help of generated Matlab plots it was shown that the circuit's performance varies depending on its location on the wafer. That variation was shown to be non-random and dependent on the manufacturing-parameter fluctuations across the wafer. That was seen after the correlation of the Chua's circuit characteristic in the form of equilibrium-level separation and different PCM parameters. The correlation process resulted in finding fairly high correlation coefficients between the CCM characteristic and certain PCM parameters.

The reticles on which the designed circuit was located also contained other functional circuits, including two similar driver amplifiers. It was selected to estimate the variation of their nonlinear performance across the wafer in order to check it for similarity with the performance of the proposed CCM. For that purpose the 1 dB compression point of the two drivers was measured for all the circuits on the quarter-wafers in our possession. Thus *P1dB* was correlated with the equilibrium-voltage level separation, and a close match between the two was observed. The correlation coefficients appeared to be rather high for the circuits of BCB and partial EMR backend processes, however much poorer similarity was observed on the PBO polymer packaged wafer. The most probable reason is not the effect of the circuit-level packaging materials but rather erroneous CCM measurement data of the last wafer which resulted from the worn-out RF pads. The presentation of data in the form of parameter wafer maps allowed a visual comparison between the CCM and driver nonlinear characteristics.

The results obtained throughout the whole experiment strongly favoured our assumption that the CCM can be a good predictor of the manufacturing process state as well as the performance of complex nonlinear circuits. Needless to say, that further investigation of the CCM concept is required before incorporating it into production. First of all, appropriate ranges of V_{dif} have to be specified in order to predict faulty reticles. Much more statistical data are needed in order to define the values of the equilibria separation that correspond to a faulty behaviour. Secondly, even though the

CCM, at least in principle, is able to predict the yield, the process control monitor is still required for the device parameter extraction. However, it is assumed that using both the CCM and the PCM can maximise the predictability of the process control mechanism and minimise the response time, i.e. the time between wafer production and fault detection.

The benefit of a CCM is that it does not require complicated measuring equipment and can be organised employing such a platform as LabView, in which it is possible to incorporate all the scripts for equilibria detection and thus perform automated wafer tests. The advantage of an oscillator-based CCM is that only DC source is required for powering the circuits, no external signal generators are needed. Measurements can be done using an oscilloscope, which does not require frequent calibration.

The area of the designed CCM is approximately 17% of the PCM area used in that experimental run. However we assume that benefits of using a CCM can exceed a disadvantage of reducing the functional area. Moreover it is possible to greatly optimise the layout in order to reduce the occupied area.

A general rule of quality control is that the expected commercial benefits should outweigh the costs of introducing a new control method. We regard our method relatively simple and inexpensive for implementation. The author thinks that after obtaining more statistical data on the CCM it would be possible to incorporate this type of monitor into the existing process control mechanisms and consequently improve the methods of semiconductor manufacturing quality control.

There is a number of improvements that can be done in the layout of the existent circuit. It is possible to optimise the design to save the area on the wafer or even to completely reconsider the chaotic oscillator implementation approach.

9.2 Suggested Improvements and Future Work

It was shown that the developed design is functional and is capable of operating as a CCM. However there are still certain matters that can be improved.

During the experiments we did not monitor the voltage across capacitor C_2, thus

we did not utilise the V_{C2} RF pads. That means that we can remove them to use area more efficiently. Furthermore, as has been stated before, the RF pads allowed measuring capacitor potentials relative to ground, however measuring the voltage across the capacitor could be more indicative.

We assume that a higher resonance frequency increases a circuit's degree of nonlinearity, thus making it more sensitive to different parameter fluctuations. That said, we can try to make the capacitors smaller, both size-wise and capacitance-wise. Reducing the capacitor dimensions and changing the aspect ratios can help in optimising the occupied area.

Taking all those suggestions into account, a new design was sketched for hypothetical further tapeouts (Fig. 9.1). The new dimensions are approximately 777 μm by 695 μm thus making the occupied area equal to approximately 0.5403 mm^2 versus 0.9425 mm^2 for the manufactured CCM.

The circuit is capable of generating chaotic signals, as can be seen from Fig. 9.2. Time-consuming EM simulations were not performed, therefore it is possible that further layout modification is necessary to make the oscillator operational.

One disadvantage of the optimised design is that the pad for V_{C1} has the line connecting the outer pads lying too close to the signal pad, which may result in damaging the line by a probe during measurements. However, taking into account the experimental nature of the design, this problem could be overcome by taking care during the circuit testing. Otherwise this layout can be changed for a production CCM, planning the pads appropriately for automated probe testing.

The area occupied by the PCM on the reticles with the designed PL-15 Chua's circuit is approximately 5.52 mm^2. Our CCM design has an area of around 17 % of this value. The optimised design would be less than 10 % of the PCM area. In production runs the PCM area could be even bigger, reaching up to 6.5 mm^2 for a 400 mm^2 reticle.

Another possible improvement that can be made involves reconsideration of the

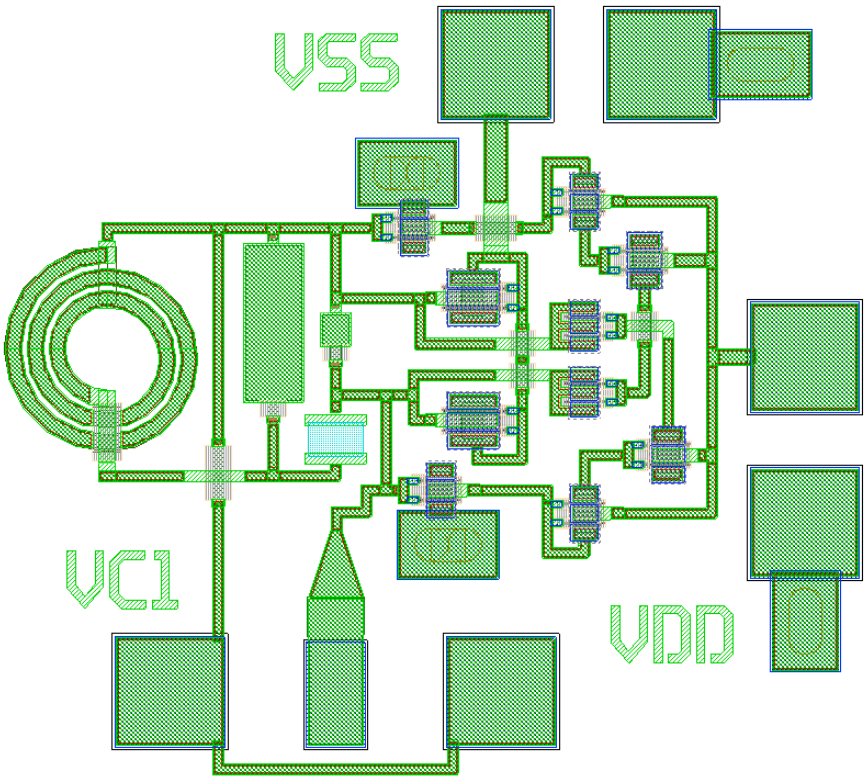


Figure 9.1: Suggested improved CCM design.

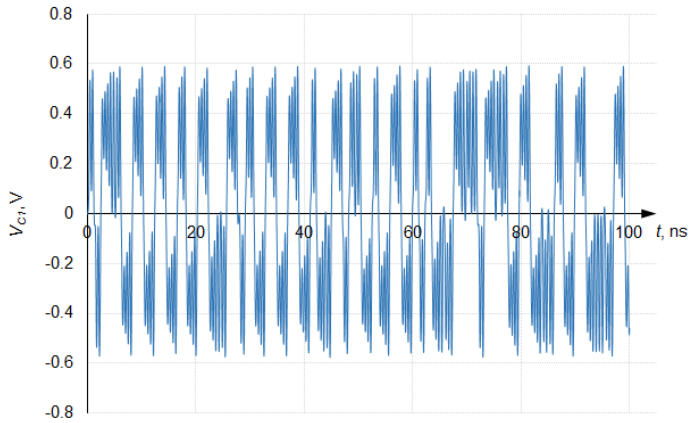
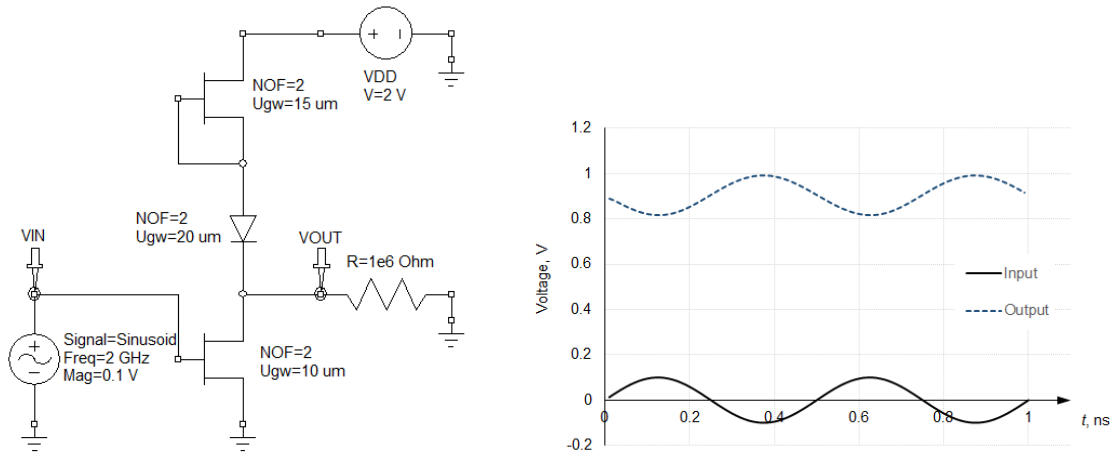


Figure 9.2: Time-domain simulation of V_{C1}.

NR schematic. The current NR employs saturated-buffer logic with four pHEMTs and one diode in each inverter. If we could come up with a different inverter schematic involving fewer pHEMT devices we would make our CCM more compact. The draft of an optimised inverter and its performance in the time domain are presented in Fig.



(a) Scematic of optimised inverter (b) Response of the inverter to a sinusoidal input

FIGURE 9.3: Optimised inverter design.

9.3.

As can be seen from Fig. 9.3(a) this circuit involves only two pHEMTs and one diode. The gate widths used are also small. This circuit functions as an inverter as supported by Fig. 9.3(b). Moreover this graph shows that the input signal is not only inverted but also is level-shifted. This voltage shift does not allow a cross-coupled pair of these inverters to produce a current-voltage characteristic with a negative slope. Although it is possible to include more level-shift diodes and thus move the output signal closer to the input signal (that is, remove the offset), this still does not help with generating a negative conductance of the NR characteristic.

This inverter design proves that it is possible to perform inversion with fewer pHEMT devices than in saturated-buffer logic, however a method for level-shifting the output signal has to be developed.

Approximately half of the CCM's area is occupied by passive components. This is possibly the biggest drawback of the suggested candidate because designers try to avoid bulky capacitors and especially inductors in the IC layout. Therefore this CCM can be significantly improved if the resonator is removed from the CCM and placed off-chip in a custom-made test probe. Such a modification would reduce the CCM's size quite notably. Furthermore, the oscillator's behaviour will not be affected by variations of TFR sheet resistance and MIM capacitance across the wafer. Therefore

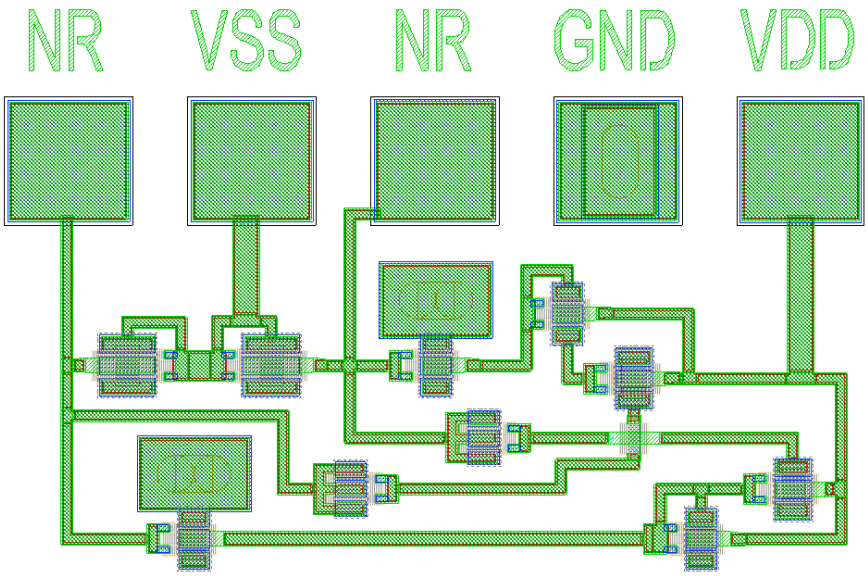


Figure 9.4: Layout of the NR-based CCM for external resonator.

the performance of the oscillator would be dependent on the pHEMTs' condition *only*.

The draft layout of a nonlinear-resistor-only CCM is shown in Fig. 9.4. It is presumed that a custom probe would be designed with the resonator placed between the 'NR' contact pins. This layout has dimensions of approximately 705 μm by 455 μm including pad labels (390 μm excluding the labels). Thus this CCM would occupy only 0.275 mm^2 (labels excluded) therefore being only 30 % of the produced CCM's area. A new design of the NR could decrease the size ever further. Another advantage of this design is the possibility of measuring the NR's current-voltage characteristic, thus the theoretical location of the equilibrium points could be calculated.

A production version of the Chua's circuit-based CCM should have pads which can accommodate automated probes. Moreover, a computer program has to be developed for interpreting the measured signals and storing their characteristics. This program has to include an algorithm for locating the equilibrium levels. The current algorithm is quite accurate, however better noise-filtering techniques could improve the accuracy of equilibrium-level estimation. The measurement systems can be based on such a widespread platform as LabView or similar.

The testing procedure could be performed in the following manner. The PCM and

CCM are tested in a single operation and their results are combined to get a good insight into the manufacturing process state and the condition of the real circuits on the wafer. It is important to obtain good statistical data on not only the reticle-to-reticle variation of the CCM characteristics but also wafer-to-wafer and batch-to-batch changes, in order to see how these fluctuations correlate with PCM parameters. As a result, it would be possible to develop a reliable yield-predicting model.

The author believes that, after addressing all known issues of the manufactured CCM and applying suggested changes, this CCM would greatly expand the capabilities of a PCM and considerably improve the yield-prediction accuracy.

A

Appendix A: Matlab program listings

This appendix contains listings of Matlab scripts used during the course of this project.

Listing of the Matlab script for solving Chua's equations with a cubic nonlinearity, plotting the signal spectrum and attractor with the eigenplanes.

```
clear all;
clc;

%Circuit parameters
C1 = 1e-9;
C2 = 10e-9;
L = 220e-6;
R = 600;
RL = 1;
```

```
G = 1/R;

%Calculating dimensionless coefficients
alpha = C2/C1;
beta = R^2*C2/L;
gamma = R*RL*C2/L;

%Cubic nonlinearity paramteters;
a = 0.297;
c = -1.257;

%Chua's Equations
F = @(t,y) [ alpha*(y(2,:)-y(1,:)-a*y(1,:)^3-c*y(1,:));
    y(1,:)-y(2,:)+y(3,:);
    -beta*(y(2,:))-gamma*(y(3,:)) ];

%Equilibrium point coordinates calculation
xec = sqrt(-(c*gamma+beta*c+beta)/(a*(gamma+beta)));
yec = xec*gamma/(gamma+beta);
zec = -beta*yec/gamma;

%Jacobian matrices
M1 = [-alpha*(1+3*a*xec^2+c) alpha 0; 1 -1 1; 0 -beta gamma];
M0 = [-alpha-alpha*c alpha 0; 1 -1 1; 0 -beta gamma];

%Finding eigenvalues of Jacobian matrices
eigen0 = eig(M0);
eigen1 = eig(M1);

%Extracting real eigenvalues
```

```
gam0 = eigen0(1);
gam1 = eigen1(1);

%Simulation time
N = 100;

%Initial conditions
yo = [.001;.0015;.05];

%Solving Chua's equations
[tsc, ysc]  = ode45(F, [0 N], yo);

%FFT analysis starts here
y1t = ysc(:,1);  %analysis of Vc1

Nsamps = length(y1t);
Fs = 5e6;
t = (1/Fs)*(1:Nsamps);          %Prepare time data for plot

%Raised Cosine Filter
for i = 1:Nsamps
y1(i) = y1t(i)*(1-cos(2*pi*i/Nsamps));
end

%Do Fourier Transform
y_fft = abs(fft(y1t));            %Retain Magnitude
y_fft = y_fft(1:Nsamps/2);      %Discard Half of Points

f = Fs*(0:Nsamps/2-1)/Nsamps;   %Prepare frequency data for plot
```

```
%Plotting the Vc1 spectrum
figure
grid on;
plot(f, log(y_fft));

%Attractor analysis starts here

%Defining the sizes of planes
xm=linspace(-0.5,-1.5,15);
ym=linspace(-0.3,0.3,15);
xp=linspace(0.5,1.5,15);
yp=linspace(-0.3,0.3,15);
xo=linspace(-0.4,0.4,15);
yo=linspace(-0.4,0.4,15);
[xm,ym]=meshgrid(xm,ym);
[xp,yp]=meshgrid(xp,yp);
[xo,yo]=meshgrid(xo,yo);

%Origin equilibrium point planes
Er0 = -beta*xo / ((1+gam0)*(gamma+gam0)+beta) + beta*yo / (gam0+gamma); %real
Ec0 = -xo* ((1+gam0)*(gamma+gam0)+beta) / alpha - (gam0+gamma)*yo; %c.c.

%Non-trivial equilibrium points real eigenvalue planes
ErPm = -1/alpha*(((1+gam1)*(gamma+gam1)+beta)*(xm+xec))-(gamma+gam1)*(ym-yec)
-0.97*zec;
ErPp = -1/alpha*(((1+gam1)*(gamma+gam1)+beta)*(xp-xec))-(gamma+gam1)*(yp+yec)
+0.97*zec;

%Plotting the attractor with eigenplanes
figure
```

```
zlim ([-2, 2]);
ylim ([-2, 2]);
xlim ([-2, 2]);
hold on
grid on
axis tight
box on
plot3(ysc(:,1), ysc(:,2), ysc(:,3),'LineWidth', 1.1)
scatter3(xec,yec,zec);
surface(xo,yo,Ec0,'EdgeColor',[1 0.8 0.9], 'FaceColor', [1 1 0.1],
 'FaceAlpha', 0.7)
surface(xp,yp,ErPp,'EdgeColor',[1 0.25 0.7], 'FaceColor', [1 0.3 0.7],
 'FaceAlpha', 0.7)
surface(xm,ym,ErPm,'EdgeColor',[1 0.25 0.7], 'FaceColor', [1 0.3 0.7],
 'FaceAlpha', 0.7)

%Bifurcation analysis can go here
```

Loop for plotting the bifurcation diagram (Author: Mike Audet)

```
for R=Rmin:Rstep:Rmax
    clc;
    percomp = (R - Rmin)/(Rmax - Rmin)*100;
    beta = R.*R.*C2./L;
    gamma = R.*RL.*C2./L;
    disp([num2str(percomp) '% completed']); %Displaying the progress in %

    %Chua's equations
    %F = @(t,y) [ alpha*(y(2,:)-y(1,:)-a*y(1,:)^3-c*y(1,:));
```

```
    y(1,:)-y(2,:)+y(3,:); -beta*(y(2,:))-gamma*(y(3,:)) ];

%Initial conditions
    yo = [.1;.15;.05];

    %Solving the Chua's equations
    [ts, ys]  = ode45(F, [0 N], yo, odeset('reltol', 1e-6, 'abstol', 1e-9));
m1 = yec/xec;
    b1 = 0;
    for k=length(ys)-1000:length(ys)-1
        flag = 0;
     if ys(k,2)>(m1*ys(k,1))
         flag = flag+1;
     else
         flag = flag-1;
     end
     if ys(k+1,2)>(m1*ys(k+1,1))
         flag = flag+1;
     else
         flag = flag-1;
     end
     if flag == 0   %this will calculate the intersection
      %and plot the point on the bifurcation
            m2 = (ys(k+1,2)-ys(k,2))/(ys(k+1,1)-ys(k,1));
            b2 = ys(k,2)-m2*ys(k,1);
         if m1-m2 ~= 0
            hold on; plot(R,(-b1+b2)/(m1-m2), '.k', 'markersize', 3);
         end
     end
    end
```

```
end
```

The script for finding equilibrium levels from noiseless data.

```
clear all;
clc;

%Reading the time-series from a text file
[A] = textread('vc1.txt', '%f');

%Define the lenth of the series
l = length(A);

%Plot the time-series data
figure
plot (A)

%Dividing the series into above-0 and below-0
for i = 1:l;
    if (A(i)>mean(A))
        Bn(i) = mean(A);
        Bp(i) = A(i);
    else
        Bn(i) = -A(i);
        Bp(i) = mean(A);
    end
end

%Inverting series for minima search
for i = 1:l;
```

```
   Cp(i) = -Bp(i);
   Cn(i) = -Bn(i);
end

%Defining median lines as threshold levels
mp = max(Bp)/2;
mn = max(Bn)/2;

%Declining the data below threshold levels
for i = 1:l;
   if (Bp(i)<mp)
       Bp(i) = 0;
   else Bp(i) = Bp(i);
   end
   if (Bn(i)<mn)
       Bn(i) = 0;
   else Bn(i) = Bn(i);
  end
  if (Cp(i)>mp)
       Cp(i) = 0;
   else Cp(i) = Cp(i);
  end
  if (Cn(i)>mn)
       Cn(i) = 0;
       else Cn(i) = Cn(i);
  end
end

%Finding peak for positive data
pkspp = findpeaks(Bp);
```

```
pksmp = -findpeaks(Cp);

%Finding peaks for negative data
pkspn = findpeaks(Bn);
pksmn = -findpeaks(Cn);

%Finding equilibrium points as median distance between minimum upper peak
%and maximum lower peak
a = min(pkspp);
b = max(pksmp);
pp = b + (a-b)/2;

a1 = min(pkspn);
b1 = max(pksmn);
pn = b1 + (a1-b1)/2;

%Length of the equilibrium-level line
len = min(length(pkspp), length(pksmp));
len1 = min(length(pkspn), length(pksmn));

%Plot of peaks on upper side
figure
hold on;
xlabel('Peaks');
ylabel('Vc1, V');
plot (pkspp, 'm')
plot (pksmp, 'm')
%Positive equilibrium-level line
line ([0 len], [pp, pp],'Color', 'k', 'LineStyle', '--', 'LineWidth', 1)
%Plot of peaks on lower side
```

```
hold on;
plot (-pkspn, 'r')
plot (-pksmn, 'r')
%Negative equilibrium-level line
line ([0 len1], [-pn, -pn],'Color', 'k', 'LineStyle', '--', 'LineWidth', 1)

%Printing the values of equilibrium level
fprintf('Positive equilibrium point:');
disp(pp);
fprintf('Negative equilibrium point:');
disp(-pn);
```

The script for plotting PCM, CCM and P1dB wafer maps.

```
clear all;
clc;
%CCM
s = pwd; %Matlab Directory

%Prepare the list of files in the directory
matfiles = dir(fullfile(s,'LVM','TXT','BCB','*.txt'));
nf = length(matfiles); %Define the number of files

for i = 1:nf
%The path to the file to read
    vcpath = fullfile(s,'LVM','TXT','BCB',matfiles(i).name);
    %Reading the data from the file into the array
    [A] = textread(vcpath, '%f');

    %Reading coordinates from filename
```

```
    Ab = matfiles(i).name; %Recording the name of the read file
    xco(i) = sscanf(Ab(1),'%d'); %First character is x-coordinate
    TF = strcmpi(Ab(3), '-');
    if TF == true
        yco(i) = - sscanf(Ab(4), '%d'); %Fourth character is y-coordinate
        else yco(i) = sscanf(Ab(3), '%d'); %For the case of 0 coordinate
    end;

    %Statistical equilibrium levels locator starts here
    peaksup = findpeaks(A); %Finding positive peaks
    peaksdown = -findpeaks(-A); %Finding negative peaks
    pksu = peaksup(:);
    pksd = peaksdown(:);
    AYmin = min(A); %Define the top limit
    AYmax = max(A); %Define the bottom limit
    %Plot the peaks density function for positive peaks
    [fru, x] = ksdensity(pksu);
    %Plot the peaks density function for negative peaks
    [frd, x2] = ksdensity(pksd);

%Finding the intersections of the two density functions
    [xo,yo] = intersections(x, fru, x2, frd);

%For the case when the top intersection comes above the equilibrium
    if abs(AYmax-max(xo)) < 0.012 %
        pplus = xo(2);
    else
  %Defining the equilibrium point as the highest intersection
      pplus = max(xo);
    end
```

```
%For the case when the bottom intersection comes beyond the equilibrium
    if abs(AYmin-min(xo)) < 0.005
        pmin = xo(2);
    else
        %Defining the equilibrium point as the lowest intersection
        pmin = min(xo);
    end

    EQM(i) = pmin; %Recording the negative equilibrium coordinate
    EQP(i) = pplus; %Recording the positive equilibrium coordinate
    DCO(i) = abs(pplus - pmin); %Distance between the points

end

%Normalising the equilibrium separation
DCOn = abs((DCO - max(DCO))/(max(DCO)-min(DCO)));

%Preparing the meshgrid
xlin = linspace(min(xco), max(xco), 40);
ylin = linspace(min(yco), max(yco), 40);
[A, B] = meshgrid(xlin, ylin);
fp = scatteredInterpolant(xco',yco',DCOn');
Cp = fp(A, B);

%Omit the surface outside radius 7
roy = zeros(40,40);
for i = 1:(40^2)
   roy(i) = ((A(i)).^2) + ((B(i)+5).^2);
   if roy(i) > (7^2)
```

```
        Cp(i) = NaN;
    end
end

figure
hold on;
axis tight;
surf(A,B,Cp, 'FaceAlpha', 0.75)
axis tight;
plot3(xco,yco,DCOn,'r.','markersize', 15);
grid on;
xlabel('X');
ylabel('Y');
title('CCM BCB');

clear all;

%Driver P1dB
%reading x coordinates
xc = csvread('BP287/bcb1600p1db.csv',0,0,[0,0,0,34]);
%reading y coordinates
yc = csvread('BP287/bcb1600p1db.csv',1,0,[1,0,1,34]);
%reading gain
G = csvread('BP287/bcb1600p1db.csv',2,0,[2,0,25,34]);
y = G(:,2);

for i=1:24
    k = i-19;
    %constructing Pin series
    x(i)=k;
```

```
end

for i=1:length(xc)
    y = G(:,i)'; %write gain values
    xq = linspace(-18, 5, 100);
    vq = interp1(x,y,xq,'linear');
    %Setting the range for small signal gain
    ssg = y(6:12);
    %Finding the small signal gain and point 1dB below
    gain1db = mean(ssg) - 1;
    %Line of 1dB below the small signal gain
    gain1dbline = repmat(gain1db,1,length(xq));
    %Finding the coordinates of P1dB
    [x0,y0] = intersections(xq,vq,xq,gain1dbline);
    TF = isempty(y0);
    if TF == 0
    p1db(i) = y0(1); %Output P1dB
    else
        disp(xc(i));
        p1db(i) = p1db(i-1);
    end

end

%Normalising P1dB
p1dbn = (p1db - min(p1db))/(max(p1db) - min(p1db));

%Plotting the P1dB wafer map
xlin = linspace(min(xc), max(xc), 40);
ylin = linspace(min(yc), max(yc), 40);
```

```
[A, B] = meshgrid(xlin, ylin);
f = scatteredInterpolant(xc',yc',p1dbn');
C = f(A, B);

%Make the surface of radius 7
ro = zeros(40,40);
for i = 1:(40^2)
   ro(i) = ((A(i)).^2) + ((B(i)+5).^2);
   if ro(i) > (7^2)
       C(i) = NaN;
   end
end

figure
surf(A,B,C, 'FaceAlpha', 0.75)
axis tight; hold on
plot3(xc,yc,p1dbn,'.','markersize', 15);
title('P1dB 1600 BCB');
xlabel('X');
ylabel('Y');

%PCM
%Reading coordinates
X = csvread('287-bcb-101qrt.csv',0,0,[0,0,8,0]);
Y = csvread('287-bcb-101qrt.csv',0,1,[0,1,8,1]);

%Reading Parameters
PARAM = csvread('287-bcb-101qrt.csv',0,2,[0,2,8,12]);

GM = PARAM(:,1); %Maximum gm of FET @ Vds=1.5V
```

```
IDSS = PARAM(:,2); %Drain current of FET @ Vgs=0V, Vds=1.5V
ISEP = PARAM(:,3); %Epi isolation leakage current @ 10V
IDMAX = PARAM(:,4); %Drain current of FET @ Vgs=0.5V, Vds=1.5V
RSEP = PARAM(:,5); %TLM Epi sheet resistance
RSTR = PARAM(:,6); %TLM TFR sheet resistance
VDG = PARAM(:,7); %Breakage between Gate-Drain @ 1mA/mm
VGMP = PARAM(:,8); %Vgs @ Gm peak
VPO = PARAM(:,9); %Threshold Voltage @ Vds=1.5V
VTO = PARAM(:,10); %Pinch-off voltage @ Vds=1.5V, Ids=1mA/mm
IPO = PARAM(:,11); %Pinch-off current @ Vgs=-2V, Vds=1.5V %Vdiff data

xlin = linspace(min(X), max(X), 20);
ylin = linspace(min(Y), max(Y), 20);
[A, B] = meshgrid(xlin, ylin);
f = scatteredInterpolant(X,Y,VTO);
C = f(A, B);

%Omit the surface outside radius 7
roy = zeros(20,20);
for i = 1:(20^2)
   roy(i) = ((A(i)).^2) + ((B(i)+6).^2);
   if roy(i) > (7^2)
       C(i) = NaN;
   end
end

%Plotting the PCM data
figure
surf(A,B,C, 'EdgeColor', 'none')
axis tight; hold on
```

```
plot3(X,Y,VTO,'.','markersize', 15)
title('VTO BCB');
xlabel('X');
ylabel('Y');
```

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