GaN Power Switches for X-Band RFPA Supply Modulators

by

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Abstract

High Power Amplifier is the most critical element within a multifunctional transceiver chip. The need for high linearity and high output power for RF input signals with a high peak-to-peak average power ratio makes the design of high power amplifiers extremely challenging. Drain bias modulation techniques like envelope tracking is used to improve the efficiency of a wideband power amplifier by modulating the drain supply voltage to the envelope of the input RF signal using an envelope amplifier. The critical element within an envelope amplifier is the high frequency switch-mode power converter. The key enabler for delivering high efficiencies at high switching frequencies within an envelope amplifier is the power switch.

The low on-resistance and input capacitance of RF GaN HEMT transistors make them ideal candidates as power switches. The integration of power switches within a high power amplifier would allow the minimization of all circuit parasitics, enabling delivery of high voltage and high currents at an extremely high slew rate to the drain of the high power amplifier.

This thesis investigates the above mentioned properties and presents the use of commercial foundry GaN HEMTs as power switches for RF power amplifier supply modulators. Pulsed I-V characterisation was undertaken to study the impact of trapping on switch efficiency as well as a transient analysis in a hybrid implementation. MMIC supply modulators fabricated in 0.25 μm GaN process delivering an output power of 40 dBm with measured efficiencies over 80%.

A modulator integrated X-Band HPA was designed and fabricated in 0.25 μm GaN

process. The calculated PAE for the supply modulated HPA at a drain bias of 20 V was 26.65% with an output power of 35 dBm. This is the first reported supply modulator integrated HPA in a 0.25 μm GaN process, and will enable on chip supply modulation capability for use with efficiency enhancement techniques like ET, to deliver high efficiency, high power and high linearity in HPAs.

Certificate of Originality

I certify that the work in this thesis entitled **GaN Power Switches for X-Band RFPA Supply Modulators** has not previously been submitted for a degree nor has it been submitted as part of requirements for a degree to any other university or institution other than Macquarie University.

I also certify that the thesis is an original piece of research and it has been written by me. Any help and assistance that I have received in my research work and the preparation of the thesis itself have been appropriately acknowledged.

In addition, I certify that all information sources and literature used are indicated in the thesis.

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Aaron Thomas Pereira

29 May 2015

Dedication

Neque enim quaero intelligere ut credam, sed credo ut intelligam. Nam et hoc credo, quia, nisi credidero, non intelligam.

I do not seek to understand that I may believe, but I believe in order to understand. For this also I believe, that unless I believed, I should not understand.

Anslem of Canterbury

Acknowledgements

This doctoral thesis is the culmination of several years of effort and patience. From the time I commenced my candidature to this point, I can say that I have experienced a gamut of emotions and moods. To say that the experience has been challenging would be an understatement. There are people who have given me support, encouragement and warmth to pick me up and push me onward. This support has come in many forms, but all involved have made this undertaking a little easier. I would like to say a heartfelt 'thank you' to you all – there are too many of you to name exhaustively.

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Dr Larry Dunleavy deserves warm thanks for allowing me to spend some time in Tampa and use the pulsed IV system at Modelithics. Many thanks Larry for the continuing friendship. I'm grateful to Scott Skidmore who helped me set up the pulsed I-V measurement system. Bryan Bothwell from Triquint needs a special mention for all the help and support extended to me during my candidature.

I also benefited from the help of a number of people during my time at Fraunhofer, in Freiburg, Germany. I am immensely thankful to my supervisor at Fraunhofer IAF, Dr Rudiger Quay, who took a real interest in my research and allowed me to get an in-depth understanding of it. He guidance and leadership was crucial in the successful design, fabrication and and testing of the MMICs. The time at IAF was the most fruitful part of my PhD and that was mainly due to the support provided by Rudiger. Im also grateful to my friends, Dr Vince Carrubba, Dr Giuseppe Moschetti, Dr Beatriz Aja and Ms Belen Amado of the "alien group" at Fraunhofer whose friendship and advice Ive come to cherish. I'm also indebted to Professor Ingmar Kalfass with whom i had a conversation that led me to IAF.

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Maria deserves a warm hug for welcoming me into her house and making it a home away from home. Finally, I would like to thank my dad , mum and Ashley for all their prayers, understanding and support.

Aaron

List of Publications

Some of the work presented in this thesis has been accepted for publication at the time of writing, or has been presented at conferences. Listed below are the papers in reverse chronological order. I was the main contributor to the listed publications. The role of all co-authors who appear in these publications has a supervisory role.

1. Pereira, A.; Parker, A.; Heimlich, M.; Weste, N.,**"Integrated Power Switches for X-Band PA"**, 2015 IEEE International Radar Conference (RadarCon2015), Arlington, Virginia from May 11-15, 2015. (cf. chapter 6)

2. Pereira, A.; Parker, A.; Heimlich, M.; Weste, N.; Quay, R.; Carrubba, V., **"X-band high efficiency GaAs MMIC PA"**, Wireless and Microwave Technology Conference (WAMICON), 2014 IEEE 15th Annual , vol., no., pp.1,4, 6-6 June 2014 doi: 10.1109/WAMICON.2014.6857786. (cf. chapter 7)

3. Pereira, A.; Parker, A.; Dunleavy, L., **"Pulsed IV characterization of GaN HEMTs for high frequency, high efficiency integrated power converters"**, Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE , vol., no., pp.2874, 2879, 16-20 March 2014. (cf. chapter 3)

4. Pereira, A.; Parker, A.; Heimlich, M.; Weste, N.; Dunleavy, L., **"Characterization of GaN HEMTs for integrated supply modulator"**, Power Amplifiers for Wireless and Radio Applications, 2014 IEEE Topical Conference on , vol., no., pp.

64,66, 19-23 Jan. 2014. (cf. chapter 2)

5. Pereira, A.; Albahrani, S.; Parker, A.; Heimlich, M.; Weste, N.; Dunleavy, L.; Skidmore, S., **"Trap model for GaN RF HEMT Power Switch"**, Microwave Measurement Conference, 2013 82nd ARFTG , vol., no., pp.1,6, 18-21 Nov. 2013. (cf. chapter 4)

6. Pereira, A.; Albahrani, S.; Parker, A.; Town, G.; Heimlich, M.; Weste, N., **"SRH based trap model for GaN MMIC Power Switches"**, Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on , vol., no., pp.1, 4, 23-26 June 2013, doi: 0.1109/ COMPEL.2013. (cf. chapter 4)

7. Pereira, A.; Albahrani, S.; Parker, A.; Town, G.; Heimlich, M., **"MMIC process for integrated power converters"**,TENCON Spring Conference, 2013 IEEE , vol., no., pp.277, 279, 17-19 April 2013, doi: 10.1109/TENCONSpring.2013. (cf. chapter 2)

Table of Contents

List of Figures

List of Tables

Abbreviations

2DEG- 2-Dimensional Electron Gas

DE- Drain Efficiency

EA- Envelope Amplifier

ET- Envelope Tracking

FPGA- Field Programmable Gate Array

GaAs- Gallium Arsenide

GaN- Gallium Nitride

HEMT- High Electron Mobility Transistor

HPA- High Power Amplifier

LT- Load Transistor

MMIC- Monolithic Microwave Integrated Circuit

PAE- Power Added Efficiency

PAPR- Peak-to-Average Power Ratio

PS FET- Parker Skellern FET

PWM- Pulse Width Modulation

RFPA- Radio Frequency Power Amplifier

SM- Supply Modulator

SRH- Schottky Reed Hall

ST- Switching Transistor

1

Introduction

High power amplifiers (HPA) in airborne platforms and satellite communication system face similar requirements to amplifiers developed for ground applications [1]. Primarily efficiency and linearity are key requirements. Moreover, there are additional requirements like weight, space, performance and extreme reliability. Multifunctional Tx/Rx GaN MMICs have been shown to have a tremendous advantage over existing GaAs implementations [2], [3], [4], [5]. The foremost benefit with a fully integrated AlGaN/GaN transceiver front-end is that both size and weight are reduced signicantly and is of great interest for airborne and space-based platforms as reported in [6], [7], [8], [9], [10].

HPA efficiency can be improved by employing drain bias modulation techniques like envelope tracking (ET), where the drain voltage can be dynamically adjusted to the

incoming RF power level and to minimise the dissipated heat. The major factor that influences the efficiency within an ET system is the switcher power stage within the envelope amplifier (EA). The switcher stage consists of power switches that forms the switched mode power supply circuity which deliver an output current with extremely high efficiency. The major component within the switching power stage is the power stage FET. One of the last remaining functionalities not yet integrated is the power converter. Integrating the supply modulator with the power amplifier (PA) will minimise external parasitic losses, and the switch could be designed to deliver large voltages and high currents at very high slew rates. Integration of the supply modulator on to a multifunctional Tx/Rx in GaN opens the possibility of a new generation of highly efficient PAs compared to existing designs.

1.1 Integrated Supply Modulators

In next generation Tx/Rx systems there is an ever increasing need to increase the data throughput of wireless links, which causes the signal peak-to-average power ratio (PAPR) and channel bandwidth to increase. This is very challenging to implement, as the operational requirements of very good linearity and high efficiency place enormous stresses on the power amplifier. Because of the high power consumption of the HPAs and the limited availability of energy sources, the development of highly efficient power amplifiers is of great interest for airborne and space-based platforms. Various drain bias modulation techniques which improve the overall efficiency, like envelope tracking have been investigated for space based RF amplifiers [1], [11].

The standard functionalities in a MMIC Tx/Rx transceiver, shown in Figure 1.1 [12],

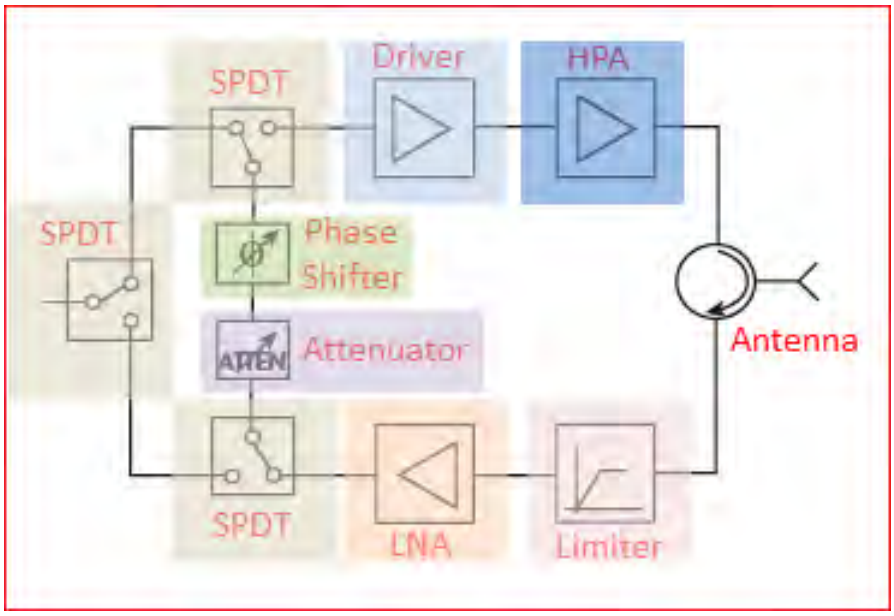

Figure 1.1: Functionalities within a MMIC Tx/Rx Transceiver

include, High Power Amplifiers (HPA) with their associated drivers, Low Noise Amplifiers (LNA), control elements in the form of SPDT switches, phase shifters, attenuators and limiter circuits [13], [14]. Integration of a supply modulator on to a multifunctional Tx/Rx in GaN opens the possibility of a new generation of highly efficient HPAs compared to existing designs. The increased integration factor, hence the reduced footprint and potentially lower cost at the same power levels compared to existing GaAs designs are of large interest for airborne sensor platforms and satellite communication systems.

1.2 X-Band High Power Amplifier

High power X-band amplifiers are necessary for radar and satellite communication systems. The F-35 (JSF) fighter uses the APG-81 X-band (Figure 1.2 [15]), an advanced fire-control radar which features both air and surface modes and an active electron-

ically scanned array (AESA) antenna for enhanced performance [16]. Military communications systems, such as MILSATCOM, operate in lower X-band (7-8 GHz). The TerraSAR-X (Figure 1.3 [17]) is an advanced X-band space based sensor platform that provides near real-time, all weather imaging capability based on advanced phased array technology [18]. Northrop Grumman Global Hawk (Figure 1.4 [19]) also has advanced sensors that work in the X-band enabling it to deliver high quality images with resolution down to one foot [20].

Figure 1.2: APG 81 Radar

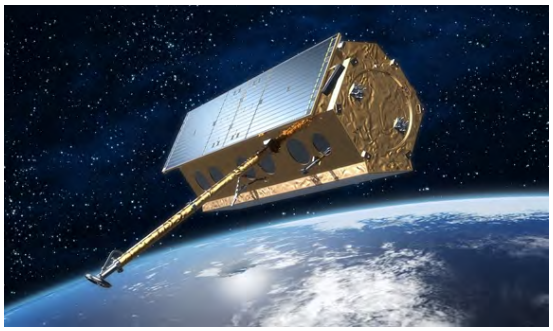

Figure 1.3: TerraSar-X

Figure 1.4: Global Hawk

In high power X-band transmitters, both power consumption and heat dissipation become important design constraints. There in an ever increasing need to improve the transmitter efficiency to reduce the power consumption and heat dissipation as the sources of energy are limited and there is a premium on weight and space in airborne and space based platforms.

Typically, the output stage power amplifier is the dominant component of the transmitter efficiency, therefore this is often the component which receives the most attention. The majority of RF transmitters suitable for power levels and signal bandwidths of interest for airborne and satcom applications share common standardised system architectures for power conversion. The final stage DC supply from the supply bus to the RFPA is an Electronic Power Conditioner (EPC) which has a fixed-voltage DC-DC converter (Figure 1.5).

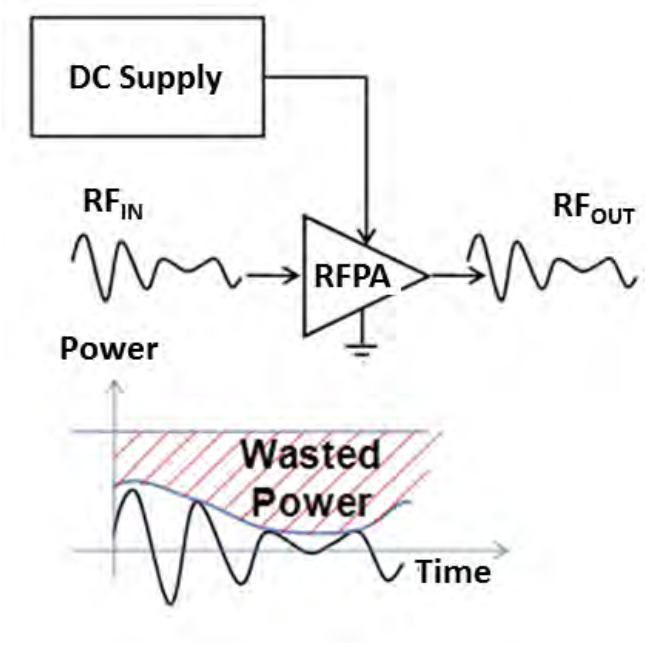

Figure 1.5: Fixed Bias

This rigid system constraint fundamentally limits the high power amplifier operating class, output power, power added efficiency, and is an impediment to high efficiency operation and integration. For example, in communication transmit apertures, an RFPA typically achieves peak power efficiency at a single operating voltage corresponding to peak output power. This worst-case operating scenario for peak power output and input drive is determined within the system requirements for the final DC supply voltage that sets the drain bias. However, many present and future RF systems

employ complex modulation techniques with high peak-to-average ratios in signal amplitude (Figure 1.6 [21]).

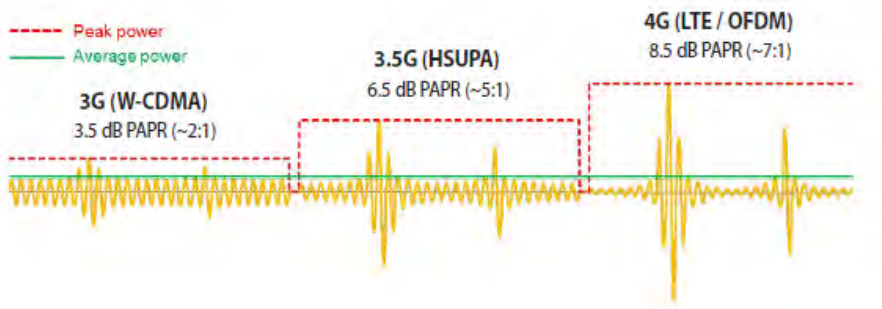

Figure 1.6: Modulation Schemes

Although the systems are designed for fixed operation at the peak condition, the PAs operate well below peak output power most of the time. At a fixed operating voltage, PA efficiency drops rapidly as the output power is reduced from its peak value by either lower input drive or wasteful attenuation, resulting in low average conversion efficiency of DC power to useful RF output. To mitigate the efficiency dilemma and enable efficient use of diverse signal waveforms, it would be desirable to implement drain bias modulation techniques [22], [23] as shown in Figure 1.7. High efficiency operation can be achieved if the power converter can rapidly change the DC voltage that it supplies to the RFPA.

The ability to rapidly modulate the DC supply voltage of an RFPA with the associated RF signal allows the PA to be biased in efficient operating regimes to gain back much of the energy presently wasted as heat. Since the DC supply voltage is not fixed, but instead is tracking the RF signal envelope, the voltage difference between the supply and the RF envelope is minimised. This voltage difference determines how much power is converted into waste heat. Such techniques will greatly relieve the thermal management burden traditionally associated with large signal, high power RF electronics

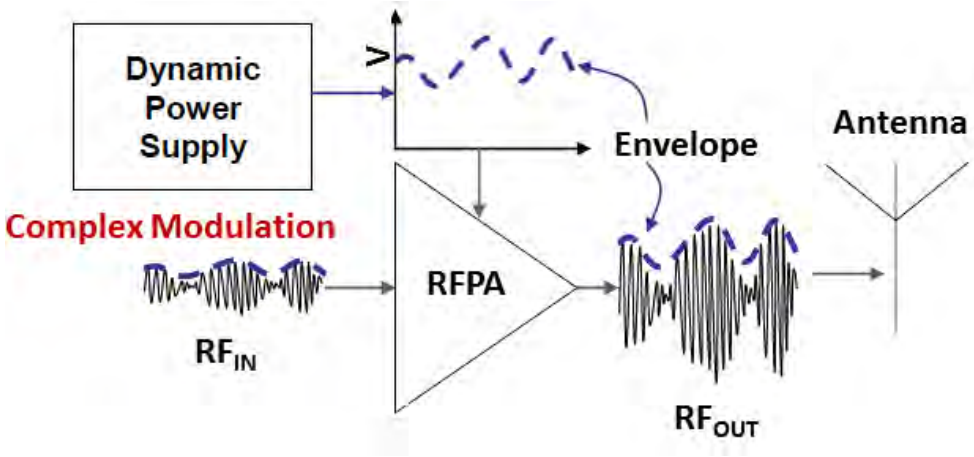

Figure 1.7: Dynamic Bias

using fixed-voltage power supplies. The result is higher overall RF system efficiency and a more flexible architecture for implementing a variety of operating conditions.

1.3 Envelope Tracking and Supply Modulators

The Envelope-Tracking (ET) technique (Figure 1.8 [24]) consists in adjusting the voltage supplied to the RF transistors with the modulation envelope of the RF signal (Figure 1.9 [24]). In such a system, an Envelope Amplifier (EA) converts the bus DC voltage into a dynamic DC voltage, typically in the range of tens of volts, as required instantaneously by the RFPA. Such a dynamic voltage provides the PA with an adjusted power level, resulting in an increased efficiency compared to a PA supplied with a constant drain bias voltage.

An Envelope Amplifier consists of a switch-mode DC-DC converter and linear regulator. The high frequency content of the baseband envelope signal is fed to a linear regulator while the low frequency content is delivered to the DC-DC converter to realise

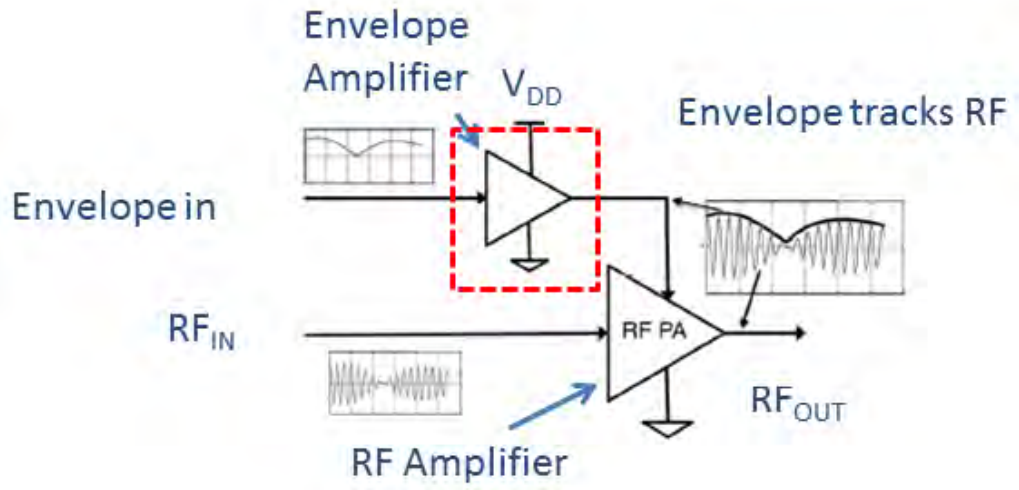

Figure 1.8: Schematic of ET system

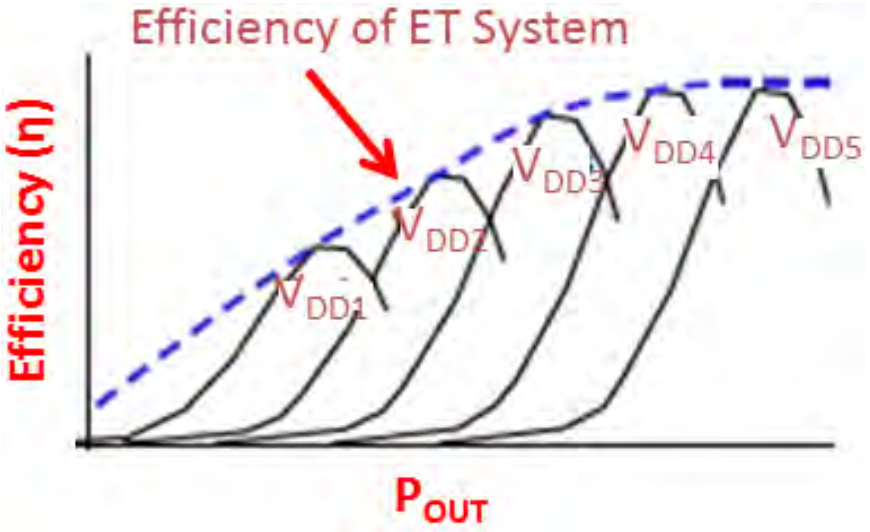

Figure 1.9: PAE improvement with ET

high efficiency. In this way the RFPA is kept near saturation throughout the dynamic changes of the signal, improving the average efficiency. This technique is independent of carrier frequency and thus allows for wideband RFPA designs. The switcher stage acts as a current source, efficiently supplying a majority of the DC and low frequency power while the linear stage fills in the remaining high frequency components. Thus the design of the high frequency, high efficiency switcher stage is very critical to

achieve wideband EA [25].

1.4 Motivation for Integrated Supply Modulator

Integration of a supply modulator on to a multifunctional Tx/Rx in GaN opens the possibility of a new generation of highly efficient HPAs as compared to existing designs. The increased integration factor, hence the reduced footprint and potentially lower cost at the same power levels compared to existing GaAs designs are of large interest for airborne sensor plaforms and satellite communication systems.

The inherent properties of GaN combined with innovative circuit topologies can be used to design high efficiency RF systems. In many airborne and space platforms with shared supply bus, DC power conversion can be done at the local, on-chip level with very good efficiency with an integrated supply modulator. Decentralised power conversion brings forth greater flexibility and added redundancy in complex land, airborne and marine systems which operate in very hostile environments. In addition to the gain in the valuable space due to the reduction in size and weight, it opens up avenues for efficiency improvements in the amplifier by employing drain bias modulation techniques like ET, where the drain voltage can be dynamically adjusted to the incoming RF power level to minimise the dissipated heat.

Hence by leveraging the inherent strengths of GaN, power conversion and a power amplification circuit can be combined to design a supply modulator integrated HPA that would help improve the DC to RF conversion efficiency, thereby reducing the power consumption in mission critical systems, reducing the overall cost while improving system reliability.

1.5 Aims and Significance

The main aim of this thesis is to investigate the use of RF HEMTs as power switches within a supply modulator integrated with an X-Band High Power Amplifier. In order to achieve the stated aim, four major tasks are identified.

1. **Impact of traps on the efficiency of the power switch**

   The major objective of this task is to investigate the impact of trapping on the efficiency of commercially available GaN RF HEMTs. The HEMTs are characterised using a pulsed I-V system to identify R_{ON} modulation at high quiescent drain bias conditions which emulate power switch operating conditions. Develop and implement trap model for power switching.

2. **Characterise the GaN power switches in Hybrid Switching Circuit.**

   In this task, loss mechanisms within modulator circuits are identified with a view to maximise efficiency. Commercially available bare-die GaN HEMTs were characterised in a hybrid modulator topology to identify losses within the circuit.

3. **Characterise the GaN power switches in MMIC Modulators.**

   Develop and test MMIC modulators based on the data obtained from hybrid testing. Identify areas of improvement for integration with an HPA like layout issues, interface to external world along with circuit performance.

4. **Supply Modulator Integrated High Power Amplifier Development.**

   The objective here is to integrate a high efficiency supply modulator with an X-Band high power amplifier. By successfully undertaking the four tasks it is conceived that an in-depth understanding of the intrinsic device limits and circuit

parameters that influence the high frequency and high efficiency operation of the supply modulator integrated with a power amplifier will be gained.

1.6 Synopsis

This thesis is organised into eight chapters. These include the introductory chapter, and a chapter that provides the necessary background materials for this thesis. The next five chapters form the original contributions offered by this thesis. This is followed by a chapter that summarises the results and suggests avenues for further research.

1.6.1 Thesis Overview

Chapter 1 has introduced the general field into which this thesis fits. The need for a high efficiency, high power amplifier within an X-band Tx/Rx module for airborne and space based platforms is introduced. Efficiency enhancement techniques are introduced and the role of power transistors within the switcher stage of an ET system is identified. The case for integrating a high efficiency, high frequency switch mode power converter circuit with an HPA is introduced. The aims and scope of the investigation presented in this thesis are also discussed.

Chapter 2 discusses the background material that is useful in the development of this thesis. Efficiency enhancement techniques are described and the role of GaN technology as a key parameter for power switch fabrication and its operation is identified. Trap phenomena within a power switch are discussed and the role of field plates and

passivation techniques for high voltage operation are also given in this chapter. A simple first order figure of merit for a GaN HEMT power switch is identified as the product of R_{ON} and input capacitance. A review of the latest GaN and GaAs power switch implementations given in the literature is also given.

The results presented in this chapter have been reported in the following publication: Pereira, A.; Parker, A.; Heimlich, M.; Weste, N.; Dunleavy, L.,**"Characterization of GaN HEMTs for integrated supply modulator"**, Power Amplifiers for Wireless and Radio Applications, 2014 IEEE Topical Conference on , vol., no., pp.64,66, 19-23 Jan. 2014.

Pereira, A.; Albahrani, S.; Parker, A.; Town, G.; Heimlich, M.,**" MMIC process for integrated power converters"**,TENCON Spring Conference, 2013 IEEE , vol., no., pp.277, 279, 17-19 April 2013, doi: 10.1109/TENCON, Spring.2013.

In **Chapter 3**, power switch characterisation using pulsed IV is described. Commercial foundry GaN HEMTs available from Triquint Semiconductors and Cree Semiconductors were investigated using Diva 265 and Auriga 4850 Pulsed IV systems. R_{ON} modulation and current collapse phenomena were observed when pulsing from a high quiescent bias condition, indicating the presence of gate-drain charges that depletes the channel causing an increase in the ON resistance and leading to a decrease in the power switch efficiency. The Figure of Merit was also degraded due to an increase in R_{ON} at high switch voltages. The major challenge in characterising the GaN HEMT as a power switch using a pulsed I-V is the low switching frequency. The HEMTs were characterised at a switching frequency of 500 kHz.

The results presented in this chapter have been reported in the following publication:

Pereira, A.; Parker, A.; Dunleavy, L.,**" Pulsed IV characterization of GaN HEMTs for high frequency, high efficiency integrated power converters"**, Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE , vol., no., pp. 2874, 2879, 16-20 March 2014. The co-author contribution to this paper was supervisory.

In **Chapter 4**, a power switch trap model based on the SRH theory of holes and electrons is introduced. A comprehensive power switch model which accounts for the dynamic R_{ON} and the current collapse phenomenon is described. A Spice model based on the Parker-Skellern FET was introduced, and simulations the of power switch, predicted the shift in knee voltage caused by dynamic R_{ON} and the current collapse caused by shift in the pinch-off voltage.

The results presented in this chapter have been reported in: Pereira, A.; Albahrani, S.; Parker, A.; Town, G.; Heimlich, M.; Weste, N., **"SRH based trap model for GaN MMIC Power Switches"**, Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on , vol., no., pp.1, 4, 23-26 June 2013, doi: 0.1109/ COMPEL.2013.

and

Pereira, A.; Albahrani, S.; Parker, A.; Heimlich, M.; Weste, N.; Dunleavy, L.; Skidmore, S., **"Trap model for GaN RF HEMT Power Switch"**, Microwave Measurement Conference, 2013 82nd ARFTG , vol., no., pp.1,6, 18-21 Nov. 2013.

In **Chapter 5**, Cree 0.25 μm and 0.40 μm depletion-mode bare-die GaN HEMTs were implemented in a hybrid modulator circuit topology switching at 10 MHz. The high side driver circuitry was identified as the major contributor to loss within the modulator topology. An ST-R-LT driver circuit was introduced and output powers of 12 and

14 watts were measured with power stage efficiencies of over 90%. The hybrid circuits consisted of GaN power stage, high and low side drivers and GaN diodes. The circuit was fabricated on RF PCB board made of Rogers 4003 substrate. The circuit topology, device sizing and passive components were chosen with a view to understand the high frequency switching behaviour of the converter and to gain insight to assist in the development of MMIC integrated power converters. A major challenge was in high frequency measurements. External noise, capacitive coupling and the intrinsic high gain of GaN HEMTs caused the circuit to oscillate and hence it had to be stabilised using decoupling capacitors, shielded cables and common ground nodes for the power supply, oscilloscope and pcb backside. The results presented in this chapter are being readied for a future publication.

Chapter 6 expands on the work done in the previous chapter, and two MMIC power switches with integrated gate drivers were designed and fabricated in Triquint semiconductor 0.25 μm GaN processes. The gate driver circuit was optimzed to minimize power dissipation and features a bootstraped ST-R-LT driver and a switch node connected ST-R-LT driver. The switching frequency of the MMIC modulator was 100 MHz and efficiencies over 80% with output powers of 39 dBm and 40 dBm were respectively measured. A major challenge was in obtaining the correct level shifted gate driver voltages using the external bias tees to drive the high side. The work presented in this chapter was accepted for an upcoming conference: Pereira, A.; Parker, A.; Heimlich, M.; Weste, N.,**"Integrated Power Switches for X-Band PA"**, 2015 IEEE International Radar Conference (RadarCon2015), Arlington, Virginia from May 11-15, 2015.

In **Chapter 7**, two broadband power amplifier topologies in GaAs and GaN are introduced for X-Band applications for use in space and radar applications.

At first a broadband GaAs MMIC PA was designed and fabricated in a 0.10 μm GaAs process. On-wafer measurements showed a PAE greater than 50% in the 8-13 GHz frequency range with maximum a P_{OUT} of 27.5 dBm and an associated gain of above 11 dB. The measured performance of this PA had the highest bandwidth, DE and PAE of any GaAs X-Band design reported in the literature. A maximum DE of 68.2%, PAE of 62.91%, P_{OUT} of 27 dBm and a corresponding gain of 12.89% was measured at 10 GHz. The results from the design presented in this chapter was reported in : Pereira, A.; Parker, A.; Heimlich, M.; Weste, N.; Quay, R.; Carrubba, V., **"X-band high efficiency GaAs MMIC PA"**, Wireless and Microwave Technology Conference (WAMICON), 2014 IEEE 15th Annual , vol., no., pp.1,4, 6-6 June 2014, doi: 10.1109/WAMICON.2014.6857786. The co-author contribution to the paper was supervisory.

The GaN design features a supply modulator integrated HPA. The main highlight of this chapter is the development of a supply modulator integrated HPA for satellite communications. A two stage high power amplifier integrated with a DC-DC power converter was designed and fabricated in Fraunhofer IAF 0.25μm GaN technology. The wafer-mapped X-band HPA had an PAE of over 41% and delivered an output power of 39 dBm. The supply modulator was characterised over a wide range of operating conditions and resistive loads. It delivered a maximum output power of 14.6 dBm with a peak efficiency of 88%.

As mentioned earlier, the major challenge was in obtaining the level shifted drive voltages as well as stabilising the HPA which was oscillating at 1.18 MHz. Extra decoupling capacitors at the supply node stabilised the HPA and it was mounted on a peltier cooler to minimize any thermal degradation at high output power. The calculated PAE for the supply modulated HPA at a drain bias of 20 V was 26.65% with an output power of 34.98 dBm. At 15 V supply modulator bias, the PAE was 20.3% with P_{OUT} at

33.7 dBm.

The results presented in this chapter are being readied for a future publication.

Finally, **Chapter 8** summarises the results of this thesis and suggests avenues for further research.

1.6.2 Thesis Objectives

The major objective of this thesis is to investigate the use of commercially available RF GaN HEMTS as power switches within a supply modulator integrated with an X-Band high power amplifier in a 0.25 μm GaN MMIC foundry process. The research on which this thesis is based looked at four different aspects of modulator design in terms of efficiency. These are:

- The efficiency of the GaN HEMTs when used as power switches.
- Efficiency of the circuits which drive the GaN power HEMTs.
- Optimisation of driver circuits for implementation in MMIC technology.
- Integration of the supply modulator with an RF HPA in a 0.25 μm GaN process.

The thesis will describe in detail all four aspects of this research topic. These include the investigation of the efficiency of GaN HEMTs by the use of a pulsed I-V system and the characterization of these GaN HEMTs in a switching topology fabricated as a hybrid circuit. The impact on the overall efficiency of the modulator by integrating the gate drivers along with the power HEMTs in a MMIC process is undertaken and finally the overall efficiency of an optimsed modulator circuit integrated with a HPA is detailed. These four aspects complete the research which is detailed in this thesis.

1.6.3 Statement of Originality

The research reported in this thesis was carried out between October 2010 and October 2014, under the supervision of Professor Anthony Parker and co-supervised by Professor Michael Heimlich. The initial phase of the research was done at Macquarie University. From September 2012 to August 2013, I undertook off-site research at the University of Colorado, Boulder (UCB), under the supervision of Professors Zoya Popovic and Dragan Maksimovic. During this period, I also undertook measurements at Modelithics Inc, in Tampa, Florida, under the supervision of Professor Larry Dunleavy.

This thesis comprises eight chapters and two appendix sections. An outline of the main achievements of the work is given in chapter 1. The work of others is acknowledged and cited in the body of the thesis. The following paragraphs state those portions of the work which are claimed as original contributions of the author.

Chapter 2 is mainly background information on the need for HPA efficiency improvement, the role of integrated supply modulators and the importance of GaN technology for the development of power switches. A review of high frequency supply modulators in GaAs and GaN technologies is also given. Appropriate citation for all the relevant literature is also given.

Chapter 3 the role of traps within commercially available RF GaN HEMTs, when used in power switching, is identified using pulsed I-V characterisation. The author undertook all the measurements, Triquint 0.25 μm GaN devices were tested using a Diva 265 system available at Modelithics Inc., Tampa, FL. Scott Skidmore of Modelithics helped the author with the measurement setup. Cree GaN HEMTs were tested using

an Auriga 4850 pulsed I-V system available at Fraunhofer IAF, Freiburg, Germany.

In chapter 4, a Power Switch Trap Model based on Schottky Reed Hall theory was developed and a comprehensive power HEMT model based on Parker-Skellern FET model incorporating traps was developed. Spice simulations accurately predicted the ON-resistance modulation due to traps between the gate and the drain, while a current collapse was observed due to traps present in the bulk of the HEMT. Dr Sayed Al Bahrani had investigated the role of trapping in the saturation region of a GaN HEMT, while the author investigated the role of trapping in the linear region of the HEMT.

In chapter 5, the author investigates the role of trapping in GaN power HEMTs at 10 MHz switching frequency. The gate driver topology designed by Dr Stefan Mardolt for switch mode power amplifiers was adapted for hybrid synchronous buck converterer. The design was optimised in AWR Microwave Office and transient simulations were also undertaken by the author. Moreover, the layout and switching measurements were undertaken by the author. Simulations of the hybrid modulator mated with a HPA was also undertaken by the author. All the hybrid modulator testing was undertaken at Fraunhofer IAF, Freiburg, Germany.

In chapter 6, two integrated supply modulators were designed and fabricated in Triquint Semiconductor 0.25 μm GaN processes. The supply modulators were designed during the author's research visit to the University of Colorado, Boulder. The designs were based on authors experience with the DARPA MPC program where Triquint Semiconductor 0.15 μm GaN process was used while in this thesis the main focus is on 0.25 μm GaN process. The two modulators were mounted on PCBs designed by the author and the testing was done at the facilities at Fraunhofer, IAF, Freiburg, Germany.

In chapter 7, two broadband X-Band RFPAs in 0.10 μm GaAs and 0.25 μm GaN processes. The 0.10μm Win Semiconductor GaAs PA was designed by the author at Macquarie University, while it was wafer-mapped at the facilities of Fraunhofer IAF, Freiburg, Germany.

A modulator integrated X-Band HPA was designed and fabricated in 0.25 μm Fraunhofer IAF GaN process. The HPA amplifier was designed by Dr Jutta Kuhn. The HPA small and large signal simulations presented in this thesis were also undertaken by Dr Jutta Kuhn. The author designed, simulated and laid out the supply modulator along with the HPA. The original HPA layout was modified by the author to minimise the layout area of the supply modulator integrated HPA. The author also undertook all the on-wafer and PCB mounted measurements of the HPA as well as the supply modulator characterisation. The PCBs on which the chip was mounted was also designed by the author. The combined supply modulator and HPA measurements were performed by the author at Fraunhofer, IAF, Freiburg, Germany. The author was assisted by Thomas Maier in setting up the test bench and calibrating the measurement setup.

The material in this thesis has not been submitted towards another degree at this or any other university.

1.7 Scope

The scope of this thesis is limited to the investigation of GaN RF HEMTs from commercial foundries. The type of transistor that is investigated in this thesis is limited to GaN HEMTs. GaAs based FETs are not considered because the current and voltage levels that are available from a GaAs process are much lower than from GaN.

As part of this thesis, high efficiency, high frequency stand alone integrated supply modulator circuits were developed in a GaN process. Understanding gleaned from such a circuit topology was used to design a supply modulator integrated high power amplifier on 0.25 μm GaN process. The operating frequency of the power amplifier is limited to X-Band (8-10 GHz) with an output power of 3 Watts.

The testing of supply modulator integrated HPA was a standard RF characterisation with no input modulation scheme applied and with the drain bias voltage directly fed by the integrated modulator.

1.8 Next

Chapter 2 gives an introduction into the need for efficiency enhancement and an overview of GaN technology. A review of the literature pertaining to this topic is also given.

2

Power Switch Technology

2.1 Introduction

High-power amplifiers (HPAs) are an integral part of any advanced Tx/Rx multifunctional RF transceiver system. Conventional HPAs reach maximum efficiency when they are pushed into saturation, yet to meet linearity specifications while amplifying signals with high peak-to-average power ratios (PAPRs), the PA must be operated with the average power backed-off from compression. This results in low average efficiencies. Airborne and space based HPAs have similar requirements along with the need for reliability and extreme ruggedness for operation in very hostile environments.

The efficiency of wideband HPAs for space based platforms can be improved by the

use of drain bias modulation techniques like ET. The overall efficiency of an ET system is determined by the switching supply modulator, and the power switch within the supply modulator is the key enabler for high efficiency. This chapter introduces Gallium Nitride HEMTs, their operational principles are described, and a switching figure of merit is introduced. A literature review of existing state of the art GaN RF HEMT power switches is also given.

2.2 High Power Amplifiers

High efficiency HPAs are critical in modern communication systems. Power amplifiers demonstrate the highest efficiency when operated in the compression region. With modern communication systems evolving to more spectrally efficient and higher data rate modulation formats, highly linear power amplifiers are required to avoid out-of-channel interference (e.g., adjacent channel power ratio (ACPR)) and distortion (e.g. error vector magnitude (EVM)). The traditional approach to linearly amplify the non-constant envelope modulated signal is to back-off the linear Class A or Class-AB PA output power until the distortion level is within acceptable limits. Unfortunately, this lowers efficiency significantly, especially for high PAPR signals. Thus, there is an inherent tradeoff between linearity and efficiency in PA design.

The majority of RF transmitters suitable for power levels and signal bandwidths of interest for airborne and satcom applications share common standardised system architectures for power conversion. The final stage DC supply from the supply BUS to the RFPA is an Electronic Power Conditioner (EPC) which has a fixed-voltage DC-DC converter (Figure 2.1). The electronic power conditioner (EPC) provides the interface

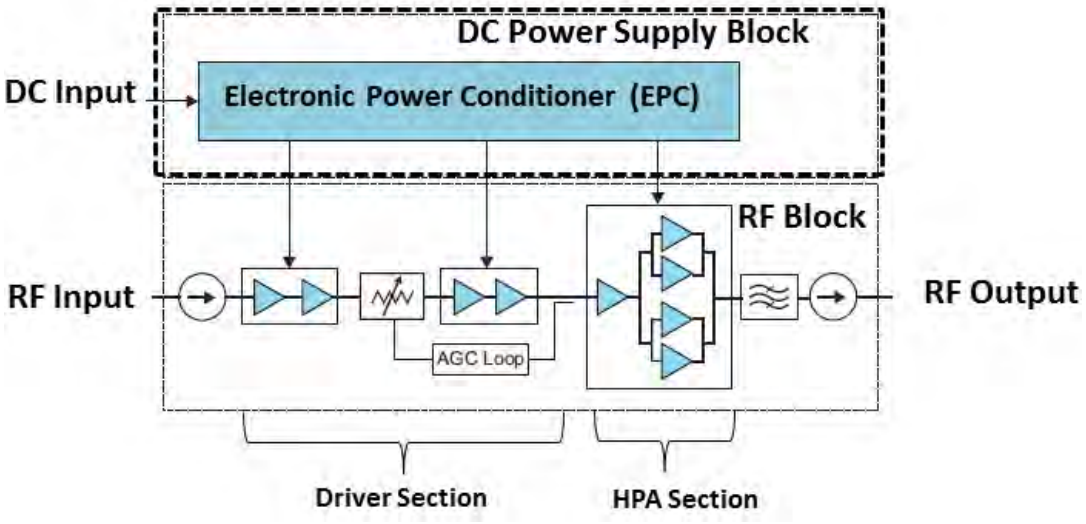

Figure 2.1: Satellite SSPA System Schematic

to the spacecraft bus [26] and a regulated bias voltage to each section of the RF block from the spacecraft bus as shown in Figure 2.2.

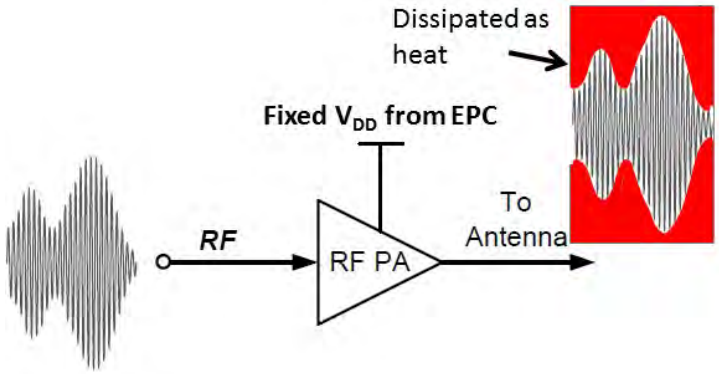

Figure 2.2: Drain Supply: Constant Bias

2.3 HPA Efficiency Enhancement: ET System

Efficiency enhancement techniques like ET are the subject of intensive research and development efforts since they offer PAs with improved efficiency in power back-off operation. The key component in such systems is the supply modulator. It has to pro-

vide a highly efficient conversion of a fixed supply voltage to the desired instantaneous voltage level with sufficient current to operate the PA. This must be accomplished over a bandwidth much larger than the modulation bandwidth of the RF signal [27]. Several supply modulator topologies for high power wideband applications have been suggested. Among the most promising are buck-converters and linearly assisted buck-converters also known as hybrid switching amplifiers (HSA) [28], [29].

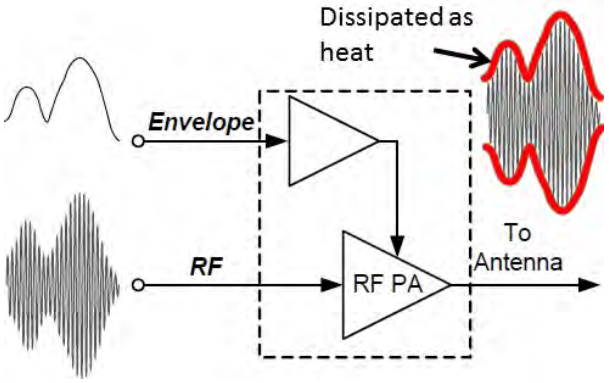

Figure 2.3: Drain Supply: Envelop Tracking

In such a system, an Envelope Amplifier (EA) converts the bus DC voltage into a dynamic DC voltage, typically in the range of tens of volts, as required instantaneously by the RFPA (Figure 2.3). Indeed, such a dynamic voltage provides the PA with an adjusted power level, resulting in an increased efficiency by comparison to a PA supplied with a constant voltage as shown in Figure 2.4 [30].

Under ET, the supply voltage of the RF PA is dynamically adjusted by the envelope modulator/amplifier (EA) to track the envelope of the RF signal. In this way the RF PA is kept near saturation throughout the dynamic changes of the signal, improving average efficiency. This technique is independent of carrier frequency and thus allows for wideband RF PA designs. It is composed of a switch-mode DC-DC converter and linear regulator. The high frequency content of the baseband envelope signal is fed

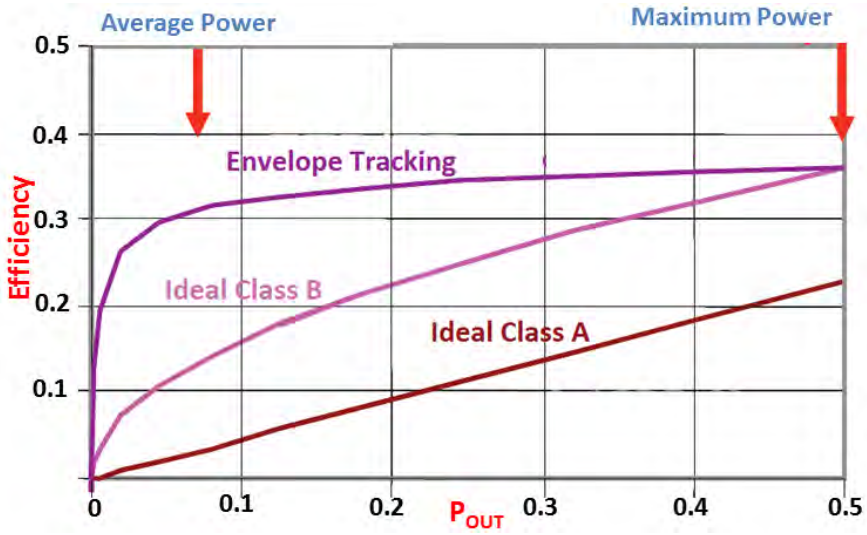

Figure 2.4: Efficiency enhancement in ET

to the linear regulator while the low frequency content is delivered to the DC-DC converter to realize high efficiency. While ET does not inherently limit the carrier frequency, wide modulation bandwidths such as those used by radios that operate at high carrier frequencies require wideband EAs. The nonlinear function which is used to calculate the signal envelope causes bandwidth expansion.

In Figure 2.5 the power spectrum of a 20 MHz (modulation bandwidth) 16 QAM LTE envelope signal, which has a 6.6 dB PAPR, is shown. The majority of the envelope power exists within a few hundred kHz of DC [30]. Still it is important that the modulator is able to accurately reproduce higher frequency portions of the signal to maximise system linearity and efficiency. The unique properties of the envelope signal allow for an EA design that is accurate and efficient. A high efficiency DC-DC switching converter is combined with a wide band linear stage via a hysteric feedback loop as shown in Figure 2.6. The switcher stage acts as a current source, efficiently supplying a majority of the DC and low frequency power while the linear stage fills in the remaining high frequency components. Thus a high efficiency DC-DC converter is critical to

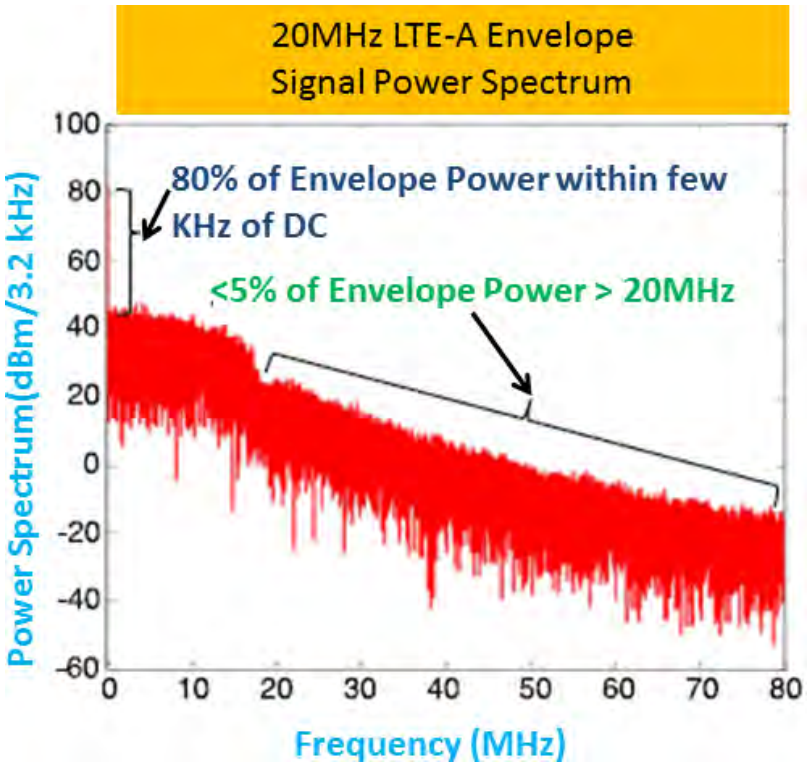

Figure 2.5: Power Spectrum of a 20 MHz 16 QAM LTE-A envelope signal

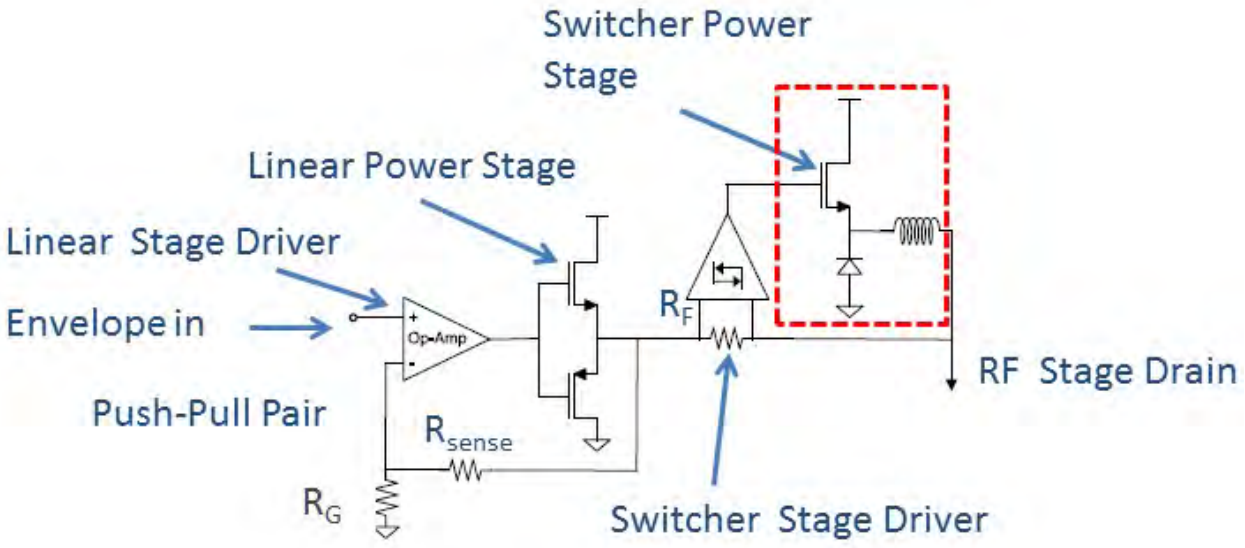

Figure 2.6: Schematic of Envelope Amplifier

having an extremely efficient EA stage [25].

The key enabling device technology to be developed for the high-speed modulator is a fast, low-loss GaN-based power switch. Traditional MOSFET-based converters may operate at frequencies as high as 10 MHz by using novel switching techniques such as ZVS or ZCS. However increasing operating frequencies above 10 MHz for such converters necessitate new advanced power semiconductors with high speed and low losses. Incorporation of III-V devices as switching elements will enable the high frequency operation needed to satisfy the envelope bandwidth requirements of RF supply modulators for PAs with complex input modulation schemes. GaN technology has emerged as a possible transistor technology for realising supply modulators [25].

GaN-on-silicon is already established as the future mainstream technology for high-power DC-DC converters, but the bandwidth demands of the most recent generation of telecommunication systems exceed the speed limits of these devices, which are optimised for high voltages and currents rather than for high frequency. This has sparked the interest of using RF GaN HEMT for wideband RFPA supply modulators [31]. State of the art RF GaN HEMTs technology promises even better performance than existing power GaN devices; their exceptional characteristics could enable very high frequency switching without the need for purely resonant operation, which might provide advantages in terms of component count, size and ease of design while maintaining high efficiency, as demonstrated in [11].

2.4 III-V Material Properties

The fundamental properties of the III-V materials are the small bond length between constituent atoms and the wide bandgap energy. The small bond length leads to a strong bonding energy between constituent atoms and, consequently, the chemical stability is extremely high. In addition, the large bonding energy and the small mass bring about large phonon energy, so lattice scattering hardly occurs. This results in high thermal conductivity and high saturation drift velocity, macroscopically. Figure 2.7 shows the electron velocities within various semiconductors as a function of the electric field [32].

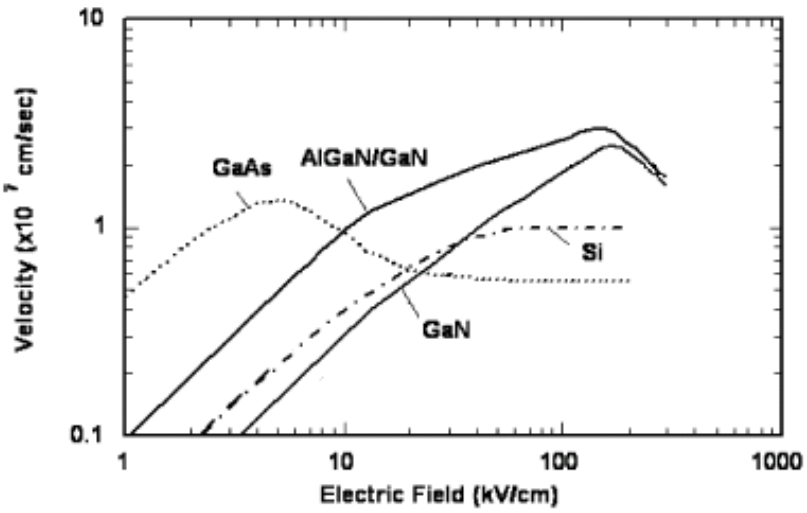

Figure 2.7: Electron velocity v Field Strength

Moreover, the large bandgap leads to a high breakdown electric field and low intrinsic carrier generation at high temperature. This allows high temperature operation without excessive leakage current. A large bandgap results in a high breakdown electric field which enables the application of high supply voltages. Also, it leads to low intrinsic carrier generation at high temperature. Both GaN and SiC have

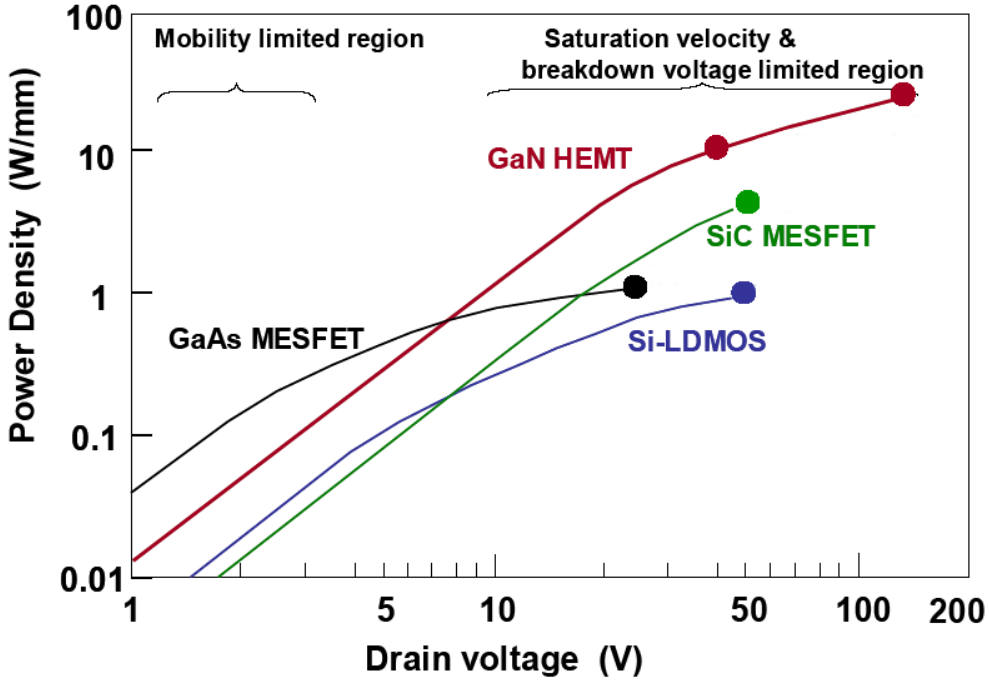

Figure 2.8: Power Density v Drain Voltage

a very large band gap energy which results in a breakdown electric field ten times as high as for Si and GaAs. These characteristics are extremely attractive for high-frequency, high-power, high-voltage, high-temperature and low-loss operating specifications. Figure 2.8 shows the power densities of various semiconductors and the corresponding drain voltage [33].

Table 2.1: Comparison of Material Properties

Material Properties	Units	Si	6H-SiC	GaN	GaAs
Bandgap Energy	(eV)	1.1	3.0	3.4	1.43
Breakdown	(MV/cm)	0.3	2.4	3.3	0.4
Relative Dielectric constant		11.8	9.7	9.0	12.8
Electron Mobility (μ)	$cm^2V^{-1}s^{-1}$	1400	400	900	8500
Saturated Drift Velocity		1.0	2.0	2.5	1.0
Thermal Conductivity	$Wcm^{-1}K^{-1}$	1.5	4.5	1.3	0.5

Generally, to achieve high currents and high frequency operation in a semiconductor device, a high charge carrier mobility (μ) and a high saturation velocity (v_{sat}) are de-

Table 2.2: Comparison of Figures of Merit

FOM	Si	6H-SiC	GaN	GaAs
JM(E_c $v_{sat}/2\pi$)	1	260	760	7.1
KM (v_{sat}/ϵ)$^{1/2}$	1	4.68	1.6	0.45
BM($\epsilon\mu$ $E_C{}^3$)	1	110	650	15.6
BHM(μ $E_C{}^2$)	1	16.9	77.8	10.8

sirable. The high electron mobility of GaAs (8500 $cm^2V^{-1}s^{-1}$) is the main reason that field-effect transistors (FETs) fabricated from this material have such excellent high-frequency performance . A primary disadvantage of fabricating transistors from bulk GaN is the relatively low value for the electron mobility, of 900 $cm^2V^{-1}s^{-1}$.

In general, wide-bandgap semiconductors have relatively low mobility but very high saturation velocity, which is reached at high electric fields that can easily be supported . The mobility and saturation velocity of the 2-dimensional electron gas (2DEG) at the AlxGa$_{(1-x)}$N/GaN heterojunction is very suitable for high-power and high-frequency device applications. The room temperature mobility of the 2DEG, which is typically between 1200 $cm^2V^{-1}s^{-1}$ and 2000 $cm^2V^{-1}s^{-1}$, is significantly better than that of bulk GaN. The 2DEG sheet charge density of the $Al_xGa_{(1-x)}$N/GaN structure is very high due to piezoelectric and spontaneous polarization induced effects.

The figures of merit (FOM) combine the most relevant material properties, shown in Table 2.2, into a number which represents a rough measure of the relative strengths of the material with respect to high-power and high-frequency applications. Here ϵ is the relative dielectric constant, μ the mobility, E_C the breakdown electric field, v_{sat} the saturated electron drift velocity and κ the thermal conductivity.

JM is the Johnsons figure of merit defining a value for high-frequency handling capability. KM is the Keyess figure of merit for high-temperature, handling capability.

Baliga derived two figures of merit, one for low frequency and one for high frequency operations, which are a measure of the high-power handling capability. As is shown in Table 2.2, SiC technology is a strong competitor of GaN technology. In particular, in the applications where high temperature is required SiC, is the best choice due to the higher thermal conductivity.

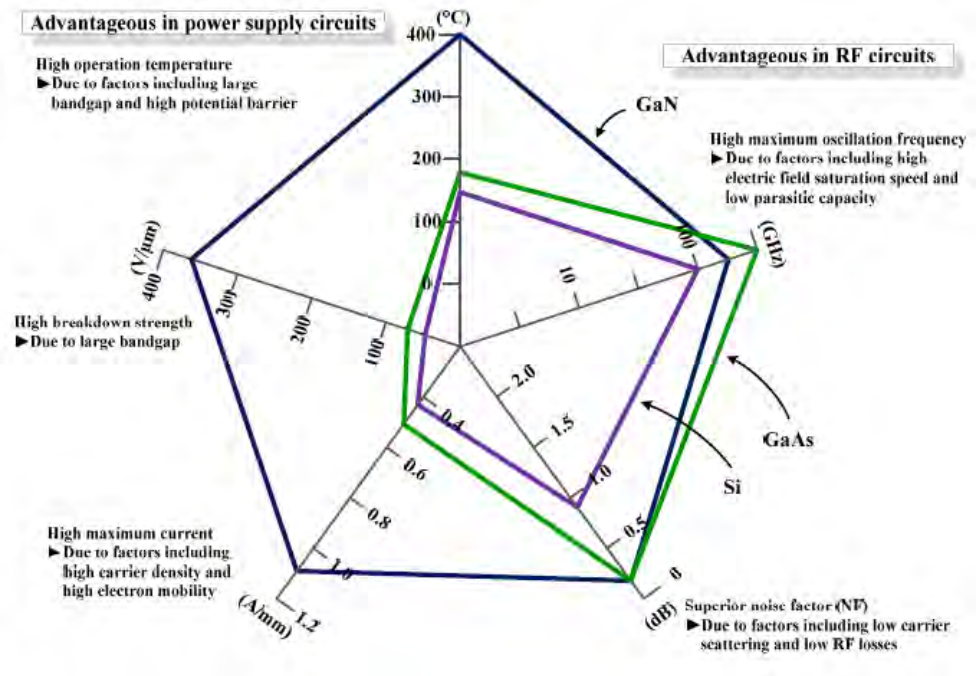

Figure 2.9: Semiconductor Comparisions

Gallium Nitride is a highly promising material system for both RF and power electronics applications. Compared to existing Si and GaAs devices, they combine lower power losses with output up to ten times as great, yielding circuits that are smaller and draw less power, making them more efficient and minimising any cooling requirements. GaN-based semiconductor devices offer five key characteristics as shown in Figure 2.9 [34]: high dielectric strength, high operating temperature, high current density, high-speed switching and low ON-resistance. These characteristics are due to the properties of GaN which include electrical breakdown characteristics ten times as

high as Si, a carrier mobility as good as or better than that of Si, and a bandgap three times or more that of Si.

2.5 GaN HEMT Technology

The main feature of GaN-based power and high-frequency devices is the two-dimensional electron gas, 2DEG, at the AlGaN/GaN heterojunction. The first report on the fabrication and operation of AlGaN/GaN heterojunction FETs, also called HEMTs, was by Khan in 1993 [35]. A high carrier density is generated at the AlGaN/GaN heterointerface due to spontaneous and piezoelectric polarization effects. The combination of the large carrier density and the high breakdown voltage enables high output power.

In this section, a general overview of AlGaN/GaN HEMT is given. This includes its basic operation, which is similar to other HEMT devices, and also its main properties. A main difference between AlGaN/GaN and other HEMT devices is the dependency of its operation on the piezo-electric effect, which is closely related to power switch trapping and has a huge impact on switch efficiency. The high electron mobility transistor (HEMT) is a heterostructure field effect transistor. A heterostructure is a structure that consists of at least two layers of semiconductor materials with different bandgaps. The interface between the different layers is refered to as heterojunction.

The AlGaN/GaN HEMT is a three terminal device where the 2DEG is the device's channel. The current between the source contact and the drain contact flows through the two dimensional conducting channel, and the channel is controlled by applying a gate voltage which depletes the channel thereby eliminating the source-drain current. The metal semiconductor junction can be divided into an ohmic contact and a Schottky

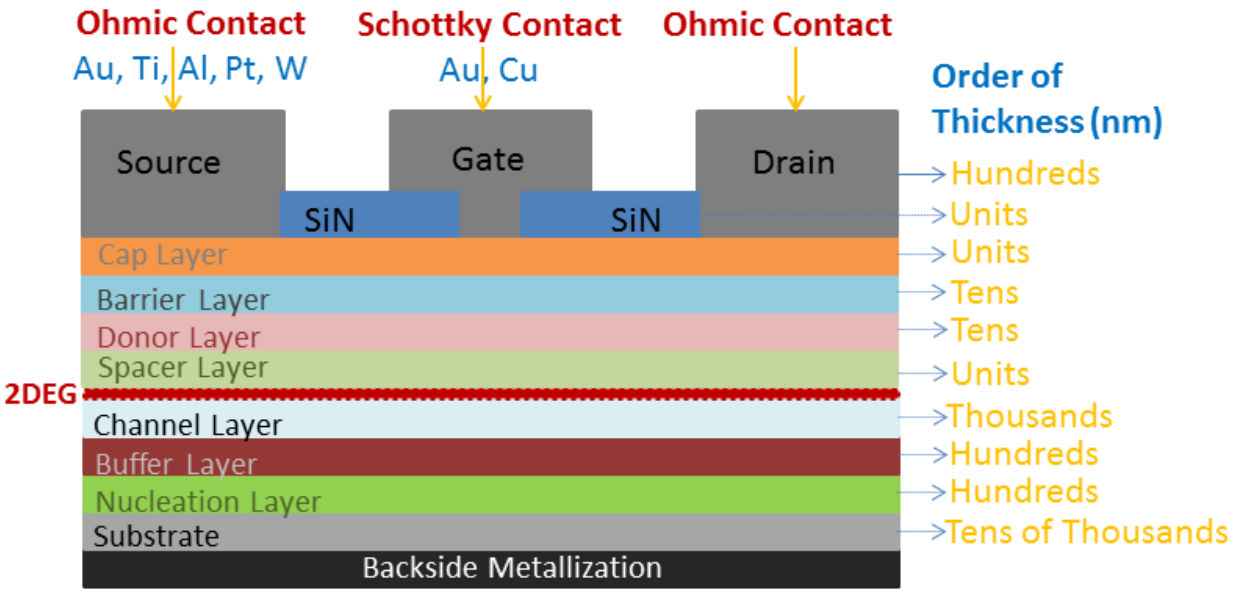

Figure 2.10: GaN HEMT Cross Section

contact. A contact with a linear I-V characteristic is defined as ohmic while a contact with a rectifying I-V relationship is defined as Schottky. Ohmic contacts are used as the drain and the source contacts in the device, whereas Schottky contacts are used at the driving gate. Generally, ohmic contacts on an AlGaN/GaN heterostructure are fabricated by depositing several metals followed by a rapid thermal anneal to alloy them. Titanium, aluminium, molybdenum and gold are the metals used to form the ohmic contacts. Several metals can create a Schottky junction with AlGaN. Nickel, Platinum, Molybdenum and Iridium are some of the common metals used because of their large work functions.

With the AlGaN/GaN heterostructure, it is possible to obtain, simultaneously, high voltage, high current and low on-resistance [36]. This results in high power-high efficiency operation. The AlGaN/GaN HEMT has demonstrated the ability to produce RF power on the order of hundreds of watts [32]. This is an achievable task due to the unique properties of the GaN material.

2.5.1 Basic Operation

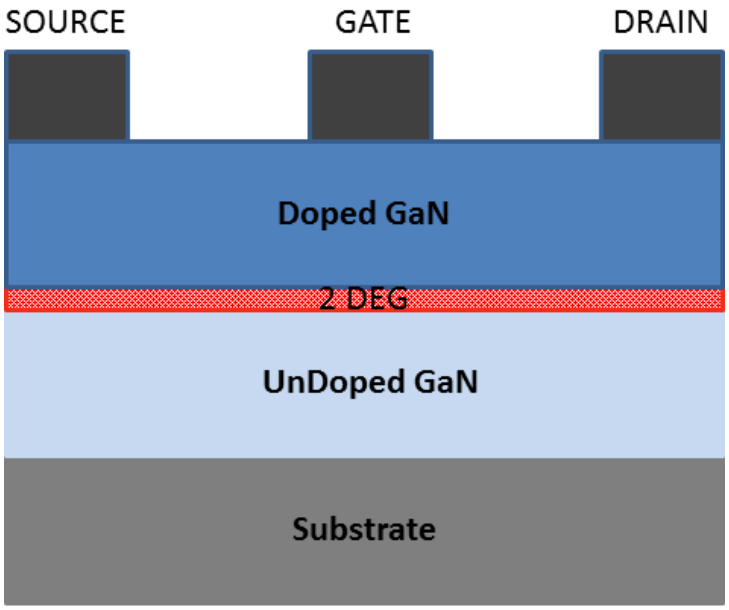

Figure 2.11: Cross Section of GaN HEMT: Basic Operation

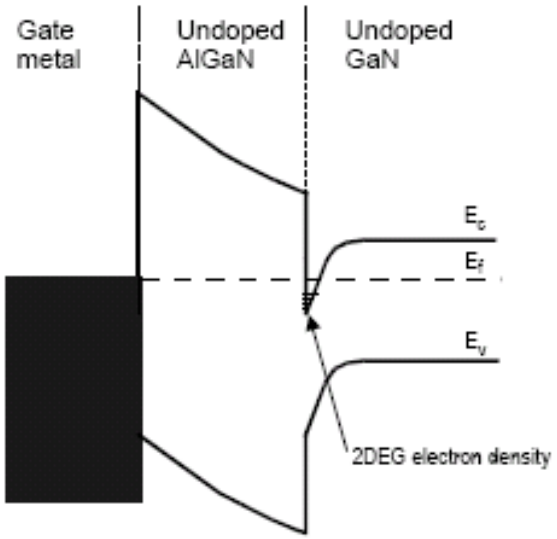

Figure 2.12: GaN HEMT Band Diagrams

The simplified structure of an AlGaN/GaN HEMT is shown in Figure **??** [37]. The wide-bandgap semiconductor material (doped AlGaN) lies on a relatively narrow bandgap

semiconductor material (undoped GaN). In a similar manner to an AlGaAs/GaAs HEMT, a sharp dip occurs at the AlGaN/GaN interface in the conduction band edge, which results in the formation of a two-dimensional electron gas (2DEG) (Figure 2.12 [37]). The mechanism behind this is given below.

When the doped AlGaN and the undoped GaN layers are placed into contact, electrons transfer from the doped layer to the undoped layer in order to align the Fermi levels. As a result of this, a large electron concentration will be formed in the undoped GaN layer without the introduction of ionized impurities. At equilibrium, the net negative charge in the GaN layer balances, the net positive charge in the AlGaN layer that results from the departure of electrons to the GaN layer. The electrons in the GaN layer in this case will have a higher mobility than when the GaN layer is intentionally doped. This is because in this case, the spatial separation between the positive charge (in the AlGaN layer) and the negative charge (in the GaN layer) mitigates the Coulomb interaction between them [38].

This process of increasing the carrier concentration without compromising the mobility is referred to as modulation doping. The electrons in a modulation-doping process are confined by a triangular- well-like potential, with a very small thickness compared to the width and length of the channel (Figure 2.12). Spatial quantisation occurs within this potential well, where it produces discrete energy levels called subbands [39]. The quantisation is in the direction perpendicular to the heterojunction, so there is no quantisation in the two directions that are parallel to the interface. This forces the electrons to move in a two-dimensional plane parallel to the heterojunction. This two-dimensional electron sheet is referred to as a two dimensional electron gas (2DEG) [38].

Experimental results show that, over a wide range of temperatures, the 2DEG mobility is higher than the mobility of electrons in an intentionally-doped material [40]. The high-frequency performance capability and the very low noise performance of GaN HEMTs is mainly due to the high mobility of the 2DEG [32]. In contrast to the formation of the 2DEG in the AlGaAs/GaAs HEMT, the following two phenomena have been observed with regards to the formation of the 2DEG in the AlGaN/GaN HEMT [37]:

- The 2DEG is formed in the AlGaN/GaN interface even when AlGaN layer is not intentionally doped.
- The charge density in the 2DEG is not proportional to the amount of doping when the AlGaN layer is intentionally doped.

2.5.2 GaN HEMT Power Switches

The use of a FET as a switch results from the fact that the path between source and drain can be seen as a voltage-controlled resistance [41]. In contrast to the situation when the FET is used as an amplifier there is no DC bias applied to source or drain. A DC bias applied to the gate controls the opening and closing of the switch. In addition to the variable resistance there is also a capacitance associated with the FET which is dependent on the size of the device and also on the process used for manufacture.

The I-V characteristics of a typical power switch is illustrated in Figure 2.13. An ideal transistor conducts current in the ON-state with zero voltage drop and blocks voltage in the OFF-state with zero leakage current. In addition, the ideal device can operate with a high current and voltage in the active region, with the saturated forward current

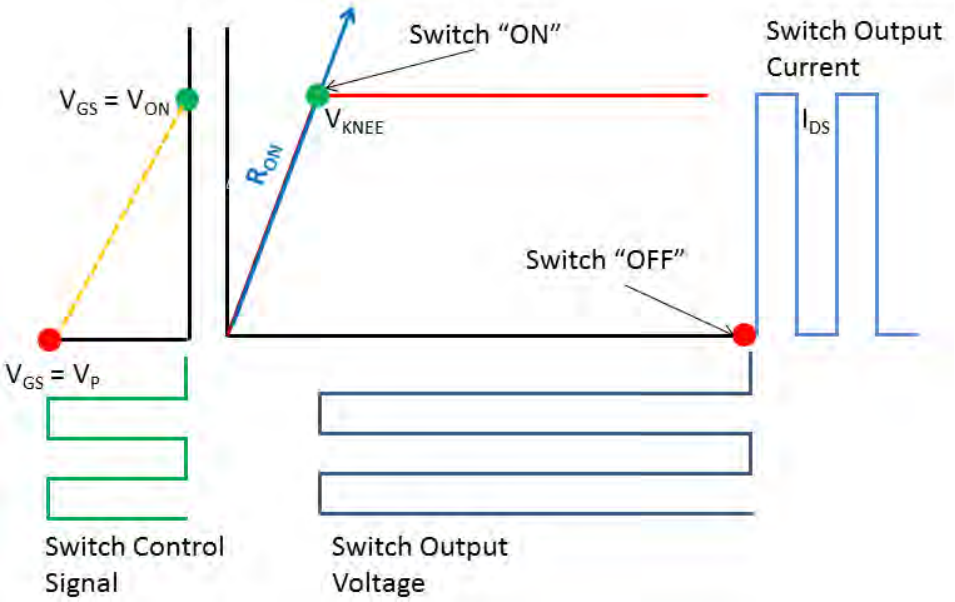

Figure 2.13: Power Switch Loadline

in this mode controlled by the applied gate bias. The spacing between the characteristics in the active region is uniform for an ideal transistor, indicating a gain that is independent of the forward current and voltage.

The typical transistor can operate with a high current and voltage in the active region. This current is controlled by the gate voltage. In reality the device exhibits a finite resistance when carrying current in the ON-state as well as a finite leakage current while operating in the OFF-state. The spacing between the characteristics in the active region is non-uniform for a typical transistor, with a square-law behaviour for devices operating with channel pinch-off in the current saturation mode.

2.5.3 Switch Operation

AlGaN/GaN HEMTs are three-terminal devices where the current flows from the source to the drain via the 2DEG at the AlGaN/GaN interface. The current flow is regulated by the gate Schottky diode that can deplete the channel. Figures 2.14 and 2.15 depict the schematic representation of the electron flow under the "ON" condition. where electrons flow from source to drain via the 2DEG, and the "OFF" state with no electron flow. When the gate is in overdrive (Figure 2.16), the electrons flow via the 2DEG from source to drain and through the AlGaN from source to gate.

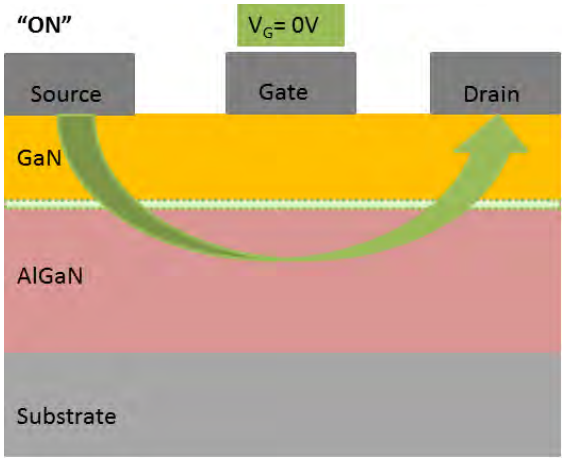

Figure 2.14: GaN HEMT: ON State

Figure 2.17 shows the transfer characteristic of an AlGaN/GaN HEMT which highlights the features of these devices, where there is a large negative threshold voltage and then a sudden increase of the gate current for large positive gate bias. The negative threshold is a consequence of the natural presence of the 2DEG which leads to a normally-on device configuration.

The sudden increase of the gate current for positive gate voltage is a consequence of the Schottky nature of the transistor's gate: when it is biased in the forward condition the

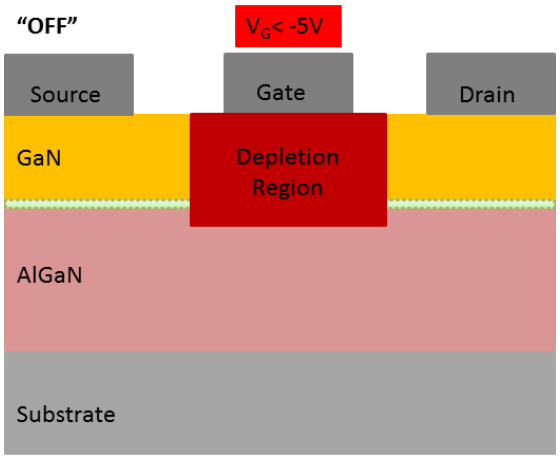

Figure 2.15: GaN HEMT: OFF State

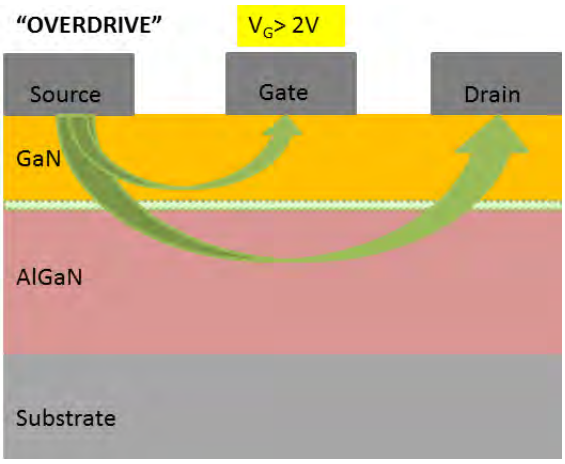

Figure 2.16: GaN HEMT: Overdrive

current exponentially increases with the gate voltage. Moreover this state corresponds also with saturation of the drain current, since the carriers injected from the source are now collected both on the drain and on the gate contact. This condition is normally avoided during device operation since an excessive gate current jeopardises both the device and the driving circuit. Therefore, normally the gate swing is limited from the off-state to the gate voltage that results in 1 mA/mm of gate current.

Adjustment of the gate-drain spacing, as well as the addition of field plate structures are commonly used to increase the device breakdown voltage. The gate width, W_G, de-

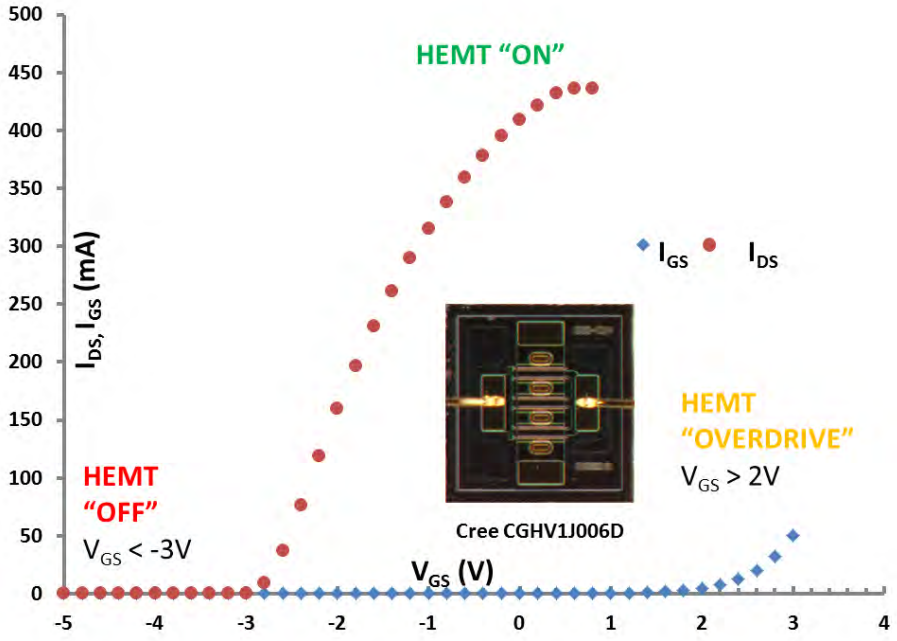

Figure 2.17: I_{GS} and I_{DS} curves

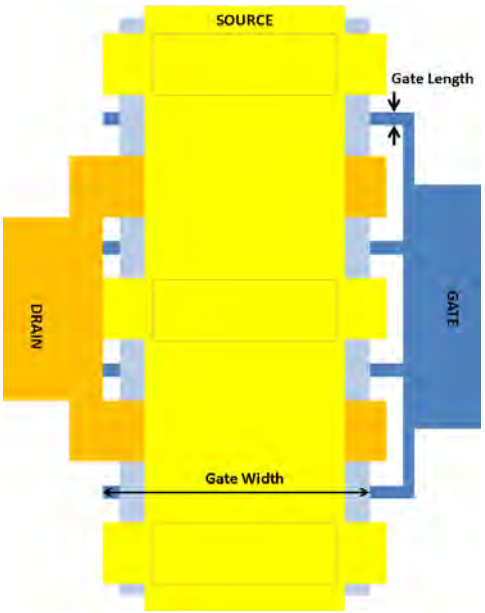

Figure 2.18: Large Periphery GaN HEMT structure

termines the drain saturation current. Unit cells are paralleled to obtain larger devices, the sizes of which are defined in terms of the gate periphery, $N_G \times W_G$, and N being the

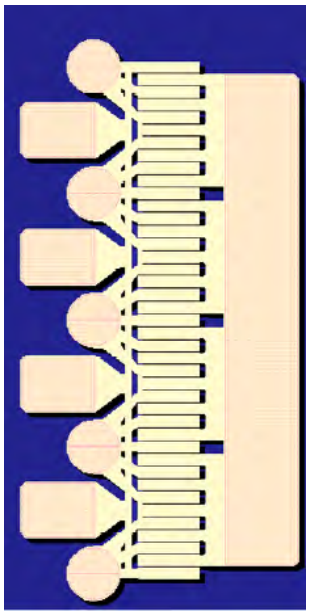

Figure 2.19: TQS 25 W Die

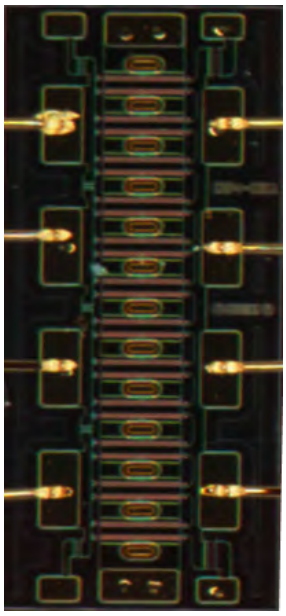

Figure 2.20: Cree 25 W Die

number of gate fingers. As with other technologies, device size determines the on resistance, device capacitances and current handling capabilities. Figure 2.18 shows a schematic of a large-periphery GaN device made up of smaller unit cells. Figures 2.19 and 2.20, show 25 W large-periphery 0.25 μm devices from Triquint Semiconductor and Cree Semiconductor respectively.

2.5.4 Normally-Off GaN Power Switch

A GaN-based HEMT transistor is a three-terminal device in which the current flowing between the ohmic source and the drain contacts is modulated by the Schottky metal gate contact. The majority carriers, electrons, are traveling through the highly conductive 2DEG channel formed at the AlGaN/GaN interface, and their number is modulated by the electric field resulting from the gate bias. Such transistor is usually working in the depletion mode, i.e. at V_{GS} = 0 V, the device is normally in its ON

state allowing current to flow through it. Such characteristics are a big concern for switching applications to ensure operation. High current levels in the device may occur unintentionally when gate control is lost. Therefore, reliable normally-OFF devices are needed.

There are 3 primary approaches in the literature to achieve E-mode operation, which is particularly important for power FETs. The first approach is to employ a deep gate recess. However, in this approach, the gate diode can be composed of a very thin AlGaN barrier (< 5-10 nm depending on the Al composition in the barrier) with a low turn-on Schottky barrier (< 1 V). Employing an AlGaN barrier offers an attractive solution in achieving E-mode operation with a thick AlGaN barrier under the gate [42]. The second approach is to use Flourine treatment, where F ions/atoms with high electron negativity are implanted into the AlGaN barrier, thus depleting electrons in the channel [43]. However, in this approach, the carrier mobilities generally degrade; furthermore, the stability of F- implanted in the barrier, thus device reliability, is still a debatable issue. The third approach is to use an AlGaN/GaN heterostructure on nonpolar substrates [44]. Since the spontaneous and piezoelectric charges are zero along the nonpolar directions, the as-grown heterostructure has no 2DEG formed without external doping (generally Si). However, in this approach, a gate recess is still necessary; furthermore, high quality non-polar substrates are currently prohibitively expensive and of small size.

2.5.5 Switch Efficiency and Figure of Merit

The energy losses of a switching device are divided into static losses and dynamic losses. The static losses are the losses when the transistor is in the on-state or the

off-state. In the on-state a transistor should demonstrate very low on-resistance in order to reduce the conduction losses. In the off-state the transistor should behave as a perfect open but, inevitably, some residual current, leakage current, flows. This leakage current should be very low in order to reduce the standby power consumption. The switching losses are due to the capacitance when switching from the on-state to the off-state and vice versa.

Static losses are frequency independent. The on-state loss, also known as conduction loss, is correlated to the effective on resistance of the power switch. The off-state loss results from a non-ideal off-state of the transistor at high voltages, where an off-state current causes power dissipation. In principle there is a trade-off between both mechanisms, since a lowered on-resistance causes higher off-state currents or reduces the available operating voltage and, potentially, the output power. In GaN HEMTs the on-state power loss is most relevant. GaN transistors have a typical on-resistance of several ohms per millimetre gate width (W/G).

Switching losses are dynamic losses that occur when switching the device ”ON” and ”OFF”, due to the charging/discharging of capacitances at the input and output of the device. Switching losses are frequency dependent and thus increase with increasing switching speed. There are two major components to switching loss, the one occurring at the output drain side (switch node) while the gate drive losses occur at the input side. Switch Node loss is considered to be determined solely by charging and discharging the equivalent switching node capacitance. The same considerations apply to the term related to gate driving losses, except that in this case energy is lost both during charging and discharging of the equivalent gate capacitance.

Switch based models for switching power amplifiers are given in [45], [46]. For sub-

giga-hertz switching power FETs, a resistive switch (R_{ON}) and associated gate-drain (C_{GD}), gate-source (C_{GS}) and drain-source (C_{DS}) intrinsic capacitances along with intrinsic drain and source inductance form the core of a HEMT power switch model as shown in Figure 2.21. In addition to the intrinsic parasitics within the device, additional extrinsic parasitics can be added to obtain a much more complex loss model.

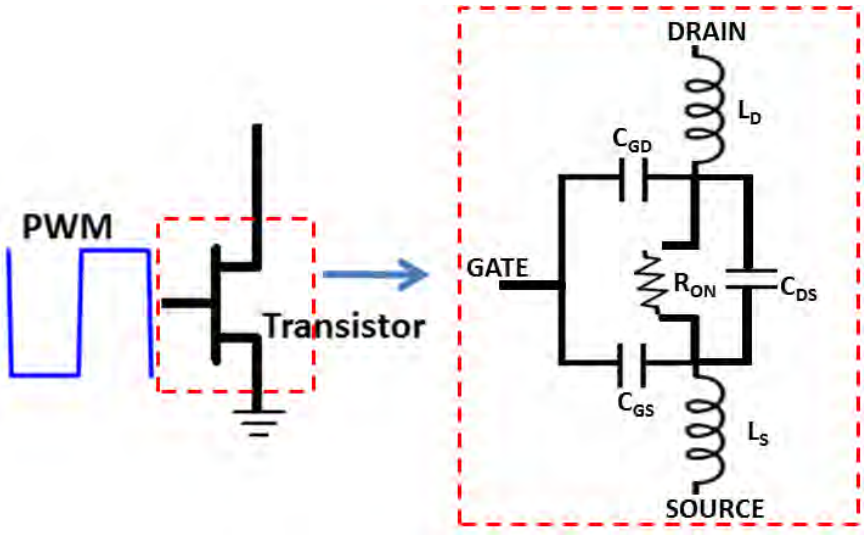

Figure 2.21: Power Switch Core HEMT Model

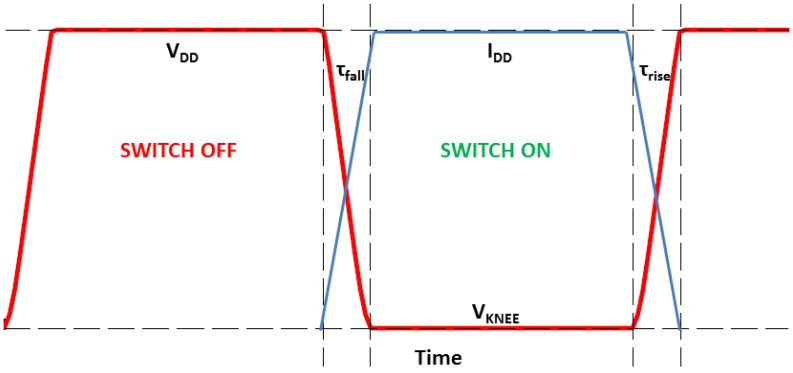

Figure 2.22: Power Switch Square-Wave Operation

The conduction loss within a FET can be calculated as :

$$P_{Cond.Loss} = I_{RMS}^2 R_{ON} \tag{2.1}$$

where R_{ON} is the on-resistance of the HEMT and I, is the current through the device. The rms value of the rectangular current waveform shown in Figure 2.22 is given by:

$$I_{DD} = \frac{I_{RMS}}{\sqrt{D}} \tag{2.2}$$

where D is the ON-time duty-cycle fraction.

The switching loss within a FET can be calculated as :

$$P_{SW.Loss} = \frac{1}{2}(C_{SW} V_{SW} f_{SW}^2) \tag{2.3}$$

where $C_{SW} = C_{OUT}$ is the output capacitance at the switch node, with C_{SW} = 2 x C_{IN} at the input gate side. (Here it is multiplied by a factor of two to denote the charging and discharging of the gate capacitances.) The voltage swing, $V_{SW} = V_{DD}$, is the output voltage at the switch node, and at the input gate $V_{SW} = V_{GS}$ denoting the voltage drive swing. Here C_{GS} and C_{GD} contribute towards C_{IN} while C_{DS} influences C_{OUT}.
f_{SW}^2 is the switching frequency of the power switch.

The total power loss within a HEMT in a switching topology can be given as :

$$P_{TOTAL} = P_{Cond.Loss} + P_{Sw.Loss} \tag{2.4}$$

The use of microwave FETs as high frequency switching power devices can be described in terms of their RF characteristics like Power added efficiency (PAE), current-gain cut-off frequency (F_T), ON-state resistance (R_{ON}) and input capacitance (C_{IN}).

They were first report for GaAs devices in [47].

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{1}{2}\frac{(V_{BD} - V_{KNEE})}{(V_{BD} + V_{KNEE})}(1 - \frac{1}{G(j(\omega)}) \tag{2.5}$$

and

$$F_T = \frac{g_m}{2\pi C_{IN}} \tag{2.6}$$

The PAE expression above emphasises the two types of power losses induced in the RF devices :

a) The dc losses is given by $\frac{1}{2}\frac{(V_{BD}-V_{KNEE})}{(V_{BD}+V_{KNEE})}$ where V_{KNEE} which represents the lower limit of the linear voltage range of the transistor. V_{KNEE} is known to be proportional to the on-state parasitic resistance R_{ON} of the device.

b) The high frequency or dynamic power loss given by (1-$\frac{1}{G(j(\omega)}$) decrease when the frequency increases and reaches unity gain at a cut-off frequency slightly smaller than F_T. At this frequency, PAE drops to zero. As a consequence, the dynamic losses depend on the input capacitance.

For power switches the DC power losses or the on-state power losses are directly proportional to R_{ON} and thus to V_{KNEE}. The switching power losses depend on the transition times, which are proportional to C_{IN}.

As a result, the efficiency of a power transistor, regardless of it RF or power switching application , may be represented by $R_{ON}$and C_{IN}. The smaller the product of R_{ON}

and C_{IN}, the higher is the power efficiency. The design of efficient GaN-based HEMT switching devices should then take into consideration the two main parameters: ON-state resistance and gate-channel capacitance. The gate-channel capacitance is the main contributor to the rise and fall times leading to switching loss. Hence the intrinsic capacitance is very much dependent on the process technology used for fabrication of the device [41].

2.5.6 Lateral Depletion Region

One of the major advantages of the GaN process, is the high drain voltage capability, enabling it to deliver large output power. The key parameter to this is the high off-state device break down voltage. The large off-state breakdown routinely measured on AlGaN/GAN HEMTs is a consequence of an extended lateral depletion region that considerably extends from the gate area towards the drain side with increasing gate-drain bias [48], [49].

The breakdown voltage of AlGaN/GaN HEMT increases with gate-drain spacing, however, R_{ON} also scales with gate-drain distance. A large breakdown voltage translates into a larger R_{ON}, and therefore it negatively impacts the final device efficiency. In the ideal scenario, the device breakdown should be designed to be as high as the maximum operating voltage and not beyond it, in order not to impact R_{ON}. However, real devices are designed with a breakdown voltage considerably larger than the maximum operating voltage, therefore not benefitting from the full potential of the device. Hence a tradeoff between R_{ON} and maximum breakdown has to be found. This translates to an appropriate process technology and its corresponding R_{ON} value for a given switching frequency and breakdown value. Figure 2.23 shows the breakdown voltage and the

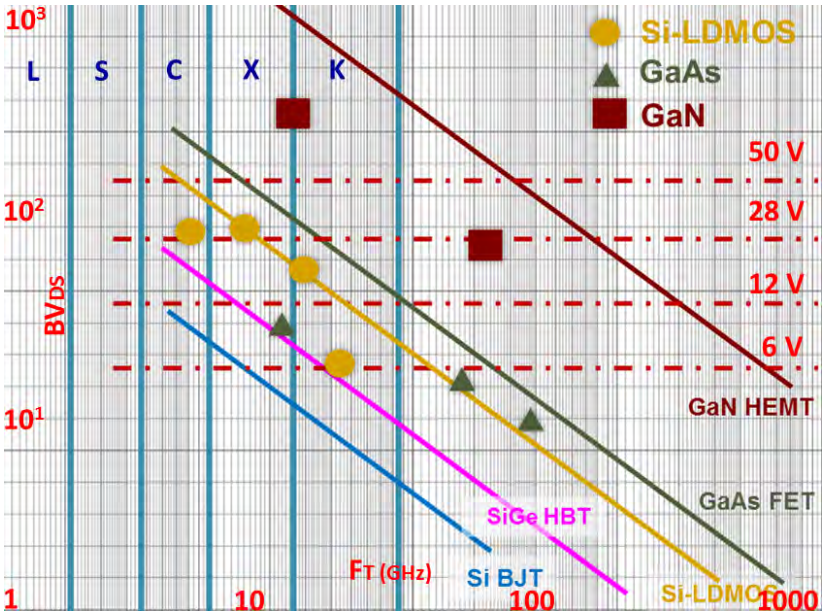

Figure 2.23: BV v F_T of Microwave Transistors

corresponding F_T of microwave transistor FETs [33].

2.5.7 Field Plates

In order to increase the RF output power it is necessary to decrease the leakage current resulting from the tunnelling of electrons from the gate metal to the surface of the semiconductor. This can be accomplished by decreasing the magnitude of the electric field at the gate edge. The use of field plate (FP) technology has long been recognised as a useful technique for suppression of voltage at critical locations within a semiconductor device [50]. The concept has recently been revisited for use in AlGaN/GaN HEMTs with excellent success [51]. The field plate consists of an additional metal layer located over the gate metal and extending into the region between the gate and drain. The gate metal provides an electric-field termination layer that reduces the magnitude of the field at the gate edge, thereby suppressing the gate leakage current

[50].

The use of field-plate technology permits high drain bias voltages to be applied, thereby producing improvements in RF output power. In fact, the degree of gate leakage suppression is sufficient to permit drain bias on the order of $V_{DS} \geq 140V$ to be applied. This allows high RF output power to be generated [50]. However, field plates also introduce additional capacitance and reduce the transconductance of the transistor. Therefore a degradation in frequency performance occurs. For this reason, a minimum field-plate length should be employed [50].

Two different configurations for field-plates have been investigated: gate connected and source connected, and they are illustrated in the following two sub-sections.

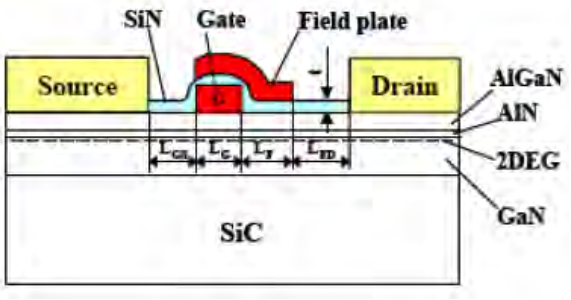

Figure 2.24: Cross Section of GaN HEMT with field plate

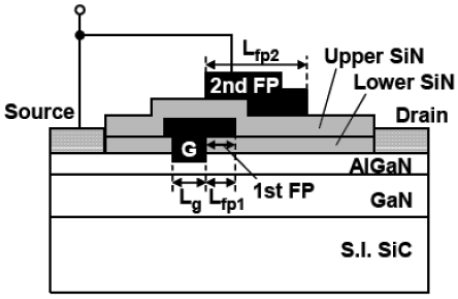

Figure 2.25: Cross Section of dual field plate FET

Figure 2.24 shows the cross section of a field-plated GaN HEMT [52]. The function of a FP is to modify the electric field profile and to decrease its peak value, hence reducing trapping effects and increasing breakdown voltages. Initial FPs were either constructed as part of the gate or tied to the gate externally. This has been effective in increasing signal swings.

The longer the FP, the more output power is achieved. However, in this configuration the capacitance between the FP and drain becomes gate-to-drain capacitance (C_{GD}),

resulting in negative Miller feedback. This causes reduction in current-gain and power-gain cut-off frequencies (F_T/F_{MAX}) [52].

Source connected field plates were investigated in [52]. It was revealed that, since the voltage swing across the gate and source is only 4-8 V for a typical GaN HEMT, much less than the dynamic output swing of up to 230 V, terminating the FP to the source also satisfies the electrostatics for it to be functional. In this configuration, the FP-to-channel capacitance becomes the drain-source capacitance, which could be absorbed in the output tuning network. The drawback of additional C_{GD} is hence eliminated [52].

Figure 2.25 shows a dual-FP structure, which combines a conventional FP and a source-terminated FP, applied to a AlGaN/GaN FET to improve collapse, breakdown, and gain characteristics, simultaneously. The first FP is a part of the gate, which improves the breakdown characteristics while suppressing the current collapse. The second FP is formed on a SiN film at the gate edge and connected to the source. This functions as a shield of the electric field between the first FP and the drain, and hence eliminates the drawback of increased C_{GD} [53]. Using this technique a breakdown voltage of 250 V was achieved, and C_{GD} was halved thereby increasing the MSG by 3 dB at 2 GHz [53].

The breakdown voltage can also be increased by increasing the dielectric constant of the insulator beneath the field plate [51]. Another way to reduce the feedback capacitance, and thereby improve the transconductance and gain characteristics of AlGaN/GaN FP FET, is the use of a recessed-gate structure [54], shown in Figure 2.26.

In [54], it was found that the gate recess was effective in removing residual current col-

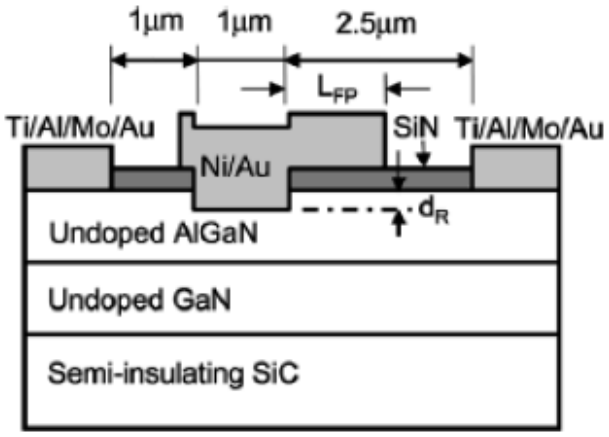

Figure 2.26: Cross Section of field plate with recessed gate structure

lapse and increasing transconductance and consequently linear gain. This technique was also investigated [55] at mm-wave frequencies. Although the use of field plates permits a high drain voltage to be applied, operation of the device at a high bias can produce physical effects that influence the performance of the device. The field-plate introduces a high electric field region within the conducting channel located under the edge of the field plate. It moves the high electric field region away from the gate edge, but moves it into the conducting channel region between the gate and drain where it can facilitate channel breakdown in an AlGaN/GaN HEMT [56].

2.5.8 Trap Effects

A high drain voltage in GaN makes it possible to get higher output power, however when used as power switches it suffers from trapping effects that lower the knee current and increase the knee voltage, thereby increasing the R_{ON} and hence dramatically reducing the output power.

The concept of dynamic R_{ON} has been introduced to explain the influence of trap-

ping effects in a power switch [48]. Assuming that trapping of electrons leaking from the metal gate take place at the AlGaN surface, this would reduce the total amount of positive charge present at the AlGaN surface between the source and drain, therefore leading to an increase in the resistance between the gate and the drain region within the HEMT. The amount of trapped electrons accumulating between the gate and the drain terminals is directly proportional to the quiescent drain bias voltage [57], [58], [59], [60], [61]. These trapped charges deplete the electrons in the channel, thereby increasing the resistance and leading to a decrease in the drain current. This sudden increase in resistance, called dynamic-R_{ON}, is normally associated with switching from a high drain bias condition [62], [63], [64], [65].

Consequently, the effect of trapped surface negative charge is to act like a negatively biased metal gate. In this condition, there are now two gates on the surface, between the source and drain, connected in series. The potential on the metal gate is controlled by the applied gate bias while the potential on the second gate is controlled by the amount of trapped charge in the gate-drain access region. This second gate is often referred to as the "virtual gate" [48].

The power switch output drain current in the presence of trapped charges between gate and drain is then controlled by the mechanism that supplies charge (trapping) and removes charge (de-trapping), in addition to the applied gate bias. Therefore, the trapping and de-trapping times govern the frequency response of the device. Consequently, if the frequency response of the device is lower than the frequency of the applied signal, then dispersion phenomena occur and, if the applied signal is slow enough, the device is able to react as in a DC case.

It should be noted that the trapping phenomenon is also present in the bulk layer.

These trapping centres are normally energetically close to the valence band (deep states) and physically located far from the AlGaN/GaN interface [66]. Nevertheless, electrons can get trapped in these trapping centres, therefore influencing the device is built-in (V_{bi}) potential.

Trapping affects the properties of the active layer in the HEMT, depending on the position of the trap, either as a change in V_P or of the access resistance(R_{Do}). When the traps are located in the proximity of the region underneath the gate terminal, the g_m-V_{GS} characteristic exhibits a shift in V_P. This could be interpreted as traps modifying the built-in potential, V_{bi}, of the HEMT.

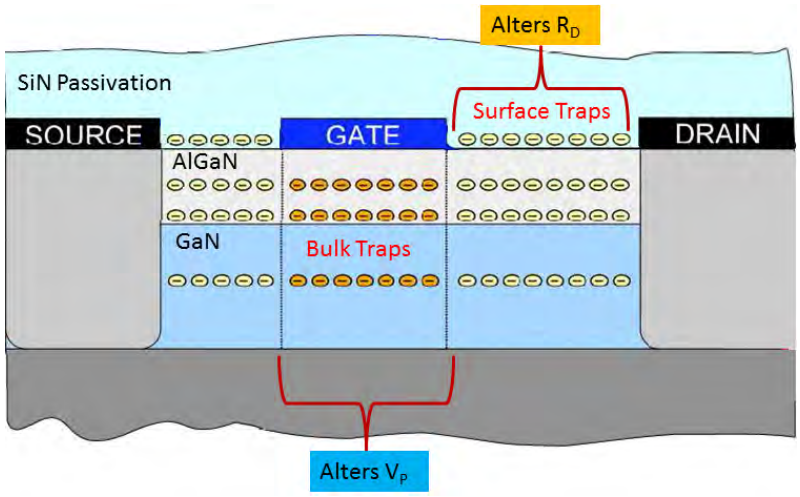

Figure 2.27: Trap location within GaN HEMT

Figure 2.27 shows the trap location within a GaN HEMT [67]. Traps located on the surface between the gate and drain terminals alter the knee voltage of the I_{DS}-V_{DS} characteristic by increasing the resistance. In GaN power switches, electrons get trapped near the channel region between the gate and the drain, which causes an increase in R_{ON}.

Figure 2.28, shows the power switch load line for a Cree CGHV4006 device and the

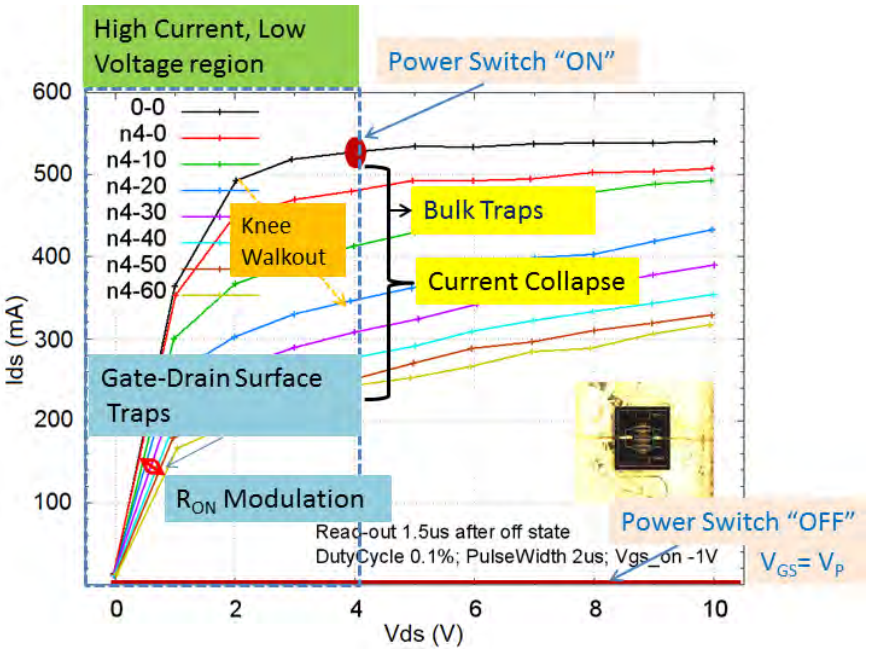

Figure 2.28: Trapping Effects: Power Switch Load-line shift

corresponding downward shift in power switch "ON" position. This shift in the R_{ON} and the corresponding current collapse evident in the linear region of the I_{DS} - V_{DS} load line can be captured using an SRH based trap model which is described in detail in the next section.

2.5.9 Surface Passivation

Depositing a passive layer on top of the AlGaN surface helps to mitigate the effect of traps between the gate and drain terminals. With appropriate passivation, the output power level could almost reach its maximum output level [68], suggesting that the surface passivation prevents the accumulation of charges between the gate and drain terminals [62]. Figure 2.29 shows the cross section of GaN HEMT with passivation.

Nevertheless, it has to be highlighted that, if the AlGaN/passivation interface or the

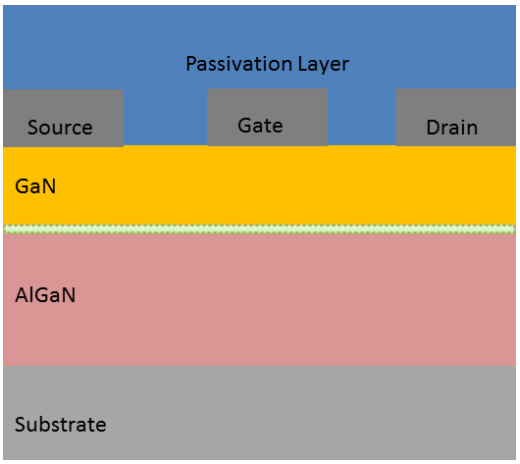

Figure 2.29: Cross Section of GaN HEMT with Passivation Layer

bulk of the passivation contains charge trapping sites, then electrons leaking from the gate metal under the influence of the large electric field present during high power operation can get trapped. This trapped negative charge can cause a negatively charged virtual gate to develop in a manner similar to that of an un-passivated surface as previously described. Therefore the effect of passivation is a strong function of surface and material quality. However large variation exists even with nominally the same passivation process and surface treatments. For this reason, different foundries usually have their own preferred passivation dielectrics. Silicon nitride (Si_3N_4) is the most widely used one on AlGaN/GaN HEMTs [69]. Variation in the passivation techniques and the fact that large periphery devices contain more trap centres, causing increased trapping phenomena to occur within the device, and explains the R_{ON} modulation under high quiescent drain bias voltage in a large area device.

2.6 SRH Trap Model

A number of trap models have been surveyed by Rathmell *et al.* in [70],[71]. These trap models have either not dealt with large signals [72], or have fixed trap time constant [73]. These two factors can be considered as drawbacks of many previous models, as trapping characteristics, including trap time constant, have been shown to be highly dependent upon the operating condition of the transistor. Another drawback of some of previous models is the complexity of the model [74].

Trapping-related dispersion spans frequencies from DC to many GHz. Thus, a robust and accurate model that describes the FET behaviour from dc to RF is required [71]. This model can be applied through a feedback network that is separate from other effects such as impact ionisation [75] and self-heating [76]. A simple model, the SRH trap model, that overcomes the drawbacks of previous models, was proposed by Rathmell *et el.* in [70]. This trap model is based on the Shockley-Read-Hall theory of recombination of holes and electrons in solidstate. This model is able to predict both small- and large-signal behaviours of the FET. The following is a detailed description of this model.

Trapping in semiconductors occurs in energy states within the band gap. There are four competing processes for transferring charge from the trap level to the valence and conduction bands. These are:

Electron capture: defined as an electron dropping from a conduction-band level to the trap level. This is a reduction of electron energy.
Electron emission: defined as the promotion of electrons from the trap level to the

higher energy of the conduction band.

Hole capture: defined as a hole moving from a valence-band level to the trap level.

Hole emission: defined as the promotion of a hole from the trap level to the higher energy of the valence band.

All these four processes are governed by Fermi-Dirac statistics.

In the SRH trap model proposed in [70] a single-energy level trap is modeled by a capacitor charged by an emission current I_E and a capture current I_C and which is a function of the operating condition of the HEMT. Both currents are also functions of the potential v_{Tr} across the capacitor, C. Figure 2.30 illustrates this model. The trap current, i_{Tr}, is given by :

$$i_{Tr} = I_E - I_C, = \omega_0 C(V_0 - v_T) - \omega_0 C(v_T) exp(\frac{v_i}{kT}) \tag{2.7}$$

where V_0[V] is the trap potential when it is fully ionised, T[K] is the ambient temperature, k[eV/K] is the Boltzmann constant, ω_0 is the characteristic frequency of the charge capture process, v_i is the trap control potential given by,

$$v_i = \left\{ \frac{F_I - E_D}{+q} \right\} DonorTrap \tag{2.8}$$

$$v_i = \left\{ \frac{F_I - E_A}{+q} \right\} AcceptorTrap \tag{2.9}$$

where F_I is the quasi-Fermi level for holes and electrons and E_D E_A are the donor and acceptor energy levels respectively.

2.7 Circuit Model of Trap

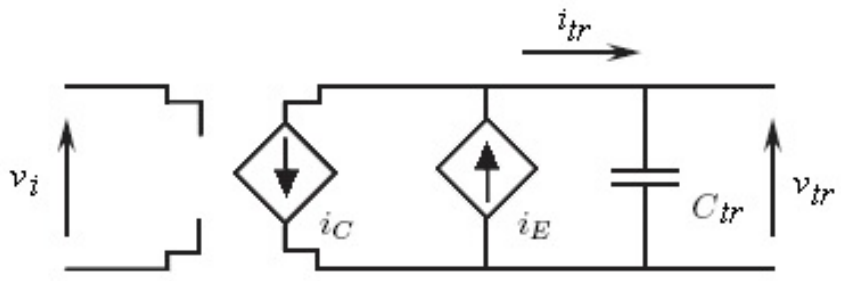

Figure 2.30: Schematic of Trap Model

Following on from the definitions of electron capture and emission, and hole capture and emission, given previously, the trap current, i_{Tr} can be separated into two terms: capture current which represents the rate of charge capture, and emission current which represents the rate of charge emission. The capture current is given by:

$$i_C = \omega_{0,Tr} C_{Tr} v_{Tr} exp(v_i/kT) \tag{2.10}$$

The emission current is given by:

$$i_E = \omega_{0,Tr} C_{Tr} v_{Tr} (V_0 - v_{Tr}) \tag{2.11}$$

A circuit model of the emission and capture processes in a trap centre is shown in Figure 2.30 [70]. The capture and emission currents are equal under steady-state con-

ditions. Thus the following relationship between the trap potential and the control potential is obtained :

$$v_{Tr} = V_0/(1 + exp(v_i/kT)) \tag{2.12}$$

Field-effect transistors can be affected by several trap processes. These are donor or acceptor traps in either the surface or bulk regions. Each of these dynamic trap processes exhibits specific frequency and bias dependencies that can be used to identify them. The dependence of the trap potential on the terminal potentials is implemented by assuming the trap control potential v_i to be a linear function of the instantaneous terminal potentials:

$$v_i = Av_{GS} + Bv_{DS} + C \tag{2.13}$$

where A, B and C are fitting parameters. This assumption was good enough for the studies carried out in this chapter.

It can be noted from the above equation that the two extremes of v_{Tr} are:

$$v_{Tr}(v_i = \infty) = 0, \tag{2.14}$$

$$v_{Tr}(v_i = -\infty) = Vo \tag{2.15}$$

2.7.1 Bulk Trap Model

To account for traps located in the bulk region, it is proposed that the drain current be modeled by adding the trap potential, v_{Tr}, to the gate potential. This model has been proposed [70] in a general manner without differentiating between surface and bulk traps. It is is based upon the consistency between the physical investigation of trapping and the electrical behaviour of the transistor when intentionally made traps in the bulk region are considered [67]. Traps in the bulk region have been shown to cause a shift in the threshold voltage in the g_m-V_{GS} characteristic in pulse measurement. The term bulk trap is used hereafter to describe this trapping behaviour. The potential of the bulk trap will be denoted here as v_{TrB}.

A first order approximation for bulk trapping can be modeled by setting the built-in potential (v_{bi}) of the HEMT to be a linear function of the trap potential:

$$v_{bi} = v_{bio} + \gamma v_{TrB} \tag{2.16}$$

where v_{bio}, is the built in potential when there is no bulk trapping and $\gamma \geq 0$ is a proportionality constant. When bulk trapping exists, the pinch-off voltage (V_P) is modified to:

$$V_P = V_{Po} + (\gamma v_{TrB}) \tag{2.17}$$

Referring to Figure 2.30, the gate source voltage is given by,

$$V_{GoSo} = V_{GS} - (\gamma v_{TrB}) \tag{2.18}$$

2.7.2 Gate-Drain Trap Model

As the applied quiescent drain voltage is increased, traps located on the surface region between the gate and the drain alter the drain access resistance which causes a shift in the knee voltage. This represents the physical effect of an increased trap potential of surface traps that increases with quiescent drain bias and depletes the underlying channel thus increasing the drain resistance. This is a valid assumption since traps in the surface region have been shown to cause a shift in $g_{m,peak}$ in the g_m-V_{GS} characteristic in the pulse measurement [18].

To account for such an alteration, it is proposed that the drain resistance (R_D) be linearly proportional to the trap potential:

$$R_D = R_{Do} + \beta v_{TrD}, \tag{2.19}$$

where R_{Do} is the isotrap drain and source resistances, $\beta \geq 0$ is a proportionality constant, and v_{TrD} is the potential of the drain trap.

The term surface trap is used hereafter to describe this trapping behaviour. Note that what distinguishes the trap location is the proximity of the trap to the terminals of the FET.

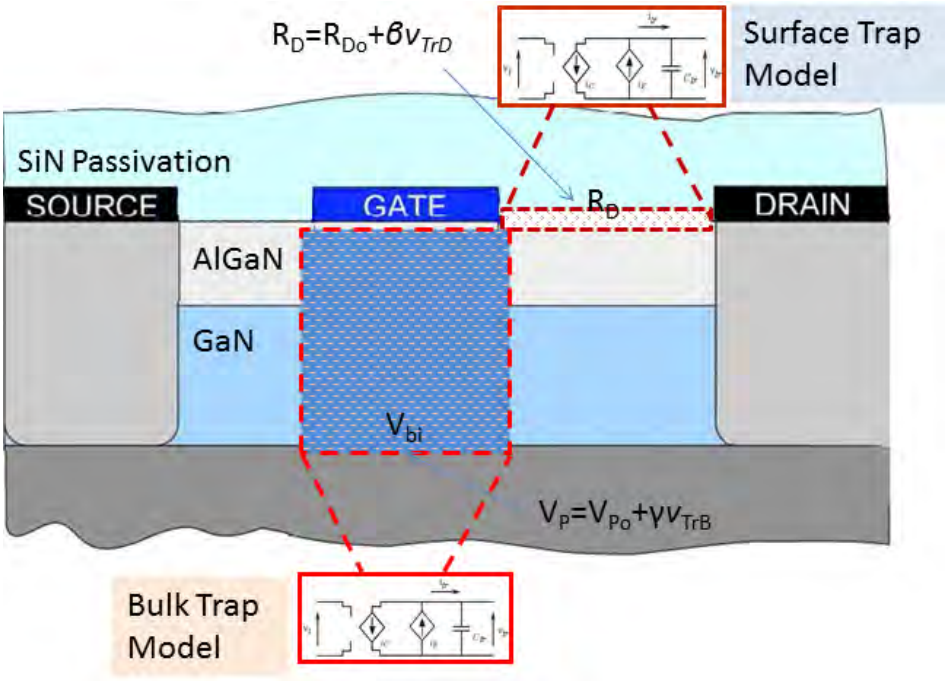

Figure 2.31: Trap location and corresponding Trap Model

2.8 Drain Current in the presence of Traps

The starting point in deriving an equation for I_{DS} in terms of v_{TrB} and v_{TrD} is to note that V_{GSo} and V_{DSo} are both functions of v_{TrB} and v_{TrD}.

$$V_{GSo} = V_{GS} - (\gamma v_{TrB}) \tag{2.20}$$

$$V_{DSo} = V_{DS} - (\beta v_{TrD}) \tag{2.21}$$

Therefore, in the presence of traps, I_{DS} will also be a function of v_{TrB} and v_{TrD}

$$I_{DS} = f(v_{TrB}, v_{TrD}) \tag{2.22}$$

In the following section, a mathematical expression of this relationship will be deduced. However, before going through the derivation, a few more notions need to be introduced.

g_d and g_m are the drain-source conductance and the drain transconductance respectively of the comprehensive HEMT model:

$$g_d \equiv \frac{\partial I_D}{\partial V_{DS}} \approx \frac{\partial I_{DS}}{\partial V_{DS}} \tag{2.23}$$

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \approx \frac{\partial I_{DS}}{\partial V_{GS}} \tag{2.24}$$

g_{d0} and g_{m0} are the drain-source conductance and the drain transconductance respectively of the inner HEMT model:

$$g_{d0} \equiv \frac{\partial I_{DS}}{\partial V_{DSo}} \approx \frac{\partial I_{DS}}{\partial V_{DSo}} \tag{2.25}$$

$$g_{m0} \equiv \frac{\partial I_{DS}}{\partial V_{GSo}} \approx \frac{\partial I_{DS}}{\partial V_{DSo}} \tag{2.26}$$

2.8.1 I_{DS} in terms of v_{TrB}

The rate of change of I_{DS} with v_{TrB} is given by

$$\frac{\partial I_{DS}}{\partial v_{TB}} = \frac{\partial I_{DS}}{\partial V_{GSo}} \frac{\partial V_{GSo}}{\partial v_{TB}} + \frac{\partial I_{DS}}{\partial V_{DSo}} \frac{\partial V_{DS}}{\partial v_{TB}} \tag{2.27}$$

$$= -g_{mo}\gamma - g_{do}(\beta v_{TrD}) \frac{\partial I_{DS}}{\partial v_{TrB}} \tag{2.28}$$

This equation can be modified to give

$$\frac{\partial I_{DS}}{\partial v_{TrB}} = \frac{-g_m \gamma}{1 + g d_o(\beta v_{TrD})} \tag{2.29}$$

The current I_{DS} can be obtained by solving the above differential equation, which gives:

$$I_{DS} = I_D SoB + \frac{-g_m \gamma}{1 + g d_o(\beta v_T rD)} (2.30)$$

where I_{DSoB} is the drain-source current when there is no bulk trapping. It should be mentioned that I_{DSoB} is still a function of the potentials introduced by drain end trapping.

2.8.2 I_{DS} in terms of v_{TrD}

The rate of change of I_{DS} with v_{TrD} is given by

$$\frac{\partial I_{DS}}{\partial v_{TrD}} = \frac{\partial I_{DS}}{\partial V_{GS0}} \frac{\partial V_{GS0}}{\partial v_{TrD}} + \frac{\partial I_{DS}}{\partial V_{DSo}} \frac{\partial V_{DSo}}{\partial v_{TrD}} \tag{2.31}$$

$$= \frac{-g_{d0}\beta I_{DS}}{1 + g_{d0}\beta v_{TrD}} \tag{2.32}$$

The above equation can be modified by the method of separation of variables, which gives:

$$I_{DS} = \frac{I_{DSoS}}{1 + g_{do}\beta v_{TrD}} \tag{2.33}$$

where I_{DSoS} is the drain-source current when there is no bulk trapping. It should be mentioned that I_{DSoB} is still a function of the potentials introduced by bulk trapping.

2.8.3 I_{DS} in terms of both v_{TrB} and v_{TrD}

I_{DS} can be obtained by solving for I_{DSoB} or I_{DSoS} in Equations(2.33) or (2.30).

I_{DSoS} can be easily found by setting v_{TrD} to zero.

When only bulk trapping exists, it simplifies to

$$I_{DSoS} = I_{DSo} - g_{mo}(\gamma v_{TrB}), \tag{2.34}$$

and when only drain trapping exists, it simplifies to

$$I_{DS} = \frac{I_{DSo}}{1 + g_{do}(\beta v_{TrD})} \tag{2.35}$$

2.9 Switch characterisation

Figure 2.32: Diva 265 Pulsed I-V System

Pulsed I-V measurement techniques have been used to visualize R_{ON} modulation by plotting the dynamic I-V characteristic of the device when used in power switching applications [77], [78], [79], [80]. Pulsed I-V measurement consists in applying a pulsed signal that drives the devices from a defined quiescent bias point (usually off-state at high drain bias) to points of the IV plane in order to chart the dynamic I-V characteristic.

A pulse measurement is performed by maintaining a constant quiescent bias on the device under test for a long enough time, and then applying a short pulse to the terminal potentials of the device. The terminal voltage and current are measured during the brief interval of the pulse. Two main criteria should be met during pulse measurements [81], [82]. These are:

• The pulses should be kept short enough so that the quiescent state is not disturbed

Figure 2.33: Auriga Pulsed I-V System

and the rate-dependent anomalies are avoided.

• The period between pulses should be kept long enough to ensure a full recovery to the quiescent condition.

Two pulsed I-V systems were used for the switch characterisations reported in this thesis. Figure 2.32 shows the DIVA 265 system while the Auriga 4850 system is shown in Figure 2.33.

2.10 Modulator Topology

The modulator circuits were characterised in a synchronous buck converter topology where an external PWM signal provides the gate driver pulses to switch the power

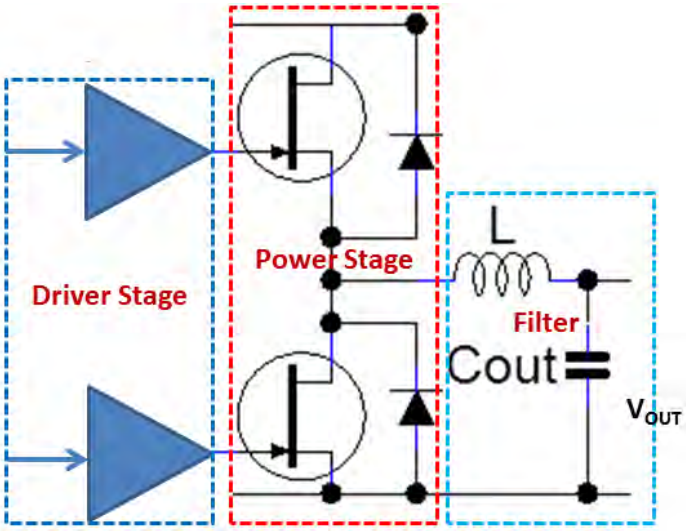

Figure 2.34: Synchronous Buck Converter

stage. The switching circuit is analogous to a voltage mode class D (VMCD) switching PA. Figure 2.35 shows the switching circuit which consists of 1) a power stage, 2) a driver stage, and 3) an output filter stage.

2.10.1 Power Switch

As discussed previously in section 2.5.9, a power switch can be modeled as a resistor between the source and drain terminals of a HEMT. A square-wave control signal at the gate turn "ON" and "OFF" the channel between the source and the drain. Inductances and capacitances can be added to the core resistor model to account for the intrinsic parasitics within the HEMTs. These parasitics play an important role in the loss mechanisms within the HEMT and will be described in detail in the next section.

An important concern is an adequate drive of the buck converter at high switching frequencies. This is accomplished by the high side and low side gate drivers which in turn are controlled by external PWM signals driven in anti-phase. The GaN power

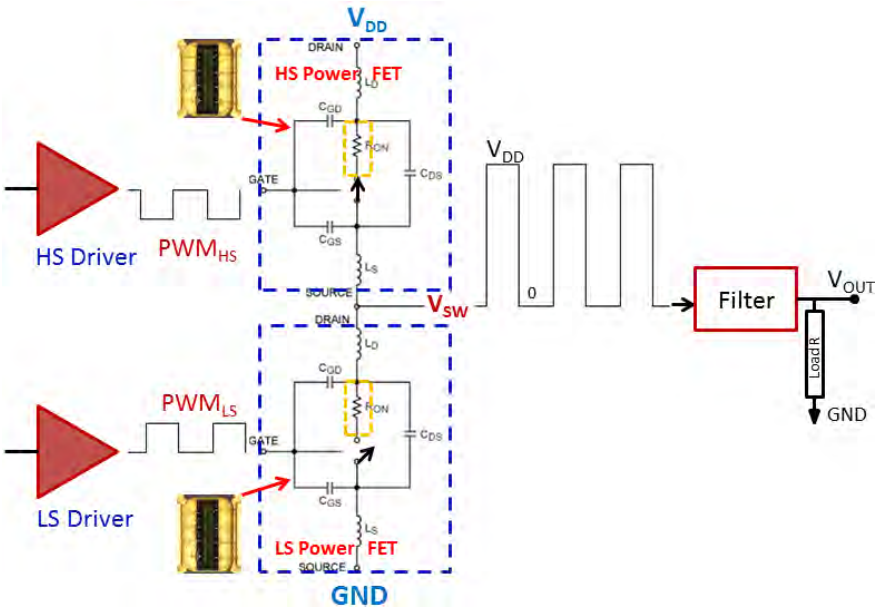

Figure 2.35: Buck Converter Schematic

HEMTs described in this investigation are normally "ON" depletion mode devices. Note that, in particular, the high side transistor poses a challenge due to the need to refer the gate control signals to the switching node, which is floating with respect to the power ground. Due to the absence of p-type transistors in the GaN process, the high side driver design is more complicated that for the low side driver because the gate voltage for the high side must have a very large voltage swing, from below ground to pinch-off the HEMT, to approximately the full power supply voltage. Gate drivers need to be optimised to minimise the power dissipation within the drive circuitry and with high voltage swing in the high side, currents through the high side drivers have to be as small as possible without compromising the power transistor gate switching voltage.

2.10.2 Gate Drivers

The gate driver circuits are inverter type circuits that generate a square wave at the gate, which turn the device ON and OFF [83]. These gate drivers in turn are driven by external PWM pulses. Inverter circuits are a functional building block of digital systems, and the availability of complementary devices in the CMOS process makes their implementation simple [84]. The GaN devices investigated were all D-mode devices and require a negative voltage for pinch-off. The lack of p-type active devices in GaN makes the design the of high side driver very challenging.

2.10.3 GaN Inverters

Inverters are based on two main parts (Figure 2.36): one is the switching transistor (ST) to which the input signal is applied and the other is a load element for the ST, which defines the type of the inverter and the switching characteristics. The inverter can be seen as two variable series resistors forming a voltage divider, where the resistance of at least one element is controlled by the input signal V_{IN}. The voltage at middle node is the inverter output signal V_{OUT}.

Maroldt has demonstrated high frequency gate drivers for gigahertz switching of switch-mode power amplifiers [85]. In the following section three inverter circuits based on switch mode power amplifier (SMPA) drivers are explored for use in a hybrid modulator topology. The main criterion in the design of a gate driver is the minimisation of dissipated power while providing adequate drive for high frequency switching of the power stage.

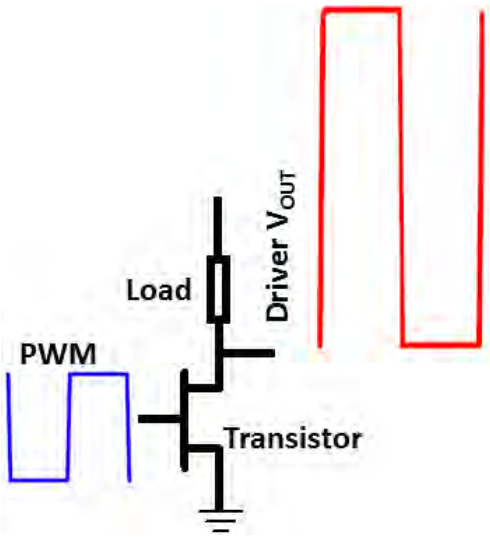

Figure 2.36: GaN Inverter Topology

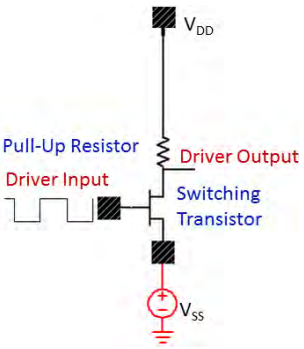

Figure 2.37: ST-R Gate Driver

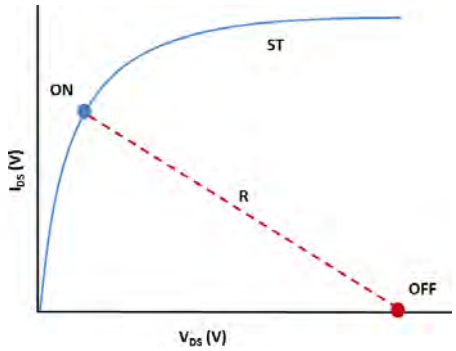

Figure 2.38: ST-R Gate Driver VTC

The most simple type uses a depletion-mode switching transistor and a pull-up resistor (Figure 2.37). It is a very simple design where the resistor acts as the load for ST. It has high static losses because of the static current flow during the on-state of the ST (output is low). Power is dissipated in the passive load resistor, R and the R_{ON} of the ST. The static operation points and switching principle of the ST-R inverter are shown in Figure 2.38. The constant resistive load produces a linear load line for the ST with two static equilibrium points referring to the on-state (output low level) and the off-state (output high level) of the ST. The transient switching trajectory between these two points is located on the linear load line.

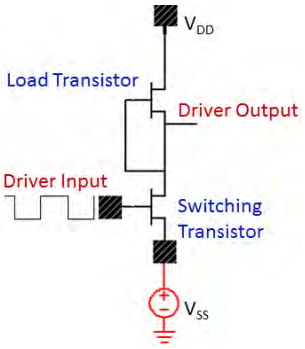

Figure 2.39: ST-LT Gate Driver

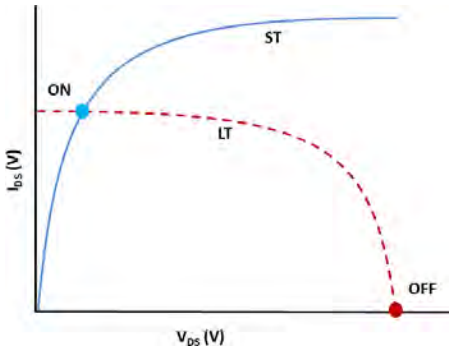

Figure 2.40: ST-LT Gate Driver VTC

Figure 2.39 shows an ST-LT inverter which uses a depletion-mode ST and a depletion-mode active load transistor (LT). The LT is designed to deliver similar static operation points for the ST-LT as compared to the ST-R. The gate-source voltage of the LT is fixed to 0 V, therefore the current level of the LT, which defines the on-state of the ST, is decided by the gate periphery of the LT. The transient switching trajectory is fixed to the I_{DS}-V_{DS} characteristics of the LT at V_{GS} = 0 V. In contrast to the resistive pull-up, the depletion-mode LT of the ST-LT produces a variable load resistance. The resistance of the load is high during the low-resistance on-state of the ST (output low level) and vice versa. A faster switching behaviour can be achieved by this design than for the ST-R inverter.

The ST-R-LT inverter (Figure 2.41) is a modified ST-LT circuit using a depletion-mode LT and a series resistor R to modulate the resistance of the LT. A current flowing through the ST and the series resistor induces a negative V_{GS} for the LT, which increases the resistance of the LT (output low). On the other hand, a minimum current of zero through the ST in off-state and through the resistor R (output high) leads to a maximum V_{GS}(LT) of 0 V and therefore a minimum resistance for the LT .

But it has to be mentioned that the minimum on-resistance for the low side of the in-

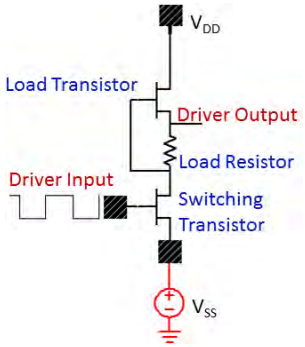

Figure 2.41: ST-R-LT Gate Driver

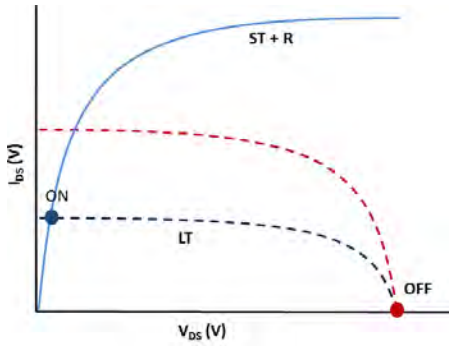

Figure 2.42: ST-LT-R Gate Driver VTC

verter voltage divider, which was given only by R_{ON} of the ST in the other inverter types, is increased in the ST-R-LT type by the value of the series resistor R. Nevertheless with this circuit an increase in the LT resistance results in a better switching behaviour compared to the basic ST-LT inverter. Finally, a lower static current and therefore lower static power consumption is obtained by the ST-R-LT inverter. The corresponding static output characteristics and static operation points are shown in Figure 2.42. Notice that the I_{DS}-V_{DS} curve for the ST is the sum of the ST and the series R as mentioned before.

2.10.3.1 Comparison of Driver Topologies

Figure 2.43 [85] gives the comparison of all three driver topologies and their transient simulations. The simple resistor pull-up topology is a robust design that will perform the switching functionality with ease.

In the second case, where the resistor is replaced by the FET as the load of the bottom switching transistor, it gives better rise and fall times, as the driver can be engineered by adjusting the W/L ratios of the switching transistor and the load transistor. In the third scenario, the driver was further optimised by introducing a resistor between the

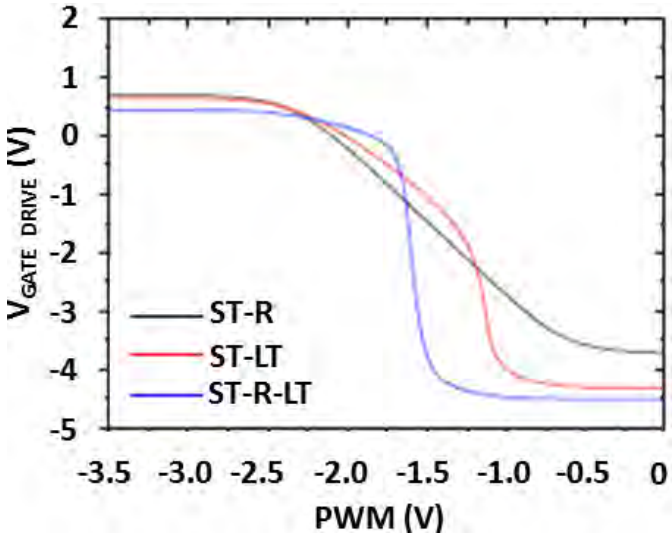

Figure 2.43: Voltage Transfer Characteristics for all driver Topologies

source of the LT and the drain of the ST. However, it should be noted that the gate periphery of commercially available bare-die devices is already set and hence only the resistance value can be adjusted externally.

2.11 Literature Review

2.11.1 GaAs Power Switches

This section details the published power switch implementation in GaAs technologies. CMOS implementations are not considered due to the fact that the output power is several times as small as with III-V technologies.

High speed GaAs vertical field-effect transistors (VFETs) with less than 2 ns switching time have been incorporated in 10 MHz, PWM Boost and Buck 5 W, power converters that demonstrated good efficiency (> 85%) and very high power densities [86].

Gallium Arsenide (GaAs) MESFET power switches like MESFET and Schottky-barrier rectifiers applied in Buck [87], Boost [88], Cuk [89], Flyback [90] DC-DC converters have allowed switching frequencies of up to 100 MHz, or even up to 250 MHz [47].

A 40 MHz to 100 MHz step down 10 V to 5 V (8 V) converter using GaAs power MESFETs was demonstrated with an output power of 2.6 W and power efficiency of 77% at 40 MHz [87]. A prototype based on hybrid circuit technology was implemented on an alumina substrate with a 1 A 15 V X-band power MESFET, an X-band MESFET based gate driver, a 110 nH HF ferrite based very low loss inductor and various DC decoupling chip capacitors.

A GaAs-based 5 V/10 V 2 W Boost converter operated at 100 MHz was presented in [88], with 69% efficiency. The hybrid technology prototype Boost converter was assembled on a 10 mil Alumina substrate. A 0.7 μm technology 2A-12 V commercial MESFET, a 150×150 μm 27 V Schottky rectifier and a gate driver were carefully mounted with very short interconnection ribbons in order to avoid parasitic oscillations.

In the work reported in [91] a 4.5 GHz DC-DC power converter was investigated, the highest frequency DC-DC converter reported to date. The converter consisted of a switching-mode Class-E power amplifier and diode rectifiers. The overall efficiency of 64% was achieved for an 87 Ω load with an output of 2.15 V.

In [23] a 10 GHz drain modulated class-E PA in which a buck converter supply was used to modulate the amplitude of the carrier was reported. The carrier frequency was 10 GHz, but the class-S switching frequency was only 200 kHz. The maximum efficiency of the PA was 60%.

In [22], a PA efficiency enhancement with 10 MHz DC-DC converter was proposed for

a CDMA transmitter. This solution was designed to step voltage up from a 3V supply to provide a dynamic supply at the drain of a gallium arsenide (GaAs) MESFET PA transistor. The supply voltage was varied synchronously with the carrier envelope to track the supply voltage required by the linear PA. The average efficiency was reported to increase from 3.89% to 6.38%.

A 0.50 μm GaAs MMIC power converter switching at 150 MHz was reported in [92]. It delivered around 3.3 W of power. The highest switching frequency reported MMIC DC-DC converter was described in [93]. The DC-DC converter switching frequency was 1 GHz, with integrated inductors and an efficiency of 64% with an output power of 0.680 W.

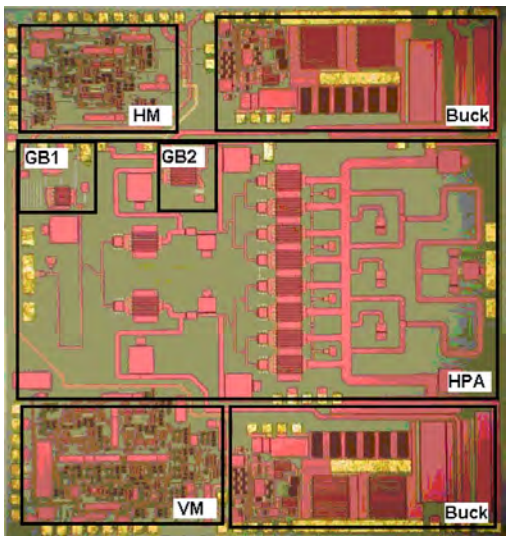

Figure 2.44: 0.5 μm GaAs HPA with DC-DC Power Converters

Figure 2.44 shows an RF HPA with an integrated DC-DC converter reported in [94], [95]. It was fabricated in a 0.50 μm GaAs process and the total output power of the DC-DC converter was 30 W with an efficiency of 77%. The combined efficiency of the HPA and DC-DC converter was 23%, with an RF output power of 10 W. The HPA featured an on-chip voltage mode and hysteretic control, either of which could be selected by

on-chip wire bonding.

2.11.2 GaN HEMT Power Switches

GaN Class-E^2, type converter switching at 780 MHz was reported in [96]. The efficiency was 72% with an output power of 10.3 W. The switching frequency was further extended to 1 GHz in [97] with FM modulation schemes and an average efficiency of 70%. These are highest reported switching frequencies for a modulator using commercially available GaN HEMTs as power switches.

The state of the art, GaN RF HEMT power switches incorporated in inverter type hybrid circuits available in the literature are given in Table 5.4. In [11] a 65 W boost converter topology for ET applications switching at 50 MHz is given and was later expanded in [1] for space based RFPA applications. The maximum output power delivered was 53 W switching at 50 MHz. A Hybrid Switching Amplifier (HSA) with a buck converter switching at 1 MHz with maximum efficiency of 85% is described in [98], and the same group at Ferdinand Braun Institute followed it up with [25], where a 50 W, 90 % efficient DC-DC converter is demonstrated; however the switching frequency is only 1 MHz.

In [31], a 3 W synchronous buck converter power stage with 96% efficiency was demonstrated for ET applications. In [99] an enhancement-mode GaN HEMT power switch in a boost converter topology that delivered up to 40 W of output power at 89% efficiency was demonstrated. Variations of driver topologies and their influence on the power cells were investigated in [100]. The maximum output power reported was 80.8 W at an efficiency of 91.6% and a switching frequency of 8 MHz. A boost

Table 2.3: State of the Art: GaN Hybrid Modulators

Ref	Topology	Technology	P_{OUT} (W)	Max η (%)	Freq (MHz)	V_{DD} (V)
[11]	Boost	0.40 μm Cree GaN on SiC	65	84-90	50	37-56
[1]	Boost	0.40 μm Cree GaN on SiC	53	91.9%	50	50
[98]	Buck	0.5 μm FBI GaN on SiC	-	85	1	15
[25]	Buck	0.5 μm FBI GaN on SiC	50	90	1	28
[31]	Sync. Buck	0.15 μm TQS GaN on SiC	3	96	40	20
[99]	Buck	EPC eGaN GaN on Si	40	89	10	42
[100]	Buck	EPC GaN GaN on Si	80.8	91.6	8	-
[101]	Boost	0.4 μm Nitronex GaN on Si	8	86-96	10	14-28
[102]	Boost	0.4 μm Nitronex GaN on Si	8	75	20	12-30

converter with an efficiency of 88.8% was mated with a RFPA to deliver 8 W at a PAE of 39.9% efficiency for phased array applications [101]. A multilevel GaN modulator with 75% efficiency and switching at 20 MHz for an envelope signal of 4 MHz is given in [102]. The major draw back in all the above mentioned work is the lack of a GaN driver circuit, as all these modulators are driven by external commercially available drivers.

A voltage mode Class-D MMIC amplifier, which is analogous to a synchronous buck converter is given in [103]. The PA was optimised for the 800 MHz LTE frequency band, and for a 50% duty-cycle pulse-width modulated input signal a maximum PAE of 59% and an output power of 5.2 W were obtained. The drain efficiency of the final stage stays almost constant over the whole output power range with values of around 80%. A dual band Class-D PA was demonstrated in [104]. For a pulse-width modulated input signal the PA achieves a maximum output power of 5.4 W at 0.85 GHz and 4.3 W at 1.8 GHz. The peak drain efficiency is 84% and 54% for 0.85 GHz and 1.8 GHz, respectively. At 6 dB power back-off, drain efficiencies of 40% (0.85 GHz) and 25% (1.8 GHz) were obtained. An Class-D PA in an H-bridge configuration at 900 MHz was reported in [105]. Using a square-wave input signal, the PA achieves a peak output power of 39 dBm and maximum drain efficiency of 48%.

In [106], an ET supply modulator using Mitsubishi Electric's 0.7 μm GaN process delivers 1.9 W of output power at an efficiency of 64%; the low efficiency is due to the high power loss in the resistive pull-up topology of the high side driver, especially at low duty cycles. An improved, bootstrap design [107] using a 0.25 μm gate length process of the same foundry had an efficiency of 73%. The switching frequency in both designs was 200 MHz, while the drain bias voltage increased from 20 V to 30 V in the bootstrap circuit. The efficiency of the bootstrap topology was improved to 87.5%

Table 2.4: State of the Art: GaN MMIC Modulators

Ref	Topology	Process	P_{OUT}(W)	η(%)	Freq (MHz)	V_{DD}(V)
[107]	Pull-up	0.70 μm ME	1.9	64	200	20
[106]	Bootstrap	0.25 μm ME	3.3	73	200	30
[109]	Sw. Node	0.15 μm TQS	7	83.5	100	20
[108]	Bootstrap	0.15 μm TQS	5	87.5	100	20
[108]	Pull-up	0.15 μm TQS	5	80	100	20

with an output power of 5 W in [108], using an external capacitor, at the expense of the low side driver, which could not be implemented due to space constraints in the MMIC layout. A resistive-pull up topology in the same technology delivered 5 W at 80% efficiency, and a modified high side driver based pull-up resistor topology described in [108] delivered around 7 W of output power with 88.5% efficiency. The same circuit was implemented as an ET supply modulator and tracked a 20 MHz LTE signal with an efficiency of 83.7% [109].

2.12 Next

In Chapter 3, the role of trapping, which degrades the power switch efficiency of power switches is investigated using a pulsed I-V measurement system at high quiescent drain bias conditions.

3

Power Switch Characterization

3.1 Introduction

Trapping phenomena represent a major performance limitation factor for AlGaN/GaN HEMTs. It has been observed that the output power measured at microwave frequencies was much lower than what was calculated from the DC parameters. This reduction in output power was first noted in GaAs [110], [111] and was attributed to the presence of traps and its manifestations have been described using various terms like dispersion, current compression, current collapse, gate/drain lag, power slump etc [63], [112], [113], [114], [115]. In power switching applications, this reduction in output power due to the increase in the R_{ON} of the HEMT severely degrades the switch

efficiency [57], [58], [64], [116].

Pulsed I-V measurement (Figure 3.1) techniques have been used to visualize R_{ON} modulation by plotting the dynamic I-V characteristic, as the device would be used in power switching applications [77], [78], [79], [80]. Pulsed I-V measurement consists in applying a pulsed signal that drives the devices from a defined quiescent bias point (usually off-state at high drain bias) to points of the I-V plane in order to chart the dynamic I-V characteristic.

This chapter details pulsed I-V characterization of commercial foundry RF GaN HEMTs to understand how traps affect the performance of the device when used as a power switch. At high quiescent drain bias voltages, the test devices showed a significant increase in R_{ON} and therefore dramatically reduced the output power.

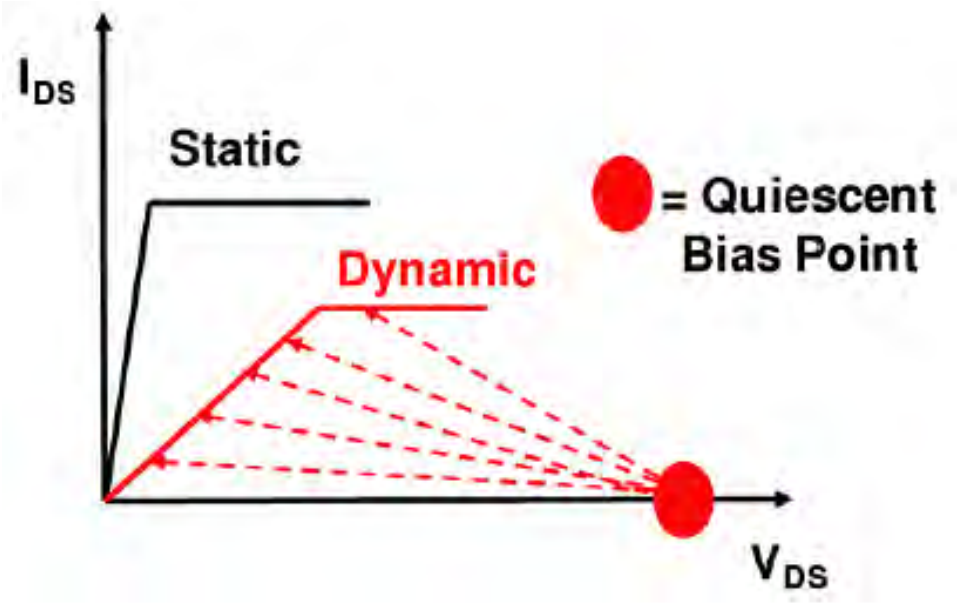

Figure 3.1: Pulsed I-V Measurement: Effect of Trapping

Pulsed-bias measurement of a transistor gives characteristics at a specified quiescent condition. These are representative of the high frequency operation of the device.

Table 3.1: Characteristics of Devices Investigated

Technology	Periphery(mm)	Bias(V)	F_T(GHz)	Density(W/mm)	V_{BD}(V)
Triquint 0.25 μm		28 V	32	6 (@10 GHz)	90
D1 4x200μm	0.8				
D2 8x100μm	0.8				
D3 2x200μm	0.4				
Triquint 0.15 μm		20 V	80	3 (@30 GHz)	60
D4 10x100μm	1				
D5 10x120μm	1.2				
D6 10x90μm	0.9				
Cree 0.25 μm		28 V	32	6 (@10 GHz)	120
D7-6x200μm	1.2				
D9-4x6x200μm	4.8				
Cree 0.40 μm		28 V	18	4.5(@8 GHz)	120
D8 -10x360μm	3.6				

Characteristics well outside the safe operating area of the device, including breakdown, can also be measured [79]. A pulse measurement is performed by maintaining, for most of the time, a constant quiescent bias on the device under test. Periodically, a short pulse is applied to the devices terminals, and during the brief interval of the pulse, the terminal voltage and current are measured [80]. The pulses are kept short enough that the devices quiescent state is not disturbed, the device is not stressed, and rate-dependent anomalies are avoided. The period between pulses is kept long enough to permit full recovery to quiescent conditions between pulses. Table 3.1 gives the devices that were investigated in this study.

3.1.1 Triquint 0.25 μm and 0.15 μm

Pulsed I-V characterization was conducted to evaluate the R_{ON} modulation and current collapse of two sets of devices (0.25 μm and 0.15 μm) from Triquint Semiconductors at different quiescent bias conditions. The devices investigated, D1-40/40 4

× 200, D2- 50/50 8 × 100 and D3- 40/40 2 × 200 GaN HEMTs were fabricated in 0.25 μm baseline RF process technology. These devices were not optimized for power switching. The 0.15 μm process technology devices were optimized for high frequency switching applications, and hence had reduced gate length, drain-source spacing, enhanced field plate engineering and passivation layers.

On-wafer pulsed I-V characterization was done using an Accent Technologies DiVa 265 system . This system allows for simultaneous pulsing of the gate and drain with pulse widths of 200 ns to 1 ms. The averaging was 32 samples with a pulse length of 500 ns. The pulse separation was 1 ms and the duty cycle was 0.049975. The V_{DS} step size was 0.0975 V.

The diced wafer chip with the test devices was placed on an on-wafer measurement system (Figure 3.2), and GSG probes with a pitch of 150 μm were used to make electrical contact.

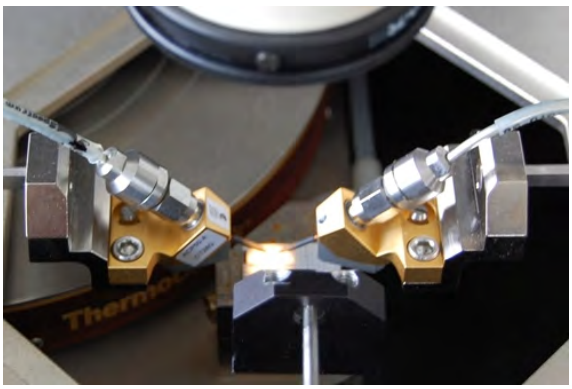

Figure 3.2: On-Wafer Measurement System

Initially, each device was set to an OFF-state by applying a gate voltage below the pinch-off (-5 V). V_{DS} was then set to various preset V_{DSQ} values (0, 10, 20, 30, and 35 V) for the 0.25 μm devices and V_{DSQ} values of (0, 10, 15, 20) for the 0.15 μm HEMTs. After holding the devices at the preset quiescent drain values they were switched back

to the ON-state by applying V_{GS} = -1 V and V_{DS} swept up to V_{KNEE}.
the R_{ON} modulation is calculated by measuring the R_{ON} (static) value for V_{DSQ} equal to zero voltage and the R_{ON} (dynamic) value for V_{DSQ} equal to the preset drain voltage for an output current near $V_{DS} \approx 0$V (linear drain current characteristics close to the origin). Here the output current was measured at V_{DS} = 0.5 V. The ratio of R_{ON} (static) to R_{ON} (dynamic) yields the R_{ON}modulation. The current collapse in both the cases was measured at V_{DS} = 2 V.

3.1.2 Switch Terminal Voltage v Output Current

The pulsed I-V characteristics of the tested GaN HEMTs are given in Figures 3.3-3.8. The pulsed I-V characteristics clearly show current collapse and R_{ON} modulation with increasing quiescent drain bias voltage. Figure 3.9 describes the on-resistance modulation observed in the tested HEMTs using the pulsed I-V system.

Triquint 0.25μm HEMT: The on-resistance under quiescent drain voltages of 10, 20 and 30 V (V_{DSQ}) increases gradually up to V_{DSQ} = 30 V, from the static R_{ON}, measured at V_{DSQ} = 0 V. The static R_{ON} of the tested devices D1, D2 and D3 were 2.95 Ω, 2.98 Ω and 5.81 Ω respectively.

The dynamic R_{ON} of the same devices under V_{DSQ} = 30 V increased to 3.41 Ω, 3.85 Ω and 7.2 Ω, indicating an increase of 15.9%, 29.2% and 24.2% from the static R_{ON} values.

When V_{DSQ} was increased to 35 V, dynamic-R_{ON} of the same devices sharply increased to 5.71 Ω, 4.81 Ω and 9.6 Ω, indicating a dramatic increase of 93.7%, 61.5% and 65.8%

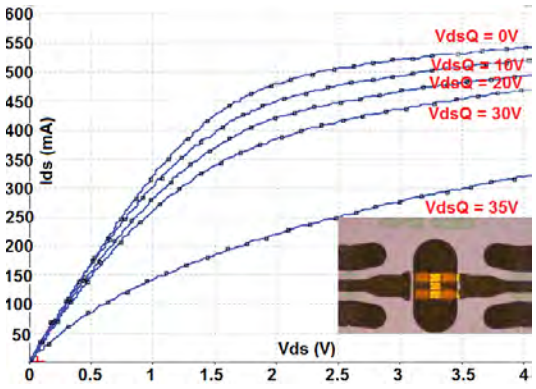

Figure 3.3: 0.25 μm GaN: D1 4×200

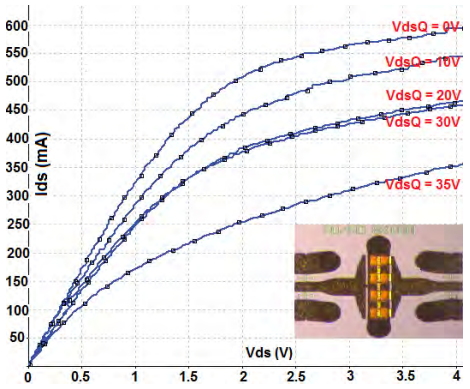

Figure 3.4: 0.25 μm GaN: D2 8x100

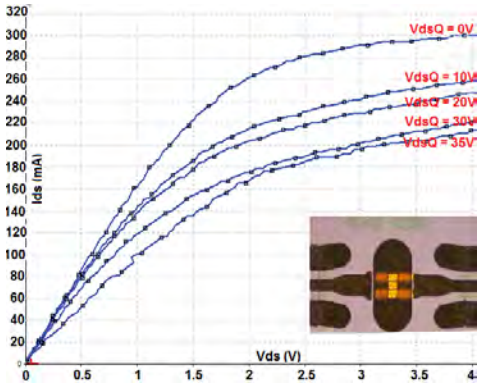

Figure 3.5: 0.25 μm GaN: D3 2×200

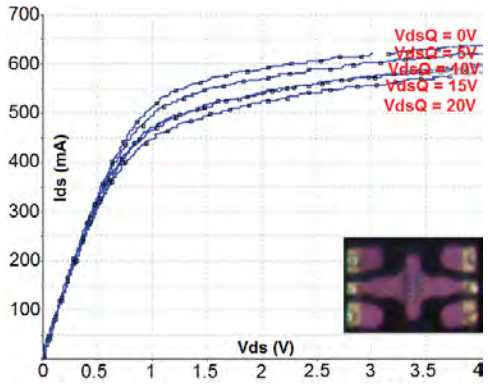

Figure 3.6: 0.15 μm GaN: D4 10×100

from the static R_{ON} values.

Figure 3.10 gives the normalized current collapse seen in the devices tested for increasing values of V_{DSQ}. The current collapse observed in devices D1, D2 and D3 was 55.6%, 52% and 43% normalized to the drain current measured at a drain bias (stress) voltage (V_{DSQ}) of 0 V. The current collapse/unit area was calculated, and at the maximum quiescent drain bias voltage of 35 V the collapse seen in D1 was 309.3 mA/mm, in D2, it was 293.8 mA/mm, while D3 exhibited a current collapse of 230 mA/mm. Devices D1 and D2 had the same gate periphery of 0.8 mm while for D3 it was 0.4 mm.

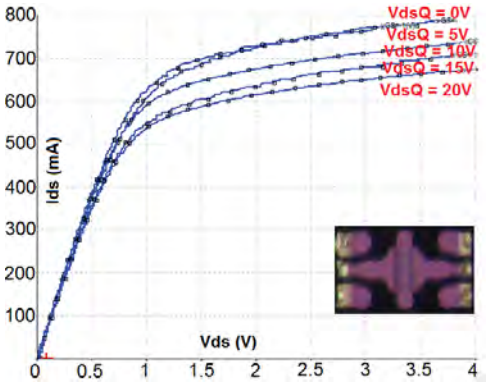

Figure 3.7: 0.15 μm GaN: D5 12×100

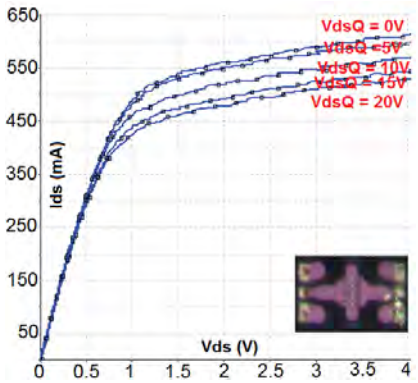

Figure 3.8: 0.15 μm GaN: D6 10×90

Triquint 0.15 μm HEMT:

As previously mentioned the devices investigated, D4 , D5 and D6 HEMTs, were optimized for switching applications. The on-resistance (Figure 3.11) under quiescent drain voltages of 10, 15 and 20 V (V_{DSQ}) increases gradually up to V_{DSQ} = 20 V, from the static-R_{ON}, measured at V_{DSQ} = 0V. The static R_{ON} of the tested devices D4, D5 and D6 were 1.58 Ω, 1.21 Ω and 1.60 Ω respectively.

The dynamic R_{ON} of the same devices under V_{DSQ} = 20 V increased to 1.61 Ω, 1.35 Ω and 1.72 Ω, indicating an increase of 6.06%, 5.12% and 6.75% from the static R_{ON} values. This increase in the dynamic-R_{ON} is very small compared to the corresponding increase in 0.25 μm devices, which showed an increase of 17.44%, 10.15% and 8.47% from the static R_{ON} values at V_{DSQ} = 20 V.

Figure 3.12 gives the normalized current collapse seen in the devices tested for increasing values of V_{DSQ}. The current collapse observed in devices D4, D5 and D6 was 11.01%, 14.28% and 15.75% normalized to the drain current measured at a drain bias (stress) voltage (V_{DSQ}) of 0 V. The current collapse/unit area was calculated and at the maximum quiescent drain bias voltage of 20 V, the collapse seen in D4 was 65

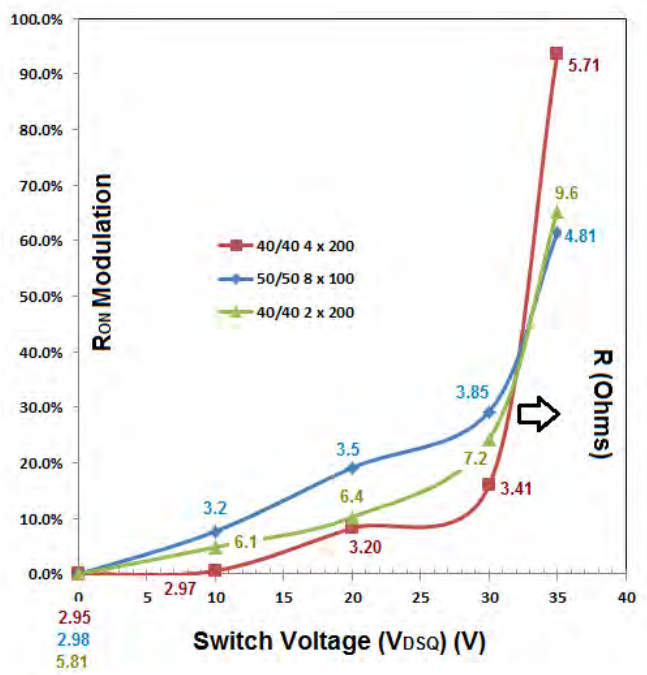

Figure 3.9: Triquint GaN 0.25μm R_{ON} Modulation

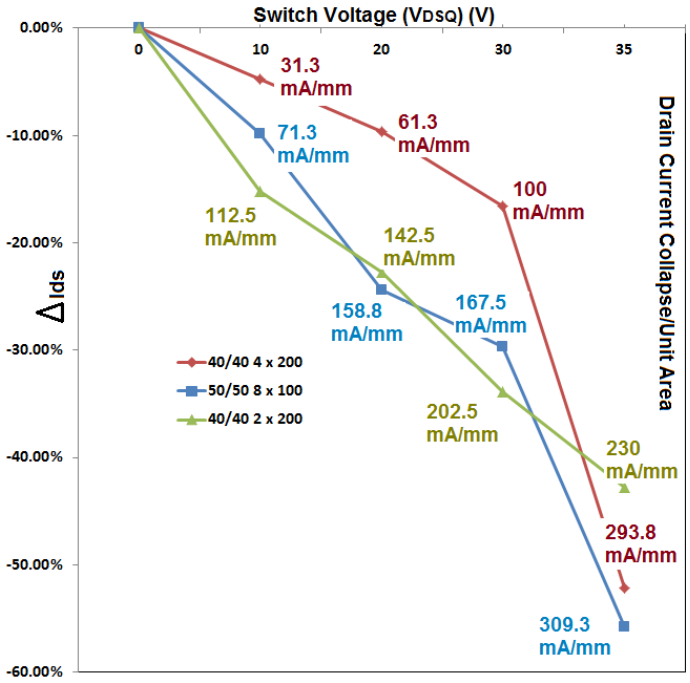

Figure 3.10: Triquint GaN 0.25 μm Current Collapse v Switch Voltage

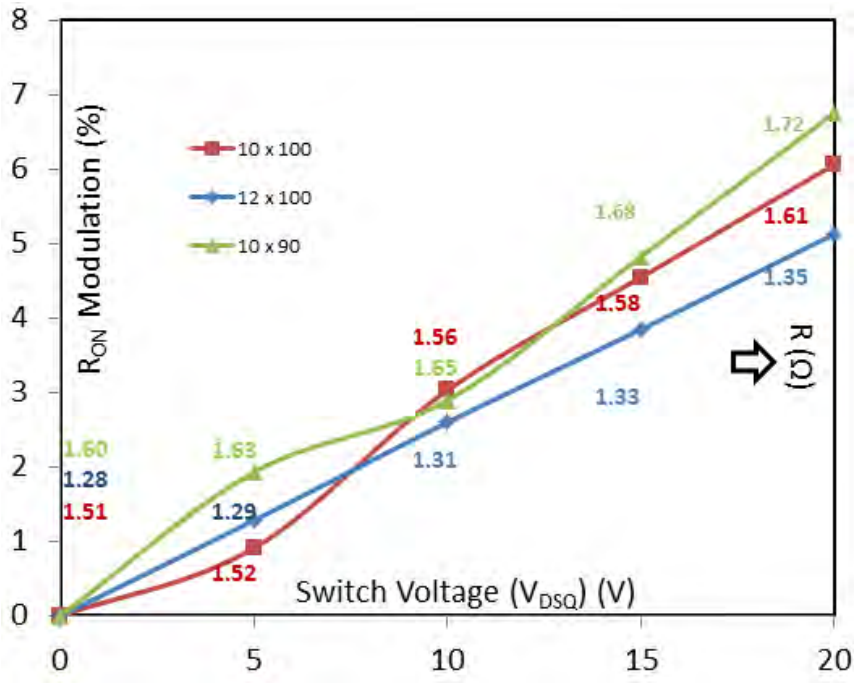

Figure 3.11: Triquint GaN 0.15 μm R_{ON} Modulation

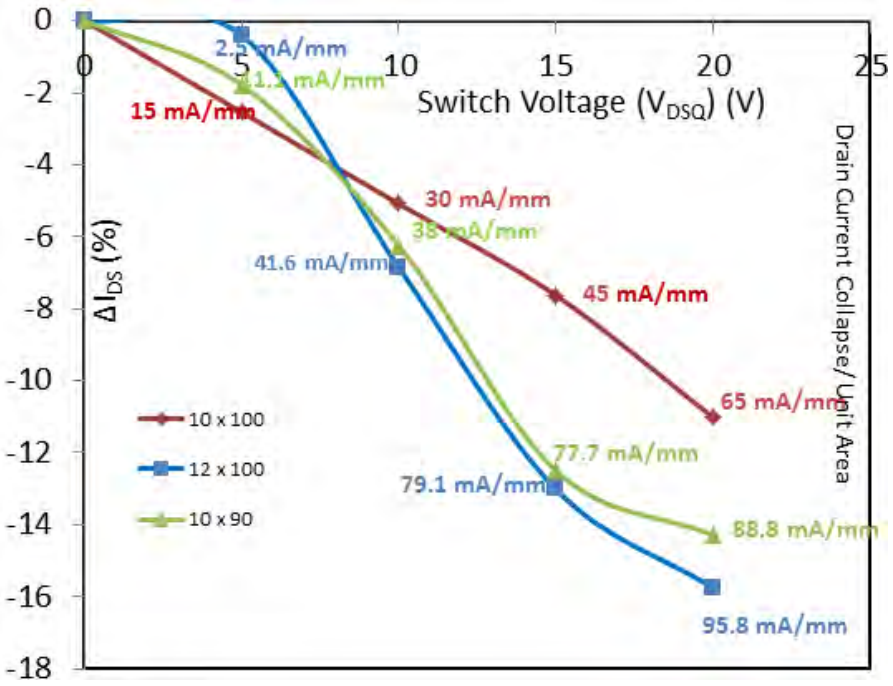

Figure 3.12: Triquint GaN 0.15 μm Current Collapse v Switch Voltage

mA/mm, in D5 it was 95.8 mA/mm while D6 exhibited a current collapse of 88.8 mA/mm. Devices D4 had a gate periphery of 1mm , D5 had a gate periphery of 1.2 mm, while for D3 it was 0.9 mm.

3.1.3 Cree 0.25 μm and 0.40 μm

For this section 0.25 μm and 0.40 μm GaN HEMTs manufactured by CREE devices were subjected to pulsed I-V investigation. The devices investigated, D7- CGHV1006D and D9- CGHV1025D, were fabricated using the Cree 0.25 μm process, while D8- CGH10015D was from Cree 0.40 μm process. These GaN HEMTs were designed for use in RF Power amplifiers and were not optimized for power switching.

The pulsed I-V characterization was done using an Auriga Microwave, AU 4850 system. This characterization platform is capable of measuring DC I-V and pulsed I-V curves, expandable to pulsed S-parameters and pulsed load pull. With pulse widths as narrow as 70 ns and duty cycles as low as 0.001%, characterization of the Cree devices was carried out with the duty cycle set at 0.1% with a pulse width of 2 μs, and the read out was 1.5 μs after the off-state pulse.

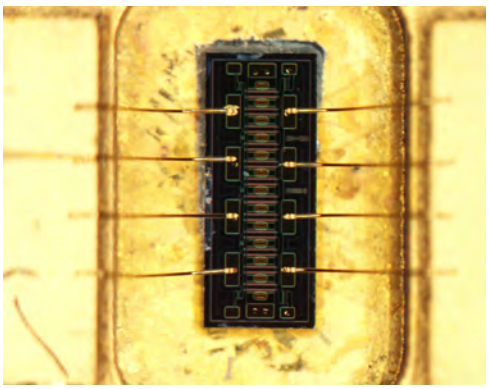

Figure 3.13: Cree 25W Packaged

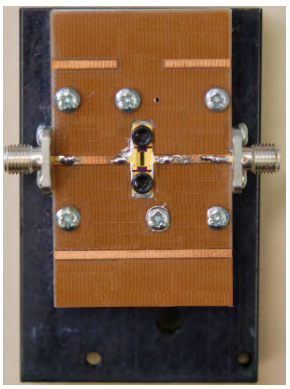

Figure 3.14: Pulsed IV Test Jig

The bare-die devices were soldered onto an RF MMIC package (Figure 3.13) and 0.25 μm gold bond wires were used to complete the electrical connection. The packaged devices were slotted into a test jig shown in Figure 3.14 with SMA connectors for connection to the pulser heads of the Auriga system.

As with previous characterization of Triquint devices using the Diva 265 system, each device was set to an OFF state by applying a gate voltage below the pinch-off (-5 V). V_{DS} was then set to various preset V_{DSQ} values (0, 10, 20, 30, 40, 50, 60) and then the device was switched back to the ON-state by applying V_{GS} = -1 V and V_{DS} swept up to V_{DS} = 10 V.

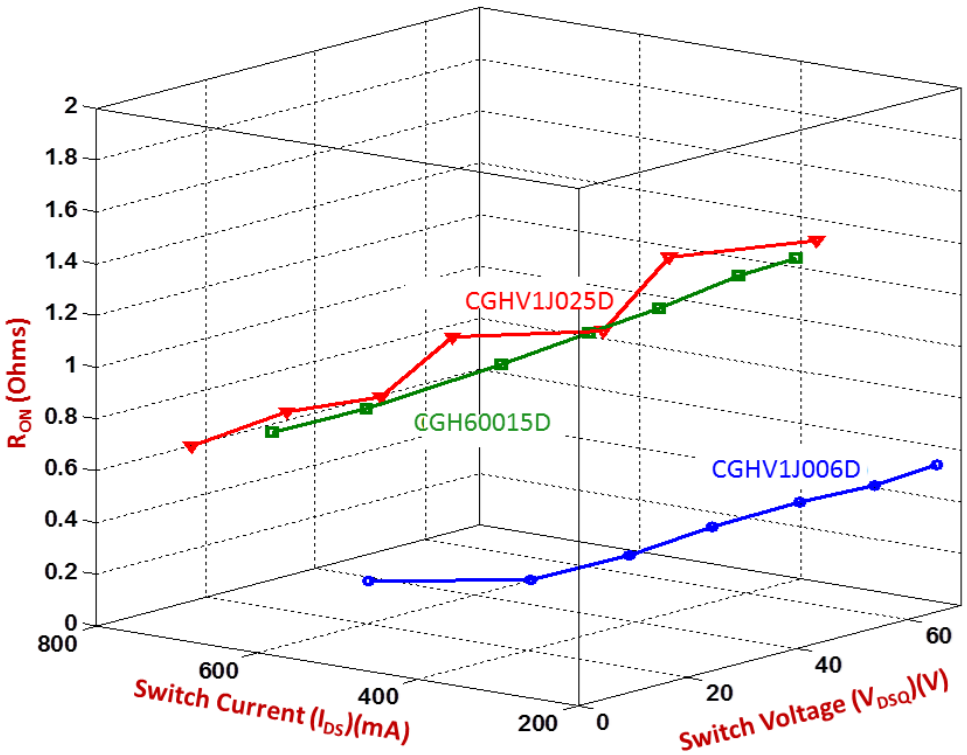

Figure 3.15: Cree GaN R_{ON} Modulation

As in the previous case, the output current was measured at V_{DS} = 0.5 V. The ratio of R_{ON} (static) to R_{ON} (dynamic) yields the the R_{ON} modulation. The current collapse

was measured at V_{DS} = 4 V. The Auriga pulsed I-V system enables real time analysis of transient gate/drain current and voltages. The pulsed I-V system emulates the power switch terminal potential when pulsed under high quiescent drain bias voltages. This feature enables visualization of the effect of R_{ON} modulation and current collapse in a GaN HEMT when used as a power switch, as shown in Figure 3.15.

The ON resistance (Figure 3.16) under quiescent drain voltages (V_{DSQ}) of 0, 10, 20, 30, 40, 50 and 60 V increases gradually up to V_{DSQ} = 60 V, from the static R_{ON}, measured at V_{DSQ} = 0V. The static R_{ON} of the tested devices D1, D2 and D3 were 2.5 Ω, 0.76 Ω, and 0.66 Ω respectively.

These GaN HEMTs are optimized for operation as an RF power amplifier with an operational bias around 30 V. When V_{DSQ} was increased to 30 V, the dynamic-R_{ON} of the devices increased to 4.10 Ω, 1.08 Ω, and 0.98 Ω, indicating an increase of 62.5%, 41.3% and 47.06% from the static R_{ON} values.

The dynamic R_{ON} of the same devices under V_{DSQ} = 60 V sharply increased to 5.40 Ω, 1.28 Ω, and 1.31 Ω , indicating an increase of 105.26%, 60.49% and 97.36% from the static R_{ON} values.

Figure 3.17 gives the normalized current collapse seen in the devices tested for increasing values of V_{DSQ}. The current collapse observed in devices D7, D8, and D9 were 56.6%, 44.74% and 53.33% normalized to the drain current measured at a drain bias (stress) voltage (V_{DSQ}) of 0 V.

The current collapse/unit area was calculated and at a maximum quiescent drain bias voltage of 60 V, the collapse seen in D7 was 250 mA/mm, in D8 it was 231.6 mA/mm, while D9 exhibited a current collapse of 250 mA/mm as shown in Figure 3.18 . D7

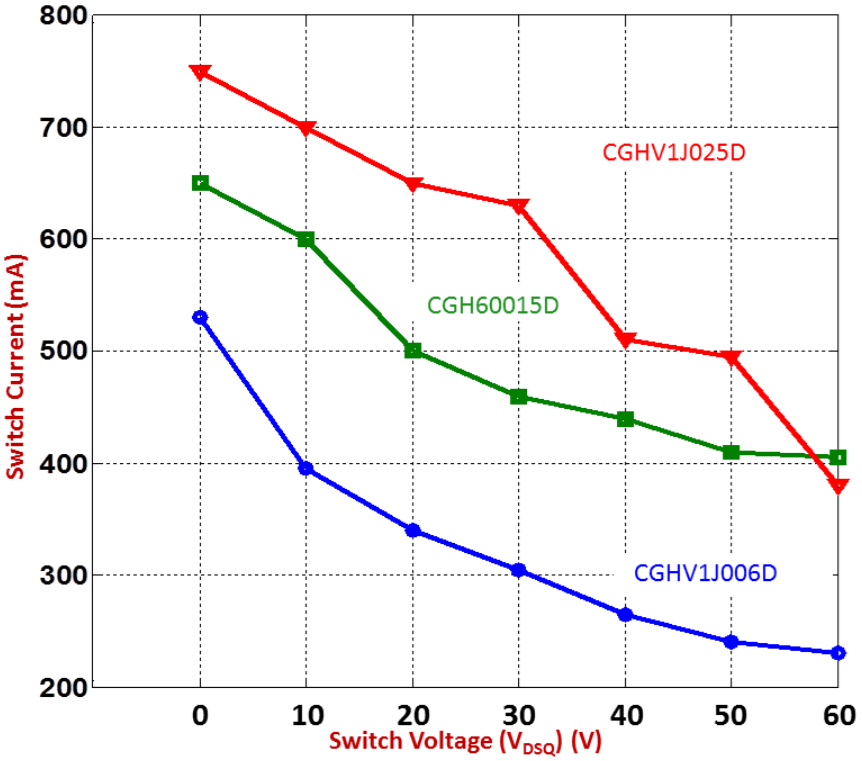

Figure 3.16: Cree GaN R_{ON} Modulation

had a gate periphery of 1.2 mm, D8 had 3.6 mm, D9 was 4.8 mm.

3.2 Output Power (P_{OUT}) and Switch Efficiency

The major advantage of GaN devices over devices in other technologies is the higher breakdown voltage (V_{BD}), low ON-resistance, smaller capacitances and increased current handling capabilities. The effect of traps in a GaN HEMT in a switching scenario is the reduction of power delivered to the load. The increase in R_{ON} and current collapse, at higher switch terminal voltages (V_{DSQ}), degrades the efficiency, leading to a loss in output power.

The amount of power available from a device in a switching topology is less than that

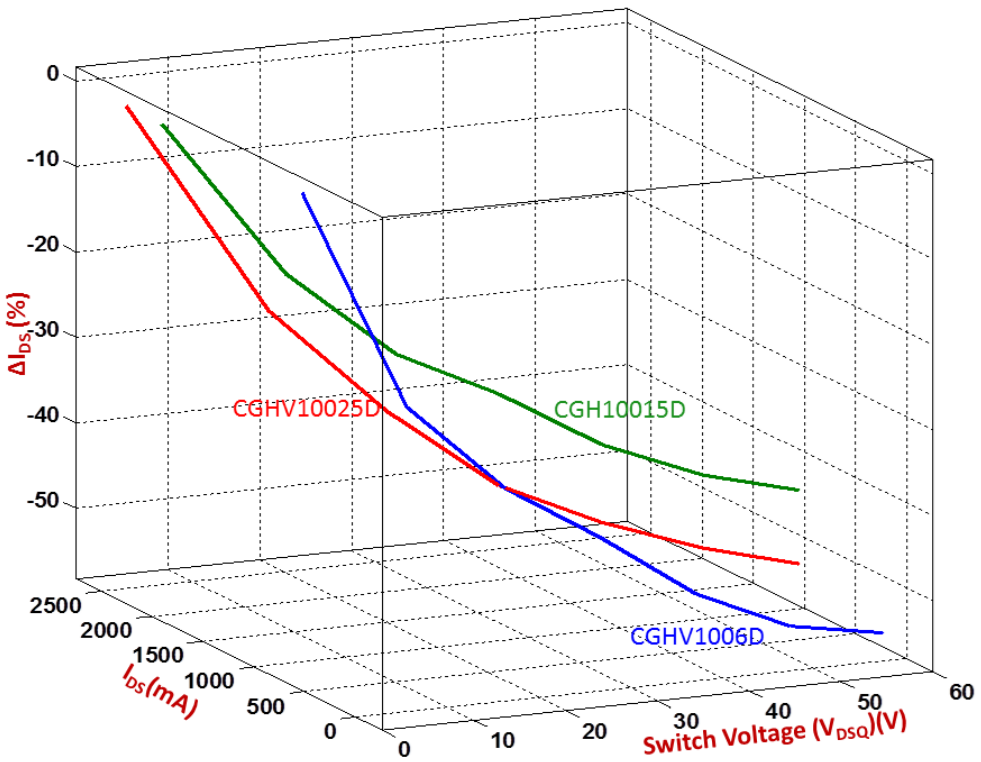

Figure 3.17: Cree GaN- ΔI_{DS} v Switch Voltage

predicted from DC I-V curve load line calculations or those from a normal pulsed I-V scenario (V_{DSQ}=0V). The actual power available from a device instead correlates with the power calculated from pulsed I-V curves measured under correct switch terminal voltages (quiescent bias conditions) to account for R_{ON} and current collapse dependence on quiescent drain voltage.

The increase of V_{KNEE} and the decrease of I_{KNEE} lead to a shift in the switch load line leading to reduced P_{OUTMAX}.

Triquint 0.25 μm GaN HEMT

Figure 3.19 shows the normalized theoretical P_{OUT} calculation for I_{MAX} measured (assuming all other losses to be zero) for an initial knee voltage of V_{KNEE} = 2 V and

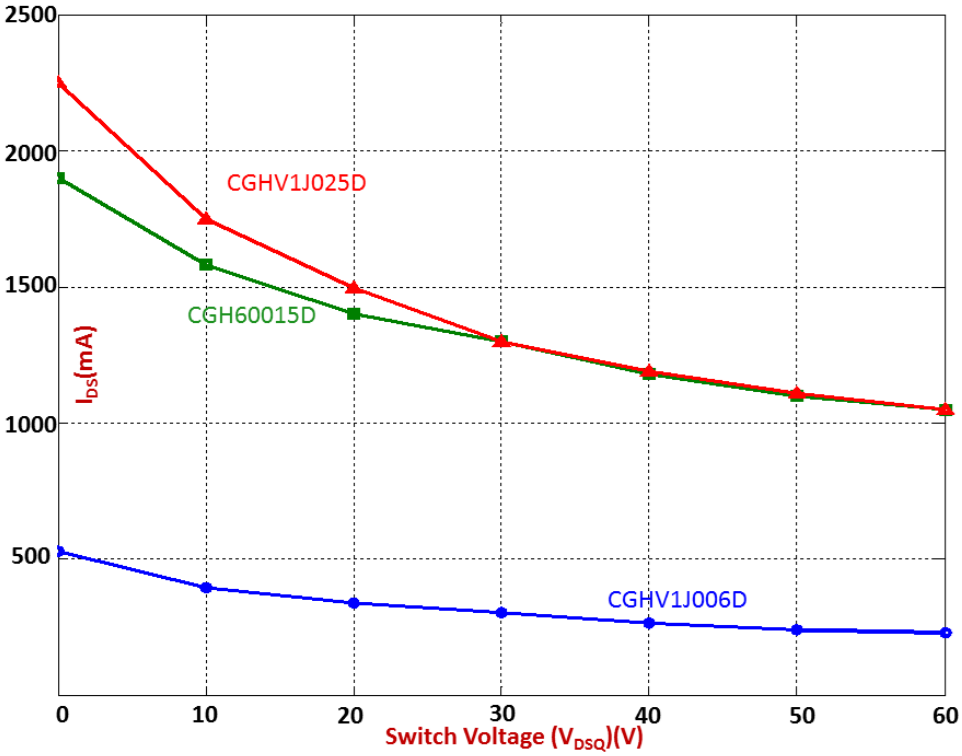

Figure 3.18: Cree GaN- Current Collapse v Switch Voltage

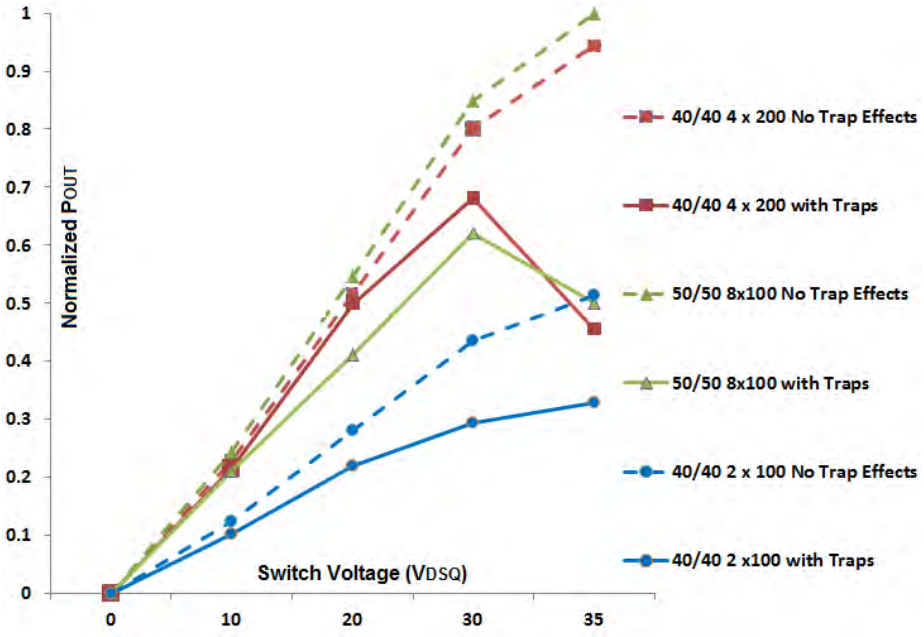

Figure 3.19: GaN Power Switch- P_{OUT} v Switch Voltage

switch terminal voltages of 0, 10, 20, 30 and 35 V. The P_{OUT} obtained from device, D2- 50/50 8 × 100 biased V_{DS} = 35 V, and an I_{DSMAX} measured from the (V_{DSQ}=0V) I-V Curve and V_{KNEE}= 2 V, was used as a baseline figure for normalization.

The presence of traps in GaN HEMTs can severely degrade the output power. At low quiescent drain bias voltages (V_{DSQ} ≤10V), the effect of traps on P_{OUT} is minimal as indicated by the proximity of the solid and dotted lines to each other in Figure 3.19.

However, with increasing V_{DSQ} voltages the solid and dotted P_{OUT} curves diverge significantly. At V_{DS} = 30 V, the reduction in P_{OUT} for D1 was 12%, 22.8% for D2, and for D3 it was 14.3%. At a switch terminal voltage (V_{DSQ}) of 35 V, the degradation in P_{OUT} for D1 increased to 48.8%, D2 to 49%, and for D3 to 18%, of its base line value calculated using V_{DSQ} = 0 V.

Triquint 0.15 μm GaN HEMT

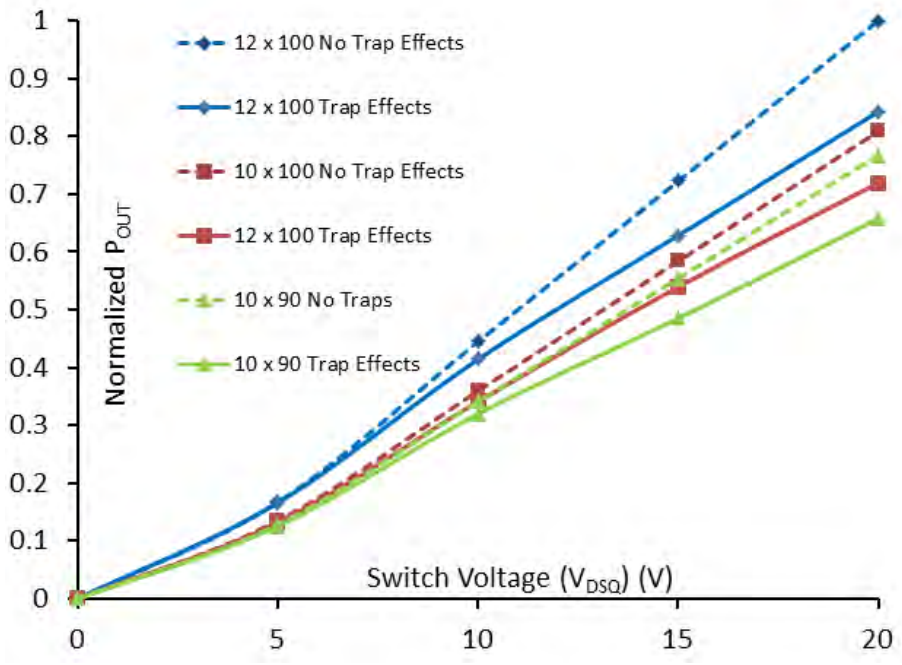

Figure 3.20: GaN Power Switch- P_{OUT} v Switch Voltage

Figure 3.20 shows the normalized theoretical P_{OUT} calculation for I_{MAX} measured (assuming all other losses to be zero) for an initial knee voltage of V_{KNEE} = 2 V and switch terminal voltages of 0, 5, 10, 15 and 20 V. The P_{OUT} obtained from device, D5-12 × 100 biased V_{DS} = 20 V, and an I_{DSMAX} measured from the (V_{DSQ}=0 V) I-V curve and V_{KNEE}= 2 V, was used as a baseline figure for normalization.

At quiescent drain bias voltages ($V_{DSQ} \leq$ 15V), trapping has minimal effect on the output power P_{OUT}, as indicated by the proximity of the solid and dotted lines to each other. At a switch terminal voltage (V_{DSQ}) of 20 V, the degradation in P_{OUT} for D4 increased to 8.8%, D5 to 15.8%, and for D6 to 11%, of its base line value calculated using V_{DSQ} = 0 V.

Cree 0.25 μm and 0.40 μm GaN HEMT

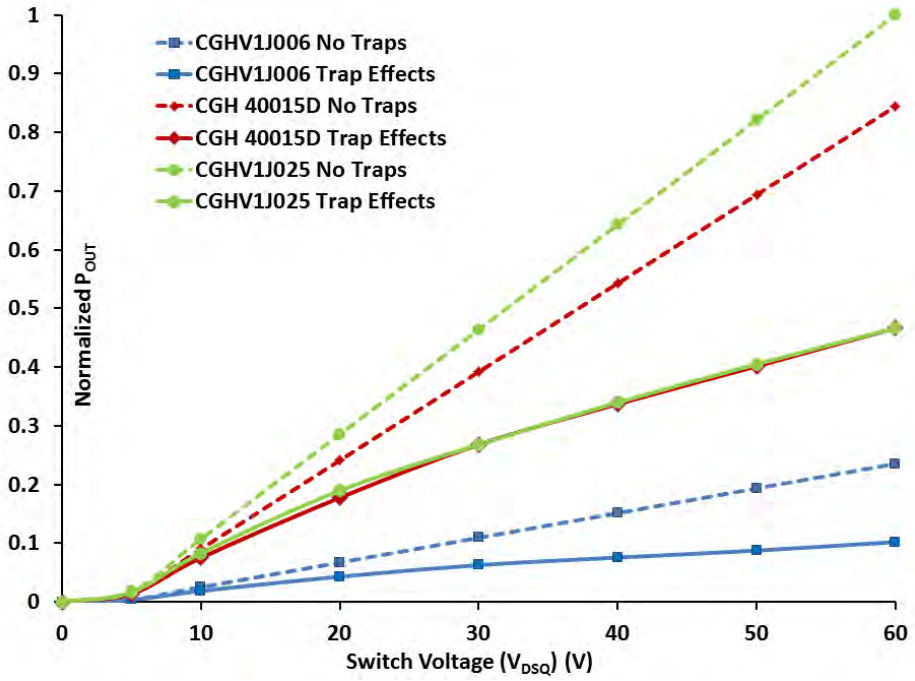

Figure 3.21: GaN Power Switch- P_{OUT} v Switch Voltage

Figure 3.21 shows the normalized theoretical P_{OUT} calculation for I_{MAX} measured

(assuming all other losses to be zero) for an initial knee voltage V_{KNEE} = 4 V and switch terminal voltages of 0, 10, 20, 30, 40, 50 and 60 V. The P_{OUT} obtained from device D9- 4 × 6 × 200 (CGHV 40025) biased V_{DS} = 60 V, and an I_{DSMAX} measured from the (V_{DSQ}=0 V) I-V curve and V_{KNEE}= 4 V, was used as a base line figure for normalization.

At quiescent drain bias voltages ($V_{DSQ} \leq$ 10 V), trapping has minimal effect on the output power P_{OUT} of all the HEMTs, as indicated by the proximity of the solid and dotted lines to each other. At a switch terminal voltage (V_{DSQ}) of 30 V, which is the normal operational bias voltage for these devices in RF power amplifiers, the degradation in P_{OUT} for D7 increased to 8.8%, D8 to 15.8%, and for D9 to 15.8%, of its base line value calculated using V_{DSQ} = 0 V.

On increasing V_{DSQ}, the clear reduction in P_{OUT} is very evident in all the devices. The reduction in P_{OUT} in device D7 was 10.23%, 37.84% in D8, and in D9 it was 53.33 %. The clear trend that can be inferred is that the reduction in P_{OUT} increases as the chip area is increased. This is due to the fact that there are significantly more traps present within these HEMTs causing a significant drop in the output drain current at high V_{DSQ}.

The FOM , given as the product of on resistance and input capacitance, gives a quantitative indication of the usefulness of the HEMT as a power switch; it needs to be qualified in terms of the output power and the efficiency with which it can be delivered by the power switch for a given switching frequency. Hence, depending on the specific requirements in terms of output power (P_{OUT}) and switch voltage, a corresponding switch efficiency can be obtained as shown in Figure 3.22.

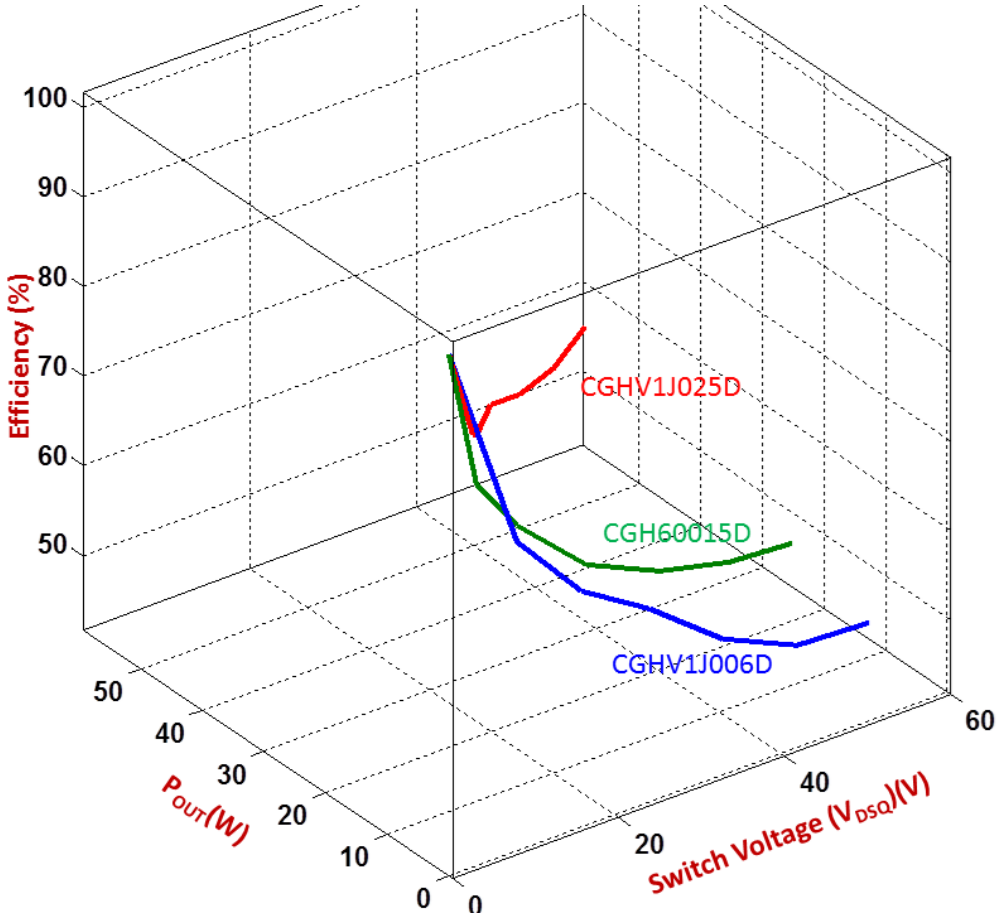

Figure 3.22: GaN Power Switch- P_{OUT} v Switch Efficiency

The maximum switch efficiency was obtained for a switch operating voltage, V_{DSQ} = 0 V which indicates the minimal action of traps in depleting the channel and increasing R_{ON}. At a switch operating voltage of 30 V, the output power delivered by D7, D8 and D9 was 7.93 W, 33.8 W and 18.2 W respectively and the corresponding efficiencies were 57.54%, 68.42% and 57.7%. At a maximum switch voltage of 60 V, the efficiency drops to 43.39%, 55.26% and 46.6% while delivering output powers of 12.8 W , 58.8 W and 25.2 W, respectively. It must be clearly stated that in these power and efficiency calculations, thermal effects at high drain currents and voltages were not considered.

Table 3.2: Device Capacitances

Process Technology		C_{IN}(pF)		C_{OUT}(pF)
Triquint 0.25 μm				
D1 4 × 200 μm		1.44		0.43
D2 8 × 100 μm		1.48		0.45
D3 2 × 200 μm		0.75		0.36
Triquint 0.15 μm				
D4 10 × 100 μm		1.6		0.62
D5 10 × 120 μm		1.8		0.79
D6 10 × 90 μm		1.4		0.57
Cree 0.25 μm				
D7-6 × 200μm		2.1		0.72
D9-4 × 6 × 200μm		5.6		2.88
Cree 0.40 μm				
D8 -10 × 360μm		4.94		2.16

3.3 Extracted Device Capacitance Measurements

The device capacitances play a significant role in the high speed switching operation of a HEMT as a power switch. Power switches tend to be large periphery devices due to the high current requirements. While the increased area leads to a decrease in the ON resistance, the capacitance of the device also scales with the size.

C_{IN} is the total input capacitance of a power switch that a gate driver sees to turn on the device. C_{IN} is directly proportional to the charge that needs to be supplied or extracted from the gate to switch the device "ON" and "OFF". C_{OUT} is the total output capacitance of a power switch seen at the output switching node.

The intrinsic device capacitances were extracted using S-parameter measurements and de-embedded for packaging effects. Table 3.2 gives the capacitance values extracted from all the devices investigated in this study. C_{IN} was measured with V_{GS} = -5 V, while C_{OUT} was extracted with V_{DS} = 20 V for Triquint 0.15 μm devices while V_{DS} =

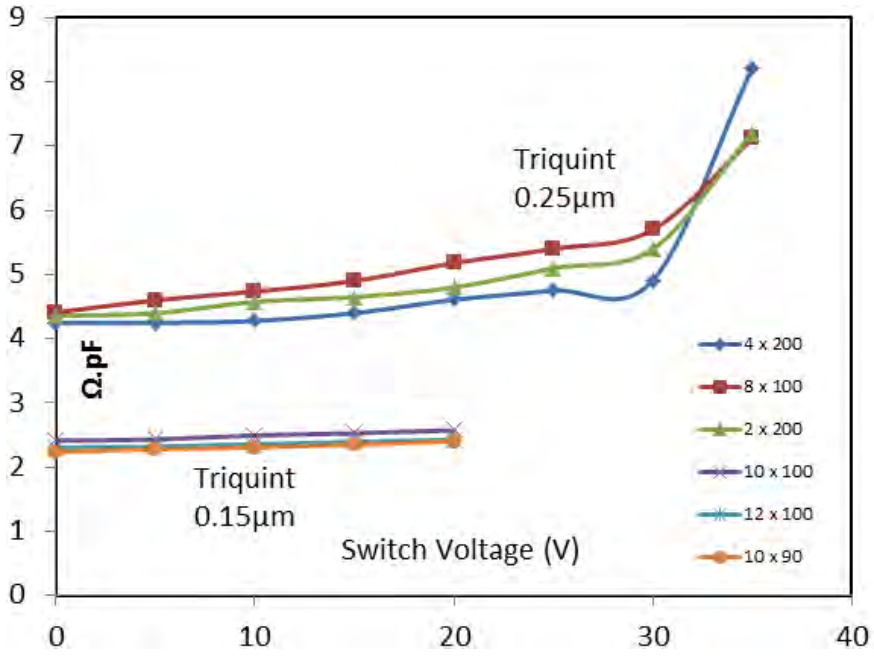

Figure 3.23: Figure of Merit for Triquint Devices

30 V was chosen for all other devices.

3.4 Figure of Merit - $\mathbf{R_{ON} \times C_{IN}}$

As mentioned in Chapter 2, $\mathbf{R_{ON} \times C_{IN}}$ can be used as a figure of merit (FOM). The lower the FOM value, the better is the device performance as a power switch. The figure of merit is normally calculated using an ON resistance measured using a curve tracer under DC conditions. The increase in R_{ON} under high voltage switching conditions due to trapping will severely degrade the FOM of a GaN HEMT Power Switch. Figure 3.23 illustrates the variation in ON resistance and its impact on the FOM of the Triquint devices.

When operated as switches at 35 V, the FOM of device D1 degrades to 93.7%, D2 to

61.5%, and D3 to 65.8%, of the value calculated under normal DC conditions (V_{DSQ} = 0 V).

The FOM of 0.15 μm devices D4, D5 and D6 at a V_{DSQ} = 20 V shows very minimal increases of 4.47%, 5.65% and 7.14% compared to their FOM measured at V_{DSQ} = 0 V.

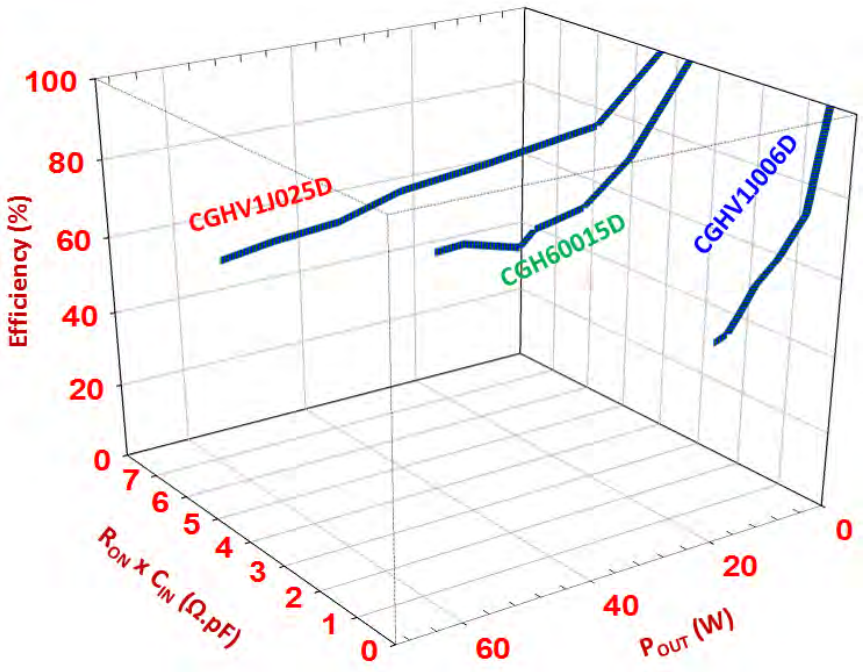

Figure 3.24: Cree Power Switch- FOM v Efficiency

The figure of merit of Cree devices with the corresponding output power and the associated switch efficiency is given in Figure 3.24. The maximum theoretical switch efficiency was obtained for , P_{OUT} = 0 W, which indicates the minimal action of traps in depleting the channel. The measured FOM was 0.54 (D7) Ω pF, 4.23 (D8) Ω pF and 3.3 (D9) Ω pF respectively. The maximum output power delivered by the devices were 12.8 W , 58.8 W and 25.2 W with corresponding efficiencies of 43.39%, 55.26% and 46.6%. On increasing the switch voltage, the figure of merit degraded to 1.12 (D7) Ω pF, 6.79 (D8) Ω pF and 6.5 (D9) Ω pF. The devices D7, D8, and D9 at V_{DSQ} = 60 V, show increases of 108%, 68.35%, and 98.60% compared to their FOM measured

at V_{DSQ} = 0 V. The switch efficiency is reduced for all three devices with increasing output power.

The degradation in the ON resistance due to traps severely impacts the drain current and hence the output power of the GaN HEMT. The trapping effect seen in these devices is dependent on the quiescent drain bias condition, V_{DSQ}, and the time interval the device is held at that voltage. The charging process in traps is a lot quicker (in the ns range) than the discharging process, which can take a lot longer (well into the milli-second to second range). The figure of merit of a power switch is very much influenced by the switch terminal potential (V_{DSQ}), the switch frequency and the duty cycle of the switch. Hence a dynamic FOM which relates the power switch efficiency to output power at a specific switch frequency needs to be introduced. A dynamic FOM is obtained by modifying the original FOM to account for the variation in ON resistance due to trapping. The dynamic FOM is given as,

$$\text{Dyn.FOM}_{P_{OUT},\eta_S,F_S} = \text{Dyn.R}_{ON} \times \text{C}_{IN}, \tag{3.1}$$

where, P_{OUT} is switch output power, η_S is the switch efficiency and F_S is the switching frequency.

When the required output power and switching frequency are known, the corresponding Dyn.$R_{ON} \times C_{IN}$ values can be computed and switch efficiency predicted. This gives better insight when comparing devices and to predict the optimum performance of the power switch in terms of efficiency and output power over a wide range of switching frequencies. It becomes clearly evident in the case of Cree devices given in Figure 3.24, the switch efficiency will be futher degraded at higher output powers if the switching

frequency is lowered since the trap time constants become comparable to the switching intervals.

3.5 Discussion

AlGaN/GaN HEMTs are ideal candidates as power switches due to their high break-down voltage, low R_{ON}, high current carrying capability and very low capacitances that enable them to switch at very high frequencies. The two main loss mechanisms within a power switch are conduction losses due to its R_{ON} and the switching losses that is related to its input and output capacitances. The conduction losses can be minimized by lowering the resistance within the HEMT. This can be achieved by increasing the HEMT size, at the expense of increased capacitances. Thus for a chosen switching frequency the optimal size is obtained by minimizing the conduction and switching losses within the HEMT. The product of $R_{ON} \times C_{IN}$ can be used as a first order switching figure of merit for RF HEMTs. Here C_{IN} is directly proportional to the gate charge (Q_G) that needs to be removed or supplied to turn the gate on and off in every switching cycle.

One of the major advantages of the GaN process, is the high drain voltage capability, enabling it to deliver large output power. The key parameter to this is the high off-state device break down voltage. The large off-state break down routinely measured on AlGaN/GAN HEMT is a consequence of an extended lateral depletion region that extends from the gate area towards the drain side with increasing gate-drain bias [117]. However, from the pulsed I-V measurements carried out, with the RF GAN HEMTs emulated as power switches at high quiescent drain bias, there is a severe degradation in

R_{ON}. Hence a dynamic figure of merit is required to accurately represent the switching performance of a power switch in terms of its output power, switching frequency and efficiency.

The implications of R_{ON} degradation on the overall system performance of a power supply modulator integrated PA module is tremendous. The main objective of integration is to improve the overall efficiency of the system given by

$$PAE_{overall} = PAE_{RFPA} X\ \eta_{DC-DC} \tag{3.2}$$

where η_{DC-DC} is directly proportional to the efficiency of the power switch within the drain supply modulator. The switching frequency of the drain supply modulator is determined by the complex RF modulation scheme used to modulate the RFPA. For example in the latest LTE envelope signal with a bandwidth of 20 MHz, the modulator switching frequency is 100 MHz and the average switch quiescent drain bias voltage is given by the PDF function of the RF modulation signal. Hence, at a chosen frequency, a design trade-off must be made to optimize the power switch by minimizing its losses due to R_{ON} degradation with high PAPR signals, which corresponds to a high quiescent drain bias voltage at the power switch terminals.

The high power Cree GaN HEMTs investigated in this chapter were characterized using using a 4850 pulsed I-V system, with the duty cycle set at 0.1%, with a pulse width of 2 μs and the read out was 1.5 μs after off-state pulse. This translates to a switching frequency of 500 Hz. In order to completely understand the behavior of the HEMT devices as power switches, they should be characterized at the chosen frequency of the supply modulator envelope modulation frequency. However, the currently available

pulsed I-V setup only allows for a maximum switching frequency in the kHz switching range; while it is possible to go further up in frequency, the slew rate of the pulser, is not high enough to obtain good pulse integrity due to slow rise time, thereby compromising the measured I-V.

Trapping effects in a GaN Power Switch are dependent on the quiescent drain bias stress voltage as well as the duration of that stress voltage. At a drain supply modulator switching voltage of 100 MHz with an envelope modulation signal of 20 MHz, it could be argued that the time interval is too small for the traps to react and influence the switch performance.

3.6 Conclusion

GaN HEMTs from commercial foundry vendors were characterized as power switches using Diva 265 and Auriga 4850 systems. Pulsed I-V measurements revealed trapping effects including R_{ON} modulation that severely degrade the switching figure of merit (FOM) of a power switch. Pulsed I-V curves show a significant increase in the ON resistance of the HEMT in the I_{DS}-V_{DS} curve causing "knee walk-out" while the g_m-V_{DS} curve clearly showed a shift in the pinch-off voltage. The effect of these traps were more predominant in larger devices and at higher quiescent drain bias voltages. Accurate power switch characterization and model development can significantly improve the efficiency of power converter circuits developed using these RF devices.

3.7 Next

Chapter 4 expands on the role of traps in ON resistance modulation and introduces a trap model for RF GaN HEMTs when used in power switching applications.

4

Power Switch Trap Model

4.1 Introduction

The integration of power amplifiers, driver amplifiers and LNAs within a space/satellite based Tx/Rx module onto a single die will lead to improvements in the cost, better performance and a size reduction [5], [12], [118]. A recent trend is to integrate the power converter with the RFPA on the same die [95].

Thus, within a power converter integrated MMIC module the same transistors are used for different functions and the transistors operate in different quadrants in the I-V plane. Designing each of these functional blocks implies having accurate transistor models for that very specific function. It is very challenging to obtain a valid model

that can predict the FET behaviour needed for all the functional blocks [119]. For example, current GaN HEMT models available within the process design kits (PDK) of various foundries all cater primarily for RF power amplifier applications [120].

Pulsed I-V characterization, presented in chapter 3, revealed the effect of traps in RF GaN HEMTs when used as power switches. Current HEMT models do not capture the quiescent drain bias dependent trap effects that cause significant reduction in drain current leading to drastic reduction in the output power. When designing integrated modulators in GaN MMIC technologies, accurate simulation models that can predict quiescent bias dependant trapping effects in power switches, especially R_{ON} modulation becomes crucial for large periphery devices, as MMIC design is very expensive and once fabricated cannot be modified externally.

In this chapter, a new power switch trap model based on the SRH theory is introduced and a PS FET model was to simulate the trap model. The SPICE simulation accurately predicted R_{ON} modulation and the corresponding current collapse seen in RF GaN HEMTs when used for power switching applications.

4.2 Power Switch Trap Model

A comprehensive dynamic model of a FET used for SPICE simulation, that accommodates surface and bulk traps, is shown in Figure 4.1.

The power switch model is composed of an inner HEMT model with its own set of unique parameters. The drain end surface and buck trap models are attached to the drain and gate terminals of the inner HEMT model.

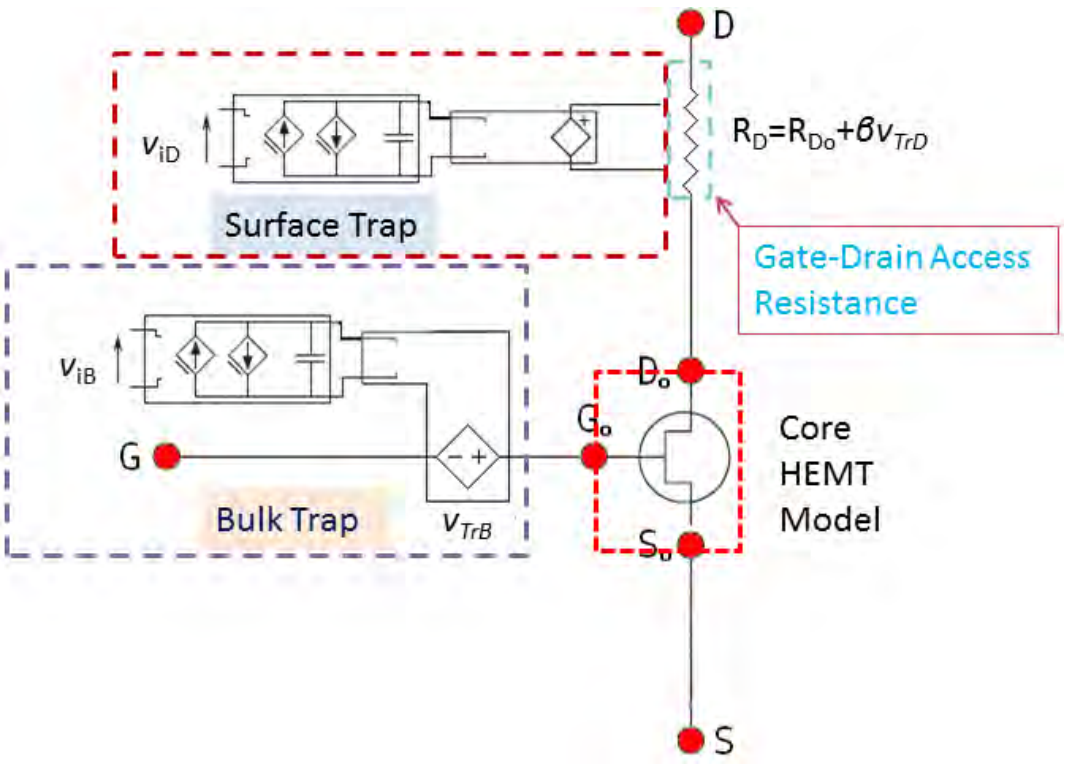

Figure 4.1: Power Switch Trap Model Circuit Implementation

Referring to Figure 4.1, the gate source voltage in the presence of traps is given by

$$V_{GoSo} = V_{GS} - (\gamma v_{TrB}) \tag{4.1}$$

while the on resistance modulation within the HEMT due to traps between gate and drain is given by

$$R_D = R_{Do} + \beta v_{TrD}, \tag{4.2}$$

Here R_{Do} is the isotrap drain and source resistances respectively, $\beta \geq 0$ is a proportionality constant, and v_{TrD} is the potential of the drain trap.

4.3 SPICE Simulation

This section of the chapter details important notes in regard to the SPICE simulation tool that has been used to simulate the transient responses associated with the trapping. The three main elements of the code used in SPICE simulation are:

- the Parker-Skellern FET model (PS FET model [121])
- the SRH trap model [70], and
- the sub-first-order thermal network to model self-heating [76].

The PS FET model has been chosen because of the ease of the accessibility and implementation of SRH trap model and the sub-first order thermal network as external elements to the SPICE PS FET model.

It should be noted that the PS FET model itself takes into account the anomalous rate-dependent behaviour due to trapping and self-heating. However, the trapping and self-heating models used in the PS FET model are too simple to predict the actual rate dependent behaviour. In terms of self-heating, the user has no control on the thermal network, and in terms of trapping the model does not account for the variation of the trap time constant with bias. Thus, it is important to disable the trapping and self-heating elements of the PS FET model when this model is implemented in the SPICE code.

For this power switch trap simulation, Vo= 5, v_{Tr}= -5.5, A_i=B_i= 0.1 and C_i= 1 were used. The internal PS FET model used β=0.1, p=0.98, p_0=1, γ=10^{-5} and V_P =-3.5 V.

Figure 4.2 shows the current collapse seen in the I-V curve. The nominal current observed at γ =0 was around 250 mA and it decreased to around 180 mA, a drop of 70 mA, when when γ increased from 0 to 0.2.

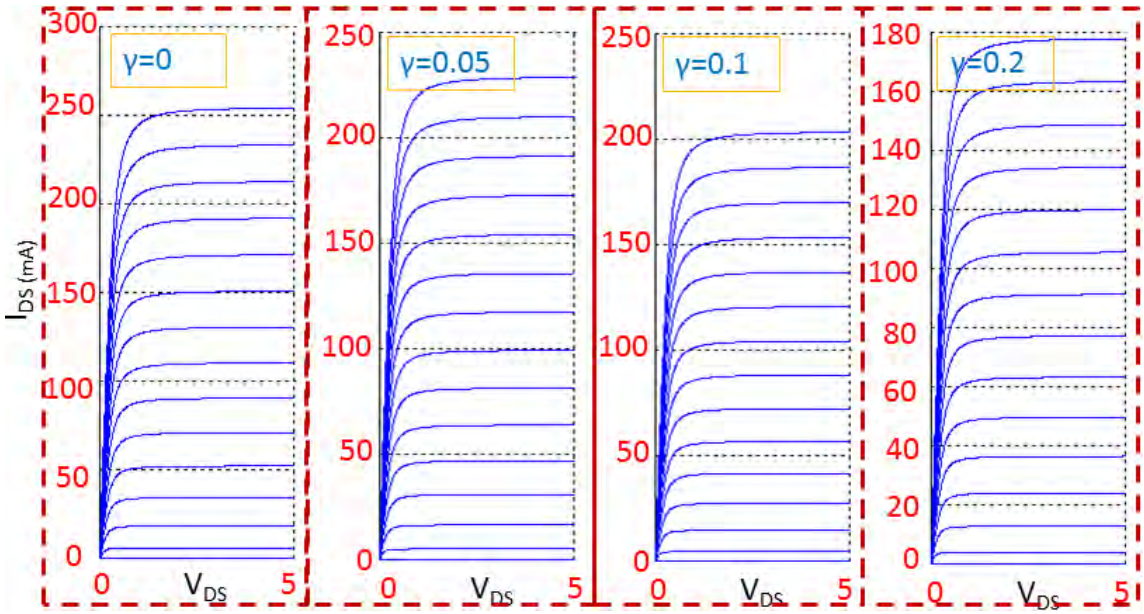

Figure 4.2: PS FET Simulation of Current Collapse

The simulated R_{ON} modulation is given in Figure 4.3. R_{ON} was calculated at 100 mA of drain current. At β =0, the observed R_{ON} was nearly equal to zero. On increasing β to 1, 5 and 10 , the increase in R_{ON} was clearly evident. The calculated R_{ON} was 1 Ω, 2.3 Ω and 5 Ω respectively.

In Figure 4.4, the combined effect of β and γ on the simulated I-V curve is very evident. With β = 2 and γ =0.1, an R_{ON} of 1.75 Ω is observed in Figure 4.4 (a), while is increases to nearly 2.0 Ω in Figure 4.4 (b), where β = 3 and γ = 0.2.

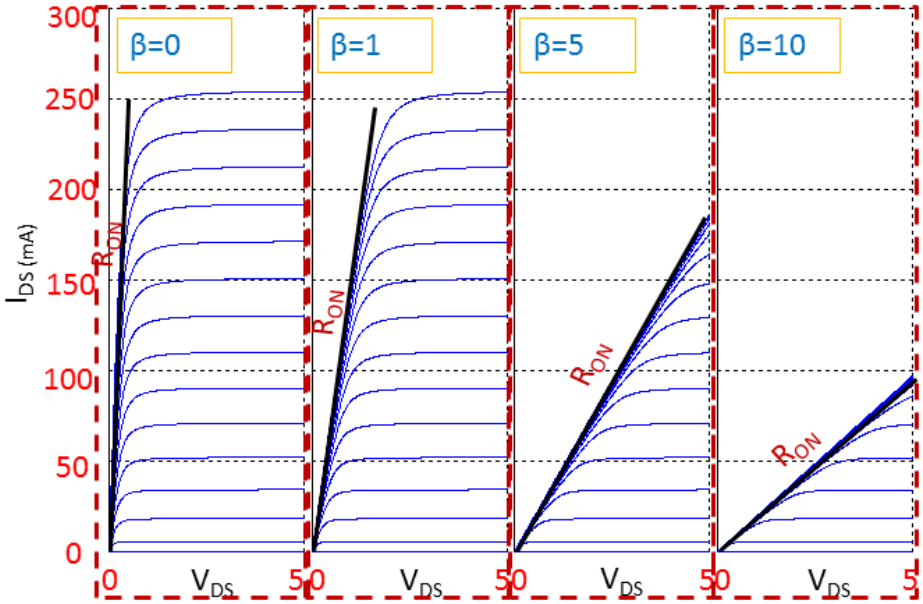

Figure 4.3: PS FET Simulation of Knee Walkout

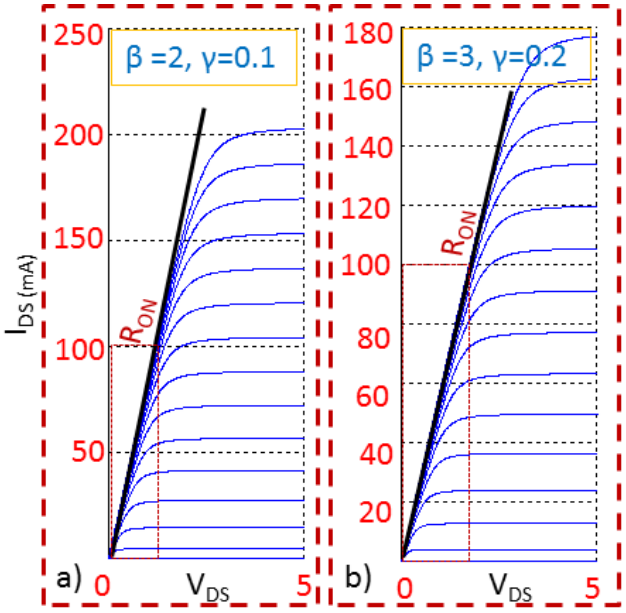

Figure 4.4: PS FET simulation of I-V curves with β and γ variation

4.4 Discussion

In order to predict the anomalous behaviour in the I-V characteristics of a GaN HEMT, a trap model based on the SRH theory was developed. This trap model can predict both small and large signal behaviours of the FET and in this study it was used to characterise trapping that affects the linear region only, between V_{DS}= 0 V and V_{DS}= V_{KNEE}. This was due to the fact that the load line of a power switch, transverses between high voltage, low current region to the low voltage, high current region. Electrons gets trapped between the gate-drain terminals due to high electric field which is dependent on the off-state drain voltage of the power switch.

The real advantage of this trap model is that it is a linear, first order model that can be easily implemented by attaching the trapping effects to the respective drain and gate terminals. The control potentials at the gate and drain terminals which influence the trap potentials at the gate and drain terminals, is directly proportional to the quiescent drain voltage. Hence it emulates the trap dependent effects which influence the R_{ON} of the power switch.

In order to accurately predict the trapping behaviour, I-V curves with quiescent drain bias dependence from full wafer mapping can be useful to obtain average values of the β and γ parameters. Thus, by using a first order trap model, the power switch R_{ON} and hence its load line at high drain bias conditions can be predicted. The efficiency of a power switch is directly related to its R_{ON}; the smaller R_{ON}, the better the efficiency. Thus this new trap model delivers the ability to predict the R_{ON} modulation of a GaN HEMT, enabling significant capability in the design of efficient power switching topologies.

4.5 Conclusion

RF GaN HEMTs suffer from trapping phenomena within the bulk of the device and on the surface between gate and drain regions. When used as power switches, the electrons trapped between gate and drain deplete the 2DEG channel causing an increase in R_{ON}, and the traps within the bulk alter V_P.

A simple new power switch trap model based on the Schottky Reed Hall (SRH) trap model implemented in PSPICE was able to predict R_{ON} modulation and its associated current collapse phenomena.

4.6 Next

In chapter 5, GaN RF HEMTs are characterised as power transistors in a high frequency switching topology. Commercially available bare die GaN HEMTs are used as the power stage in synhcronous buck converter topology. Gate driver topologies using depletion mode GaN devices are identified and implemented in the hybrid topology.

5

Hybrid Modulator

In previous chapters pulsed I-V characterization was done on RF GaN HEMTs to understand the impact of trapping when used as power switches. However the pulsed characterisation was done at a switching frequency of 500 Hz. In order to completely understand the behaviour of the HEMT devices as power switches, they should be characterised at their operating frequencies, in the tens of megahertz range. The currently available pulsed I-V set-up only allows for a maximum switching frequency of 50 KHz; while it is possible to go further up in frequency, the slew rate of the pulser, is not high enough to obtain good pulse integrity due to the slow voltage rise.

In this chapter the potential and limitations of commercially available bare-die RF GaN HEMTs as a power stage in switch-based supply modulators is investigated. The

impact of trapping on the efficiency of high frequency switching circuits was investigated by characterising RF HEMTs as power transistors in a high frequency switching topology implemented as a hybrid circuit. The performance evalutaion was based on a comparison of simulation and measured results.

As previously mentioned, the use of a HEMT as a power switch results from the fact that the path between source and drain can be regarded as a voltage controlled resistance. In contrast to the situation when the FET is used as an amplifier there is no DC bias applied to source or drain. A square pulse applied to the gate controls the opening and closing of the switch. In addition to the variable resistance there is also a capacitance associated with the FET which is dependent on the size of the device, but also on the process used for manufacture [41].

The intrinsic GaN parameters, like the gate length and the input capacitance of the HEMT, affecting the performance in high frequency modulator topology are evaluated, and the design challenges when using this technology will be the main topics in this section. The role of gate drivers, power transistors and layout techniques with a view to maximise circuit efficiency is also investigated. High frequency measurement challenges are also described.

5.1 Modulator Topology

The switching topology for the hybrid modulator was a synchronous buck converter topology where an external PWM signal provides the gate driver pulses to switch the power stage. The switching circuit is analogous to a voltage mode class D (VMCD) switching PA. Figure 2.35 shows the switching circuit which consists of 1) a power

stage, 2) driver stage, and 3) an output filter stage.

5.1.1 Power Switch Process Technology

In this section a brief summary of the power transistor technology is undertaken, while the full process details are given in [122], [123] and [124]. The epilayers for Cree commercial HEMTs are grown by MOCVD in a high-volume reactor on 100-mm semi-insulating 4H silicon carbide (SI 4H-SiC) substrates that are cut on-axis. Typical structures comprise an AlN nucleation layer, 1.4 μm of Fe-doped insulating GaN, approximately 0.6 nm of an AlN barrier layer, and a 25-nm cap layer of undoped $Al_{0.22}Ga_{0.78}N$. This nominal layer thickness and mole fractions yield sheet electron concentrations in the range of 8 to 10^{12} /cm^2 , but because of the AlN interlayer has the strong advantage of an electron mobility of near 2000^2/V-s at room temperature. The channel sheet resistance is about 335 Ω per square.

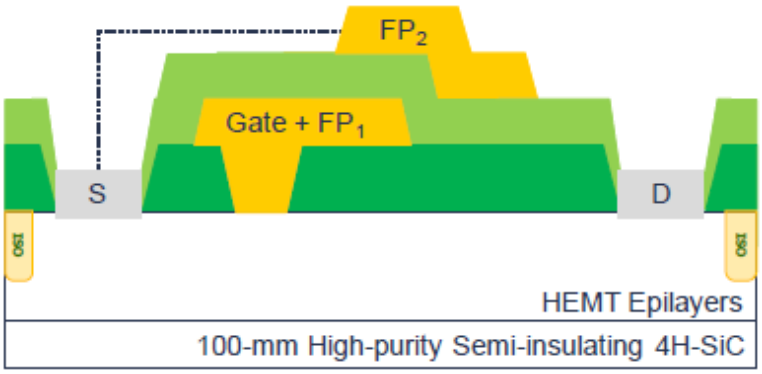

Figure 5.1: Schematic of Cree HEMT

As shown in the schematic cross section of Figure 5.1 [122], the device is fabricated with ohmic contacts that are formed directly on the top AlGaN layer. Device isolation is achieved using nitrogen implants to achieve a planar structure. Gate electrodes are formed by recessing through a SiN dielectric to the AlGaN and then depositing

Ni/Pt/Au metallisation. Field plates are optimised to engineer field shaping within the device [122]. Measured 1-mA/mm (gate current) breakdown voltage of this structure exceeds 150 V. Unit cell devices exhibit CW on-wafer output power levels of 5 W/mm when measured on a loadpull bench at 28 V and 3.5 GHz.

The 0.25 μm process employs a dielectric spacer method, which achieves short gates without serial printing of the gate pattern by costly and slow e-beam lithography [125]. The unit-cell devices exhibit CW output power levels of 7 W/mm and PAE > 60% when measured under optimum load conditions at 40 V for both 10 and 14 GHz. Devices provide 15 and 12 dB of small-signal gain at 10 and 14 GHz, respectively. The device f_T is >25 GHz at 40 V and at 10 % I_{DSS} quiescent bias [122].

5.1.2 Device Characteristics

The power stage consists of the power transistor and custom-built GaN anti-parallel diodes. The power transistors investigated in this section were 0.25 μm Cree CGHD40015 and 0.40 μm Cree CGHV0025. The corresponding I-V characteristics of the devices are given in Figure 5.2 and Figure 5.3. As can be seen, the transistors exhibit a very low R_{ON} resistance with excellent breakdown voltages of well over 100 V. Table 5.1 summarises the characteristics of the power stage devices.

Table 5.1: Power Stage: Device Parameters

Device	Gate	Size	F_T (GHz)	$R_{ON}(\Omega)$	V_{BD}(V)	C_{IN}(pF)	C_{OUT}(pF)
P_{T1}	0.25 μm	4×6× 200 μm	32	0.71	140	5.6	1.18
P_{T2}	0.40 μm	10×360μm	18	0.96	140	4.94	1.16

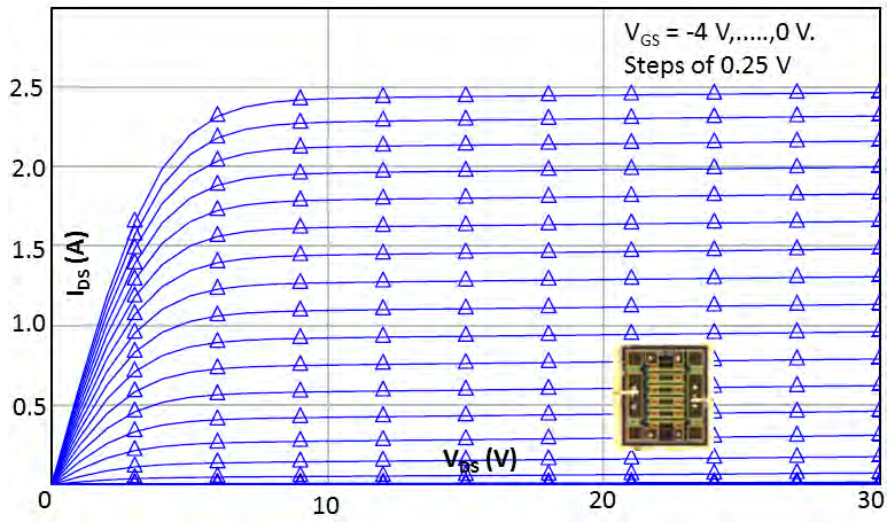

Figure 5.2: P_{T1}: I-V

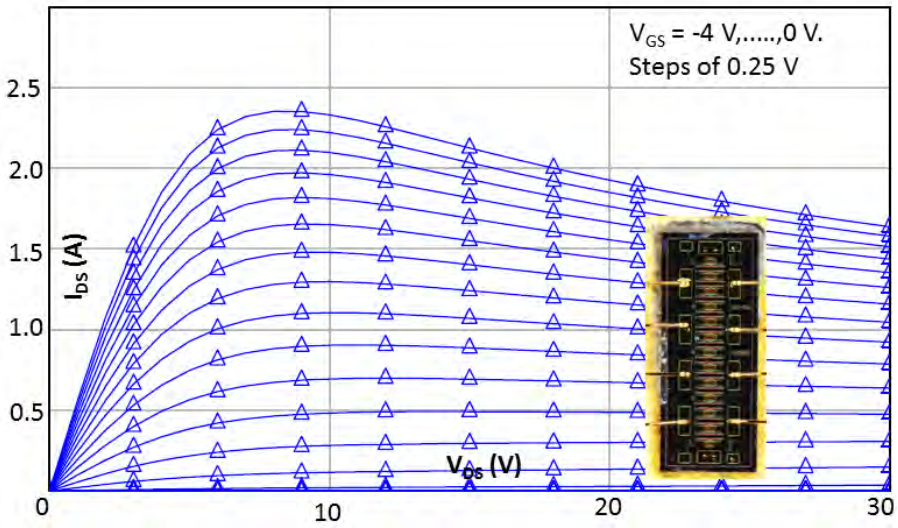

Figure 5.3: P_{T2}: I-V

5.1.3 Anti-parallel Diode

The power stage also incorporates an anti-parallel diode along with the power transistor. GaN HEMTs do not include body diodes, hence external anti-parallel diodes were integrated into the power stage. These diodes were fabricated in the Fraunhofer

IAF 0.25 μm GaN process. The forward voltage (V_F) was around 1.2 V as shown in Figure 5.4 and the measured reverse-breakdown voltage (V_{BD}) was around 100 V (Figure 5.5).

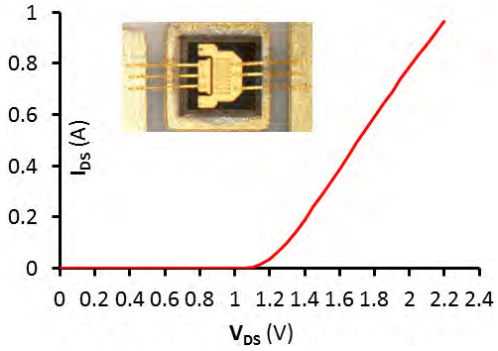

Figure 5.4: Diode Forward Biased

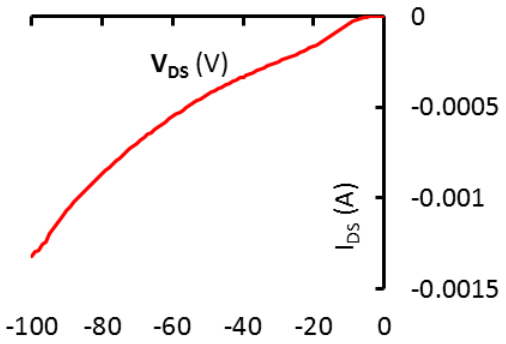

Figure 5.5: Diode Reverse Biased

5.1.3.1 Device Characteristics

The driver transistor (Figure 5.6) consists of 6 × 200 μm GaN HEMTs fabricated in Fraunhofer IAF's 0.25 μm technology. These were the smallest available off the shelf GaN transistors. Extended details of the fabrication process for the driver transistors and the power stage anti-parallel diodes will be given later in chapter 7. The device I-V characteristics are given in Figure 5.7.

Figure 5.6: IAF 1.2 mm GaN HEMT

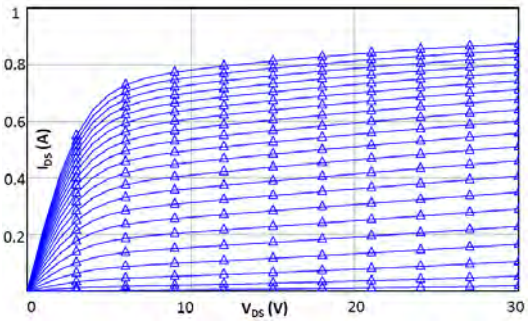

Figure 5.7: Driver Stage I-V

5.1.3.2 Output Filter

The lowpass filter passes only the low frequency components in the PWM signal. A traditional DC-DC converter power supply is designed such that the duty cycle is nominally constant, creating a constant output voltage [126]. However, in the case of a dynamic supply, the duty cycle may vary at frequencies near the RF envelope bandwidth. Therefore, the job of the filter is to pass a range of frequency content up to a cutoff frequency, f_C , but reject energy at the PWM switching frequency. SMD aircoil inductors along with multilayer high density ceramic chip capacitors will be used in the filter topology.

5.2 ST-R-LT Hybrid Modulator

An ST-R-LT gate driver based circuit topology was selected due to its superior switching characteristics. Figure 5.8 shows the hybrid power switch consisting of a totem-pole configured power stage with high and low-side gate drivers driven in anti-phase by an external PWM signal. Anti-parallel diodes are also included for reverse conduction.

When PWM_{HS} is low, ST_H is off, however the depletion mode LT_H is on and VT_{DRV} appears at the gate of PT_H. When PT_H turns on, $V_{SW} = V_{DD}$. As a result, the V_{GS} of PT_H is maintained at approximately 0 V, keeping PT_H turned on. A simplified circuit diagram corresponding to the case when $PT_H$is in the ON-state is shown in Figure 5.9 , with $R_{ON}LT_H$ being the ON-state resistance of LT_H.

While the high-side switch is on, the low-side switch is off. This is accomplished exter-

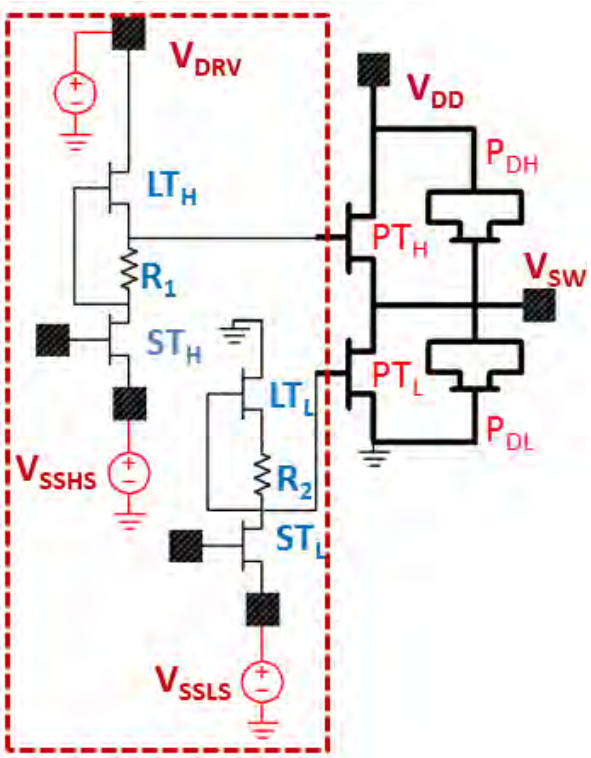

Figure 5.8: Hybrid Modulator Schematic

nally by applying a high signal to PWM_{LS}, thereby turning on the low-side gate-drive transistor PT_L and bringing the gate of PT_L to V_{SSLS} = -5 V.

When PWM_{HS} goes high, ST_H turns ON, the gate of PT_H is pulled down to $V_{SSHS} < 0$, plus a voltage drop across ST_H ($ILT_H \times R_{ON}ST_H$) and $ILT_H R_1$, which is set to produce V_{GS} = -5 V by the choice of component parameters and the bias voltage V_{SSHS}. When ST_H is on, the active pull-up transistor LT_H together with the source-degeneration resistor R_1 act as a constant current source ILT_H. The value of ILT_H can be adjusted by adjusting the size of LT_H and the value of R_1. A simplified circuit diagram for these states of the switches is shown in Figure 5.9. Once PT_H is turned off, the switch-node voltage V_{SW} is pulled down by the buck filter inductor current (not shown) towards approximately 0 V, allowing zero-voltage switching (ZVS) turn-on of PT_H .

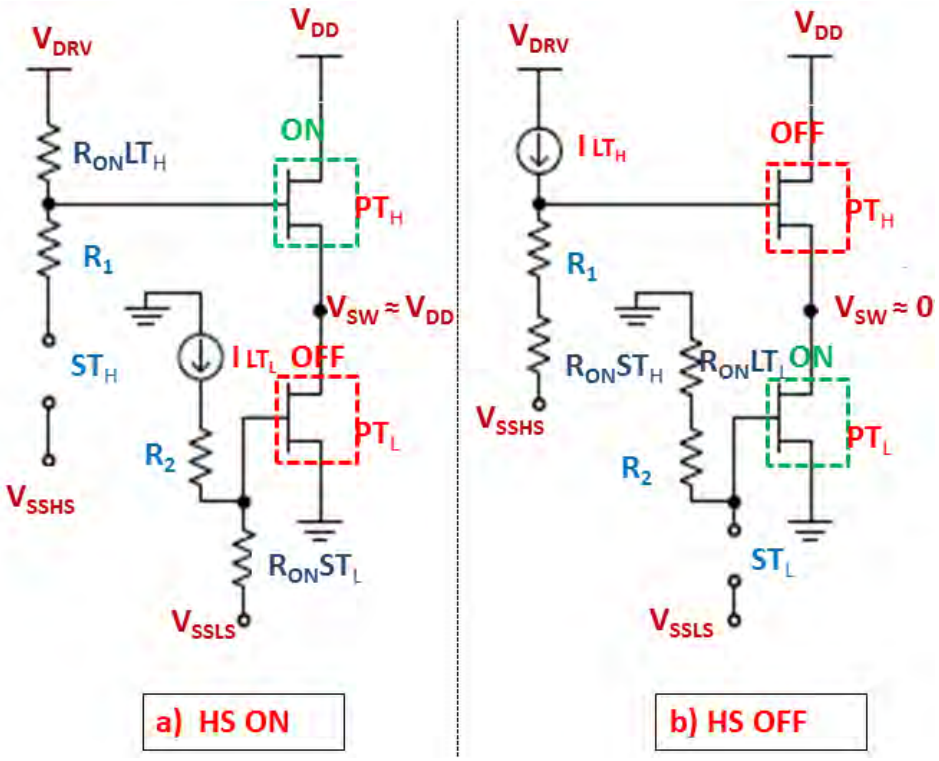

Figure 5.9: Buck Converter Operation

The gate-drive circuit design amounts to a trade-off between power consumption and speed. For instance, making R_1 smaller results in a faster falling edge in the driving signal of PT_H, at the expense of larger IST_H, and larger power dissipated on ST_H and R_1. Conversely, a larger R_1 results in reduced power losses in the gate driver, but longer fall and rise times in the gate voltage for the high-side power transistor PT_H. Driving signals with greater rise/fall times result in higher switching losses in the power stage. The values of the current sources LT_H and LT_L are determined by the device sizes and R_1 and R_2, respectively. Since the HEMTs are commercially available bare die devices, the sizes (gate periphery) are already fixed. The resistance is the only externally variable element in the driver circuit.

The power dissipation within a given duty cycle D, the static driver loss is given by

$$P_D = P_{DHS} + P_{DLS} = (V_{DRV} - V_{SSHS})ILT_H(1-D) + (-V_{SSLS})ILT_L D \tag{5.1}$$

5.3 Transient Simulations

The circuit was simulated in AWR Microwave Office, with a current sink I = 0.5A connected to V_{SW}, which resembles a synchronous buck converter with a large filter inductor. The simulated waveforms for the driver voltages are given in Figure 5.10 and switch node output voltage waveforms are given in Figure 5.11 and (Figure 5.12). Models available from the vendor was used for the transient simulation.

The gate driver simulation shows clear gate driver waveforms for both the high side and low side drivers. The high side driver has a large swing from 30 V to -5 V, which is below the pinch-off. The low side driver waveform swings from -5 V to 0 V.

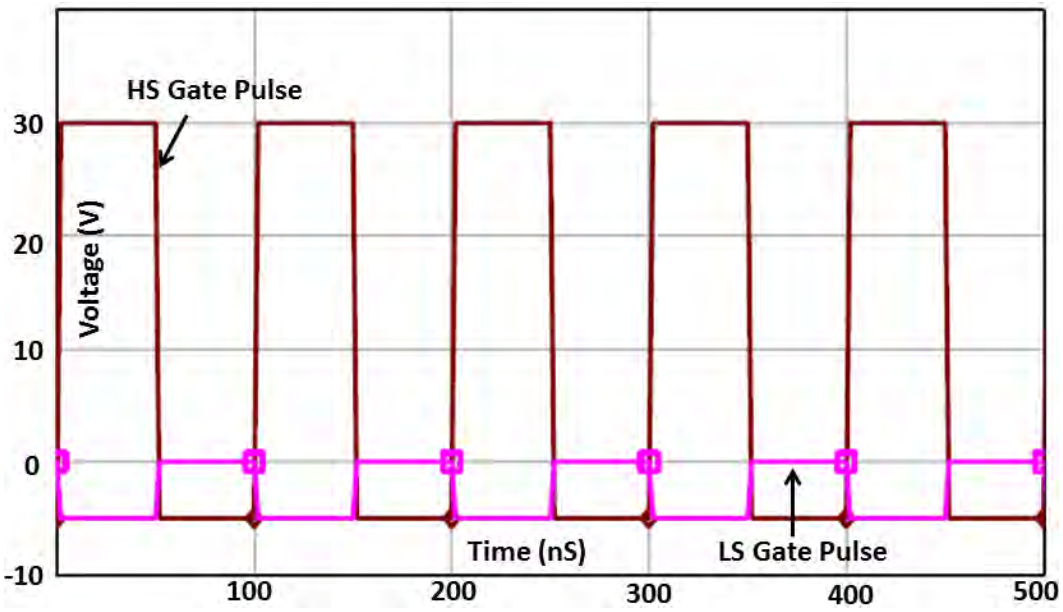

Figure 5.10: Gate Driver Transient Simulation

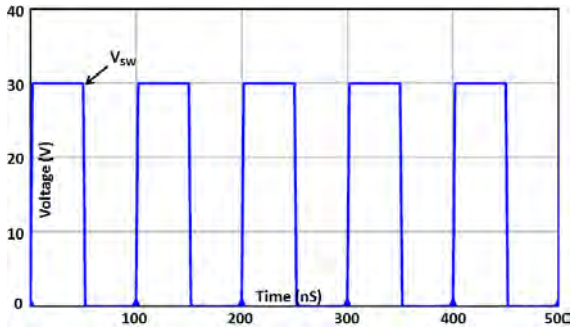

Figure 5.11: P_{T1}: V_{SW}(V), D = 50 %

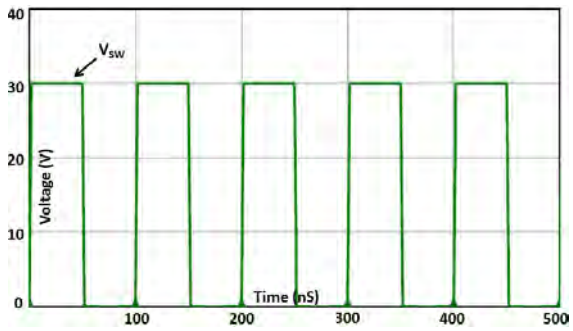

Figure 5.12: P_{T2}: V_{SW}(V), D = 50%

The switching waveforms for P_{T1} (Figure 5.11) and P_{T2} (Figure 5.12) are nearly identical due to the fact that these are RF HEMTs being used for power switching at the very low frequency of 10 MHz. Moreover, trace inductance, distributed capacitance and switch node capacitive effects due to a non-isolated power supply etc were not considered in this simulation. Hence the transient simulation is quite close to an ideal simulation and does not fully capture all of the external pcb layout effects under which the hybrid modulator will be characterised. A full EM simulation will reveal the role of trace parasitics in the circuit operation.

5.4 Circuit Layout

The circuit was laid out using the CAD layout feature available in AWR Microwave Office. The traces were optimised to minimise inductances and switching node capacitances that could affect the high speed switching characteristics of the hybrid power switch.

SMD footprints for decoupling capacitors were also added to the power lines along with the traces. The entire layout was configured to fit into an existing RF test jig of

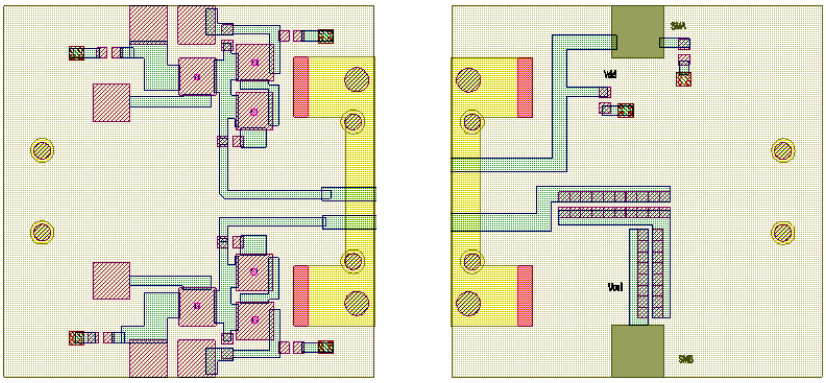

Figure 5.13: AWR Layout (100 mm x 50 mm)

110 cm x 50 cm. Figure 5.13, shows the pcb layout.

5.5 Circuit Implementation

The circuit was implemented on a 508 μm thick Rogers 4003 RF substrate with back side copper metallisation and a height of 35 μm which was mounted onto an RF test jig for support. The GaN transistors used in this design have their sources grounded on the backside. Hence, to avoid a circuit short circuit, the power stage was implemented in a standard RF MMIC package while the drivers were implemented in a QFN package.

5.5.1 Power Transistor Package

As mentioned, all transistors used in this circuit were source grounded through vias on the back side. The power transistors along with the diodes were silver epoxied onto a substrate (Figure 5.14) which then in turn was glued into the MMIC package (Figure 5.15). Vias were implemented within the substrate to ground the required

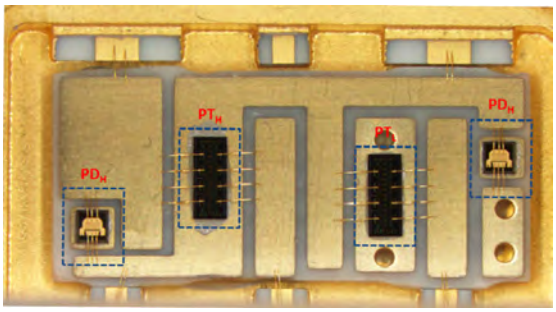

Figure 5.14: Power Stage Substrate

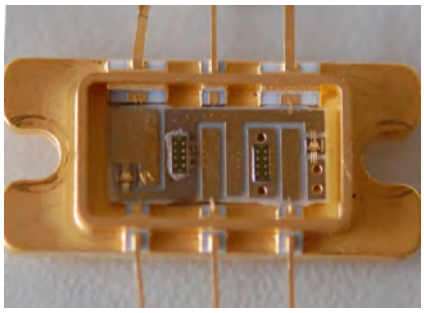

Figure 5.15: Hybrid Package

source contacts. This allows a better current distribution and a more uniform heat extraction. Multiple bond wires were used to minimise the parasitic inductance while providing electrical connectivity to the MMIC package leads.

5.5.2 Driver Stage Package

The driver transistor was silver epoxied onto a QFN package to avoid short-circuiting the source to ground. 25 μm bond wires were used to complete the electrical connectivity. As shown in Figure 5.16, the driver transistor in the QFN package was epoxied onto to the substrate while the power stage was held in position using push-in placement holders.

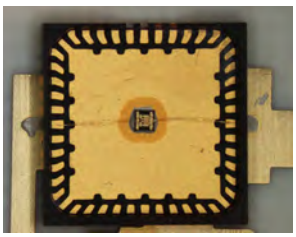

Figure 5.16: Driver HEMT in QFN package

A fourth-order Legendre filter with an 8 MHz cut-off frequency is used instead of the conventional second order filter, as the latter would lead to excessive output voltage

Table 5.2: SMD Component Values

L_1	C_1	L_2	C_2	R_1	R_2
1.5 μH	1 nF	1.5 μH	720 pF	250 Ω	250 Ω

ripple or reduced efficiency. Table 5.2 gives the values for the filter components.

Connection to the external power and measurement setup was done through SMA adapters screwed onto the test jig. The test jig gives mechanical support and acts as heat sink to draw heat away from the active elements of the circuit. Moreover, the test jig is also connected to the ground node of the power supply during measurements.

5.6 Measured Switching Characteristics

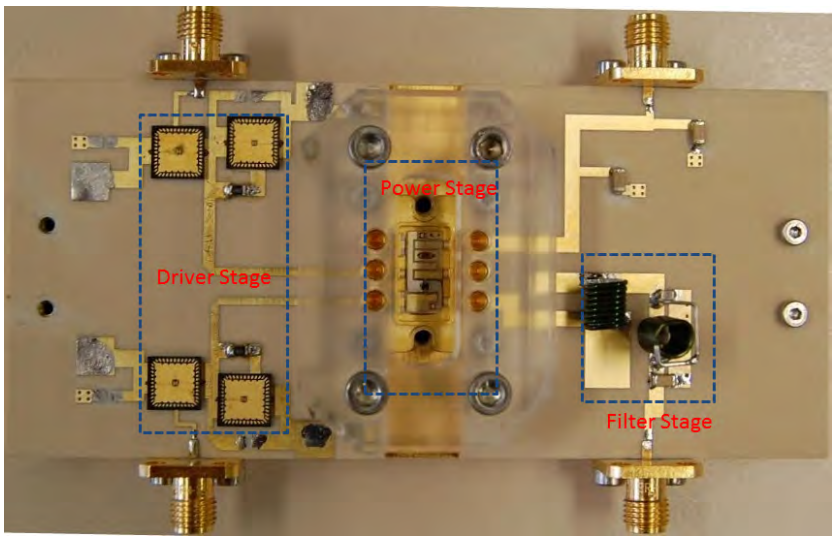

Figure 5.17: Hybrid Modulator (50 mm × 110 mm)

The synchronous buck converter modulator implemented on the PCB prototype is illustrated in Figure 5.17. Reactive components capable of operating at high frequencies were selected: decoupling and output filtering capacitors from American Technical Ceramics provided low ESR at high frequencies, chip resistors from Vishay Draloric

and Coilcraft high Q air core inductors (132SM series) were used as the buck inductor.

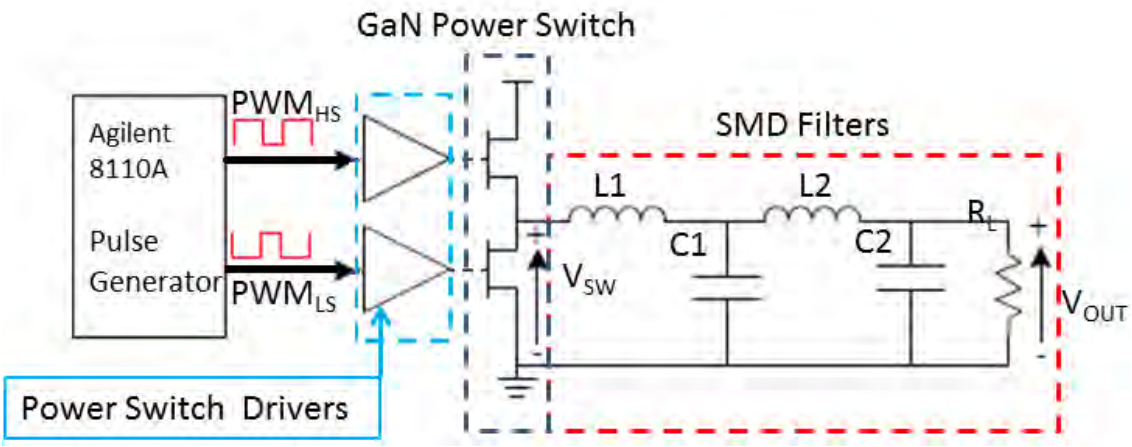

Figure 5.18: Hybrid Switch Test Measurement Setup Diagram

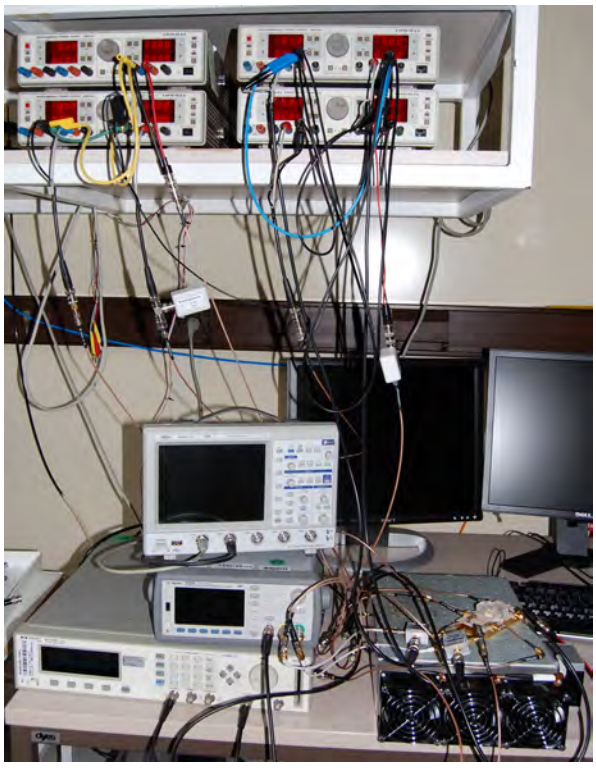

Figure 5.19: Hybrid Test Bench

The test setup schematic for characterising the hybrid modulator is given in Figure 5.18. High frequency, high resolution pulse-width modulated control signals are generated

using an Agilent 81160 pulse generator module. Initial testing of the modulator proved it to be highly unstable due to oscillation within the GaN devices. Therefore an in-house designed decoupling capacitive load ("oscillation break module") was attached to the long measurement cables (>1m) to stabilise the device in the noisy environment within the test setup is highlighted in Figure 5.19. A low capacitance differential probe (< 1pF) was used to measure the switch node waveforms to avoid any excessive effect on the measurements.

Figure 5.20 shows the gate driver voltage swings for the high side and the low side driver at 10 MHz switching frequency. The dead times were adjusted manually to obtain no overlap and zero-voltage switching condition. The high side driver voltage swing (green trace) is from 30 V at the high level to -4.7 V at the low level, while the low side driver swing (blue trace) is seen to be from -0.5 V to -5.8 V.

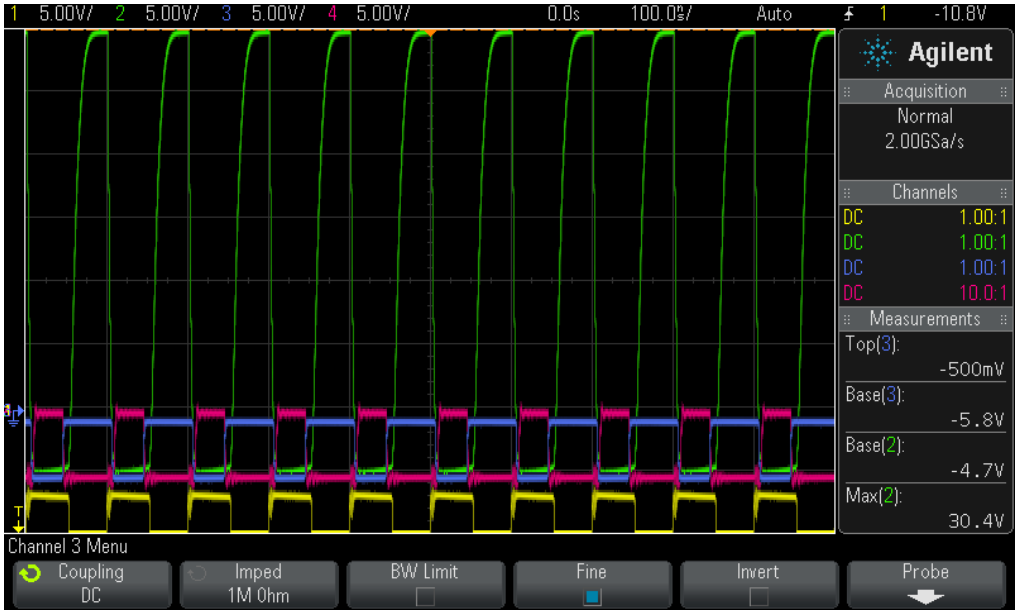

Figure 5.20: Gate Driver Waveforms

Figures 5.21, 5.22, and 5.23 show the switching node voltages of P_{T1} with 50% , 25% and 75% duty cycle. The switch node waveforms of P_{T1} are well behaved and show no

significant overshoots.

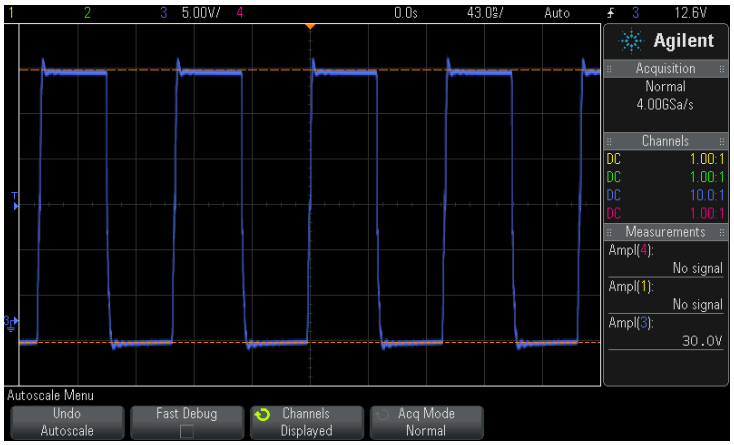

Figure 5.21: P_{T1}: V_{SW}(V), D = 50 %, P_{OUT}=10W

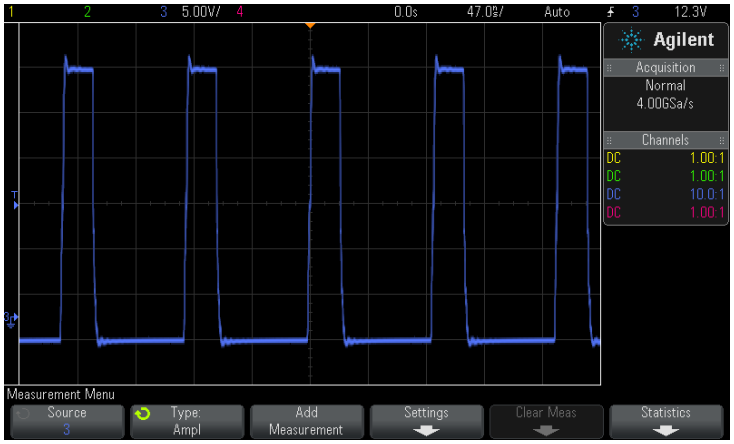

Figure 5.22: P_{T1}: V_{SW}(V), D = 25 %,P_{OUT}=4W

The switch node waveforms of P_{T2} at 50% , 25% and 75% duty cycle are shown in Figure 5.24, 5.25, and 5.26. P_{T2} switch waveforms for 50% and 75% duty cycle showed some distortion at the falling edge of the output square wave. This may be due to the fact that the current in the low side gate driver circuit need to be biased at a lower negative voltage to pull the falling edge down quicker without any distortion. It must also be mentioned that measurement of switch node voltages are very challenging due to the long cables, noisy lab environment and the need for common ground for both the test jig, the measurement oscilloscope and the power supply. Moreover additional

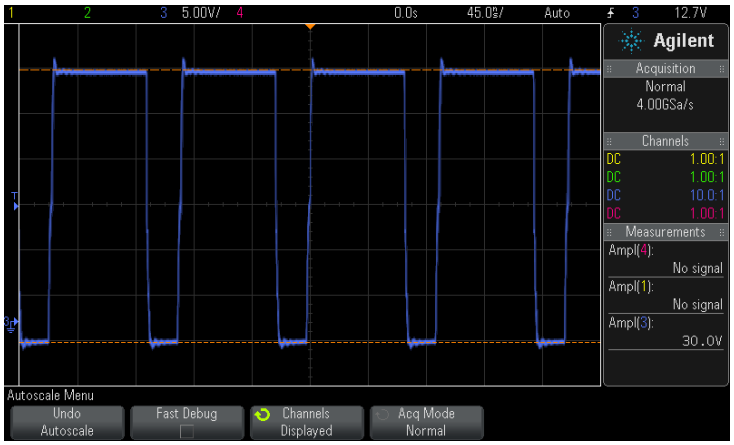

Figure 5.23: P_{T1}: V_{SW}(V), D = 75 %,P_{OUT}=12W

de-coupling capacitors were introduced into the hybrid circuit to minimise any noise in the power supply line. The use of isolated supply modules and very short measurement cables would be ideal in this situation to minimize any noise coupling into the measurements. Even though spikes appeared in the initial measurements, the use of "oscillation break" modules helped eliminate them.

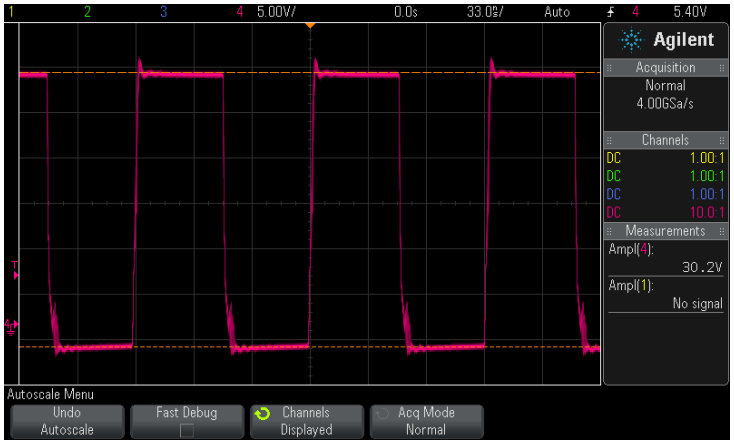

Figure 5.24: P_{T1}: V_{SW}(V), D=50%,P_{OUT}=12W

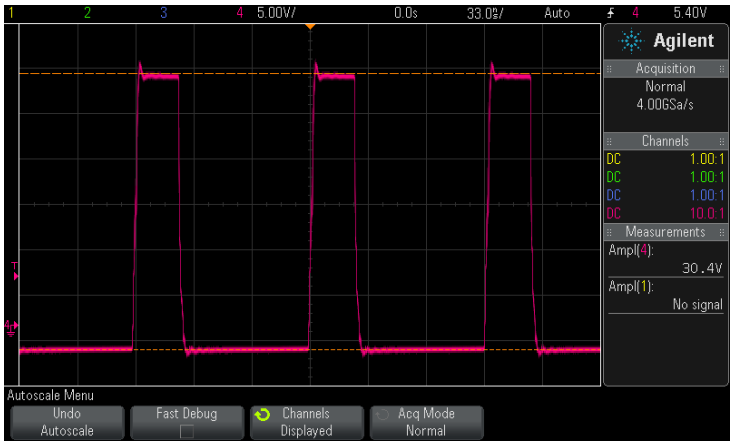

Figure 5.25: P_{T2}: V_{SW}(V), D=25%,P_{OUT}=4W

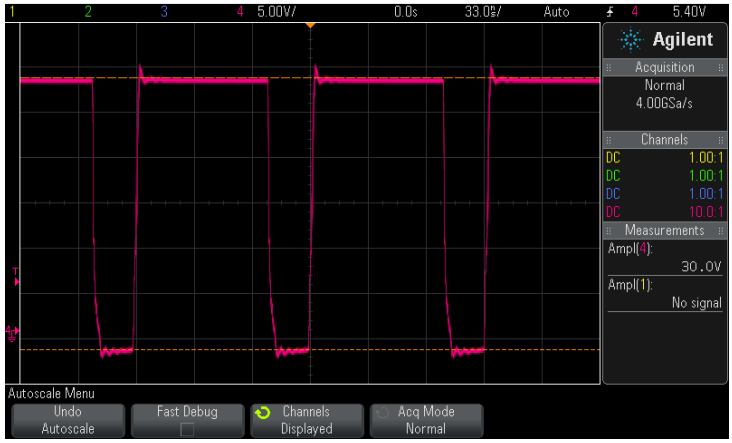

Figure 5.26: P_{T2}: V_{SW}(V), D=75%,P_{OUT}=14W

5.6.1 Measured Efficiency and Loss Analysis

Efficiency is measured at 10 MHz and a 30 V input voltage, at several duty cycle values and output power levels. The HEMT loss model described previously in chapter 2 is extended to include the ac and dc loss of the inductor. It is assumed that the switching loss is caused solely by switching node capacitance. A device dynamic on resistance, based on estimates from pulsed I-V characterization described in chapter 3, is used to calculate conduction losses. Hence the total loss within the switching device is given

by

$$P_{TOTAL} = P_{Cond.Loss} + P_{Sw.Loss} + P_{LDC} + P_{LAC}. \tag{5.2}$$

The measured power stage efficiencies for both the transistors P_{T1} (Figure 5.27) and P_{T2} (Figure 5.28) are over 90% when delivering output powers of 12 W and 14 W respectively. The efficiencies peaked at 95.8% and 93.1% for a duty cycle of 75%. Even though the power transistors are capable of high output currents, in this work the output currents were limited to under 650 mA.

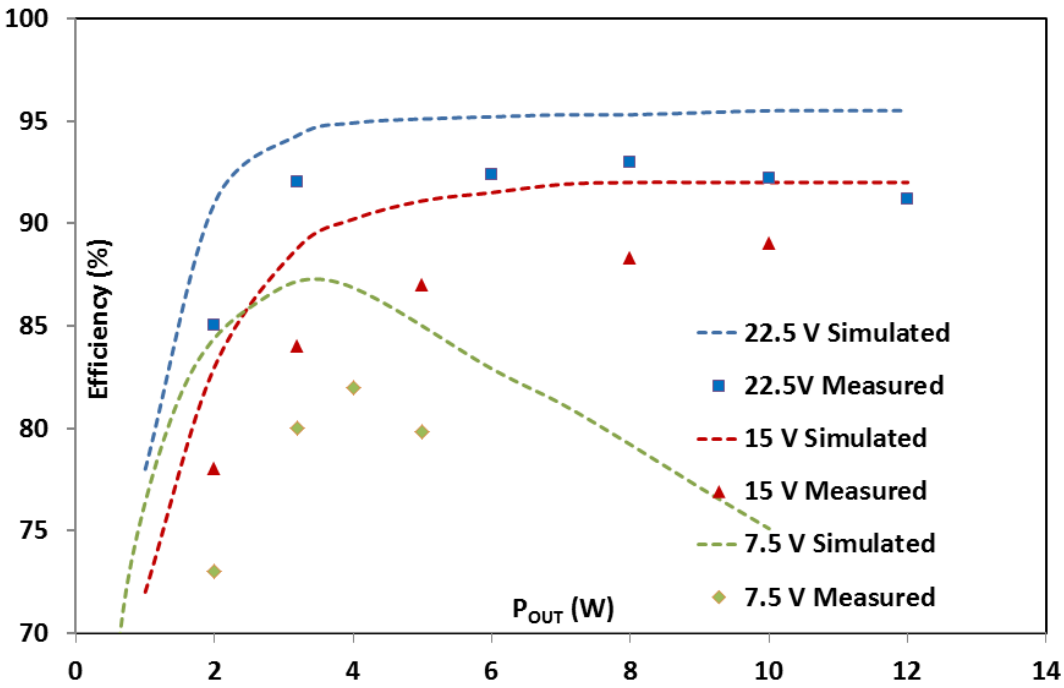

Figure 5.27: P_{OUT} v Efficiency

Figure 5.29 and Figure 5.30 give the simulated loss breakdown within the power stage of the modulator. The most dominant loss mechanism within the devices was conduction loss. Hence it is imperative to choose devices with extremely low on resistance.

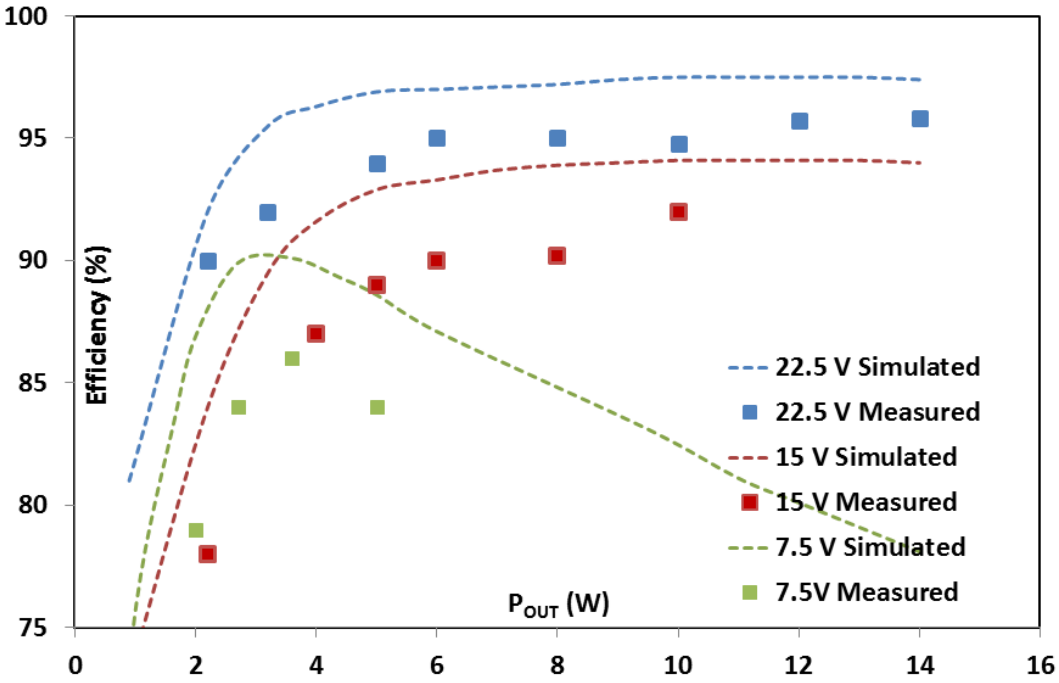

Figure 5.28: P_{OUT} v Efficiency

The losses within the gate driver circuitry are of major concern when considering the overall efficiency of the modulator. As previously described, the driver circuitry needed to drive high side power stage using depletion mode GaN devices is very challenging. Table 5.3 details the simulated and measured driver losses of the hybrid modulator. The simulated gate driver circuitry showed a maximum power dissipation of 0.68 W for the 14 W modulator. However the measured power dissipation was around 2.72 W. Here, even though the ST-R-LT topology was used to minimise the current through the driver, only the external resistance value could be modulated. The major contribution to the gate driver loss was from the high side driver. This is due to the fact that the voltage level swing is around 35 V. Hence a topology that would minimise the huge voltage swing will enable significantly lower the power dissipation within the high side driver topology.

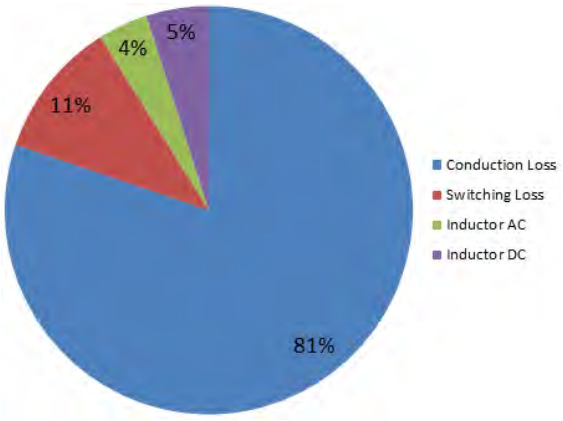

Figure 5.29: P_{T1}: Loss Breakdown

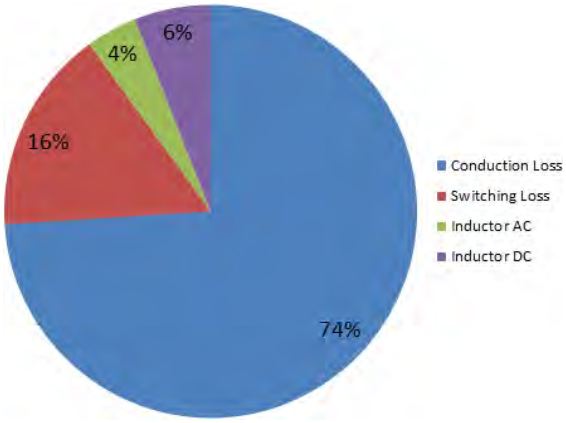

Figure 5.30: P_{T2}: Loss Breakdown

Table 5.3: Comparison of Driver Losses

	P_{T1}			P_{T2}		
	Duty Cycle			Duty Cycle		
	0.25	0.50	0.75	0.25	0.50	0.75
Simulated (W)	0.68	0.61	0.62	0.64	0.57	0.55
Measured (W)	2.69	2.72	2.70	2.64	2.70	2.68

5.7 Discussion

In this chapter, devices manufactured using RF GaN HEMTs developed by commercial foundries are characterised as power transistors in a hybrid modulator topology. Results are presented for a 12 W, and a 14 W, 30 V synchronous buck converter prototype operating at 10 MHz. Measured efficiency peaks above 93.1% and 95.8% at 10 MHz and remains above 90% over a wide range of operating conditions.

In order to accurately characterise the circuit for future integration, the driver circuits were also designed with GaN transistors. Due to the absence of p-type transistors in the GaN process, the high side driver design is more complicated than that for the low side driver because the gate voltage for the high side must have a very large voltage swing, from below ground,S to pinch-off the HEMT, to approximately the full

power supply voltage. Custom designed GaN Schottky barrier diodes were used as anti-parallel diodes in the power stage.

At a switching frequency of 10 MHz trapping within the power transistor had minimal impact on the overall performance. This is due to the fact that traps within the devices have a very limited time to react due to the high frequency of switching. Hence, the same device which showed trapping at high drain bias voltages and a switching frequency of 500 Hz showed minimal trapping effects when switched at 10 MHz. It was revealed that the high side gate driver losses were the dominant contributor to the overall loss. Hence minimising the high side gate driver sizes would significiantly improve the overall efficiency of the modulator.

Reduction of the transistor gate length is a commonly used method to improve the device speed. Therefore the most important benefit is a decrease of the gate capacitances, which have a direct influence on the device speed in terms of the cut off frequencies. The main advance due to the reduced gate length was the increased cut off frequency, f_T, which increased from 18 GHz to 25 GHz for a gate length reduction from 0.4 μm to 0.25 μm. This is caused by the gate capacitance reduction. This reduction in C_{GS} will lead to a decreased input capacitance, enabling faster switching as well as lower current requirements to drive the gate "ON" and "OFF". The two RF HEMTs characterised had input capacitances of 5.6 pF and 4.94 pF respectively. However the gate driver loss while driving each power stage was very similar, indicating that the trace inductance and capacitance of the layout contributed significantly more than the intrinsic device parasitics. Integration of the power switch and its associated drivers in a MMIC process will minimise the effect of trace inductance and capacitance which can significantly impair the high frequency operation by distorting the switch node output waveforms, and improve the efficiency by eliminating additional

capacitances/inductances.

An estimation of the PAE for a simulated 3-GHz GaN power amplier using the same transistor (GaN 0.25 μm) as the hybrid modulator is shown in Figure 5.31. It must be stated, that even though the target design was X-Band HPA with modulator, the simulation was conducted at S Band, since at higher frequencies the role of parasitics needs to be fully accounted for to accurately predict the PA efficiency. Hence a lower RFPA operating frequency was chosen for simulation purposes.

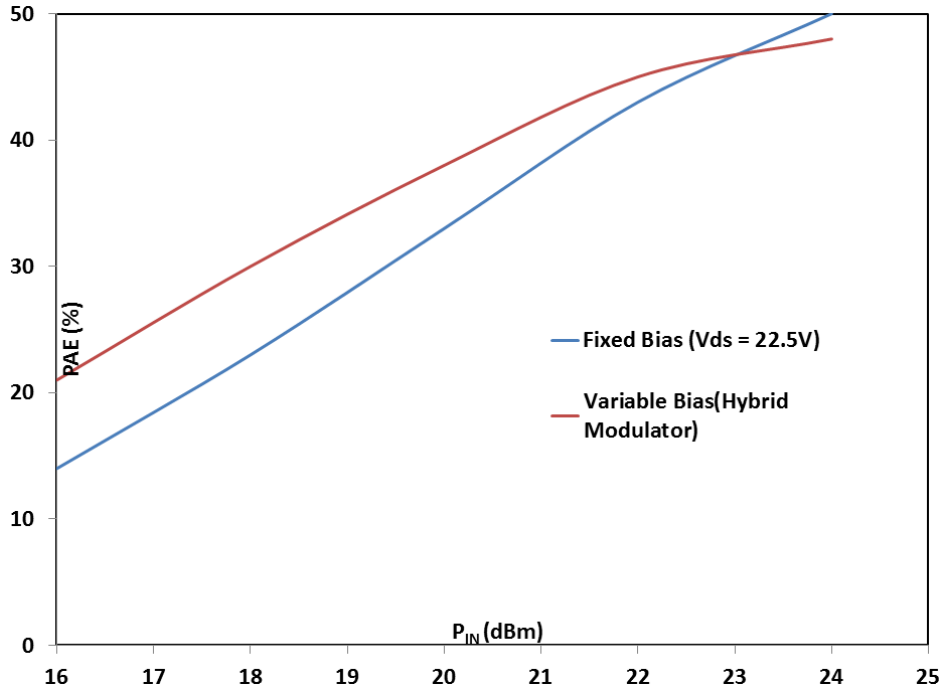

Figure 5.31: Comparison of PAE

The combined RFPA-modulator circuit was tested at a lower drain bias voltage of 22.5 V instead of the normal 28 V operation, and was done to emulate the measured modulator performance at a duty cycle of 75% with an input voltage of 30 V and an output voltage of 22.5 V. This was done with a view to avoid the destruction of the bare-die power stages within the modulator, due to the increased current at higher duty cycles and inefficient heat transfer from the bare die devices to the copper carrier substrate

Table 5.4: State of the Art: GaN Hybrid Modulators

Ref	Topology	Technology	P_{OUT} (W)	Max η (%)	Freq (MHz)	V_{DD} (V)
[11]	Boost	0.40 μm Cree GaN on SiC	65	84-90	50	37-56
[1]	Boost	0.40 μm Cree GaN on SiC	53	91.9%	50	50
[98]	Buck	0.5 μm FBI GaN on SiC	-	85	1	15
[25]	Buck	0.5 μm FBI GaN on SiC	50	90	1	28
[31]	Sync. Buck	0.15 μm TQS GaN on SiC	3	96	40	20
[99]	Buck	EPC eGaN GaN on Si	40	89	10	42
[100]	Buck	EPC GaN GaN on Si	80.8	91.6	8	-
[101]	Boost	0.4 μm Nitronex GaN on Si	8	86-96	10	14-28
This Work	Buck	0.40 μm Cree GaN on SiC	12	93.1	10	30
This Work	Buck	0.25 μm Cree GaN on SiC	14	95.8	10	30

*FBI- Ferdinand Braun Institute, TQS- Triquint Semiconductor.

within the power stage housing. Moreover non-synchronized HS and LS timing errors of the PWM at high duty cycles is always fatal to the device.

The simulated PAE of the S Band amplifier is improved by 6.5% by the dynamic drain bias (taking into account the measured modulator power stage efciencies) for input power variation between 16 and 20 dBm; the PAE was improved up to 22 dBm of input power. This translates into compatibility with the W-CDMA (PAPR = 3.5 dBm) modulation scheme.

The state of the art, GaN power switch incorporated hybrid circuits available in the literature are given in Table 5.4. In [11] a 65 W boost converter topology for ET appli-

cations switching at 50 MHz is given and was later expounded in [1] for space based RFPA applications. The maximum output power delivered was 53 W switching at 50 MHz. A Hybrid Switching Amplifier (HSA) with a buck converter switching at 1 MHz with a maximum efficiency of 85% is decribed in [98], and the same group at Ferdinand Braun Institute followed it up with [25], where a 50 W, 90% efficient DC-DC converter is demonstrated; however the switching frequency is only 1 MHz. In [31], a 3 W synchronous buck converter power stage with 96% efficiency was demonstrated for ET applications. In [99] an enhancement mode GaN HEMT power switch in a boost converter topology that delivered up to 40 W of output power at 89% efficiency is reported. Variations of driver topologies and their influence on the power cells were investigated in [100]. The maximum output power reported was 80.8 W at an efficiency of 91.6% and a switching frequency of 8 MHz. A boost converter with an efficiency of 88.8% was mated with an RFPA to deliver 8 W at a PAE of 39.9% for phased array applications [101].

In all the above reported publications, the investigated topology is a boost converter or a buck boost converter without a gate driver stage. In our work a hybrid modulator in a synchronous buck converter topology with power transistors, diodes and gate drivers, all fabricated in RF GaN HEMT is reported for the first time.

the high side gate driver was found to be the major contributor to the overall loss within the hybrid modulator circuit. An ST-R-LT gate driver topology was introduced where the gate driver current can be minimised by engineering the gate periphery (W/L) of the switching transistor (ST) and the load transistor (LT), as well as the modulation resistance (R) between the load and switching transistors. The measured power dissipation still remained high due to the fact that the total voltage swing of the high side driver was from a high level of 30 V to below pinch-off at -5 V. The total efficiency

of the system can be further improved by adjusting the voltage swing of the high side driver.

5.8 Next

MMIC power switchers with integrated drivers optimised for high frequency, high efficiency operation fabricated in a 0.25μm commercial foundry GaN process will be explored in chapter 6. Integration allows for minimisation of trace inductances and capacitances. Proper optimisation of gate drivers by engineering the gate periphery and load transistors allows minimisation of driver currents and modification of ST-R-LT gate driver topology for low voltage high side driver bias allows high efficiency operation.

6

Integrated Modulator

6.1 Introduction

This chapter details the design, fabrication and testing of high efficiency MMIC power switches with integrated gate drivers to form integrated modulators in commercial foundry GaN process. High operating frequency allows for the integration of the power switch and gate drivers onto a single die by minimising the parasitic effects, and optimal operation is achieved by the use of high Q inductors and low ESR resistors. A synchronous buck converter is preferred for high frequency switching due to its simplicity and a manageable loss breakdown analysis for performance prediction. In the last chapter an ST-R-LT driver topology is introduced which enables the minimi-

sation of current through the driver circuit by engineering the gate peripheries of the ST and LT as well as the modulation resistance between them. Even though the gate driver current is minimized, the high voltage swing of the high side gate driver causes the power dissipated to be quite high. Hence in this chapter two different topologies with reduced high side gate driver bias voltages are investigated and implemented in MMIC technology with a view to assessing the best power switch driver topology to integrate with an HPA. The integrated modulators were fabricated in 0.25μm GaN MMIC process from Triquint Semiconductor.

6.1.1 Device Characteristics

6.1.1.1 Triquint GaN Semiconductor

The process technology on which the two topologies were designed and fabricated was the commercially available GaN process from Triquint Semiconductor. The Triquint 0.25μm process caters to 6-18 GHz frequency band applications with an f_T around 32 GHz and a maximum power density of over 5.5 W/mm at 10 GHz.

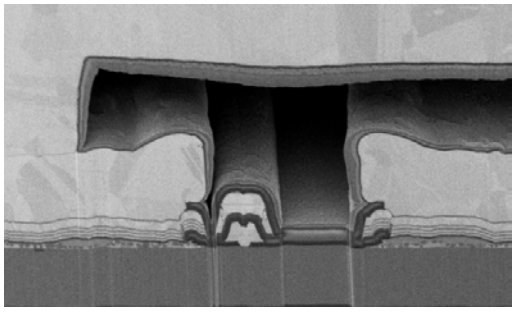

Figure 6.1: SEM photograph of 0.25μm TQ GaN HEMT

The AlGaN/GaN HEMTs investigated in this study were fabricated on a commercial foundry 3-inch GaN-on-SiC process. The epitaxial structure has a Si GaN buffer with

Fe doping for improved isolation. An AlN spacer was inserted between the buffer and the AlGaN Schottky barrier layer, and the surface is covered by a GaN cap layer for reduced leakage. The active device layers are isolated by performing a mesa etch down to the GaN buffer. The ohmic contacts were formed by alloying Ti/Al/Mo/Ti/Au. A SEM image of a Triquint 0.25 μm GaN HEMT is given in Figure 6.1 [127].

The ohmic source-drain spacing is 4 μm with nominal contact resistance of 0.5 ohm-mm. The gate length is defined by patterning and etching a 0.25 μm opening in the Silicon Nitride (SiNx). A second patterning and subsequent metallisation over the etched SiNx opening completes the gate process and forms an integrated field plate. Also a source-connected second field plate (2FP) was implemented to reduce the electric field in the device channel under high voltage operation. The 2FP geometry was designed to optimise the efficiency and gain of the device. For backside via formation the wafers are ground and polished to a thickness of 100 μm.

The DC I-V characteristics for a 10 × 100 HEMT device up to V_{DS} = 30 V and for V_{GS}= -5...0 V, is given in Figure 6.2.

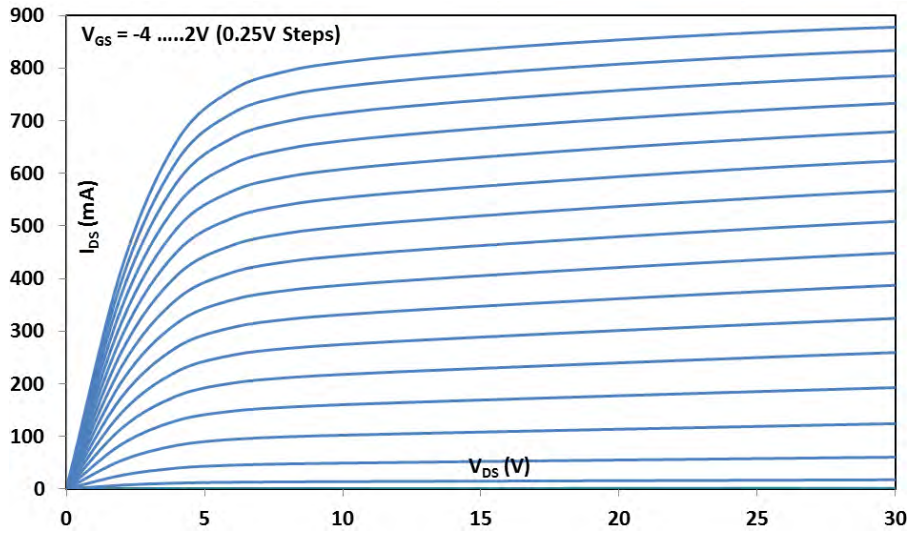

Figure 6.2: TQ GaN HEMT-10 × 100 IV Characteristics

Table 6.1: Power HEMT : Device Characteristics

GaN Process	Size	R_{ON}	C_{IN}	C_{OUT}	V_{DS}	F_T	F_{MAX}	V_{BD}
0.25 μm	(μm)	(Ω)	(pF)	(pF)	(V)	(GHz)	(GHz)	(V)
TQS	12×200	1.1	4.08	0.98	30	32	42	100

The breakdown voltage is above 100 V, which is about four times as high as for GaAs devices having similar cut-off frequencies. The characteristics of the power transistor are given in Table 6.1.

The device also exhibits excellent tranconductance characteristics. A maximum g_m of 340 mS/mm was measured at a drain bias voltage of 10 V with V_{GS} = -1.5 V, and 310 mS/mm at V_{DS} = 30 V with V_{GS} = -1.5 V.

The complete channel pinch-off is at about -3.9 V independent of the drain bias voltage. The device also shows high cut-off frequencies that are extrapolated from the measured small-signal current gain h_{21} and maximum stable gain (MSG)/maximum available gain (MAG) plots. An extrinsic transit frequency of f_T = 30 GHz and an extrinsic maximum frequency of oscillation of f_{MAX} = 42 GHz were obtained at V_{DS} = 30 V.

6.2 MMIC Power Switch Topologies

Two driver topologies were considered for implementation in the MMIC process, one based on bootstrap design and another based on switch node connected design. Given the extremely low device capacitances, and the significant impact that any additional switching node capacitance has on the achievable efficiency, minimisation of the parasitic switching node capacitance is the main focus of the design process.

In the previous chapter, an ST-R-LT topology was investigated using commercially available bare-die devices. The overall circuit efficiency can be improved by minimizing the current dissipation in the high side driver. In a MMIC process, the driver current could be engineered by adjusting the W/L ratios of the switching transistor and the load transistor along with the resistor.The ST-R-LT gate driver topology can be further improved by modifying the drain voltages present at the LT_H. A bootstrap topology with reduced drain voltage at LT_H and a switch node connected topology which completely eliminated the LT_H drain voltage are described in this section. The low side driver is based on a ST-R-LT gate driver topology.

6.2.1 Bootstrapped ST-R-LT Gate Driver

The schematic of a bootstrap driver is shown in Figure 6.3. By using a bootstrap diode, D_B, and capacitor, C_B, the required driver voltage at drain of LT_H, V_{DRV}, can be greatly decreased. Before PT_H turns on, ST_H is still on, and current flows through D_B and LT_H. V_{DB} is selected such that V_1 is ≈ 0 V at this moment. After that, turning PT_L off brings the gate of PT_{T1} up to $V_1 \approx 0$ V, thus turning PT_H on. At the same time, D_B starts to be reverse-biased, making the voltage across C_B (which is equal to V_{GS} of PT_H), stay constant at 0 V, regardless of V_{SW}. Note that C_B must be large enough to hold the voltage during the time when PT_H is on.

The ON/OFF state of the high-side switch PT_H is decided by the state of the driver transistor ST_H. When ST_H is on, PT_H is off and vice versa. Simplified circuit diagrams corresponding to the two states of the switches are shown in Figure 6.4 .

Consider the case when ST_H is on, PT_H is off, and PT_L is on, so that $V_{SW} = 0$. LT_H,

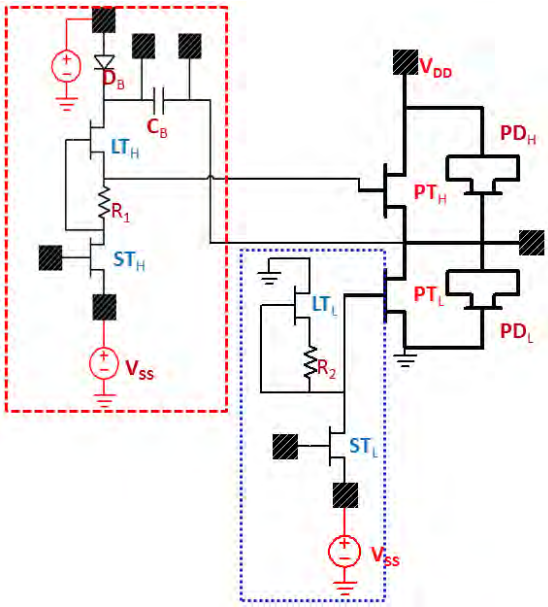

Figure 6.3: Bootstrapped ST-R-LT Gate Driver Modulator

together with the source degeneration resistor R_1, behaves as a current source ILT_H, and $V_{DRV} = V_{BD} = 1$ V, is selected such that the capacitor voltage $V_{CB} = 0$ V.

Consider next a transition to the state when PT_L is off and PT_H is on. After the low-side switch PT_L is turned off, ST_H can be turned off to initiate turn on of the high-side switch PT_H. Assuming hard switching operation, with ST_H off, ILT_H charges the gate capacitance of PT_H, which turns on and, as a result, the switch node voltage V_{SW} increases. As the voltage across LT_H drops, and the current through LT_H drops, LT_H becomes fully on, with small on-resistance $R_{ON}LT_H$ connecting $V_{CB} \approx 0$ across the gate-to-source terminals of PT_H, thus completing the turn-on transition of the high-side switch. In zero-voltage switching operation, the timing of the events is different, as V_{CB} increases to V_{DD} before ST_H is turned off, but the gate-driver operation is otherwise very similar. With $V_{SW} \approx V_{DD}$, diode D_B is reverse biased, preventing discharge of C_B.

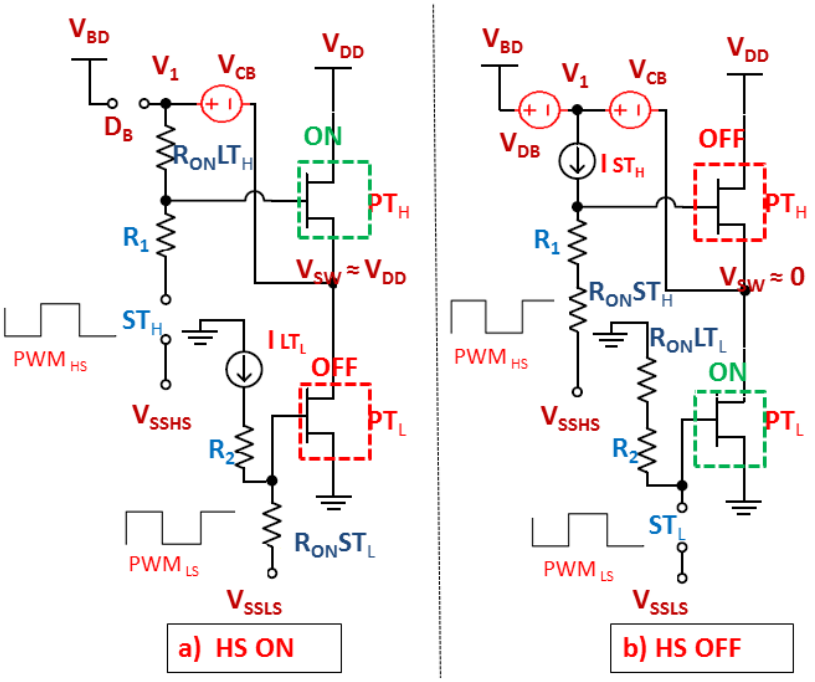

Figure 6.4: Bootstrapped circuit operation

The increased driving speed enables the use of larger power stage devices (PT_H and PT_L) and allows higher output power, compared to the case with the active pull-up driver. This circuit is simulated in AWR, using the same configuration described before, with the calculated waveforms presented in Figure 6.5.

A clear advantage of the bootstrapped driver is that it operates from a reduced V_{DRV}, which implies reduced static power losses compared to the ST-R-LT driver. This, in turn, allows a design with a larger bias current targeting faster transitions, and allowing use of larger power-stage devices. As a result, the overall efficiency and output power capability can be improved. Another advantage of the bootstrapped driver is that it allows positive gate-to-source voltages for the high-side switch. This provides additional design flexibility, and the ability to implement a driver with enhancement-mode devices.

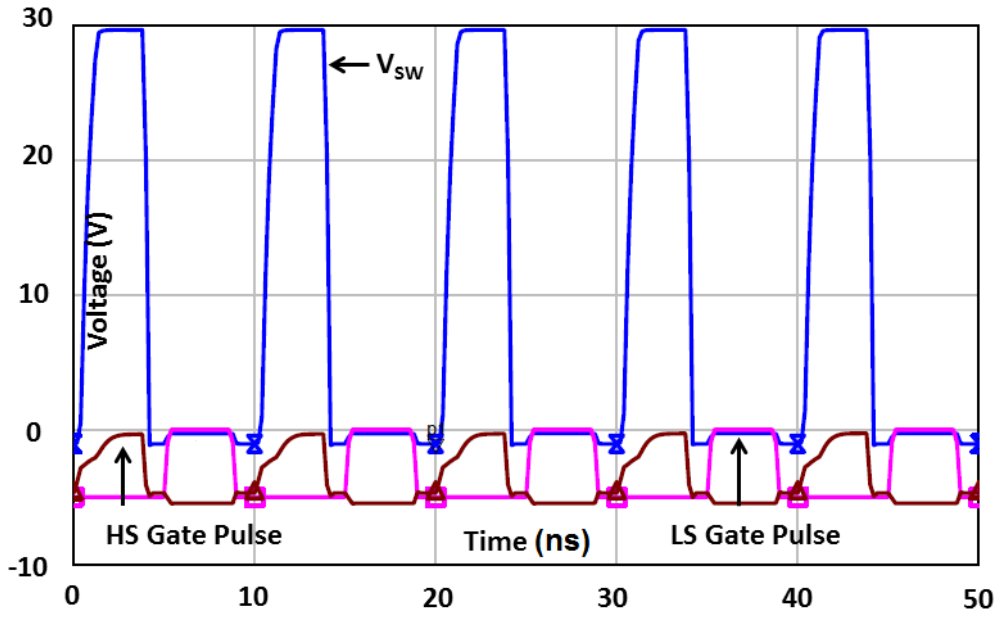

Figure 6.5: Bootstrap Modulator: V_{SW}(V), D=50%

A disadvantage of the boostrapped driver is the need for a relatively large capacitor C_B, which must hold the required voltage during the time when PT_H is on. Because of the area taken by C_B, and because of a chip-size limitation, the circuit in Figure 6.25 did not include a low-side driver. An external bootstrap capacitor must be employed, especially when switching at lower frequencies.

For the bootstrap circuit the power dissipation within a given duty cycle, D is,

$$P_D = P_{DHS} + P_{DLS} = (V_B - V_{SSHS})ILT_H(1-D) + (-V_{SSLS})ILT_L D \tag{6.1}$$

Table 6.2 gives the sizes of the active and passive elements used in the bootstrap modulator circuit.

Table 6.2: Bootstrap Circuit : Devices and Passive Sizes

GaN Process	PT_H,PT_L	PD_H,PD_L	ST_H,ST_L	LT_H,LT_L	R1	R2	D_B	C2
0.25 μm	μm	μm	μm	μm	Ω	Ω	μm	pF
TQS	12×200	12×100	4×50	4×25	100	75	4×25	25

6.2.2 Switch Node Connected ST-R-LT Gate Driver

In the modified ST-R-LT gate driver (Figure 6.6), the high drive voltages for both the high side and low side transistors are completely eliminated by taking advantage of the voltage swing at the switching node itself. Instead of using an external voltage source V_{DD}, the drain of the load transistor is connected to the switching node V_{SW}. This configuration significantly reduces the driver power consumption by taking advantage of the fact that the switching node voltage V_{SW} becomes approximately zero when PT_H is off and PT_L is on.

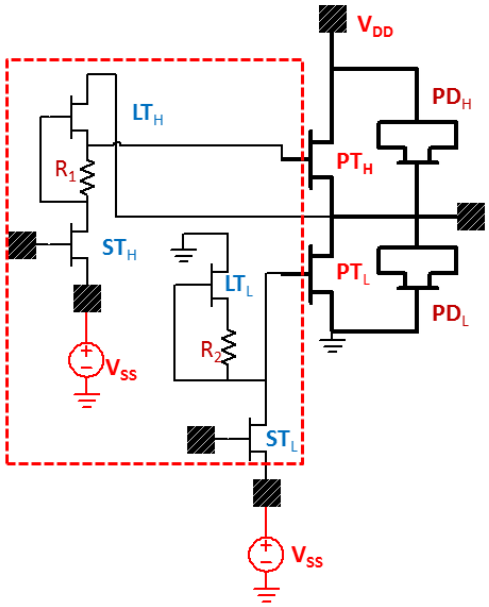

Figure 6.6: Switch Node connected Modulator

The operating principle (Figure 6.7) for the high side driver is as follows: the gate-to-

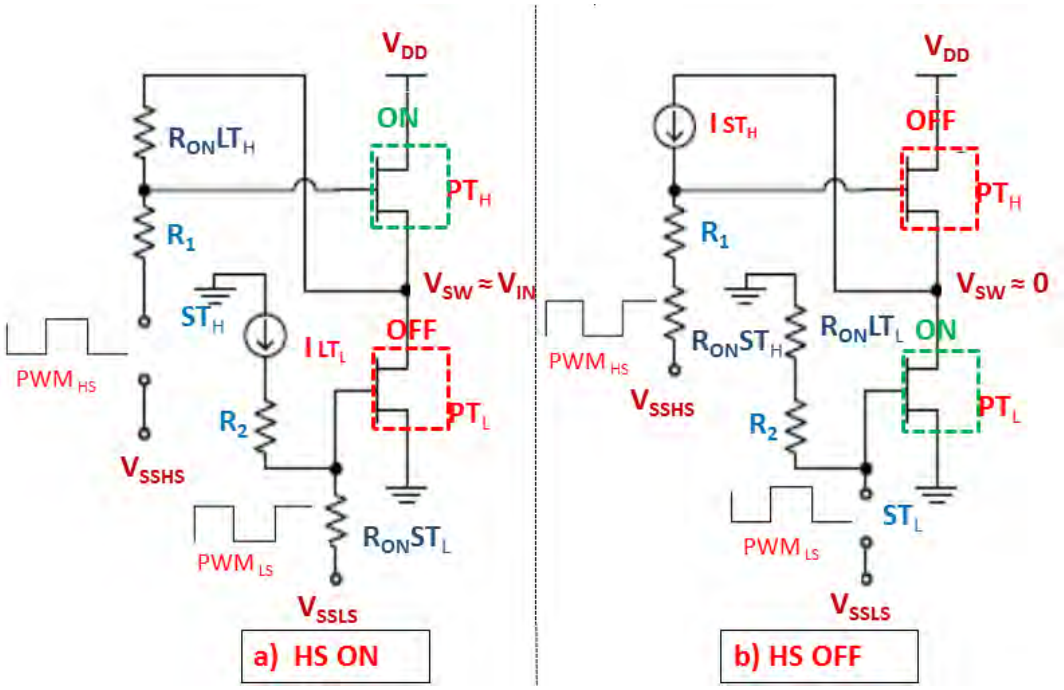

Figure 6.7: Switch Node connected circuit operation

source voltage V_{GS}HS of PT_H is equal to the source-to-drain voltage of LT_H. When ST_H is off, ST_L is on, which is represented by the small on-resistance $R_{ON}LT_H$, and V_{GS}HS is approximately 0 V. As a result, the depletion-mode high-side switch PT_H is fully on. When ST_H is turned on, the gate voltage of PT_H , which is selected to be -5 V, is determined by ILT_H, R1 and $R_{ON}ST_H$. Current ILT_H is supplied from the switching node, and is around zero. Furthermore, no external V_{DD} supply is required. Because of the reduced driver loss, a larger ILT_H can be employed to speed up transitions, allowing larger power stage devices, and overall improved efficiency and higher output power.

Compared to the bootstrapped driver, in the switch node connected driver, there is no need for a large bootstrap capacitor, for the high side driver supply voltage V_{BD} at the bootstrap diode. The design is therefore functional over a wide range of frequencies without the need for an external bootstrap capacitor.

Table 6.3: Switch Node Circuit: Devices and Passive Sizes

GaN Process	PT_H,PT_L	PD_H,PD_L	ST_H,ST_L	LT_H,LT_L	R1	R2
0.25μm	μm	μm	μm	μm	Ω	Ω
TQS	12×200	12×100	4×50	4×25	100Ω	75 Ω

The power dissipation within the switch node connected ST-R-LT circuit can be calculated as follows:

$$P_D = P_{DHS} + P_{DLS} = (-V_{SSHS})ILT_H(1-D) + (-V_{SSLS})ILT_L D \tag{6.2}$$

Table 7.5 gives the sizes of the active and passive elements used in the swith node connected modulator topology.

The MMIC circuit schematic was simulated using the Microwave Office AWR CAD tool. Figure 6.8 shows the transient simulation waveforms of the circuit seen at the output switch node.

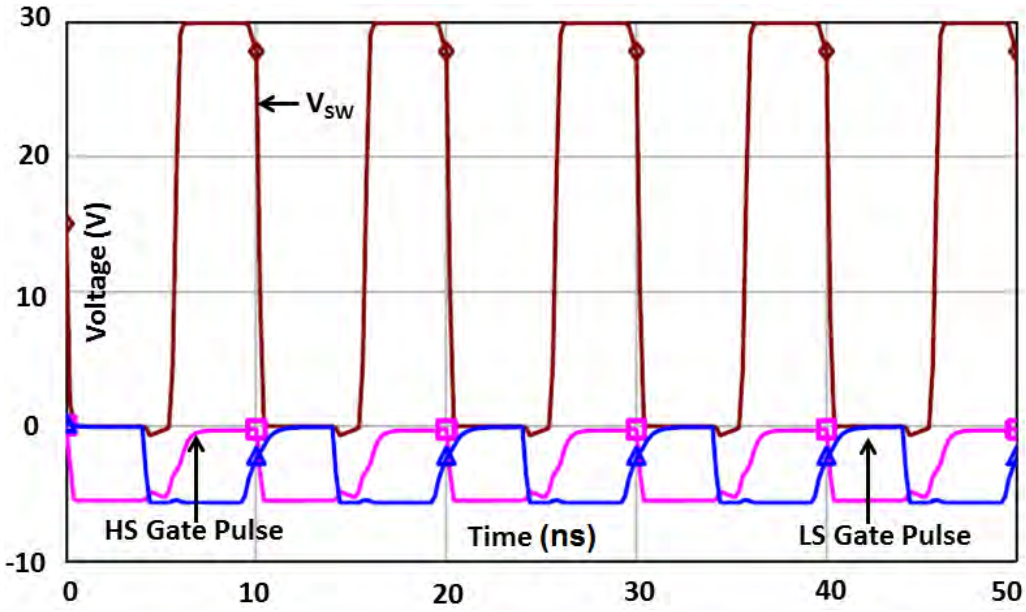

Figure 6.8: Sw. Node Connected Modulator : V_{SW}(V), D=50%

The simulation shows clean output switch waveforms at 100 MHz switching frequency. It must be mentioned that the transient simulation was done using PA models available within the PDK and optimised for Class-AB operation.

6.2.3 Layouts

6.2.3.1 Triquint 0.25 μm GaN Process

The layout of the integrated power switch was done in Triquint Semiconductor's 0.25 μm GaN processes technology. This process is a 3 metal-insulator (3MI) process with a process design kit (PDK) available and was implemented using AWR Microwave Office CAD simulator. Capacitors, resistors and inductors are available within the design kit and all the trace layouts are implemented in microstrip technology. All the active devices were designed from scratch and cleared for any design rule check (DRC) errors.

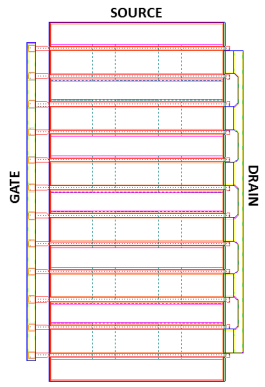

Figure 6.9: 12×200 HEMT

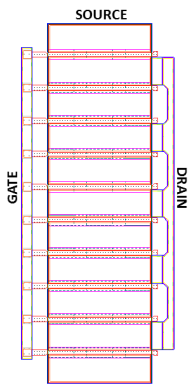

Figure 6.10: 10×100 Diode

The basic cell of the power stage consists of a 200 μm wide HEMT device with 25 μm long drain and source fingers separated by a 2 μm long gate finger. 12 of these unit cells are paralleled to give a total device periphery of 2.4 mm (Figure 6.9). In order

to accommodate the high current within the device, three 50 μm wide segments of air bridges are used to interconnect all the source fingers to the external source pad.

GaN HEMTs do not have body diodes present within the devices, hence external anti-parallel diodes were integrated into the power stage. The junctions between gate to drain and gate to source within the HEMT can be exploited to function as a diode by internally shorting the source and drain fingers using the air bridge metallisation available within the process. Hence the gate becomes the cathode and the internally shorted source and drain become the anode for the anti-parallel diode. Here a 10 × 100 μm device size was chosen for the anti-parallel diode (Figure 6.10). MIM decoupling capacitors are also incorporated within the power stage, at the input and at the output switching voltage nodes to minimise any spikes present in the supply voltage. Figure 6.11 shows the layout of the bootstrap circuit, and the switch node connected modulator layout is given in Figure 6.12.

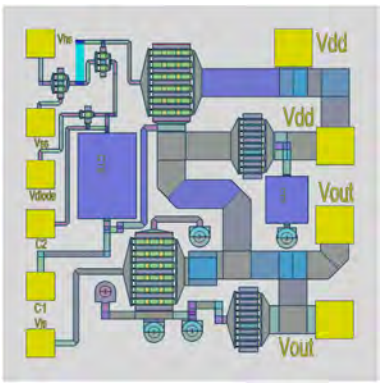

Figure 6.11: Bootstrap Layout

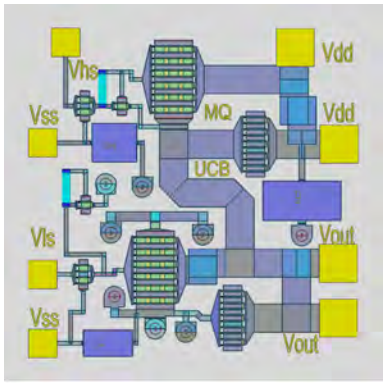

Figure 6.12: Sw. Node Layout

The metal traces for circuit interconnects were microstrip transmission lines and the widths were adjusted to deliver the required currents. Interfaces to the external circuits were done with bond pads of size 150 μm for the PWM signals, while multiple bond pads of 200 μm were used for input and output voltage nodes. Both circuits were

laid out in an area of 2 × 2 mm, however 125 μm guard rings are placed around the circuit, hence the actual available area is smaller than 2 × 2 mm. It must be noted that the switch node connected gate driver design gives a compact layout compared to the bootstrap design. The presence of on chip bootstrap capacitor as well as traces for external capacitor complicates the bootstrap layout and hence the low side driver cannot be implemented due to space constraints.

6.2.4 PCB Implementation

The fabricated MMIC chips shown in Figures 6.25 and 6.27 were directly placed on a gold-plated test jig through a hole cut in the PCB. The MMIC was epoxied onto the surface of the test jig. The PCB was fabricated from a 508 μm thick Rogers 4003 RF substrate with back-side copper metallisation and a height of 35 μm. The PCB was screwed down onto the test jig with a thin layer of silver epoxy applied to the interface between the bottom layer and the test jig top face. The traces within the PCB were optimised to minimise inductances and switching node capacitances that could affect the high speed switching characteristics of the MMIC power switch. 25 μm thick gold bond wires were used to connect from the MMIC bond pads to the PCB traces. The PCB layout is the same for both MMICs, and using wire bonding allows for flexibility in making electrical contacts. The PCB prototype for the bootstrap and the switch node MMICs are given in Figure 6.16 and 6.18 including the output filter. Low ESR decoupling capacitors were attached to the input voltage lines to mitigate the effect of any ripple on the supply voltage.

The low pass output filter values chosen are given in Table 6.4. High Q, low ESR chip capacitors from the Vishay Vitramon VJ high frequency series while the inductors from

Table 6.4: Low-pass filter component sizes

L_1	L_2	C_1	C_2
nH	nH	pF	pF
100	150	47	47

Coilcraft Midi spring series were used for the 4th-order filter implementation.

There was some room for tolerance in choosing L_2, as Figures 6.13 and 6.14 show the filter output response which indicates the change in the cut-off frequency.

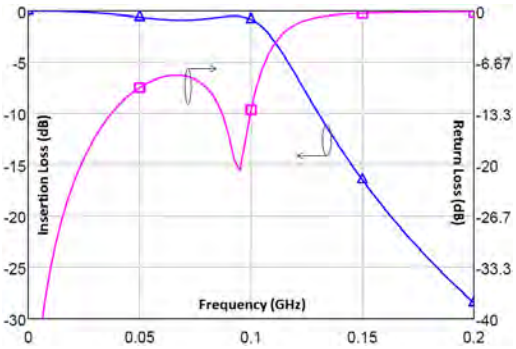

Figure 6.13: Output Filter, L_2 =120nH

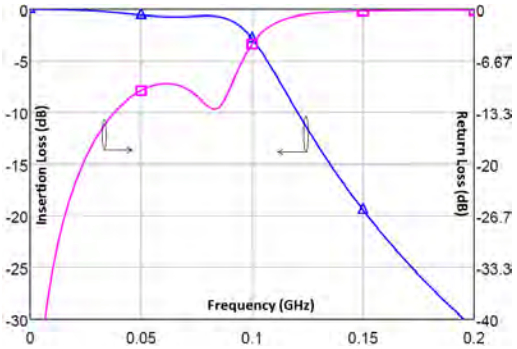

Figure 6.14: Output Filter, L_2 =150nH

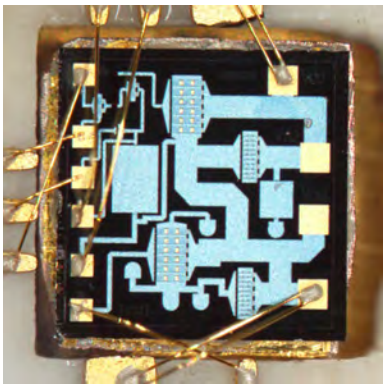

Figure 6.15: TQS Bootstrap

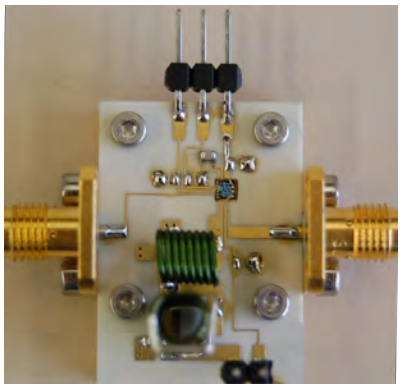

Figure 6.16: TQS Bootstrap PCB

SMA adapters are screwed onto the test jig for the PWM gate driver signals to interface to the chip. The test jig acts as the ground node since the back side of the MMIC is in contact with it and the test jig is connected to the power supply ground. In addition it provides mechanical support and acts as a heat sink for the modulator chip.

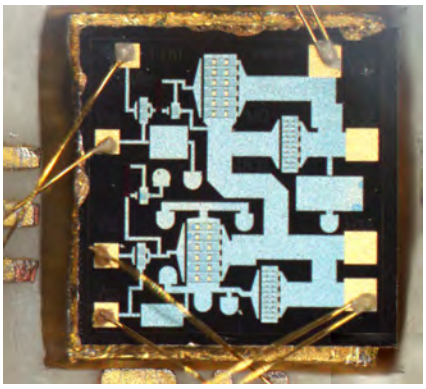

Figure 6.17: TQS Sw. Node

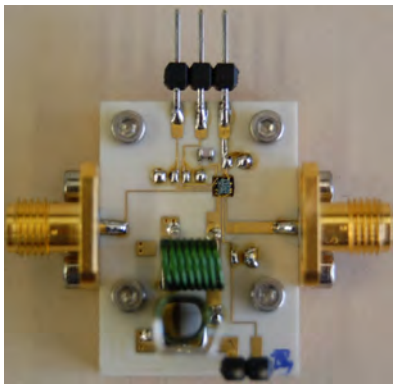

Figure 6.18: TQS Sw. Node PCB

It must be mentioned that the test jigs and the two PCBs onto which the passives were mounted with the hole cut for the MMIC were identical. Each MMIC layout was unique and the location of the voltage, control and supply nodes were different. However, with the use of appropriate bond wires, electrical contacts to the outside world were established.

6.2.5 Measured Results

High frequency, high resolution pulse-width modulated control signals are generated using an Agilent 81110A pulse generator, which is fed to a Hittie pulse driver amplifer (HMC870LC). These signals are level shifted using external, low frequency bias tees to the appropriate HS and LS PWM gate drive signals.

Figure 6.20 shows the control pulses PWM_{HS} and PWM_{LS}. The output signal is measured by connecting the output through an off-chip filter to a 50Ω high-speed Agilent DSOX3034A oscilloscope used in the time domain. As previously mentioned a fourth order filter with a 100 MHz cut-off frequency is used instead of the second order filter for higher attenuation at the switching frequency. The filter was designed using the

filter design and optimisation toolkit available in Microsoft AWR Office.

The efficiency was measured at 100 MHz, with a 30 V input voltage and at several duty cycle values and output power levels. The test setup diagram and a photo of the test bench is shown in Figure 7.43 and Figure 6.22 respectively.

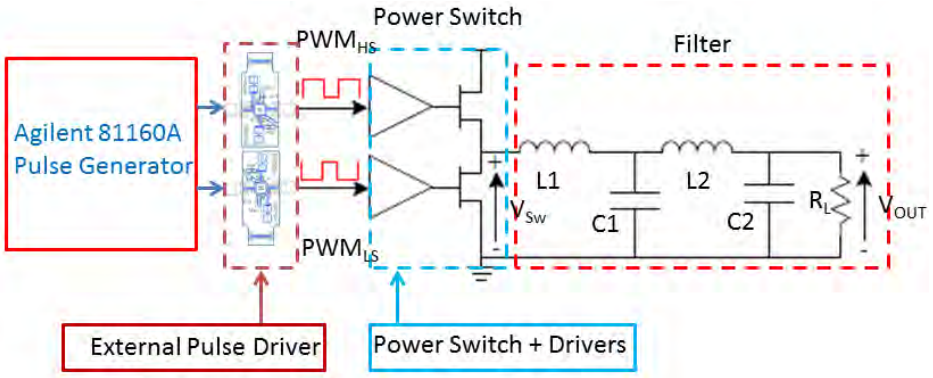

Figure 6.19: MMIC Measurement Schematic

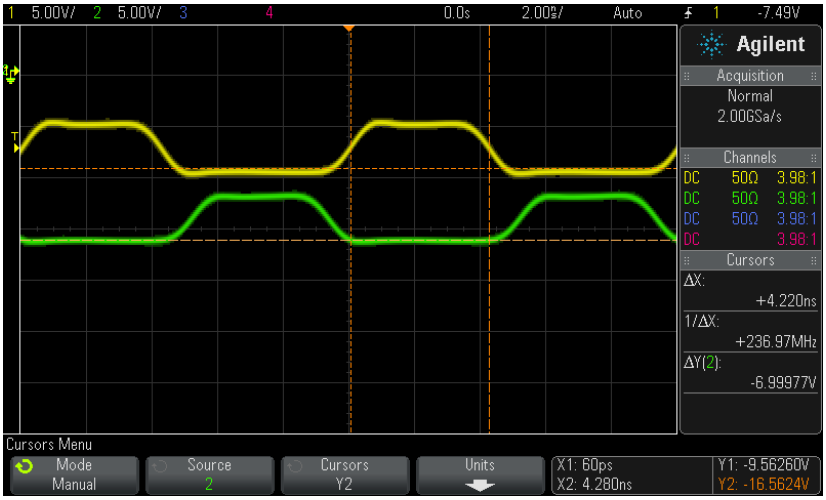

Figure 6.20: PWM Gate Driver Signals

The measured switch node output voltage waveforms for the bootstrap and switch node connected gate driver modulator are given in Figure 6.23 and Figure 6.24 respectively.

The voltage waveforms were extremely challenging to measure. Extremely short, shielded

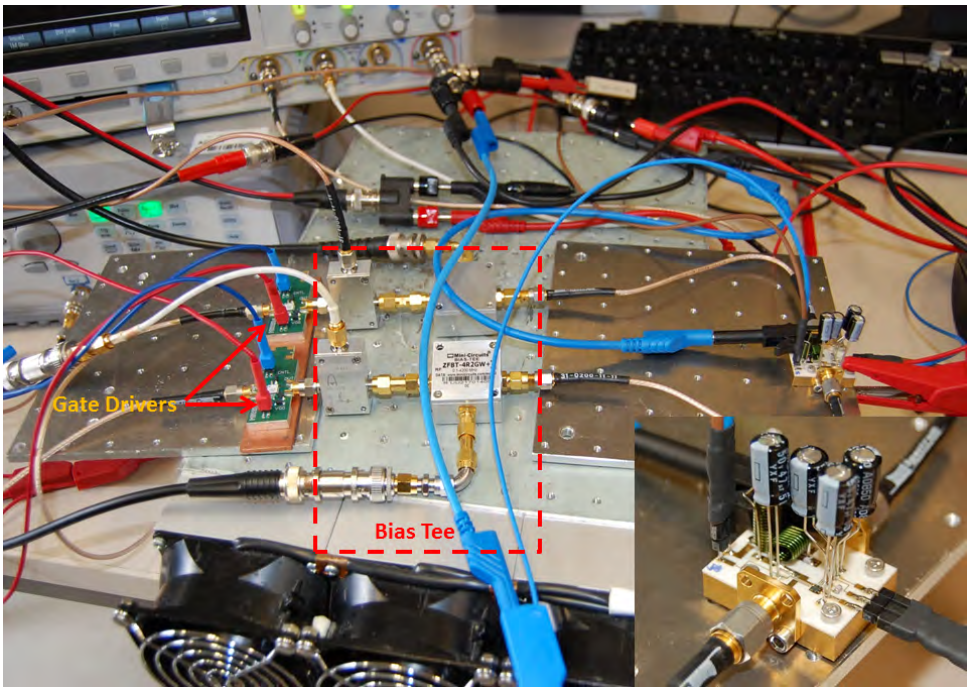

Figure 6.21: Photograph of MMIC Measurement Setup

measurement cables were used so as not to pick up any external noise spikes, and also the ground planes between the various power supply units, test jig back side, oscilloscope and pulse amplifier were connected together to a common node. The measured voltage waveforms show noisy spikes at the low voltage switching transition. Moreover the measurement probes also had a significant impact on the measurements, hence differential probes with a low capacitance were used. Moreover, proper shielding of the signals from the pulse amplifier was also seen to influence the switching behaviour due to timing errors forming a feedback loop and the noise coupling back into the measurement system.

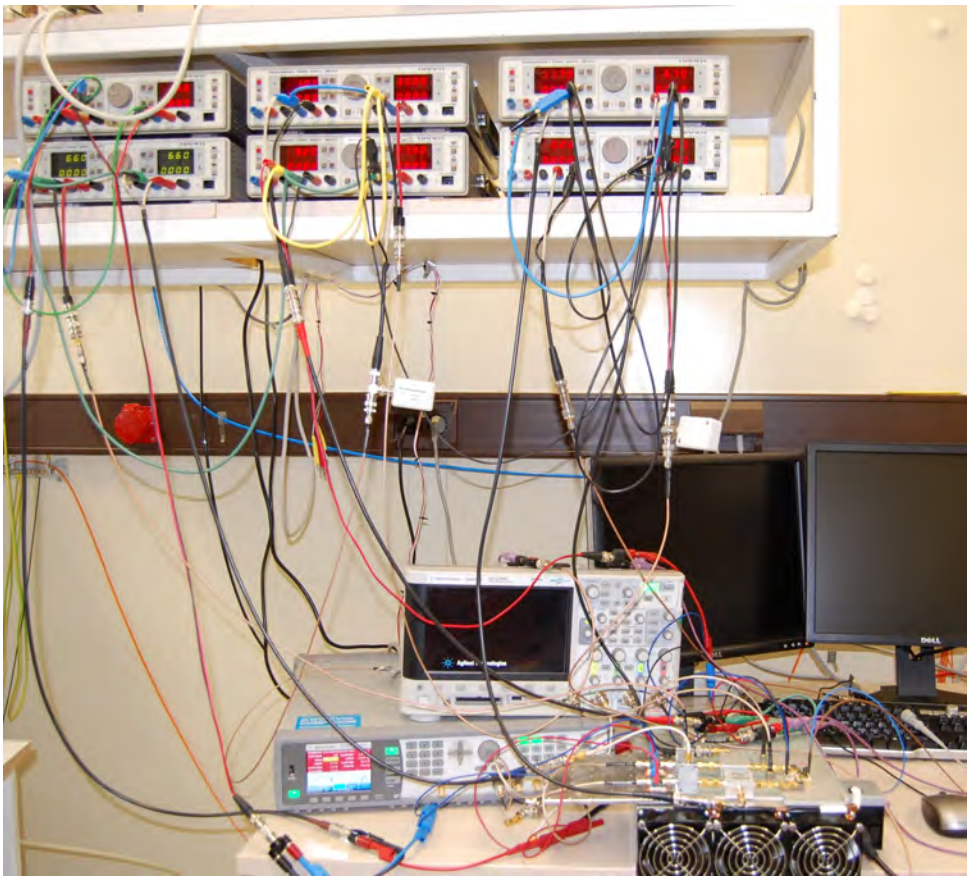

Figure 6.22: Photograph of the MMIC Testbench

6.2.6 Modulator Efficiency and Loss Analysis

An analytical loss model introduced in chapter 2 was used to estimate the efficiency and verified through comparisons with experiments. The model included AC and DC inductor loss calculated using manufacturer data, as well as conduction and switching loss in the HEMTs. Estimate of the dynamic R_{ON} based on pulsed IV data from chapter 3 was used to calculate the conduction losses. In addition the gate driver power loss was included in this analysis. The static power loss for the gate drivers can be found as the sum of the losses in the high side and low side power switch drivers. Table 6.5 details the simulated and measured gate driver losses for the two power switch driver

Figure 6.23: Bootstrap Modulator V_{SW}(V), D= 50%, P_{OUT}=36 dBm

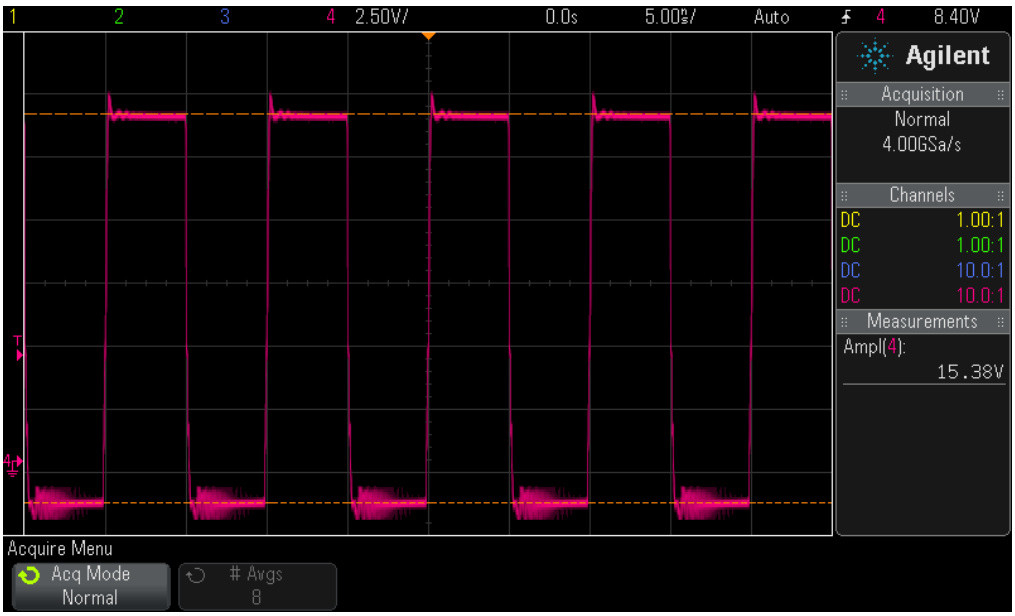

Figure 6.24: Sw. Node Modulator V_{SW}(V), D= 50%, P_{OUT}=36 dBm

topologies and at various duty cycles.

It must be mentioned that the models used for analysis are optimised for RFPAs using harmonic balance simulations. The mesured driver loss is higher than the sim-

Table 6.5: Comparison of Driver Losses

		Bootstrap	**Sw. Node**	
Duty Cycle	Sim (mW)	Meas (mW)	Sim (mW)	Meas (mW)
0.25	180	280	247	308
0.50	182	245	240	283
0.75	185	260	212	265

ulations, due to the fact that the trace capacitance of the microstrip lines, external connectors, packaging, etc all add to the external parasitics of the device. Hence the total capacitance is significantly higher than the power stage device capacitances. All these external parasitics were not considered during simulations, which assumed ideal transmission-line segments within the modulator circuit.

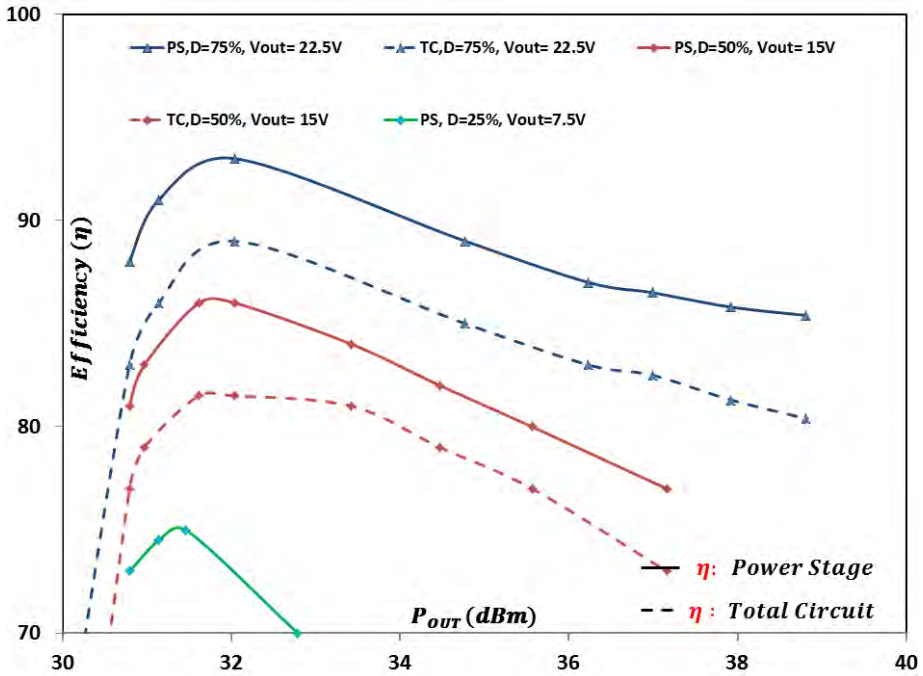

Figure 6.25: TQS Bootstrap Modulator Efficiency

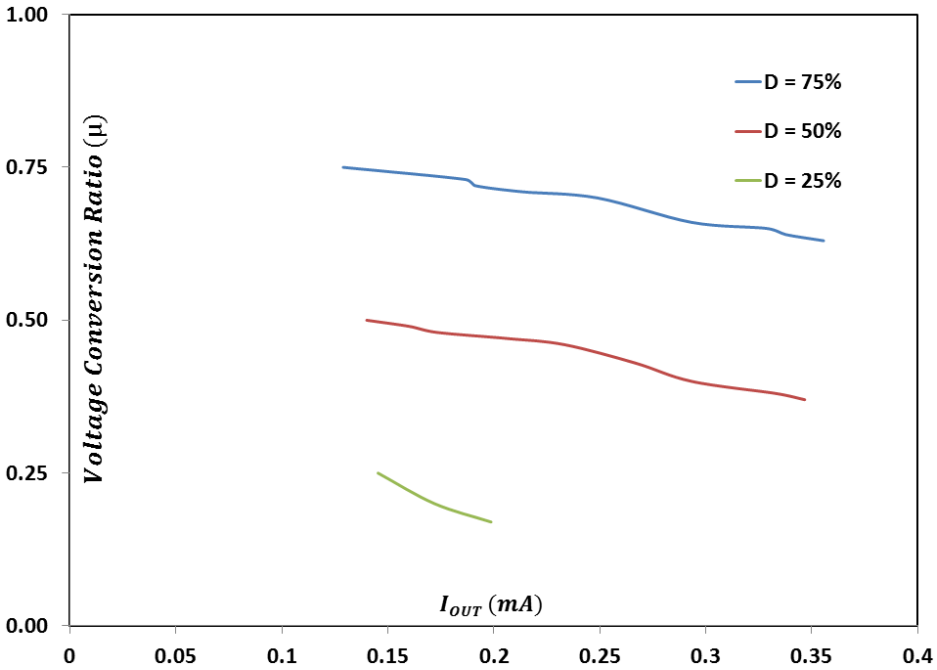

Figure 6.26: TQS Bootstrap Voltage Conversion

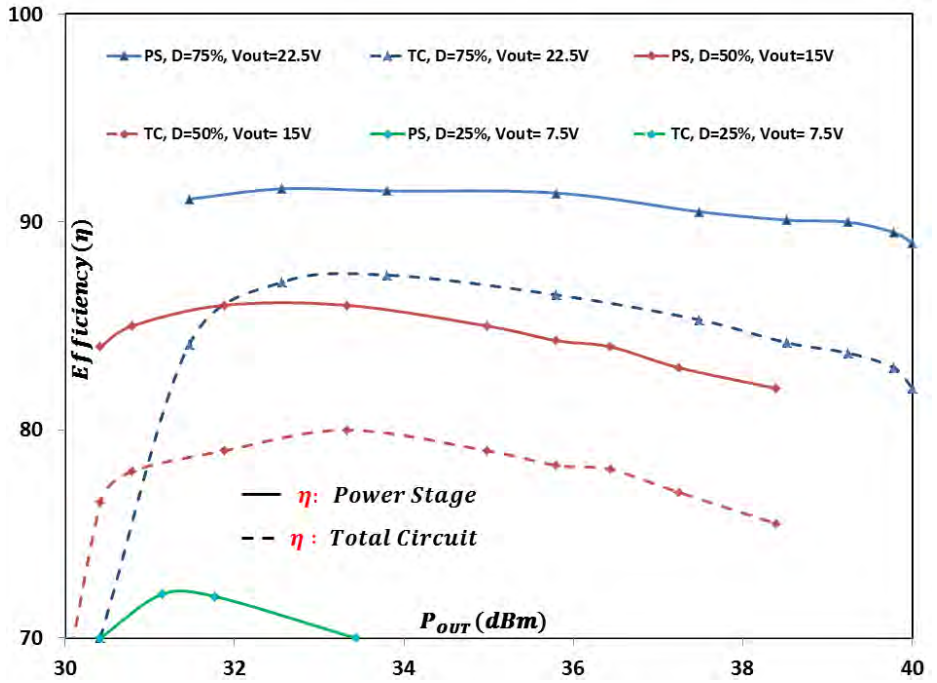

Figure 6.27: TQS Switch Node Modulator Efficiency

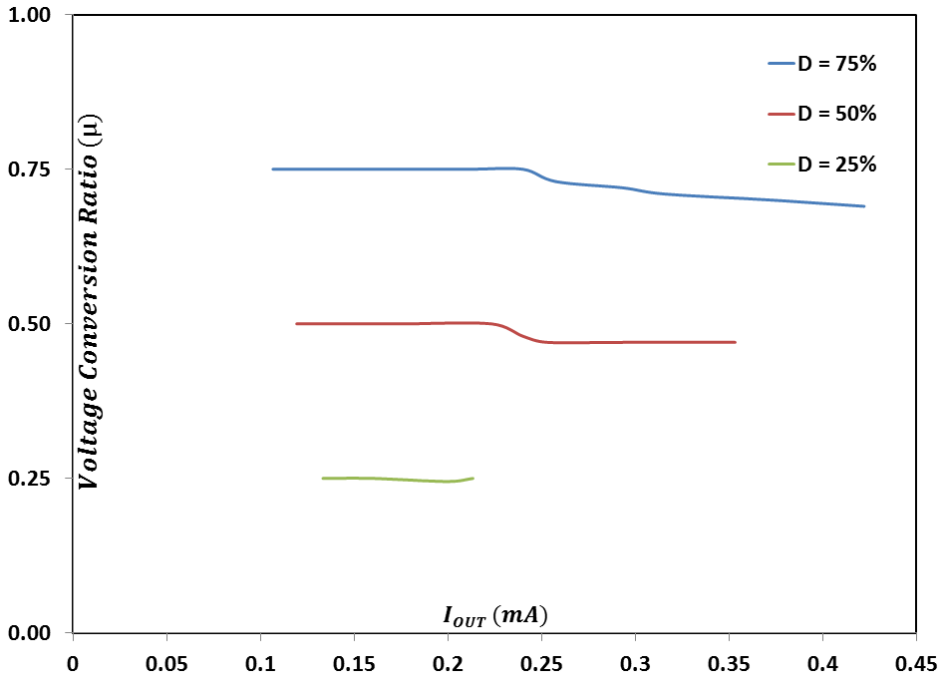

Figure 6.28: TQS Switch Node Voltage Conversion

6.3 Discussion

In this chapter, two integrated modulator topologies in 0.25 μm GaN MMIC processes have been fabricated and measured. While the two circuits share the same power stage, the predominant difference is in the high side driver topologies. The high side driver was optimised for low operating bias voltages. An ST-R-LT based bootstrap high side circuit delivers nearly 39 dBm of output power at an efficiency of 81.5% over wide range of resistive loading conditions, and the peak efficiency was 89%. The major drawback is the layout area taken up by the bootstrap capacitor, which makes implementation of the low side driver difficult. The problem of the bootstrap capacitor can be eliminated by using external capacitors.

The switch node connected ST-R-LT driver circuit had an efficiency of 83.5% over a

Table 6.6: Comparison of MMIC Modulators

Process	Topology	η (%)	P_{OUT} (dBm)	V_{DD}(V)
TQS	Bootstrap	81.5	39	30
TQS	Sw. Node	83.5	40	30

Table 6.7: State of the Art: GaN MMIC Modulators

Ref.	Topology	Process	P_{OUT}(W)	η(%)	Freq (MHz)	V_{DD}(V)
[107]	Pull-up	0.70 μm ME	1.9	64	200	20
[106]	Bootstrap	0.25 μm ME	3.3	73	200	30
[108]	Bootstrap	0.15 μm TQS	5	87.5	100	20
[108]	Pull-up	0.15 μm TQS	5	80	100	20
[109]	Sw. Node	0.15 μm TQS	7	83.5	100	20
This work	Bootstrap	0.25 μm TQS	8	80.5	100	30
This work	Sw.Node	0.25 μm TQS	10	83.5	100	30

wide range of resistive loads, and peaks at a maximum efficiency of 88.8%. The peak output power delivered was 40 dBm. Unlike the bootstrap driver topology mentioned earlier, the switch node connected driver design had both high and low side drivers. A summary of the MMIC modulator performance is given in Table 6.6.

Table 6.7 gives the state of the art in GaN HEMT MMIC power switches. These MMIC switches have been used as power supply modulators for efficiency improvement using envelope tracking in RF power amplifiers. In [92], a GaAs MMIC modulator with an efficiency of 83%, and switching at 150 MHz and delivering 3.3 W of output power under resistive loads, is demonstrated. A 1 GHz switching frequency GaAs MMIC modulator was demonstrated in [93]. However the output power delivered was only 0.860 W with an efficiency of 64.2% ; the higher voltage capability of GaN makes it superior for higher power applications.

In [106], an ET supply modulator using Mitsubishi Electric's 0.7 μm GaN process delivers 1.9 W of output power at an efficiency of 64%; the low efficiency is due to the

high power loss in the resistive pull-up topology of the high side driver, especially at low duty cycles. An improved, bootstrap design [107] using the 0.25 μm gate length process of the same foundry had an efficiency of 73%. The switching frequency in both designs was 200 MHz, while the drain bias voltage increased from 20 V to 30 V in the bootstrap circuit. The efficiency of the bootstrap topology was improved to 87.5% at an output power of 5 W in [108], using an external capacitor, at the expense of the low side driver, which could not be implemented due to space constraints in the MMIC layout. A resistive-pull up topology in the same technology delivered 5 W at 80% efficiency, and a modified high side driver based pull-up resistor topology described in [108] delivered around 7 W of output power with 88.5% efficiency. The same circuit was implemented as an ET supply modulator and tracked a 20 MHz LTE signal with an efficiency of 83.7% [109]. The MMIC modulators presented in this chapter had comparable efficiencies to the state of the art MMIC modulators, and delivered the highest output power.

Voltage conversion ratio plots are given in Figures 6.26 and 6.28, where the duty cycle D corresponds to the duty cycle of the PWM signals. As a result of losses, and other timing and dead time imperfections, the actual conversion ratio μ tends to drop when the load current is increased. Switch Node Connected driver topology exhibits the most favourable characteristics: flat conversion ratio curves with $\mu \approx$ D over the widest range of currents. A switch node connected ST-R-LT will enable simplification of control and signal pre-distortion techniques.

The major drawback in all the above mentioned GaN power switch topologies is the use of external bias tees to provide accurate voltage levels for the gate control PWM signals. This significantly complicates the test and measurement setup (especially at high supply modulator input voltages) with the need for precise external voltage levels

for the level shifting. This drawback can be overcome using integrated level shifter circuitry which can directly interface between the PWM control signal and the supply modulator without the need for external bias tees and voltage references outside the chip. The sizing of the integrated level shifters should be optimised to minimize power dissipation which might compromise the overall efficiency.

Even though the efficiencies of the two topologies are comparable, one of the major aspects of the design is the layout of the circuit. The area requirements during the layout of bootstrap capacitors in the high side driver make the implementation of the low side driver impossible. Moreover, an additional voltage node is required for bootstrap diode bias, and the traces for the external bootstrap capacitors complicate the driver circuitry. The switch node connected driver topology layout is very compact compared to the bootstrap layout and hence is a very good choice for integration with a HPA.

In this section, the results of the current work are compared to existing designs available in the literature. An OFDM modulated 4 W X-Band RFPA with a linear modulator and a combined efficiency of 34.8% is given in [128]. Here a switcher stage switches at 5 MHz, hence comparisons do not reveal true efficiencies. In [129], an X-Band RFPA is mated with an external supply modulator and delivers 1.1 W of RF output power at an overall PAE of 35.3% for a 20 MHz LTE-A signal. The envelope efficiency was 52.5%. The stand alone efficiency of the switcher stage within the envelope amplifier was 73.2% while delivering 7 W of output power into a resistive load of 8 Ω. The switch node connected ST-R-LT modulator fabricated in Triquint's process delivers a higher output power of 10 W at a better efficiency of 83.5%, showing the true potential of this work within an envelope tracking arrangement.

6.4 Conclusion

In this chapter two supply modulator circuits based on modified ST-R-LT gate driver topologies were introduced and fabricated for the first time in Triquint Semiconductor's 0.25 μm process. A bootstrap topology with a reduced high side gate driver voltage and a switch node connected high side driver which completely eliminated the need for the high side driver voltage were presented. The measured efficiencies of the modulators operating at a switching frequency of 100 MHz were over 80% while delivering 8 W and 10 W of output power. These circuits were fabricated in a GaN process optimised for RF circuits. Thus the potential for integration of the supply modulator and an RF amplifier on the same MMIC die can be explored and the switching frequency of the measured modulators can be used in envelope amplifiers within an envelope tracking system to accurately track a 20 MHz bandwidth LTE envelope signal.

6.5 Next

In the next chapter, two broadband RF power amplifiers designed in GaAs and GaN technologies are explored. The X-Band GaN HPA is integrated with a supply modulator and was fabricated in the Fraunhofer IAF 0.25 μm process.

7

Modulator Integrated RF Power Amplifier

7.1 Introduction

The power amplifier (PA) is one of the key components in the transmitter/receiver modules used in airborne radar or satellite communication systems. One of the major design issues of such a Tx/Rx system is the need for high efficiency, mainly related to the PA stage. Mature GaAs (Gallium Arsenide) MMIC (Monolithic Microwave Integrated Circuit) processes enable the integration of an amplifier and its associated driver functionalities into a single die with a view to minimise cost, improve reliabil-

ity and deliver repeatable high yield and performance in harsh environments. In this chapter two amplifier designs based on GaAs and GaN technology are investigated for X-Band applications.

In Section I of this chapter an X-Band PA based on WIN Semiconductor's 0.10 μm GaAs technology was designed and fabricated for radar applications.

In Section II, a two stage high power amplifier integrated with a supply modulator was designed and fabricated in 0.25 μm GaN technology for an X-Band Satellite downlink.

7.2 Section I: Broadband GaAs MMIC PA

7.2.1 GaAs Process Technology

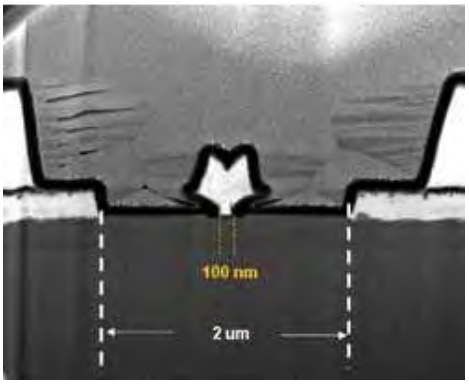

Figure 7.1: SEM cross-sectional image of 0.10 μm GaAs pHEMT

The power amplifier was fabricated in WIN Semiconductors 0.10 μm GaAs pHEMT (pseudomorphic High Electron Mobility Transistor) technology, PP-10. The critical dimension of the gate length was defined by a Leica direct-write E-beam lithography system and the PMMA/PMAA bi-layer was used for the T-gate shape, avoid-

ing the gain degradation at ultra-high frequency coming from the gate resistance. PP-10 was designed with single recess-channel geometry to achieve optimum current/transconductance characteristics while maintaining an adequate breakdown voltage for reliable 4 V operation [130]. The MMICs were fully passivated using silicon nitride deposited via PECVD and used as the dielectric for standard 400 pF/mm^2 Metal- Insulator-Metal (MIM) capacitors. A SEM image of Win Semiconductor 0.10 μm pHEMT is given in Figure 7.1 [130].

7.2.2 Device Technology

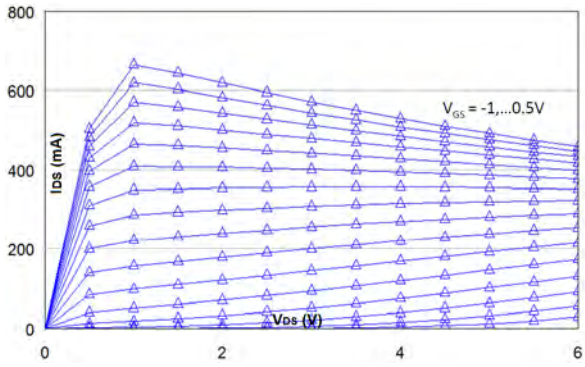

Figure 7.2: 12 × 75 DC I-V Curves

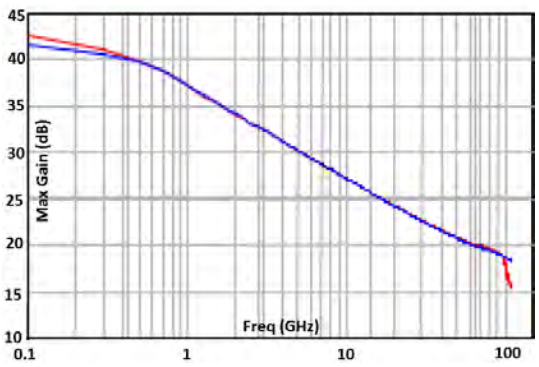

Figure 7.3: F_T v Frequency

A 12 × 75 μm pHEMT was chosen as the active element with the dc characteristic of the device given in Figure 7.2. The pinch-off voltage was around -0.95 V with an I_{DMAX} of 760 mA/mm at a gate voltage of 0.5 V. The corresponding transconductance achieved was as high as 750 mS/mm, with a knee voltage and gate-to-drain breakdown voltage of up to 1 V and 9 V, respectively. The f_T and f_{MAX} of the devices were 130 GHz and 180 GHz (Figure 7.3 [130]), respectively. The combination of high current density, large voltage swing and relatively low cost makes PP-10 the technology of choice for cost effective delivery of very high power density at X-Band frequencies.

7.2.3 Circuit Topology and Design

The power amplifier was designed using a reactively matched fundamental impedance for high efficiency similar to a Class-J PA. The Class-J PA mode consists of a new reactive impedance solution where fundamental and second harmonic output terminations can be matched in order to deliver constant (thus broadband performance) or even higher efficiencies than standard AB or B classes. While in the Class-J mode, both fundamental and second harmonic terminations have to be properly matched, but in this work only fundamental output termination is reactively matched while the second harmonic impedance is designed to be short-circuited. By short-circuiting the higher harmonics, better linearity in a satisfactory trade-off with power, gain and efficiency can be obtained.

As previously stated, for the single stage MMIC PA design a 12×75 μm GaAs pHEMT was chosen with the goal of maximising the power added efficiency (PAE), while delivering a gain greater than 10 dB at X-Band frequency. AWR Microwave CAD simulation tools were used to design and optimise the circuit. Load-pull analysis was performed using the models provided with the process design kit. The initial fundamental load-pull simulation was conducted at V_{GS} = -1 V (deep class-AB) and V_{DS} = 4 V whilst leaving the higher output harmonics at the 50 Ω reference impedance. Here, simulated DE, PAE, P_{OUT} and Gain of 45.6%, 42.2%, 22 dBm and 16 dB were respectively revealed.

After achieving these initial load pull simulations, the second harmonic output impedance termination was short-circuited and the source pull was performed with the input matched to deliver the highest PAE. In this case, conjugate matching of the input

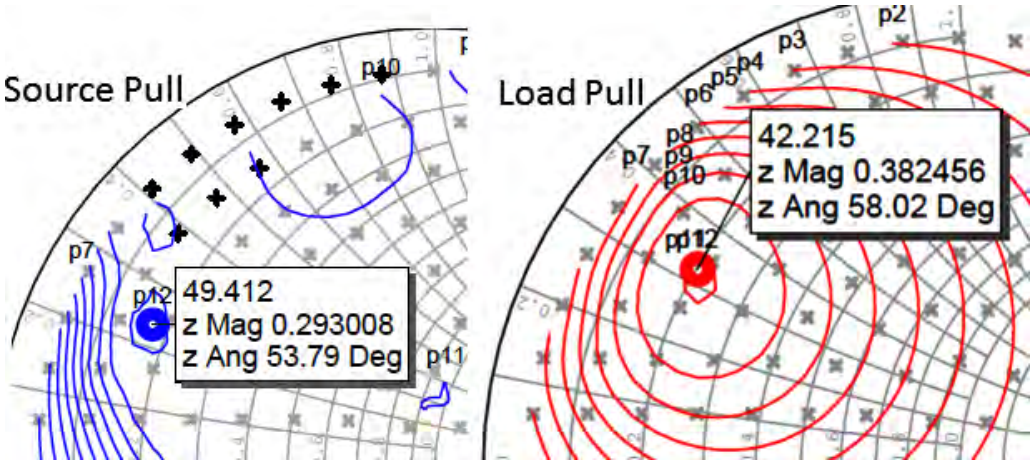

Figure 7.4: Source and Load Pull Contours

yielded a maximum PAE of 49.4% . The optimum load and source terminations are displayed in the Smith chart of Figure 7.4. For such optimum fundamental load and source impedances ($Z_{L,Fo}$, = 10.12 + j 16.22 Ω and $Z_{S,Fo}$, = 8.65 + j 11.82 Ω), the final simulated performance reveals: DE = 54%, PAE = 49.2%, P_{OUT} = 25.6 dBm and Gain = 17 dB.

Once the fundamental and second harmonic output terminations as well as the optimum source impedance have been determined, input and output matching networks were designed. Table 7.1 details the source and load impedance values for broadband matching.

The maximum available die area on the GaAs wafer was 2.4 × 2 mm and the design was laid out within this available area.

The circuit was designed using microstrip transmission lines, and a full 3-D electromagnetic simulation was done on the input and output matching networks using Microwave Offices Axiem simulator, as shown in Figure 7.5. The simulated drain current and voltage also revealed Class-J waveforms as shown in Figure 7.6.

Table 7.1: Broad Band Matching: Source and Load Impedances

Frequency (GHz)	Z_{Source} (Ω)	Z_{Load} (Ω)
6	10.65 - j 0.26	14.33 + j 2.64
7	9.92 + j 3.17	12.07 + j 5.59
8	9.43 + j 5.61	11.58 + j 7.82
9	8.73 + j 7.50	10.44 + j 11.36
10	8.65 + j 11.82	10.12 + j 16.22
11	7.88 + j 15.34	11.11 + j 19.22
12	7.83 + j 18.97	13.34 + j 20.16
13	9.75 + j 21.80	16.17 + j 19.05
14	12.16 + j 21.96	18.07 + j 16.13

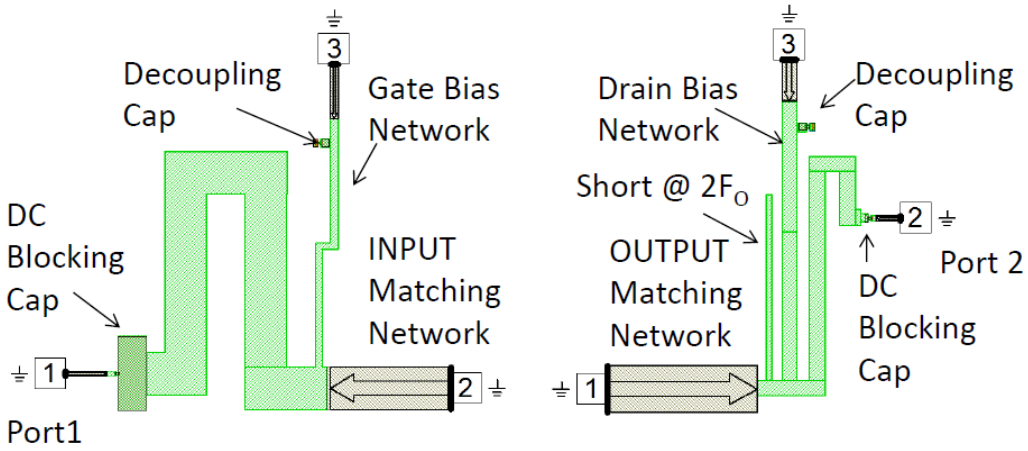

Figure 7.5: Input and Output Matching Networks

7.3 Measured Results

The fabricated GaAs Wafer was first wafer mapped using the measurement facilities available at Fraunhofer IAF. Figure 7.7 show a photograph of the fabricated MMIC.

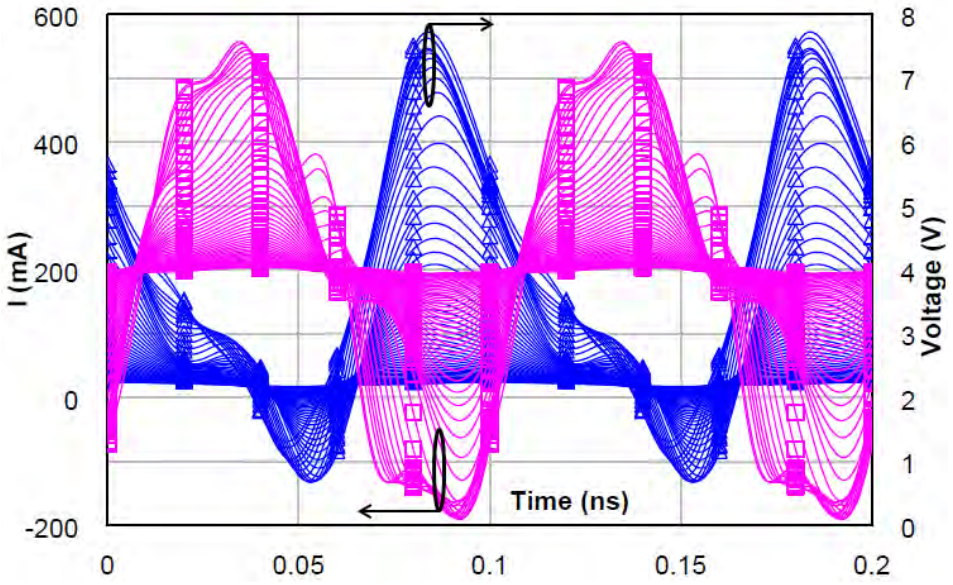

Figure 7.6: Simulated Drain Waveforms

7.3.0.1 Wafer Mapping Characteristics

The full wafer was mapped and S parameters were initially obtained. The S parameter data showed a very good yield with little spread as shown in Figure 7.8. The maximum small-signal gain, S_{21} of 18.5 dB was observed at 9 GHz. The corresponding S_{11} was around -10 dB.

a power sweep of all the cells also showed a good yield across the whole wafer as shown in Figure 7.9, with a variation in the measured PAE of around 8% from the maximum measurement to the minimum. A PAE of 56% with a maximum output power of 27.4 dBm and an associated gain of around 15 dB were measured.

A comparison of one of the measured wafer cells with the simulated amplifier performance at 9 GHz is shown in Figure 7.10. There is good agreement between the simulated and the measured DE, PAE, P_{OUT} and gain of the amplifier. The simulated

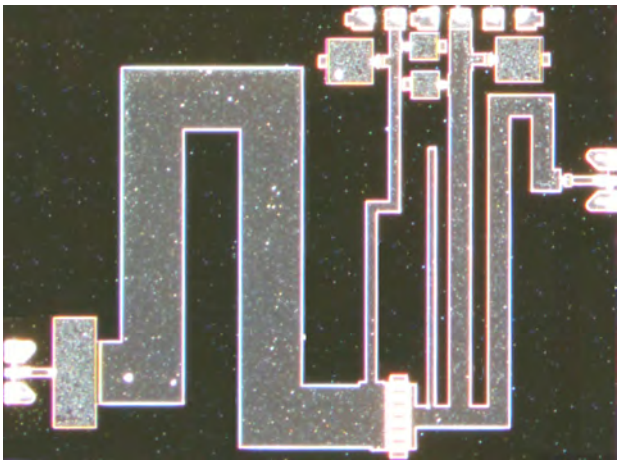

Figure 7.7: Chip Photograph of fabricated MMIC PA (2.4 x 2 mm)

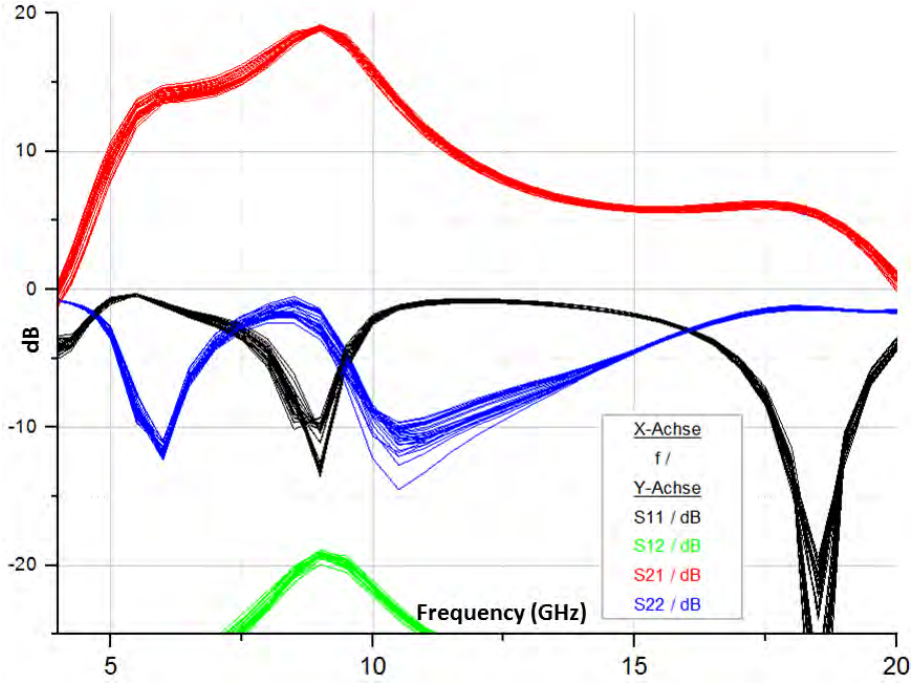

Figure 7.8: Wafer Mapping : S-parameters

DE and PAE were 60.34% and 54.85%, while the measured values were 59.14% and 55.1% for a P_{IN} of 16 dB. The output powers were comparable with a simulated output power of 26.8 dBm to 26.4 dBm for the measured cell. The measured gain at P_{IN} of 16 dB was 14.2 dB while the simulation showed a gain of 12.84%. The drain was biased at V_{DS} = 4 V while the gate bias was V_{GS}=-1 V.

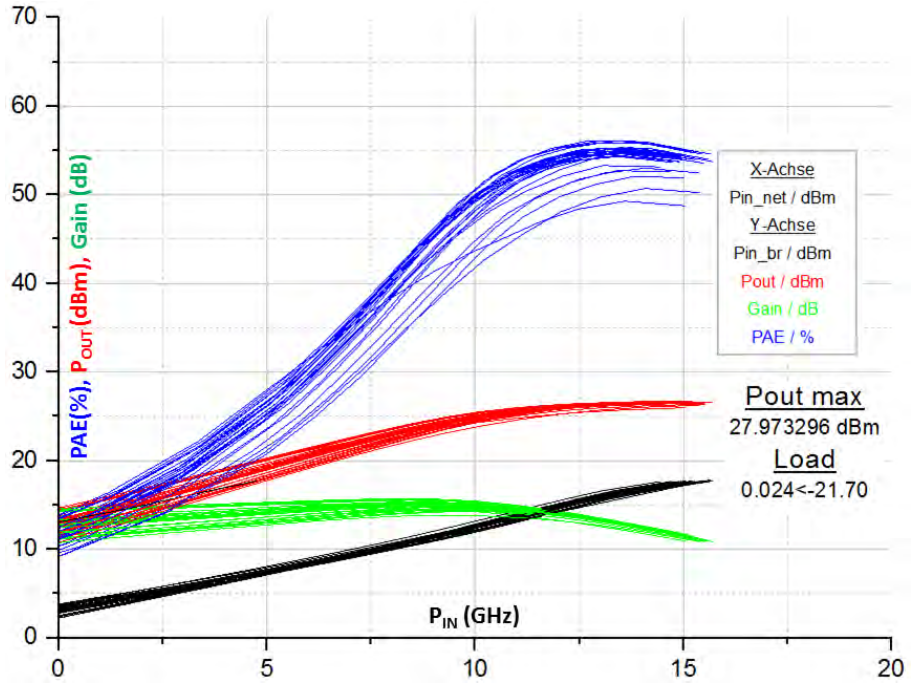

Figure 7.9: Wafer Mapping : Power Sweep

Figures 7.11 and 7.12 show the measured output performance in terms of the drain efficiency, output power and the gain function of the input power sweep for different frequencies from 6 GHz all the way up to 14 GHz in 1 GHz frequency steps. It can be clearly seen that the maximum DE of over 60% was seen from 9-11 GHz.

Figure 7.13 shows the broadband performance of the amplifier. The maximum DE of 68.2%, PAE of 62.91%, P_{OUT} of 27 dBm and a corresponding gain of 12.89 dB was measured at 10 GHz. The broadband characteristics of the amplifier are clearly visible, with DE over 50% from 7-13 GHz, a bandwidth of 6 GHz. The corresponding PAE remained over 45.31%, at the low end, while it was over 50% at 13 GHz. The corresponding output power remained over 23.86 dBm at 13 GHz, while from 7-12 GHz the output power was over 25.79 dBm, peaking at 27 dBm at 10 GHz. The corresponding gain remained over 10.4 dB from 7-12 GHz, falling to 9.23 dBm at 13 GHz.

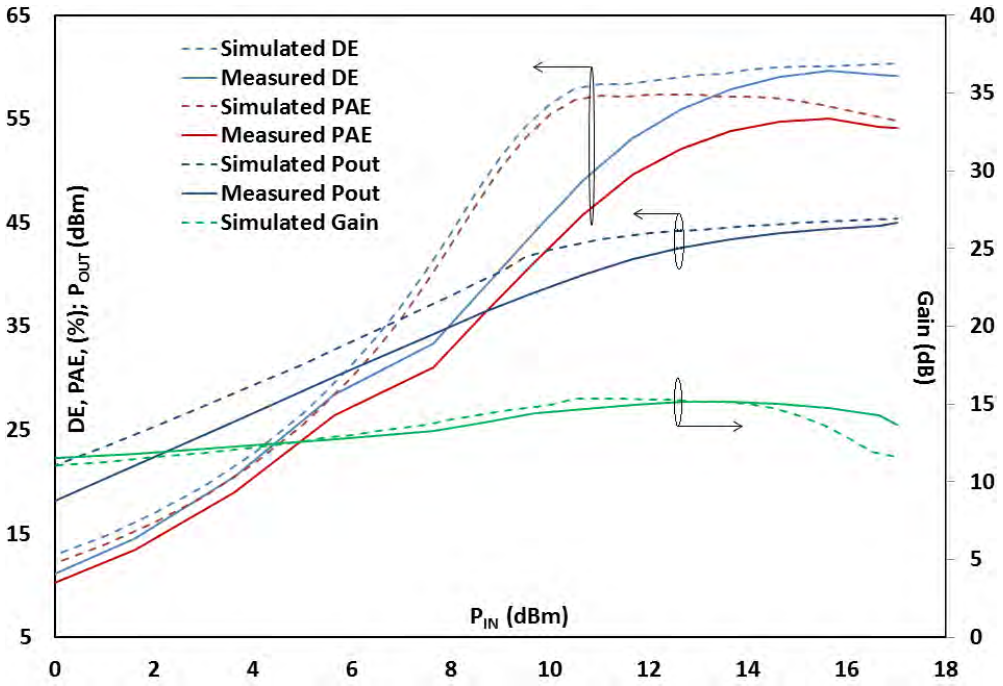

Figure 7.10: X-Band GaAs MMIC Comparison with Simulation

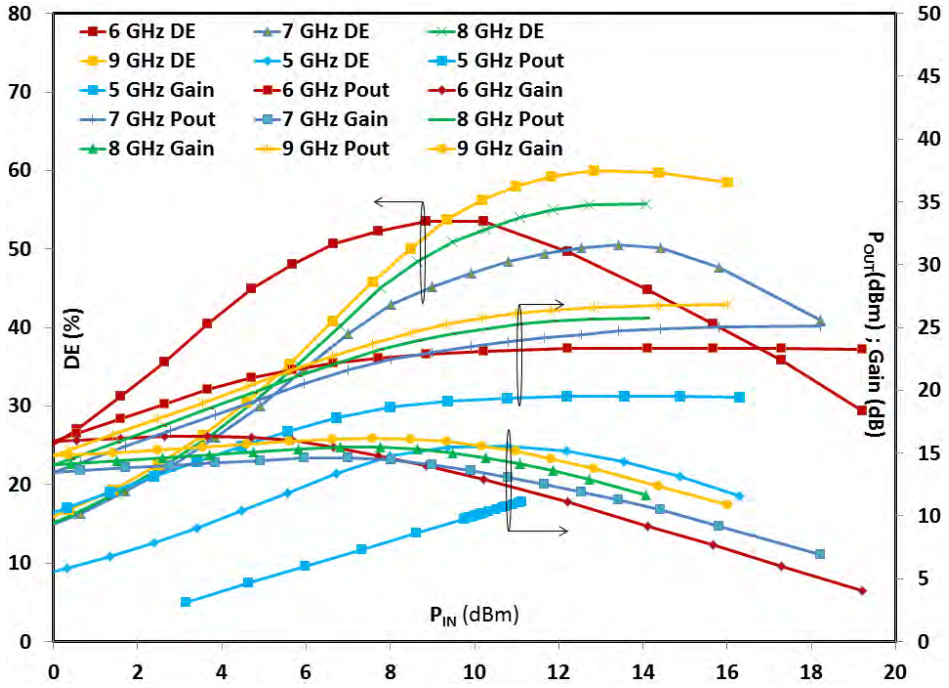

Figure 7.11: Power Sweep 5-9 GHz

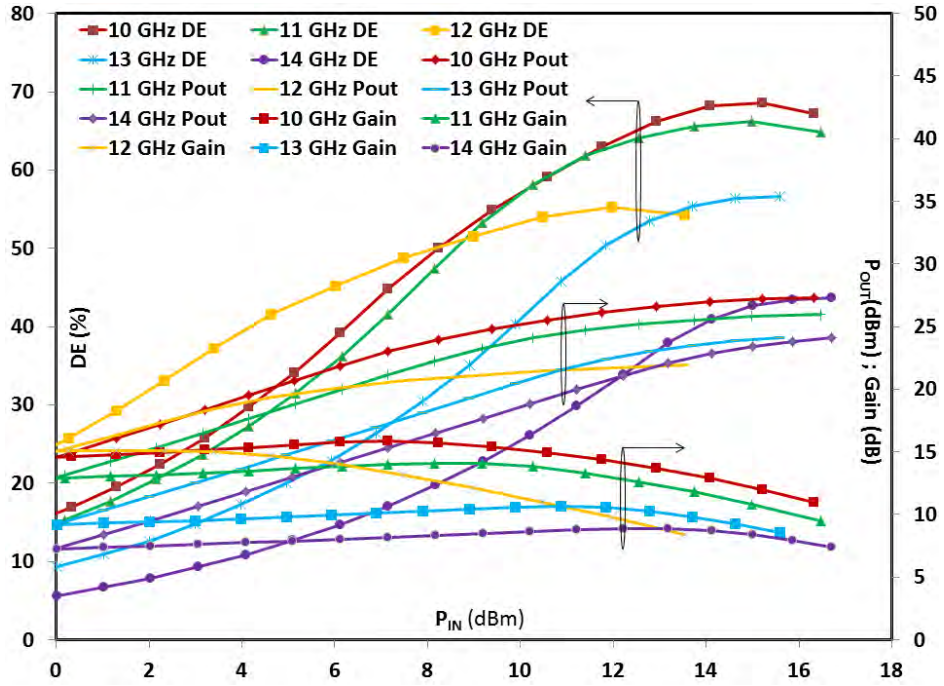

Figure 7.12: Power Sweep 10-14 GHz

The DE in the 9-12 GHz frequency range was about 55.79% while the PAE was above 51.02%. These efficiencies between 7-12 GHz are the highest reported drain and power added efficiencies for a bandwidth of 6 GHz.

In order to understand the performance of the amplifier with variations in gate and drain bias, it was subjected to gate and drain bias sweeps. Figures 7.14 and 7.15 show the measured DE, PAE, P_{OUT} and gain with bias variations.

In Figure 7.14, the drain voltage was varied from 2.4 V to 4.6 V; the performance of the amplifier was extremely stable with DE peaking at 71.02%, and a PAE of 64.16% for drain bias between 3.2 V and 3.4 V, while the output power was 26 dBm with a gain of 11 dB. The gate voltage was held at V_{GS} = -1 V and the frequency was 10 GHz.

The influence of the gate bias on the amplifier performance for V_{DS} = 4 V and a fre-

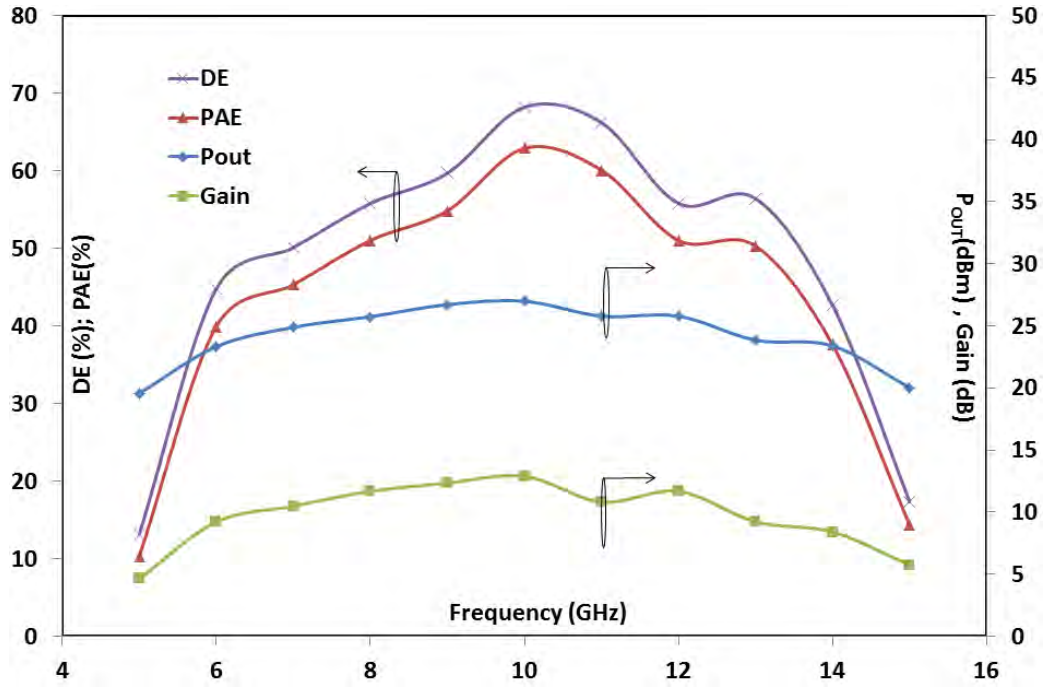

Figure 7.13: X-Band 0.10 μm GaAs MMIC Frequency Sweep

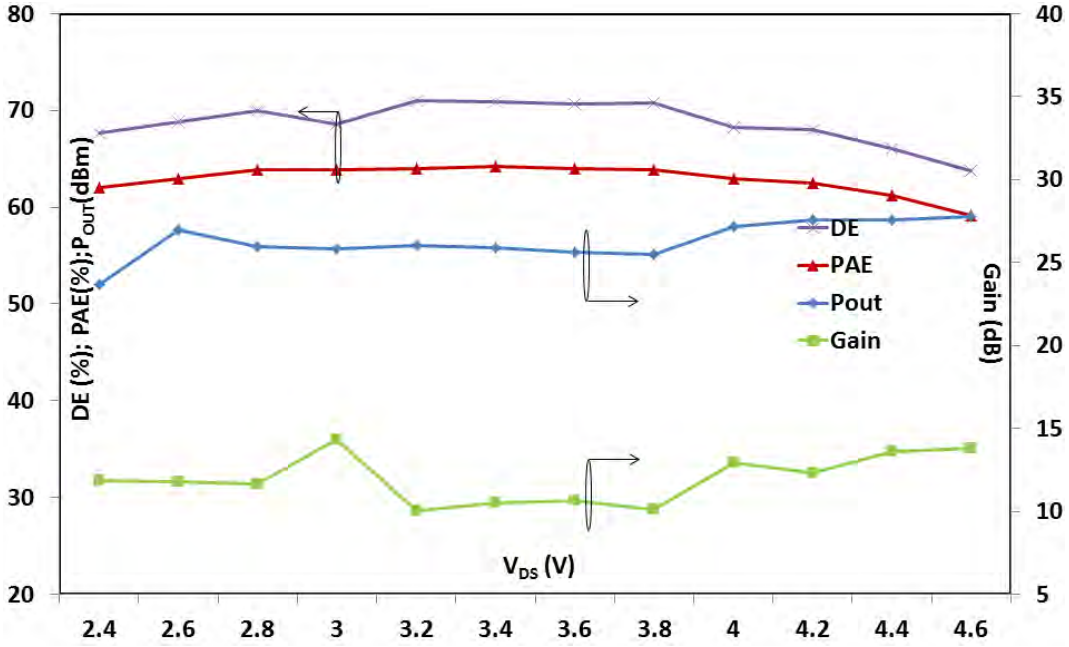

Figure 7.14: V_{DS} Sweep

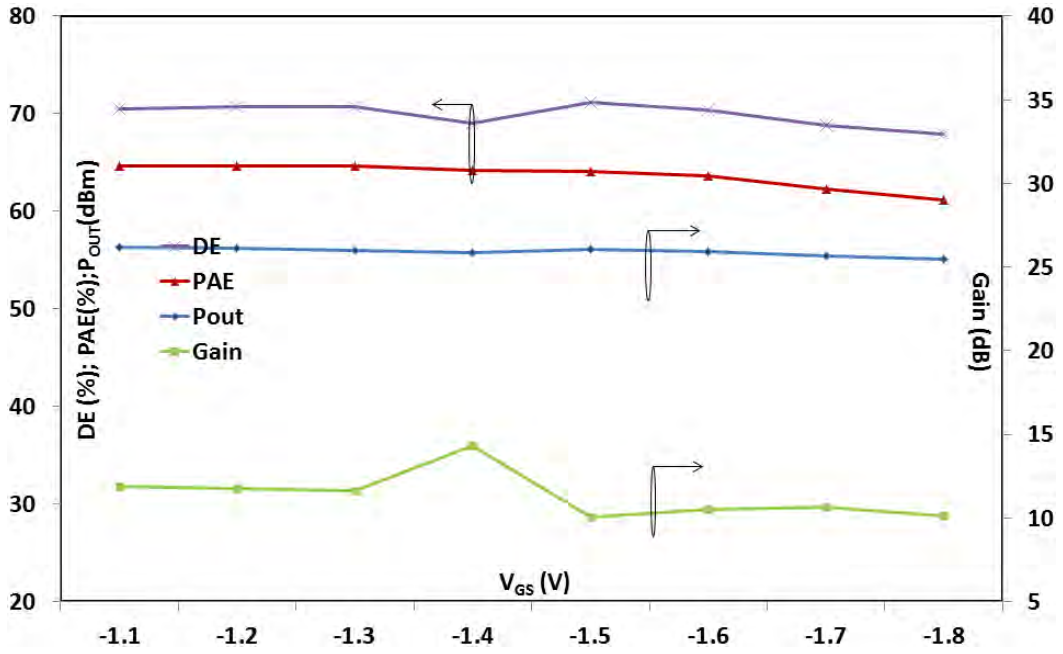

Figure 7.15: V_{GS} Sweep

quency of 10 GHz is given in Figure 7.15. A maximum DE of 71.2% and a PAE of 64.13% were measured at V_{GS} = -1.5 V. The measured output power was 26.04 dBm and the gain was 10.04 dB.

7.4 Discussion

A high-efficiency X-band MMIC power amplifier was designed, fabricated and tested on a pHEMT 0.10 μm GaAs process. A reactively matched Class-AB topology was chosen and both the input and output matching networks were optimised for highest PAE using commercially available CAD tools. Excellent performance was achieved with a saturated output power of around 0.55 W, a drain efficiency as high as 68.2% and a power added efficiency of 62.91%, with a small signal gain of 18.5 dB and a large-signal gain of 12.89 dB.A review of the literature (Table 7.2) revealed that most

Table 7.2: X-Band GaAs MMIC HPA

Ref	GaAs Process	P_{OUT} (dBm)	Freq (GHz)	PAE (%)	Gain (dB)	No.of Stages	Periphery L_GxW_G
[131]	Selex SI 0.4 μm	38	9-10.2	38	17	2	$8 \times 12 \times 125$
[132]	0.30 μm	24	9-11.0	40-63	10	1	0.6
[133]	0.3 μm RFMD	27.2	7.5-11.5	65 (DE)	5	1	0.6
[134]	0.25 μm	37	7.5-10.5	55 (DE)	14.4	2	10
[135]	0.25 μm Filtronic	37	9.5-10.6	53	17	2	$8 \times 10 \times 120$
[136]	0.3 μm IAF	36	9-11.5	25	18	2	$8 \times 8 \times 125$
[137]	0.25 μm Raytheon	35	7.4-8.4	50-60	24	3	$4 \times 12 \times 150$
[138]	0.25 μm Win Semi	40	8.25-10.25	41.4	20	2	$16 \times 4 \times 250$
This work	0.10 μm Win Semi	>23.86 (27 dBm)	7-13	>45.31 (62.91)	>10.82	1	12×75

of the published X-Band GaAs MMIC amplifiers were fabricated in 0.25 μm or larger process. This broadband amplifier has one of the highest DE and PAE achieved for a 0.10 μm GaAs MMIC PA at X-Band.

GaN technology delivers over 5 times the output power of GaAs devices. Moreover, drain bias modulation techniques can be used to improve the RFPA efficiency. In the next section a GaN HPA with an integrated supply modulator is explored for airborne and space based systems.

7.5 Section II: Broadband GaN MMIC HPA

Modern GaN Tx/Rx MMICs have shown an impressive performance compared to existing GaAs designs, with projected cost savings upto 40% per Tx/Rx module compared to GaAs [118]. The foremost benet with a fully integrated AlGaN/GaN transceiver front-end is that both size and weight are reduced signicantly [5], [139]. One of the principal requirements for airborne radar or space based PAs is the need for very high efficiency to minimize power consumption, very high linearity, as well as the reduction of system size and weight. A promising approach to improve the DC-RF power conversion of the system is to implement a dynamic drain supply modulator for each RFPA. The design of a high efficiency supply modulator becomes the key to the success of energy efficiency enhancements because the overall ($\eta_{overall}$) combined efficiency depends on both RFPA and supply modulator (SM) efficiencies given by

$$\eta_{overall} = \eta_{RFPA} \times \eta_{SM}. \tag{7.1}$$

To maximise the performance the supply modulator has to be placed close to the functional blocks to limit the interconnect parasitics, particularly when providing high current and voltage levels. Ideally the supply modulator should be integrated in the same process technology as the different functional blocks.

In this section, the technology potential of a supply modulator integrated space qualified RFPA is investigated. The switch node connected modulator topology and the X-Band HPA were implemented in the Fraumhofer IAF 0.25 μm GaN process for satellite telemetry systems. The two-stage X-Band MMIC HPA, designed and presented in

[140], has been here used as a first step for the realization of a supply modulator based high efficiency HPA.

This section describes the design and simulation of the supply modulator, as well as the integration of supply modulator into the existing HPA layout. The subsequent stand alone measurements and supply modulator integrated HPA characterization and its wider implications is also explained in detail.

7.5.1 GaN Process Technology

The GaN 25 process is a 0.25 μm gate length technology optimised for MMIC applications between 6 and 18 GHz. The AlGaN/GaN heterostructures are grown on semi-insulating SiC substrates by MOCVD with sheet resistance non uniformities of better than 2%. The growth procedure is optimised for both a highly insulating buffer as well as low trap densities. Processing is performed in microstrip transmission line technology consisting of front side processing, substrate thinning to 100 μm, and backside processing including the front-to-back substrate via holes [141], [142]. The MMICs feature thin film resistors, high-voltage capacitors and inductors for impedance matching to a 50 Ω environment.

Device fabrication is performed using standard processing techniques involving electron-beam and optical lithography: stepper alignment for front-side and contact mask alignment for back-side device definition. Special attention is paid to performance and reliability optimisation, which is mainly achieved by a combination of epitaxial growth optimisation as well as modifications in the passivation and gate modules. The process technology exhibits good uniformity across a single wafer as well as high re-

producibility from wafer [143].

In the course of this work, all AlGaN/GaN HEMTs are processed with the GaN25 process of the Fraunhofer IAF with a 0.25 μm gate length technology that is optimised for X-/Ku-band monolithic microwave integrated circuit (MMIC) applications from 6 to 18 GHz. In addition, the standard FET used within this work offers a gate geometry of 8 × 125 mm (number of gate-fingers × gate-width) with a gate-to-source spacing of 1 mm and a gate-to-drain spacing of 3.5 mm and with a gate-to-gate pitch of 50 μm. The AlGaN/GaN heterostructures are grown on semi-insulating SiC substrates by Metal Organic Chemical Vapor Deposition (MOCVD).

7.5.2 Device Characteristics

This section gives the measured DC and RF characteristics of a 8 × 125 mm AlGaN/GaN HEMT at X-band. The representative DC I-V characteristics of a 1 mm device is depicted in Figure 7.16. The DC I-V characteristics were measured up to V_{DS} = 60 V with V_{GS} = -4 . . , 2 V. A maximum drain-source current of approximately 840 mA/mm was obtained which is related to an aluminium mole fraction of 22% for this technology.

DC-to-RF dispersion causes a knee walkout and degrades the available output power. However, these effects have been minimised with technology progress over the years.

Figure 7.17 shows the measured DC transconductance g_m of the same device sample. The transconductance shows an asymmetric behaviour, i.e. a sudden rise near turn-on independent of V_{DS}, followed by a smooth decrease toward g_m = 0 mS for V_{GS} > 1V that becomes stronger for higher drain bias voltages. A maximum g_m of 310 mS/mm was measured at a drain bias voltage of 10 V with V_{GS} = -1.75 and 285mS/mm at V_{DS}

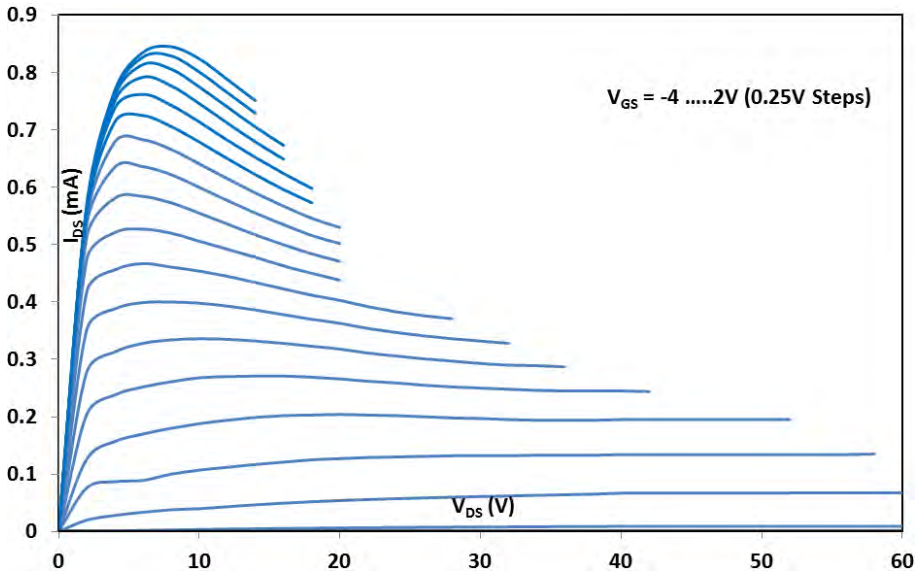

Figure 7.16: 8 x 125 -IV Characteristics

= 30 V with V_{GS} = -1.75 V, leading to correlating drain currents of 100 mA.

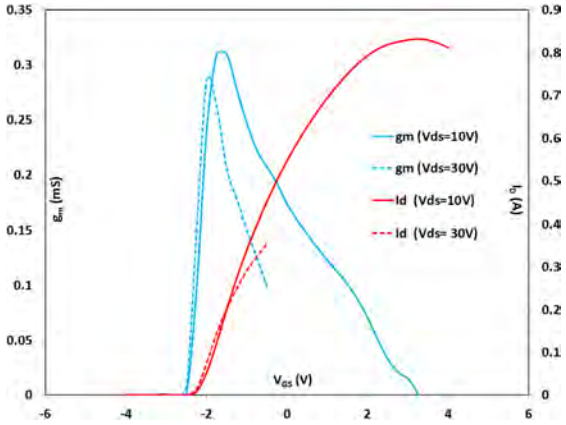

Figure 7.17: g_m v V_{GS}

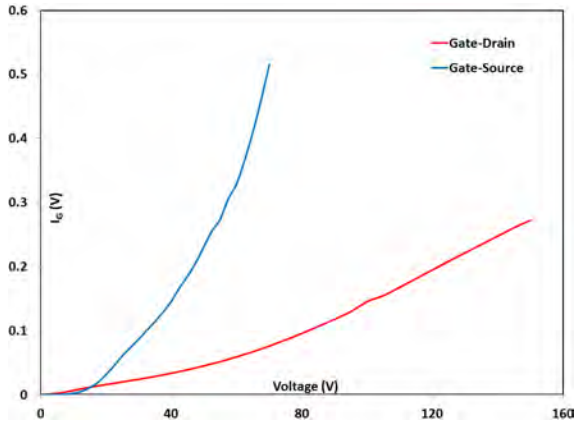

Figure 7.18: Breakdown I-V

The complete channel pinch-off is at about -2.5 V independent of the drain bias voltage. In addition, the gate-source and gate-drain breakdown behaviour of the 0.25 μm HEMT were taken at an operating temperature of 150 °C. Mostly, the gate-drain breakdown voltage is above 100 V. Figure 7.18 shows the breakdown behaviour of the reverse biased gate-drain and the gate-source diode for a 8 × 125 mm AlGaN/GaN HEMT device from the same wafer. Both the gate-drain and the gate-source break-

down behaviour were not measured up to breakdown. Nevertheless, the gate-source breakdown behavior of the measured transistor show a strong increase in gate leakage current of up to 0.5 mA at 70 V. Therefore, the expected gate-source breakdown voltage causing a gate leakage current of 1 mA/mm is about 80 V; in addition, a breakdown voltage for the gate-drain diode that is larger than 150 V.

The device also shows high cut-off frequencies that are extrapolated from the measured small-signal current gain h_{21} and maximum stable gain (MSG)/maximum available gain (MAG) curves as shown in Figure 7.19. An extrinsic transit frequency of f_T = 30 GHz and an extrinsic maximum frequency of oscillation of f_{MAX} = 42 GHz were obtained at V_{DS} = 30 V.

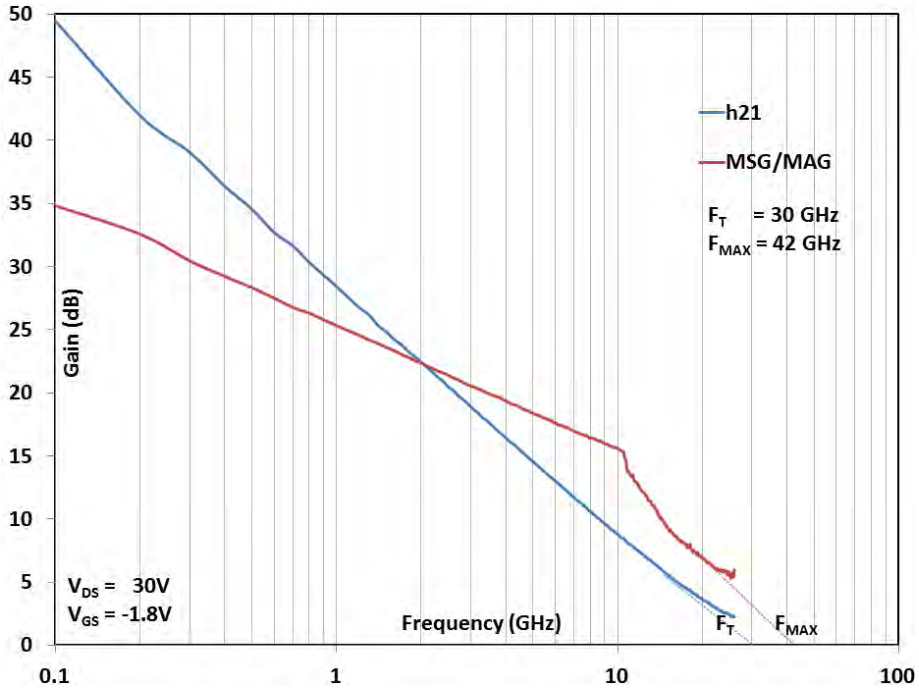

Figure 7.19: H_{21}, MSG/MAG

Table 7.3: HPA Transistor Size

P_{T1},P_{T2}	P_{D1},P_{D2}	ST_H,ST_L	LT_H,LT_L	R1	R2
20x200μm	20x100μm	4x25μm	4x50μm	100Ω	75 Ω

7.5.3 Circuit Topology

The HPA is a two stage amplifier; the first stage has a size of 85 × 8 μm. The second stage consists of 2×125 × 8 μm. The design requirements include a high power and high PAE performance at a low compression level of -2 dB in CW operation at a drain voltage of V_{DS}= 28 V. Here, an output power of approximately 37 dBm and a PAE of above 35% with an associated gain ≥20 dB is aimed at, with a 2 GHz bandwidth from 8 GHz up to 10 GHz.

The input, output and interstage networks are conjugately matched. Full details of the circuit topology and the matching networks are given in [140]. Table 7.3 gives the HPA transistor sizing.

7.5.4 HPA Simulated Results

The simulations presented in this section were undertaken by Dr Jutta Kuhn and the results were published in [140].

Figure 7.20 shows the simulated S-parameters of the HPAs. The small-signal gain is ≥ 20 dB for a frequency range from about 7.5 GHz up to 10 GHz. A maximum S_{21} of 28 dB was observed at 8 GHz. S_{21} starts dropping off sharply beyond 10.1 GHz.

The input reflection coefficients S_{11} and S_{22}, over the entire 8-10 GHz bandwidth, were

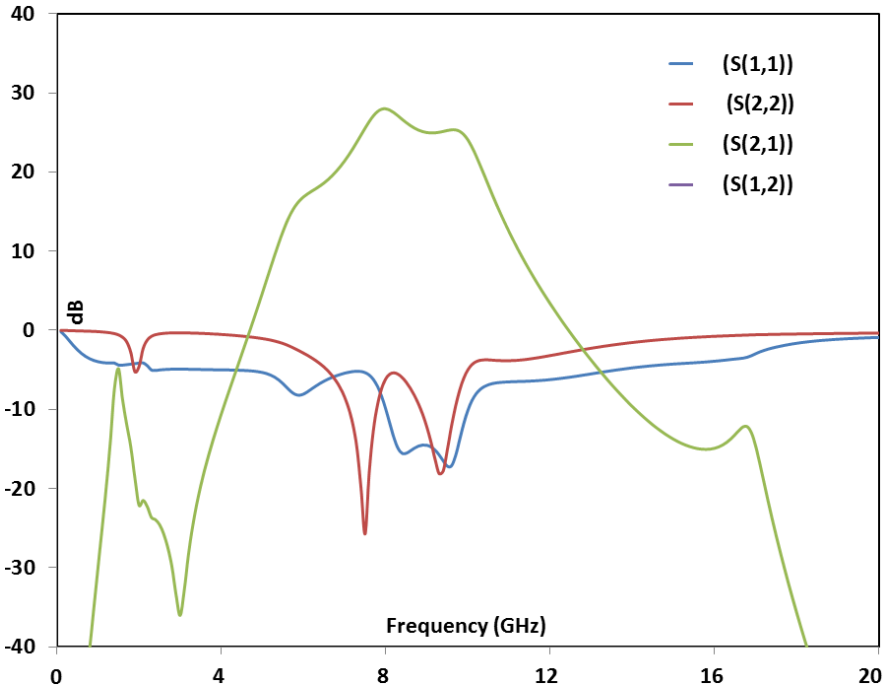

Figure 7.20: Simulated S-Parameters

below -9.92 dB and the output reflection coefficient S_{22} was below -5.37 dB. The drain was biased at V_{DS}= 28 V and I_{DS}= 100 mA.

Large-signal simulations were also done at the same bias conditions. The power-sweep results at a frequency of 8.5 GHz are shown in Figure 7.21. The drain efficiency and PAE are 45.2% and 42.7% respectively. The simulation revealed an output power of 38.8 dBm in compression at P_{IN}= 22 dBm, and a corresponding gain of 17.1 dB.

The amplifier performance over 8-10 GHz with 28 V drain bias is given in Figure 7.22, the DE, PAE, P_{OUT} and Gain over the whole bandwidth is ≥35.2%, ≥34.70%, ≥37.0 dBm and ≥17 dB respectively.

The broadband performance of the amplifier over 8-10 GHz with 20 V drain bias is given in Figure 7.23; the DE, PAE, P_{OUT} and Gain over the whole bandwidth are ≥

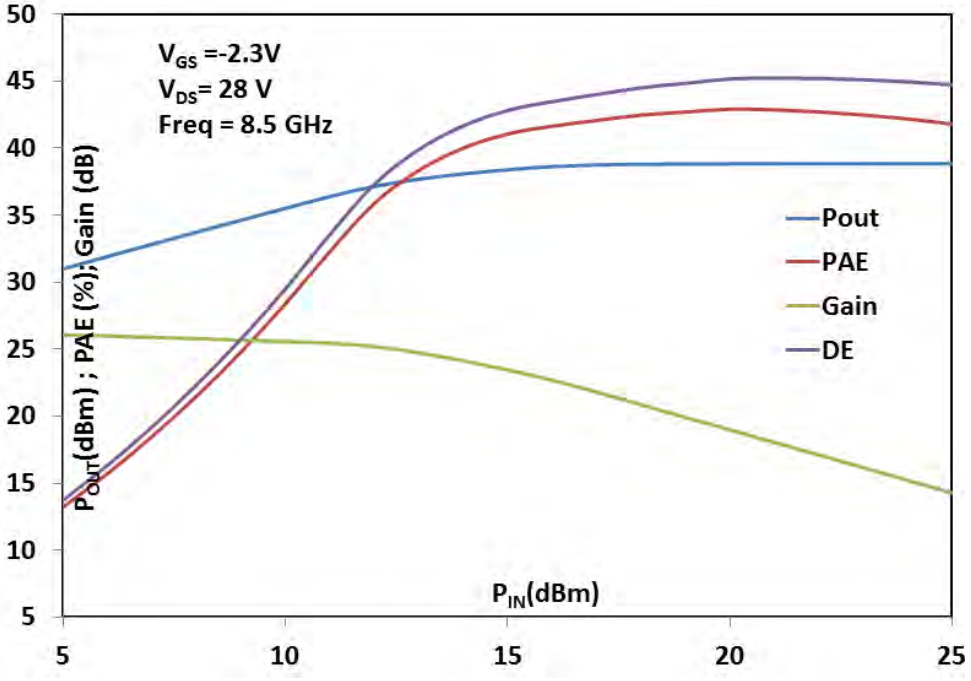

Figure 7.21: Simulated Power sweep

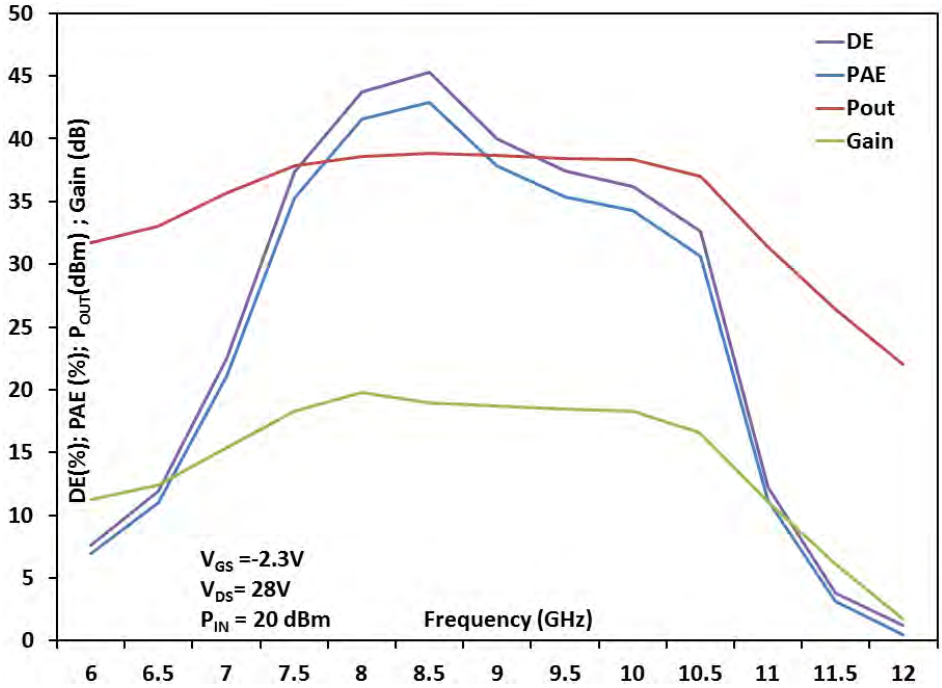

Figure 7.22: Simulated broadband sweep (V_{DS} = 28V)

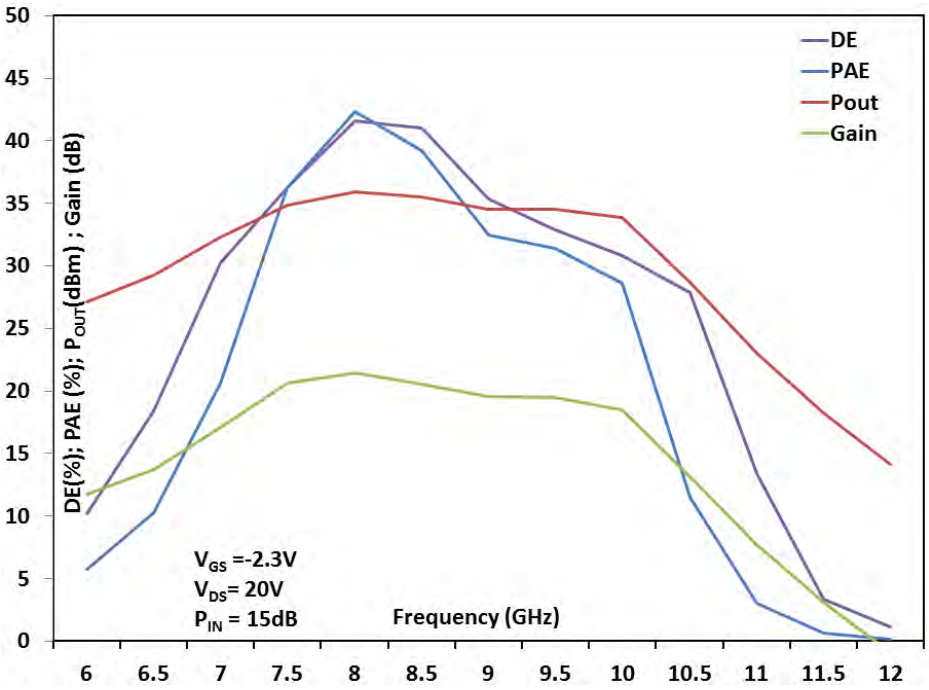

Figure 7.23: Simulated broadband Sweep (V_{DS} = 20V)

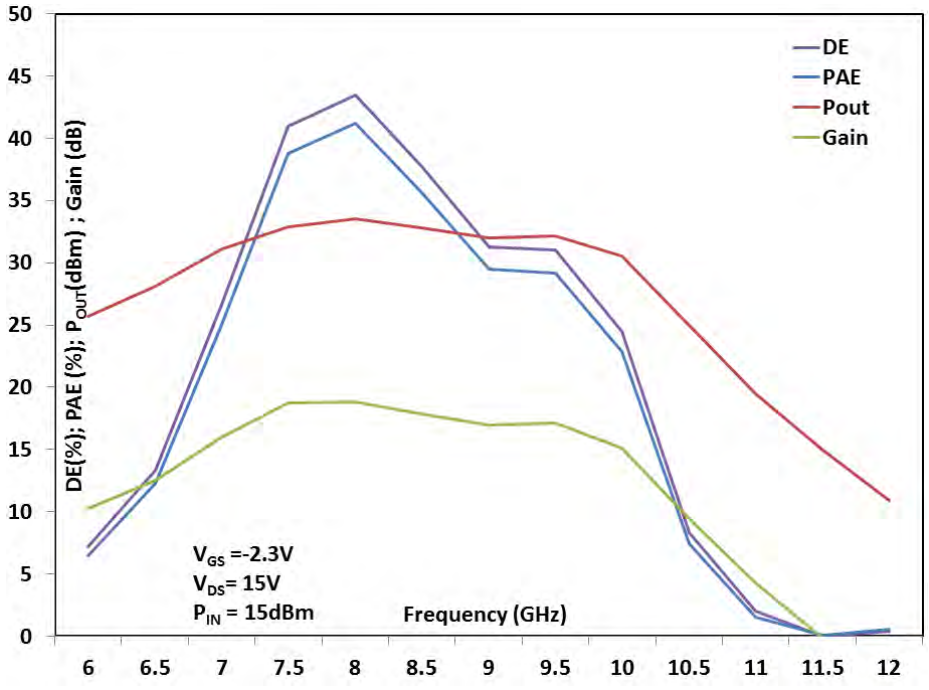

Figure 7.24: Simulated broadband sweep (8.5 GHz, V_{DS} = 15V)

30.8%, ≥ 28.60%, ≥ 33.80 dBm and ≥ 18.5 dB respectively. A degradation in performance is seen towards the higher end of the frequency bandwidth.

Subsequently, the drain voltage was changed to 15 V and the measured DE, PAE, P_{OUT} and Gain over the whole bandwidth are ≥24.40%, ≥22.80%, ≥30.60 dBm and ≥15.1 dB respectively as shown in Figure 7.24.

7.6 Supply Modulator

7.6.1 Circuit Topology

The switch node connected ST-R-LT driver topology was chosen as the integrated supply modulator circuit as in Figure 7.25. The topology and the circuit operation were already introduced in the previous chapter. The design was further optimized for integration with the HPA, and the power transistor size was increased to 10×300 μm while the diode size was 10×150 μm. The switching transistor ($ST_{H/L}$) and the load transistor ($LT_{H/L}$) sizes were 4×25μm. Table 7.4 details the transistor sizes within the integrated power switch. Figure 7.26 shows the I-V curves of the power stage HEMT.

Table 7.4: Power and Driver Stage Sizes

P_{TH},P_{TL}	PD_H,PD_L	ST_H,ST_L,	LT_H,LT_L,	R_1	R_2
10×300 μm	10×150 μm	4×25 μm	4×25 μm	100 Ω	75 Ω

The device specific characteristics of the power switch are given in Table 7.5 .

Along with the power transistor, the power stage also featured an anti-parallel diode. The forward voltage drop (V_F) shown in Figure 7.27 of the fabricated diode was around

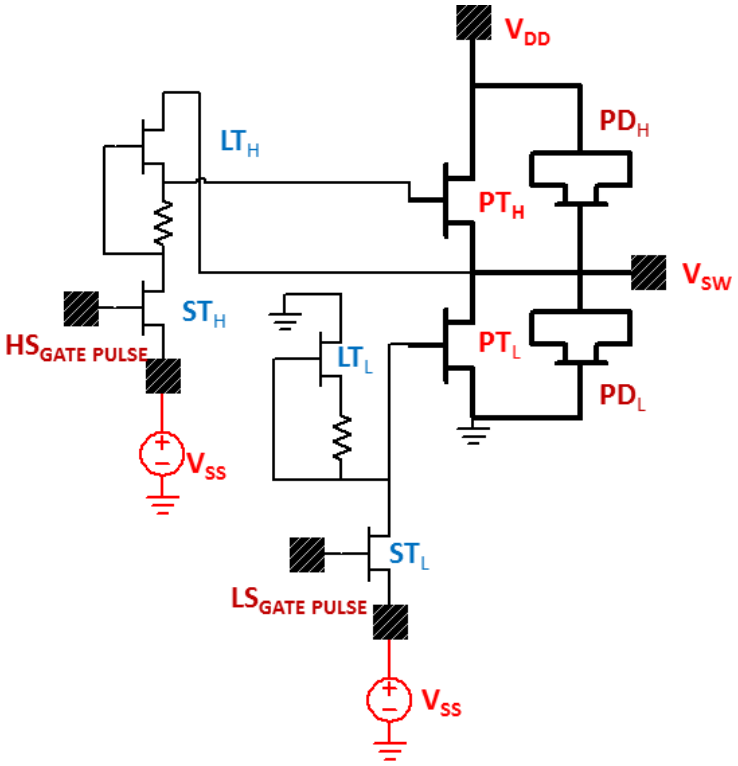

Figure 7.25: Supply Modulator Topology

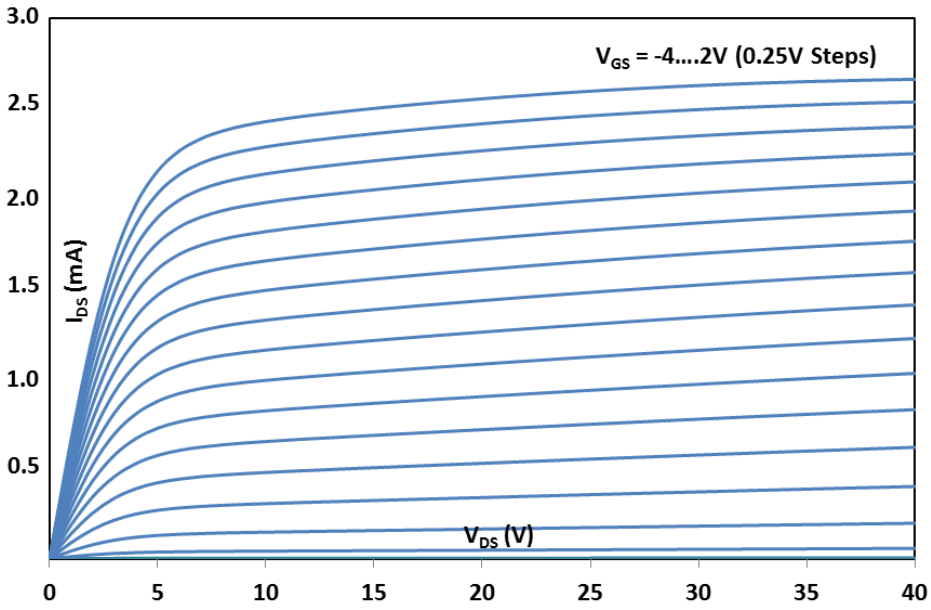

Figure 7.26: Fraunhofer IAF : 10 × 300, I-V Curve

Table 7.5: Power HEMT Characteristics

Device	R_{ON} (Ω)	C_{IN} (pF)	C_{OUT} (pF)	V_{DS} (V)
10×300	0.92	5.1	1.04	40

1.2 V and the reverse breakdown voltage (V_{BD}) was measured to be 100 V as shown in Figure 7.28.

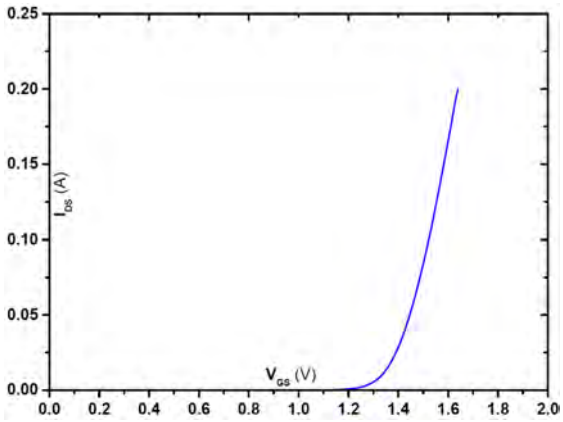

Figure 7.27: Diode Forward Biased

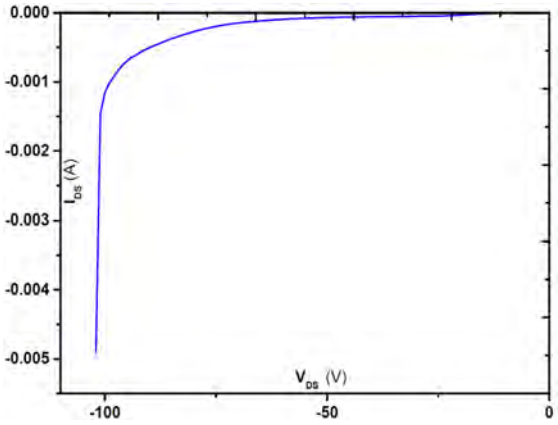

Figure 7.28: Diode Reversed Biased

7.6.2 Transient Simulation

Figure 7.29 illustrates the output voltage of the buck converter at the switch node for duty cycles of 50% with the buck converter input voltage set to 40 V.

The simulated transient waveforms show clean switching with no significant overshoot or waveform distortion at the switch node, where the voltage rises to 40 V and goes all the way down to 0 V. The breakdown voltages of these GaN devices are over 100 V and hence the input can be biased at much higher voltages than 40 V. The models provided in the PDK of this fabrication process were optimised for RF power amplifier applications and to be used in harmonic balance simulations. Time domain simula-

tions performed with these models always caused convergence issues within the ADS simulator.

However, as mentioned above, these transient simulations are done in a harmonic balance simulator using models optimized for Class-AB PA operation, and hence do not fully capture the behaviour when used as switches.

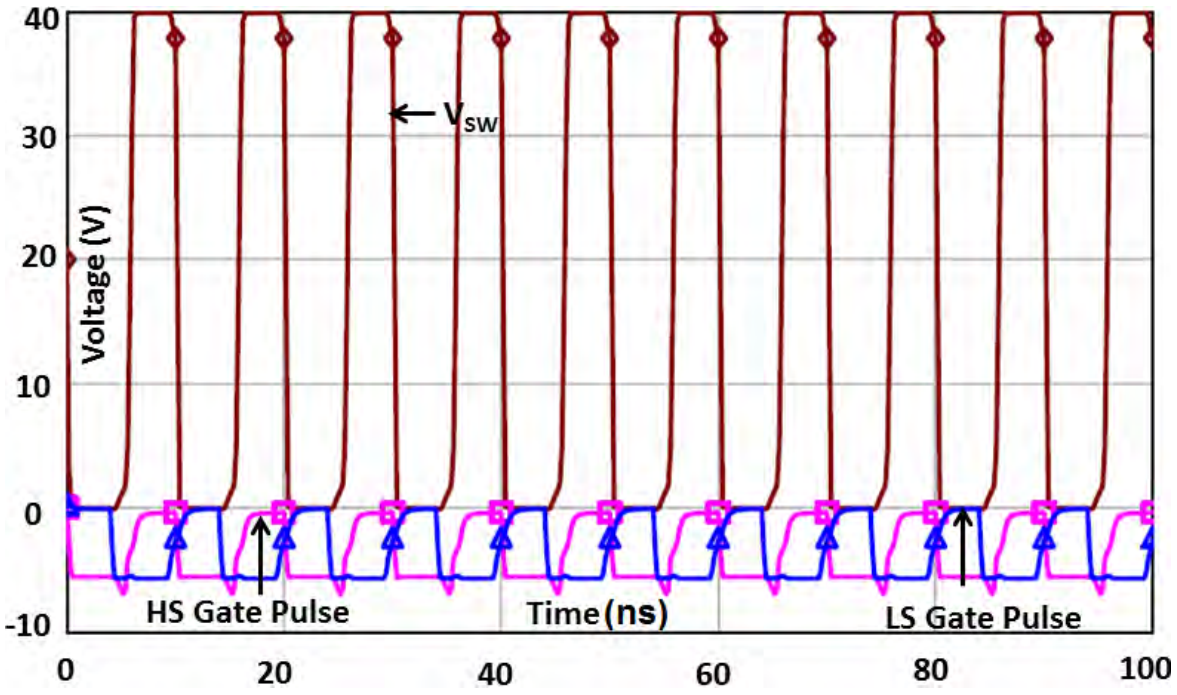

Figure 7.29: P_{T1}: V_{SW}(V), D=50%

Moreover, these simulations do not fully capture the layout effects, including the distributed capacitances and inductances due to the traces used. Hence a full 3-D simulation at 100 MHz will deliver a more complete picture of the EM enviorment of the modulator layout and the influence it may have on the switching performance of the circuit.

One of the concerns in implementing an HPA with an integrated switching supply modulator is the effect of switching spurs generated by the supply modulator that

might fall inband of the Tx/Rx spectrum. In order to fully comprehend the effect of the supply modulator switching noise coupling into the RF, a full 3-D EM simulation of the combined circuit needs to be undertaken. Due to the highly intensive computational requirements, such a simulation can only be undertaken on dedicated simulation servers and was not undertaken for this thesis.

7.6.3 Layout of HPA and SMPS

The layout of the HPA integrated supply modulator was done in Fraunhofer IAF's 0.25 μm GaN process technology as shown in Figure 7.30. This is a 3 metal insulator (3MI) proces and all circuit schematics presented in this work were designed in ADS using models available in the process design kit (PDK). The corresponding layouts are also generated in ADS, but completed in Cadence Virtuoso where the entire circuit was checked with the aid of a design rule check program (DRC). The circuit design was an iterative process with optimisation and re-simulation necessary to adjust the layout to the desired chip size.

The power stage consists of large periphery GaN HEMTs in an inverter configuration. The power stage is a 10×300 μm wide HEMT which has been optimized for RF power amplifier applications with an offset in the gate-drain and gate-source distances. The power stage also incorporates integrated 10×150 μm anti-parallel diodes that were designed by internally shorting out the drain and source terminals of the device using the air-bridge metallisation. In order to accommodate the increased current within the device, three 20 μm wide air-bridge metallisations internally connect all the source fingers of the power device to an external source pad.

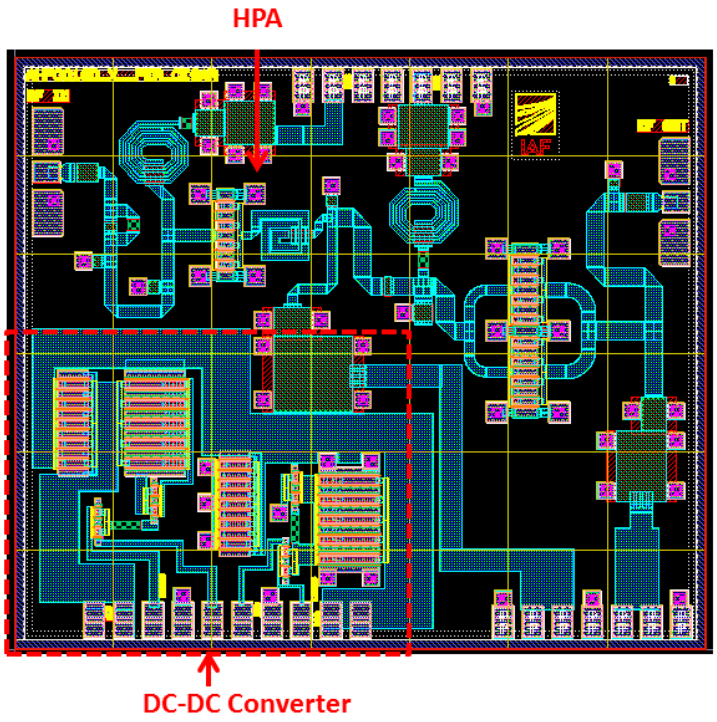

Figure 7.30: Supply Modulator Integrated HPA Layout

The layout was done with a view to test the two functional blocks, the HPA and the supply modulator, independently. Hence the RF path, gate/drain bias lines of the HPA and the bias, control and power traces of the supply modulator were clearly separated in the layout. The original amplifier layout was optimised by separating the gate and the drain supply traces to the top and bottom of the amplifier, to integrate with the supply modulator. In order to allow for on-wafer measurements on the MMIC, G-S-G pads were inserted for the RF lines while G-S-S-G-S-S-G probes were laid out for both gate and drain supplies. The pitch for both the probes was 100 μms. Supply modulator integrated HPA was laid out within a chip area of 3 × 3.5 mm.

7.7 Measured Results

7.7.1 Wafer Mapping

Small signal and large signal measurements were performed in an on-wafer configuration at a drain voltage of V_{DS}= 28 V and I_{DS}= 100 mA in CW operation. Figure 7.31 shows the measured S-parameters of the fabricated HPA. All data of the HPA MMICs shown below were taken from the same wafer and the CW S parameters were found to be very uniform over the entire wafer.

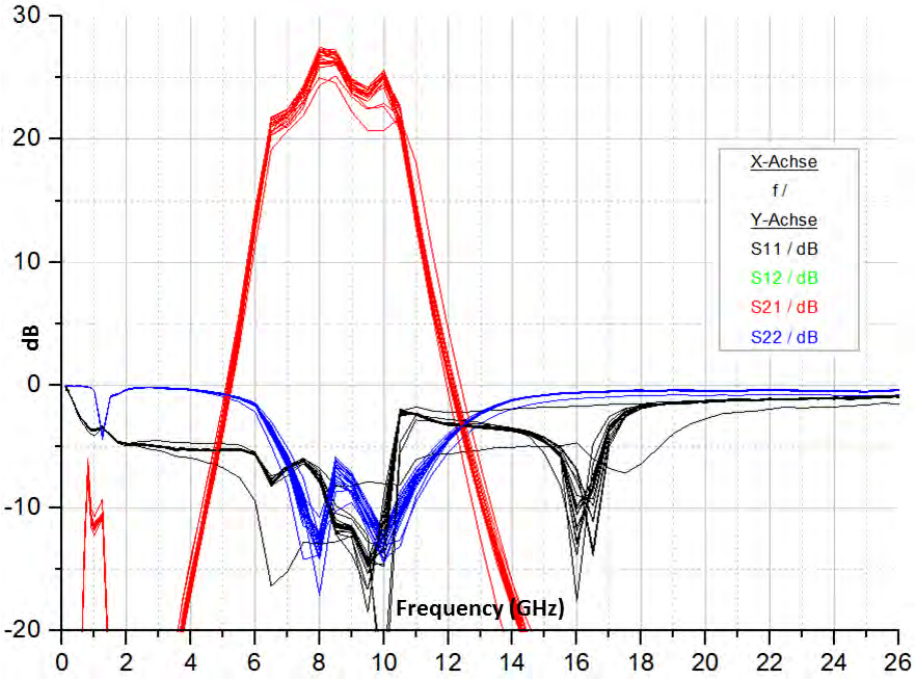

Figure 7.31: Wafer mapping: S-Parameters

Measurements show a small-signal gain of ≥ 20 dB for a frequency range from about 7 GHz up to 10.5 GHz. S_{21} peaks at 27dB at around 8 GHz.

Looking at the input and output reflection coefficients S_{11} and S_{22}, both show good

characteristics in the frequency range of interest. The HPA has an input and output reflection of about -6.5 dB for a frequency range of 8-10 GHz.

Large-signal measurements were also done in CW operation at the same bias conditions. The power sweep at a frequency of 9 GHz are shown in Figure 7.32. The measured PAE showed excellent characteristics with ≤ 5% spread among the various cells at the maximum PAE. The average PAE measured was around 41.90% and the corresponding output power was 39.48 dBm, while the gain was 15.82 dB. The input power was 22 dBm, beyond which the amplifier went into compression.

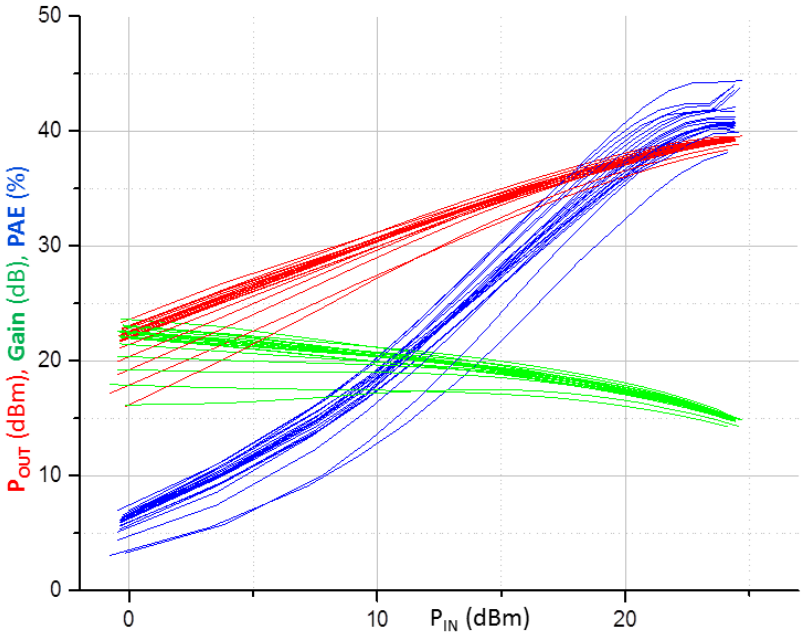

Figure 7.32: Wafer mapping: S-Parameters

The wafer was diced into individual dies and picked to be mounted on a prototype PCB; the details are given in the next section.

7.7.2 PCB Prototype

A MMIC chip photograph is shown in Figure 7.33; the chip was mounted on to a PCB as shown in Figure 7.34. The PCB was fabricated using Rogers RO4003 substrate with a height of 508 μm and a thickness of 35 μm along with RF signal lines of 50 Ω and low impedance drain and gate feeds.The MMIC was placed within a test fixture that allowed the bare die to rest directly on the heat sink within a hole cut out of the PCB. The MMIC was then directly connected to the PCB with 25 μm bond wires. SMA adapters were soldered onto to provide the interface for the RF signals, while SMBs were used for the high side and low side PWM signals. SMD decoupling capacitors were also soldered onto to the power and bias traces within the PCB. Off-chip filters were also mounted onto the PCB. The entire PCB was mounted onto a gold-plated test jig of size 3.5 × 3.5 cm, which provided mechanical support as well as heat sinking.

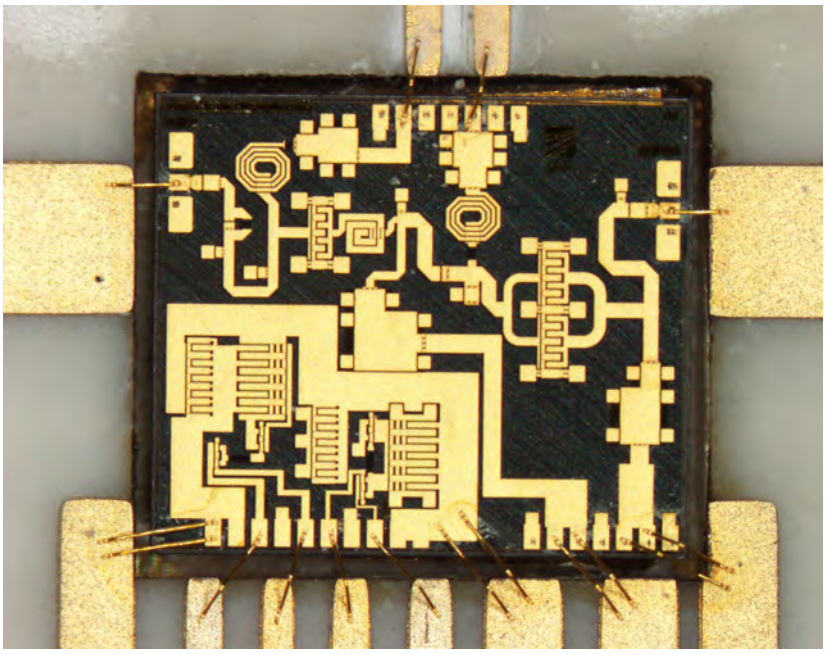

Figure 7.33: Supply Modulator Integrated MMIC Chip

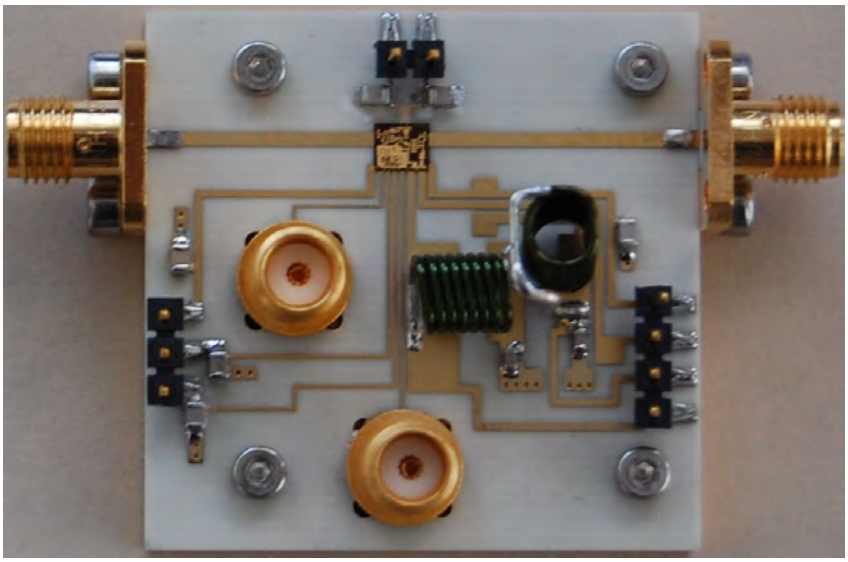

Figure 7.34: MMIC mounted on prototype PCB

7.7.3 Measured Results of PCB Prototype

7.7.3.1 HPA

The prototyped HPA was tested for stability over the whole bandwidth. It exhibited low frequency oscillations at 1.18 MHz as shown in Figure 7.35. Hence decoupling capacitors of 47 μH were added to the drain bias feeds. This eliminated the low frequency oscillations and stablilised the packaged HPA.

Figure 7.36 shows a comparision of the simulated, on-wafer and pcb-mounted MMICs. The simulated and on-wafer measurements were very similar at increasing RF input power ($P_{IN} \approx$ 17 dBm), while the measurements done on the pcb-mounted prototype had much lower efficiency. This may be due to the fact that the MMIC is epoxied onto the gold-plated test jig and the interface was a poor thermal conductor causing the degradation of the efficiency due to the heat dissipated within the circuit. At lower

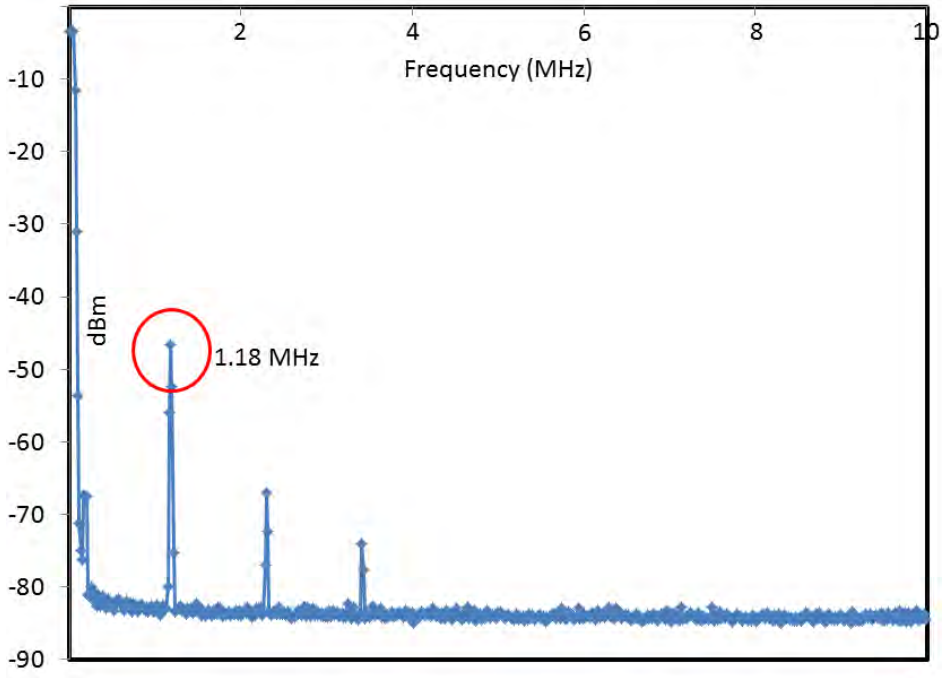

Figure 7.35: StabilityAnalysis

P_{IN} the simulations showed better performance than the measurements. Table 7.6 summarises the maximum measured performance of the HPA.

Table 7.6: Comparision of HPA Max.Performance, V_{DS} = 28 V

	Simulated	On Wafer	Prototype PCB
DE (%)	45.30	42.20	37.05
PAE (%)	42.73	41.90	34.98
P_{OUT}(dBm)	38.80	39.48	38.34
Gain (dB)	16.2	15.82	15.34

Figure 7.37 shows the power sweep characteristics of the pcb-prototype from 7.75 GHz to 10 GHz in steps of 0.25 GHz. A maximum PAE of 34.98% , P_{OUT} = 38.13 dBm and a corresponding gain of 15.34 dB were observed at 8.5 GHz. It is interesting to note that in the PAE measurements 3 distinct clusters are seen, with similar PAE performance seen in the 8-8.75 GHz band. The next cluster is 9, 9.25 and 7.75 GHz PAE cluster, the third distinct PAE cluster is seen from 9.5 GHz onwards.

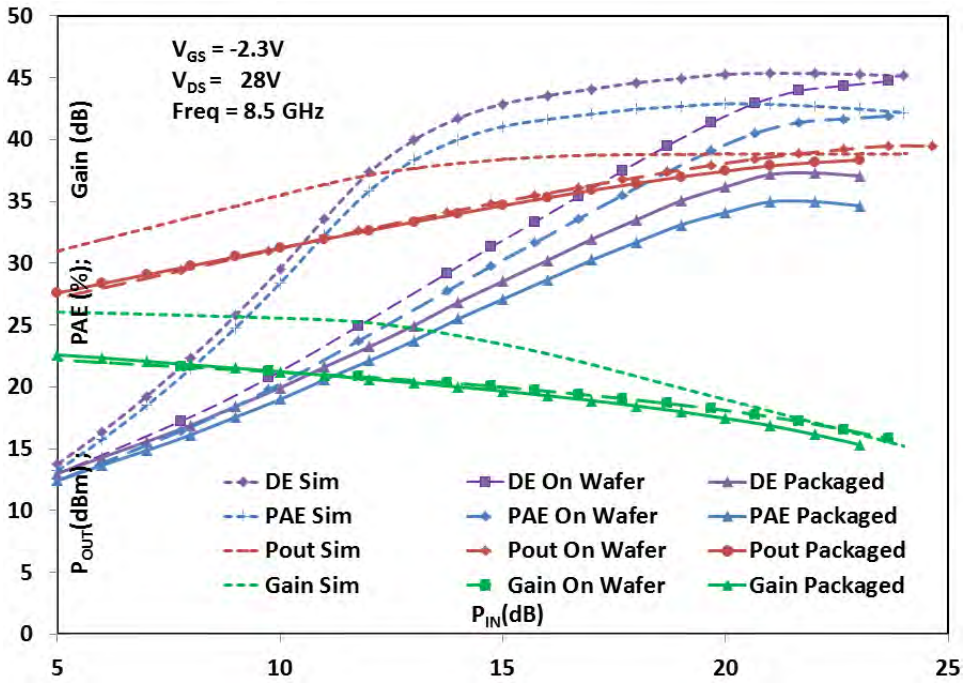

Figure 7.36: Power Sweep Comparison: On-Wafer v Packaged,V_{DS} = 28V

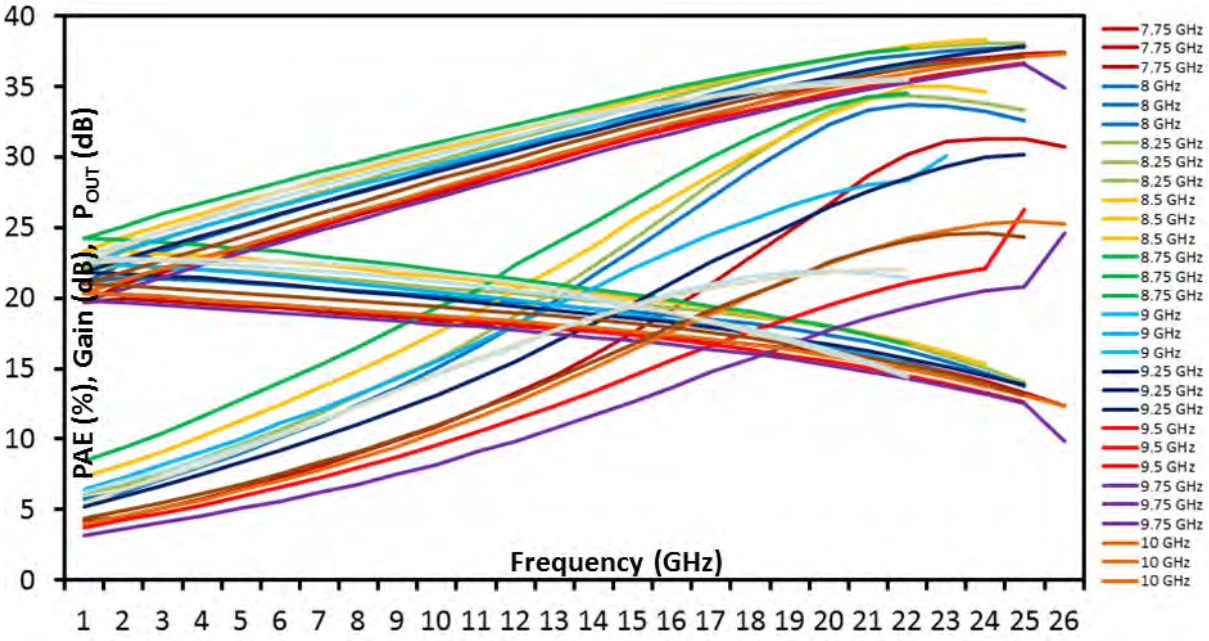

Figure 7.37: Power Sweep, V_{DS} = 28V

The broadband frequency characteristics of the pcb-mounted prototype from 7-12 GHz are given in Figure 7.38. Within the 8-10 GHz frequency band of interest, the

PAE, P_{OUT} and gain remained above 34%, 24 dBm and 12 dB respectively over the entire bandwidth.

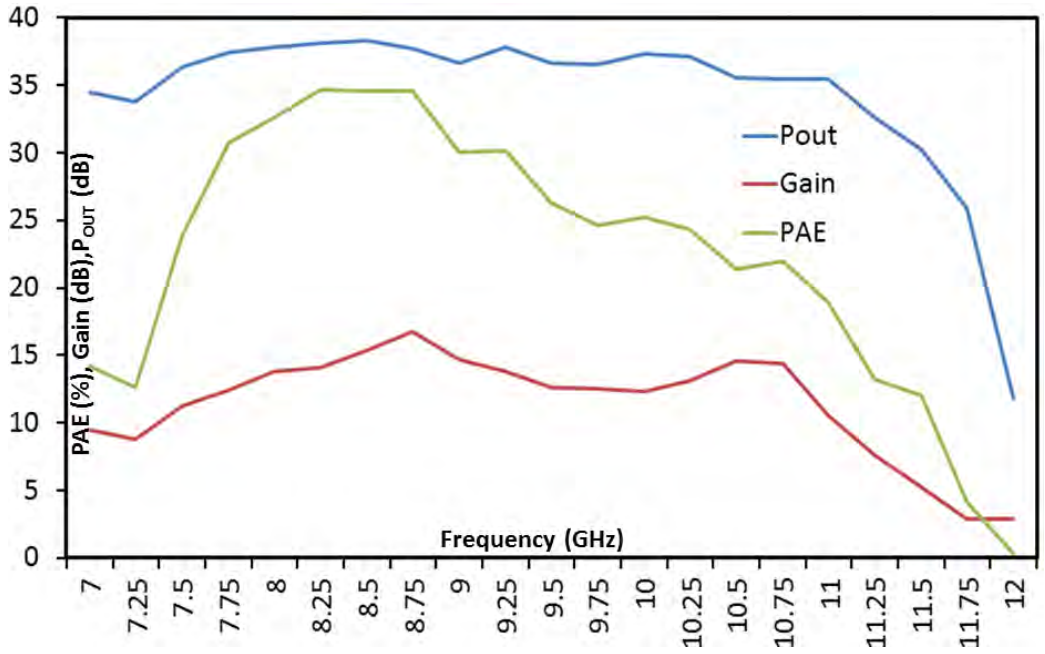

Figure 7.38: Frequency Sweep,V_{DS} = 28V

The drain voltage of the pcb prototype PA was varied from 28 V to 15 V to understand the impact of V_{DS} on PAE and P_{OUT}. Figure 7.39 shows PAE v P_{OUT} plots for various V_{DS}.

The maximum PAE of 41.66% was observed for the on-wafer measurement with a corresponding output power of 39.20 dBm. The maximum PAEs for pcb prototype at 28, 20 and 15 V drain bias were 34.98%, 34.76% and 32.44% respectively. The coresponding output powers delivered by the HPA were 38.14 dBm, 34.63 dBm and 33.87 dBm. The trend in the PAE shows the effectiveness of decreasing the drain bias voltage with lower input power actually helping to deliver a higher PAE than with a constant drain bias voltage.

The broadband frequency characteristics of the HPA under supply modulator condi-

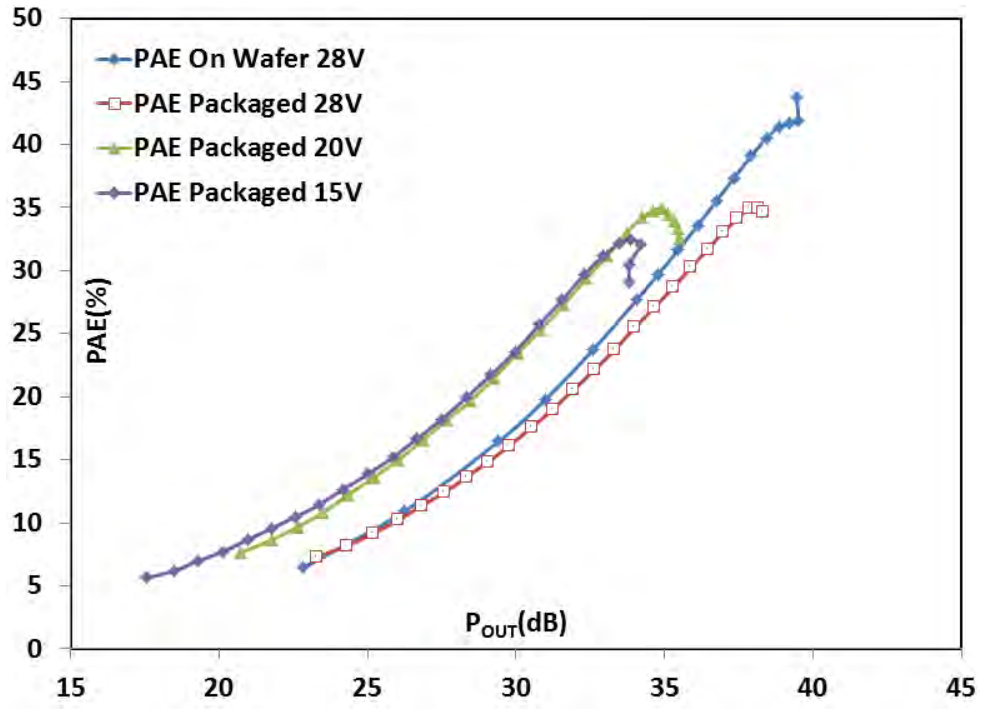

Figure 7.39: PAE v P_{OUT}, swept V_{DS}

tions were also measured for both 20 V and 15 V drain bias conditions. Figure 7.40 and 7.41 show the measured broadband performance of the supply modulated HPA.

In Figure 7.42 the drain resistance and drain current are plotted as a function of the output power. The PA drain resistance varies with the input RF power level driving the PA. R_{Load} decreases when the PA input RF level increases. For the case of on-wafer measurements the RFPA drain resistance varies from 264.4 Ω to 37.9 Ω at a drain bias of 28 V. The maximum drain current delivered was 736 mA. The drain resistance variation for the pcb protype at a 28 V dc drain bias was 272.7 Ω to 43.19 Ω, with a maximum drain current of 682 mA. Lowering the drain bias to 20 V revealed a change in drain current to 503.5 mA and a corresponding resistance variation of 364.7 Ω to 55.72 Ω. The drain resistance variation at a 15 V drain bias was 422.85 Ω to 54.8 Ω, with a drain current of 474.6 mA.

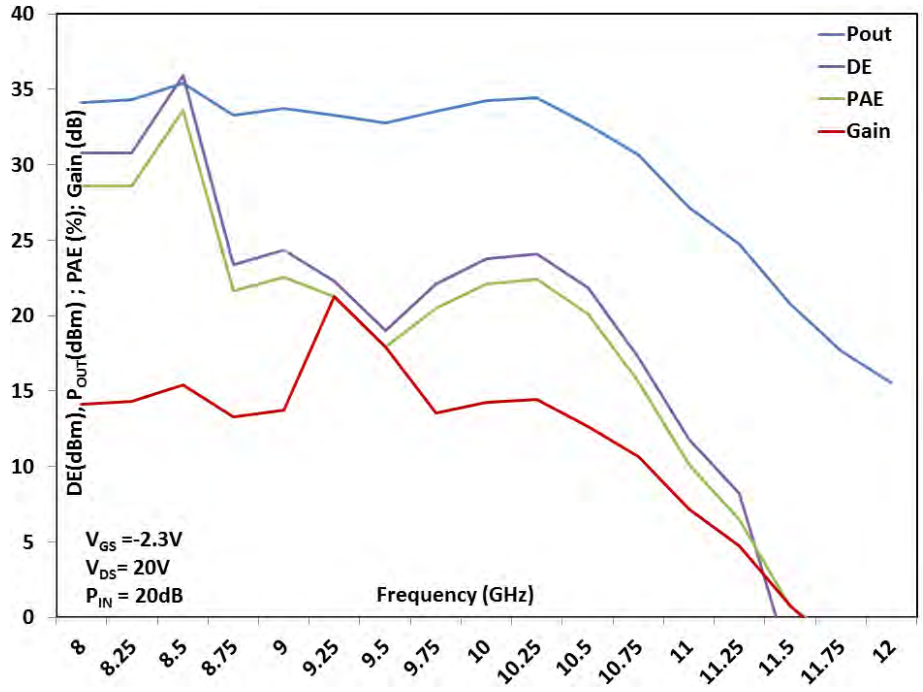

Figure 7.40: Measured Broadband Frequency Sweep, V_{DS} = 20V

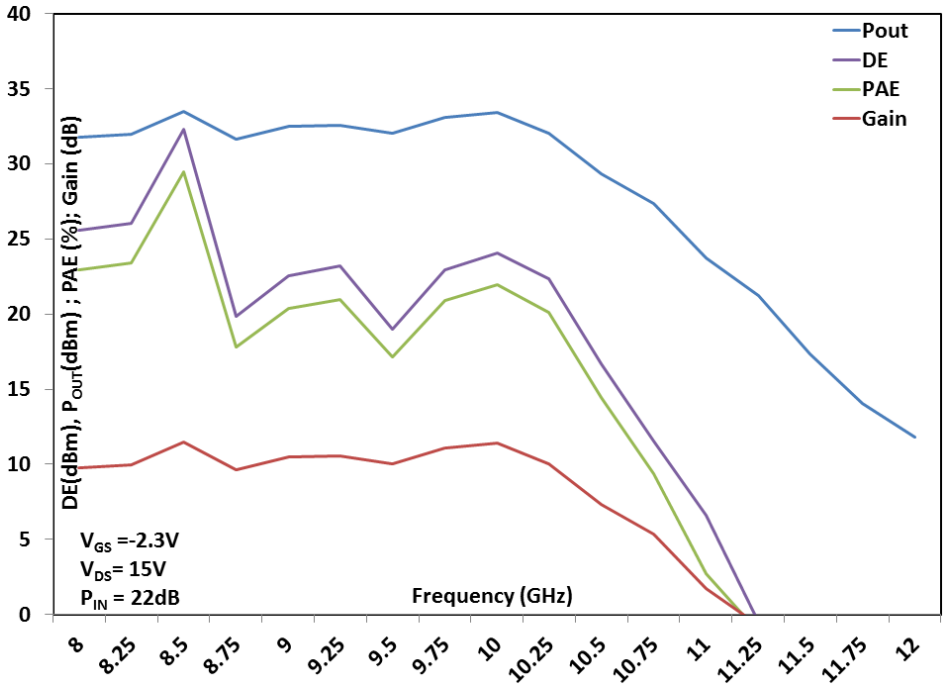

Figure 7.41: Measured Broadband Frequency Sweep, V_{DS} = 15V

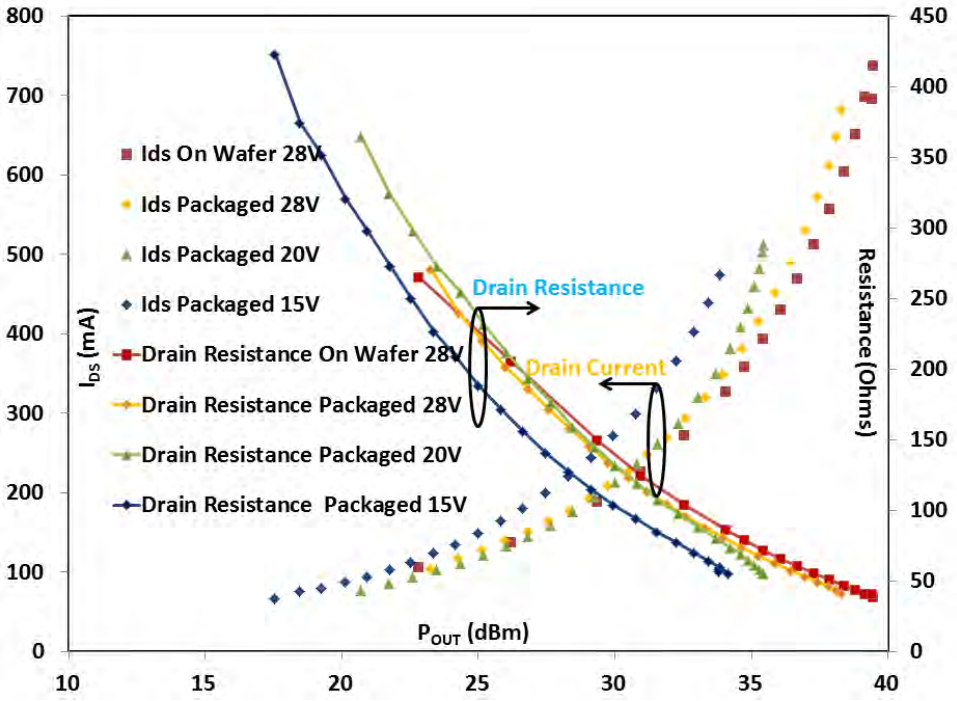

Figure 7.42: I_{DS} v P_{OUT}, swept V_{DS}

The challenge for the supply modulator is to provide an output voltage swing in the range of 15 to 28 V under that constraint of wide load variations while maintaining efficiencies greater than 80%.

7.7.3.2 Supply Modulator

The normal operational drain bias voltage for the HPA is 28 V. The supply modulator is a synchronous buck converter topology, which can step down an input voltage to much lower voltages depending on the duty cycle of the converter, with very high efficiency and at a high switching frequency.

Hence in order to supply 28 V to the drain bias, the modulator input voltage can be set at 40 V with the duty cycle set at 70%, or set the input power supply voltage of the

modulator to be 60 V which will be stepped down to 28 V at a 47% duty cycle. However precise control of the level shifter voltage levels and the corresponding source/drain bias voltages in the driver circuitry were very difficult to achieve. Moreover the manual setting of the dead time control was prone to errors, causing it to short-circuit and destroy the power transistors due to the large number of precise bias voltage levels required for a supply modulator input voltage of 60 V.

Alternatively, the supply modulator can be biased at a 40 V input voltage and run at a duty cycle of 70% to deliver 28 V output but with increased output current. However, the increased heat dissipated due to the high voltage and current was a major concern for thermal management of the device. The heat conduction at the inferface between the chip back-side to the test jig was not ideal due to the presence of epoxy which was used to attach the chip to the gold-plated test jig. From Figure 7.42, the drain current drawn by the the HPA at a 28 V bias was around 682 mA. Hence, the operational drain bias of the HPA was lowered to 20 V and the required drain bias current was around 502 mA.

High frequency, high resolution pulse-width modulated control signals were generated using an Agilent 81110A pulse generator, fed to a Hittie pulse driver amplifer (HMC870LC). These signals are level shifted using external, low frequency bias tees to the appropriate HS and LS PWM gate drive signals.

The output signal was measured by connecting the switch node output through to the off-chip filter and then onto a 50 Ω high-speed Agilent DSOX3034A oscilloscope in the time domain. A fourth-order filter with 100 MHz cut-off frequency is used instead of the second-order filter for higher attenuation at the switching frequency. The filter was designed using the filter design and optimisation toolkit available in Microsoft

AWR Office. The filter was introduced in chapter 6, and the components L_1, L_2, C_1, C_2 we used in the filter were 100 nH, 150 nH, 47 pF, 47 pF respectively.

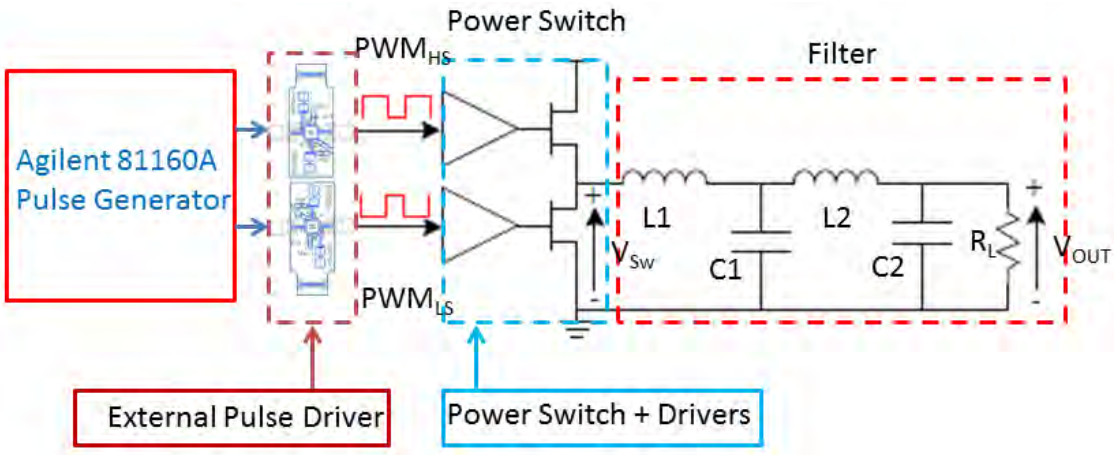

Figure 7.43: Supply Modulator Test Schematic

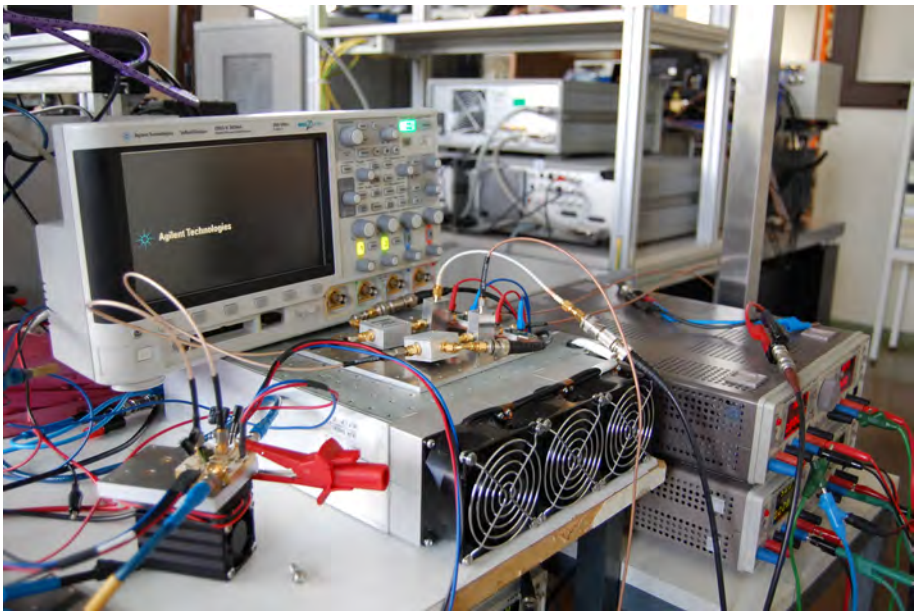

Figure 7.44: HPA + DC-DC Test Bench

The efficiency was measured at 100 MHz, with a 40 V input voltage and at several duty cycle values and output power levels. The resistance values obtained from the drain resistance variation plot were used as the load resistance to obtain the output power levels.

The test setup diagram and a photo of the test bench is shown in Figure 7.43 and Figure 7.44 respectively.

7.7.4 Supply Modulator Efficiency and Loss Analysis

Efficiency plots of the integrated modulator are shown in Figure 7.47. At a duty cycle of 75% (30 V), the power stage efficiency is above 91% for all operating load conditions, and the corresponding efficiency incorporating the driver circuitry is above 80% for a wide range of operating conditions, peaking at 88.2% for high output powers. At low output powers the total efficiency is under 80% due to the circuit driver loss.

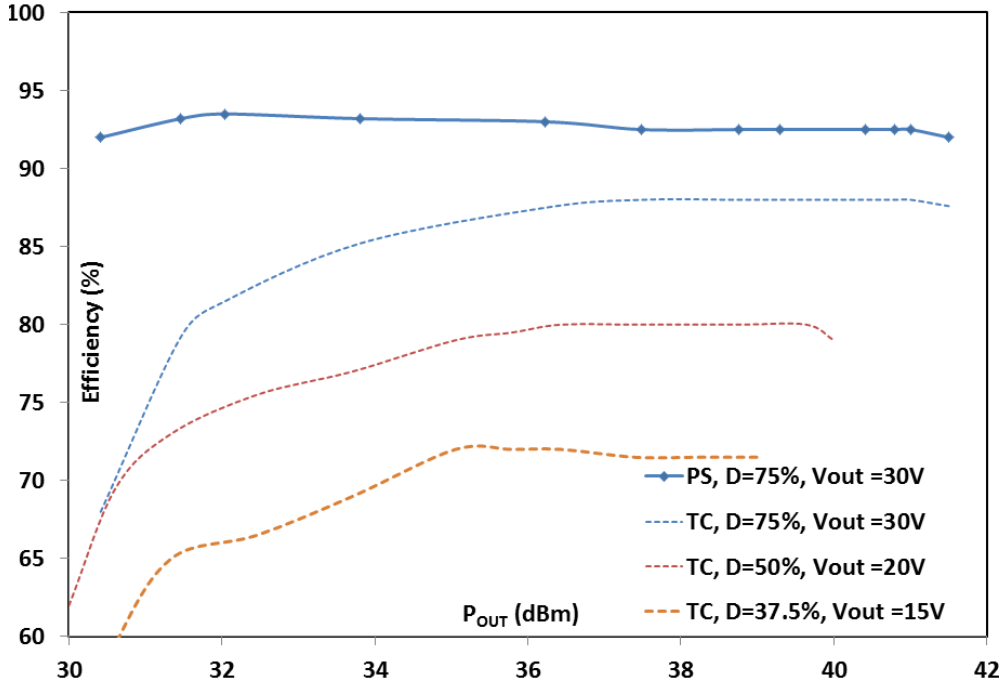

Figure 7.45: TQS Sw-Node Modulator Efficiency

At a duty cycle of 50% (20 V), the efficiency peaks at 80% and for 37.5% (15 V), the maximum efficiency was 72%. The voltage conversion ratio plot shown in Figure 7.46 also shows that for high duty cycles, the switch node connected driver circuit delivers

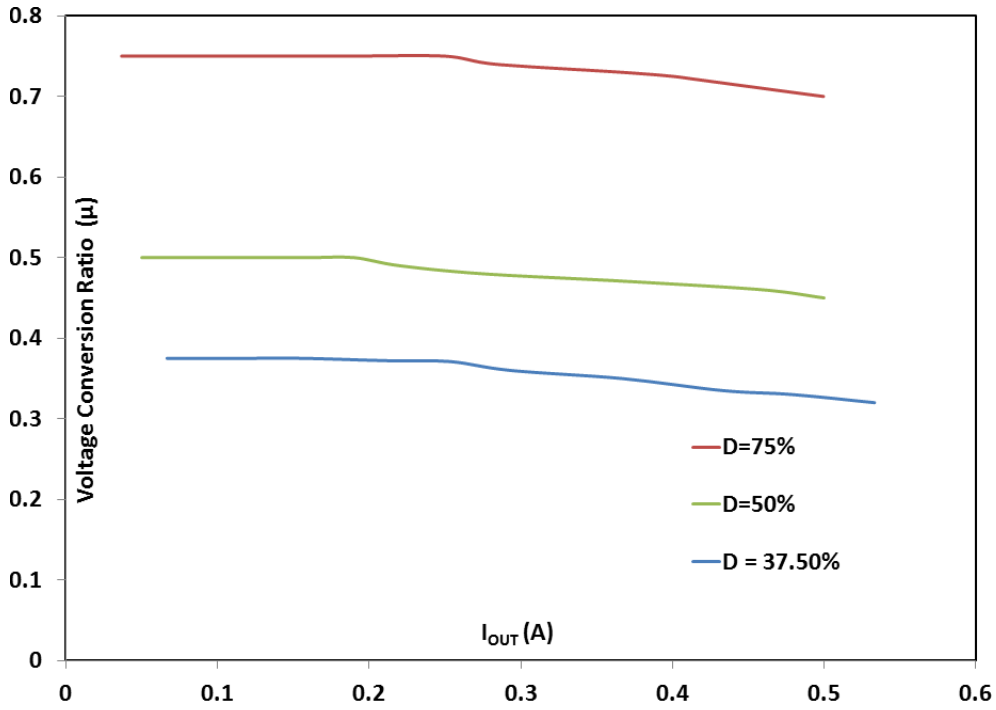

Figure 7.46: IAF Sw-Node Volt Conversion Ratio

a steady output current for a wide range of operating load conditions. At a duty cycle of 37.5% duty , there are some timing errors which caused some loss leading to a lower voltage conversion ratio with increased power levels. The supply modulator was characterised up to a maximum output power of 41.5 dBm at a duty cycle of 75%, while the output powers for 50% and 37.5% duty cycles were 40 dBm and 39.03 dBm.

The loss analysis introduced earlier in chapter 5 was used to analyse the loss mechanism within the supply modulator circuit. Figure 7.47 shows the loss breakdown and as was noted in the analysis undertaken in chapter 6, the major contributor to loss within the supply modulator topology is the gate driver circuit, especially the high side gate driver circuit. Here the gate driver circuit contributes over 89% of the loss within the circuit at a duty cycle of 75%. Table 7.7 give the simulated and measured gate driver loss for various switching scenarios.

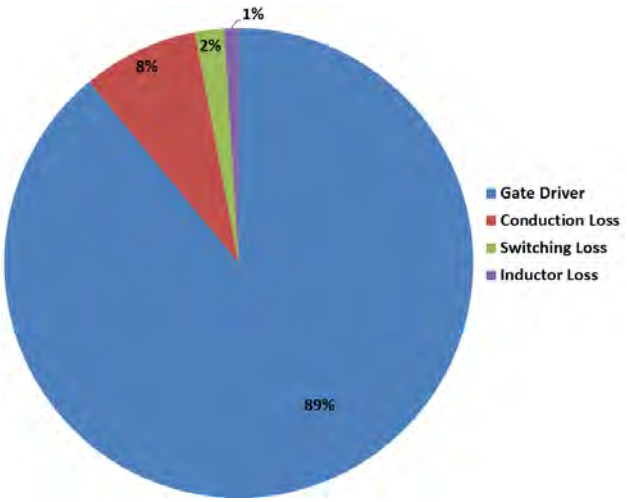

Figure 7.47: SM Loss Breakdown

Table 7.7: Comparison of Driver Losses

Duty Cycle ⇒	**0.25**	**0.50**	**0.75**
Simulated (mW)	340	305	289
Measured (mW)	437	415	410

Within the driver loss, the major loss component is the high side driver. By optimising the gate driver ($ST_{H/L}$ and $LT_{H/L}$) sizes to use very small devices like 2×25 μm devices will minimize the gate driver loss within the modulator circuitry and hence the efficiency can be further increased. The driver can be further optimised by the use of enhacement mode devices which are normally-off devices.

7.7.4.1 HPA and Supply Modulator Combined

The filtered voltage from the supply modulator was connected to the drain contact trace of the RFPA using wirebonds from the output of the filter node as shown in Figure 7.48. The PCB was mounted onto a peltier cooler as shown in Figure 7.49 to minimise any thermal degradation that may occur while operating the HPA and supply modulator simultaneously.

The PA was biased at 20 V drain voltage due to the fact that the supply modulator input voltage was set to 40 V with a duty ratio of 50%. The modulator duty cycle was adjusted manually to achieve the required drain bias voltages.

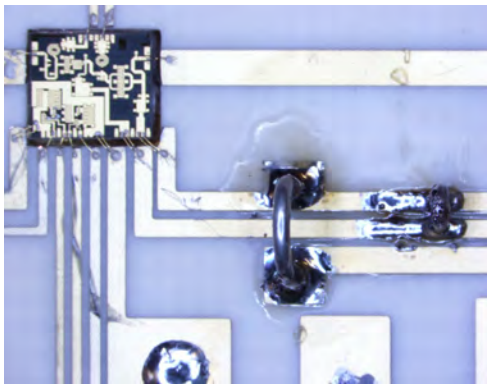

Figure 7.48: HPA + DC-DC internally connected

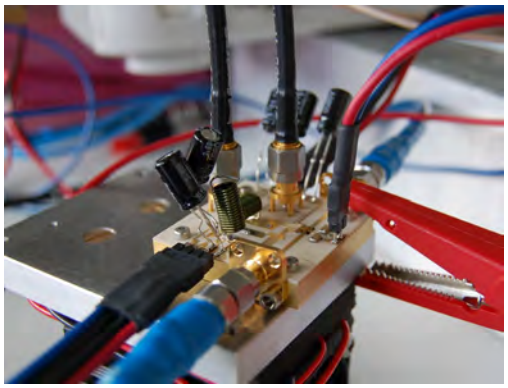

Figure 7.49: Cesar PCB test jig mounted on peltier cooler

The efficiency of the supply modulator integrated HPA was calculated separately due to the fact that the existing measurement facility did not cater to measuring the combined efficiency of the modulator and the HPA. The combined efficiency was calculated as follows:

$$PAE_{overall} = PAE_{RFPA} \times \eta_{DC-DC} \tag{7.2}$$

Figure 7.50 shows the filtered 20 V output voltage from the supply modulator with a 47 Ω load. The power sweep at 8.5 GHz is given in Figure 7.50.

The calculated DE and PAE of the HPA and supply modulator combination were 28.80% and 26.65% respectively, and it delivered an output power of 34.98 dBm.

The modulator output voltage was set to 15 V by manually adjusting the gate driver PWM signals to a duty cycle of 37.5%. Figure 7.52 shows the filtered 15 V output

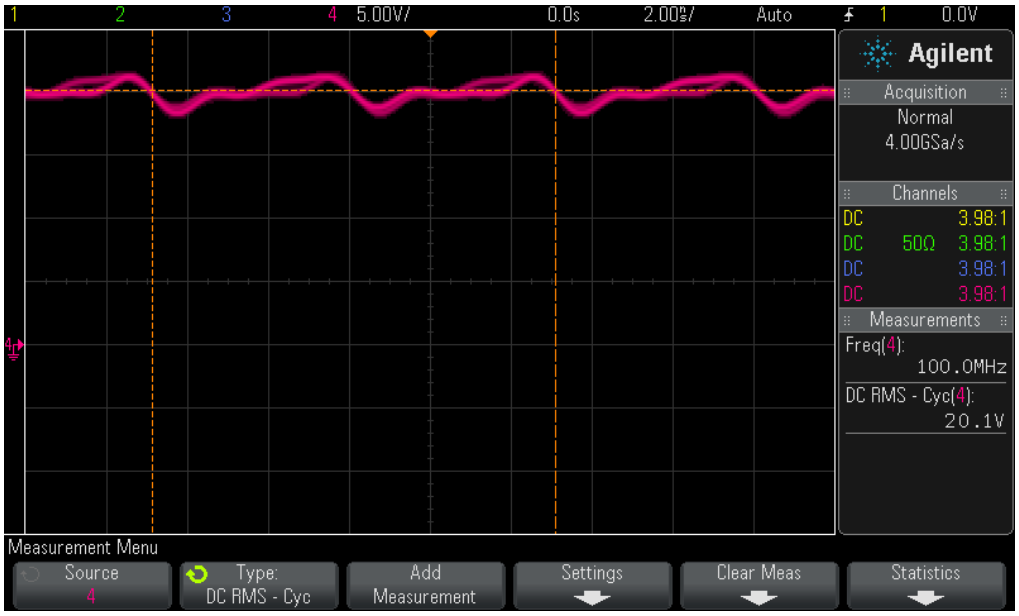

Figure 7.50: D= 50%- V_{IN}= 40V, V_{OUT}= 20V

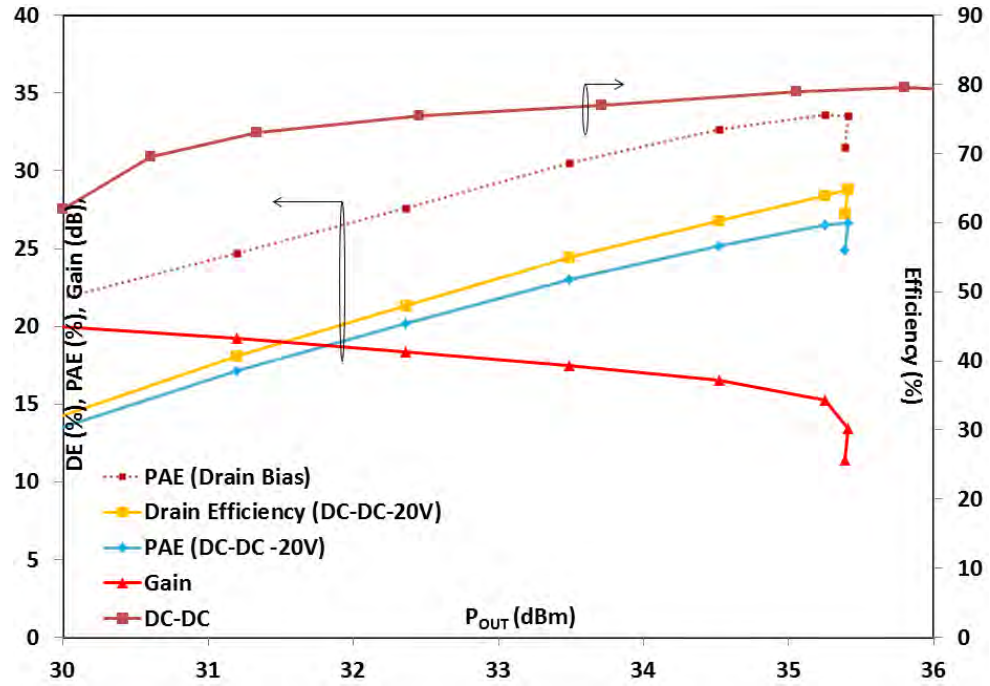

Figure 7.51: Cesar Power Sweep with DC-DC: 20V

voltage from the supply modulator with a 47 Ω load. The power sweep at 8.5 GHz is given in Figure 7.53.

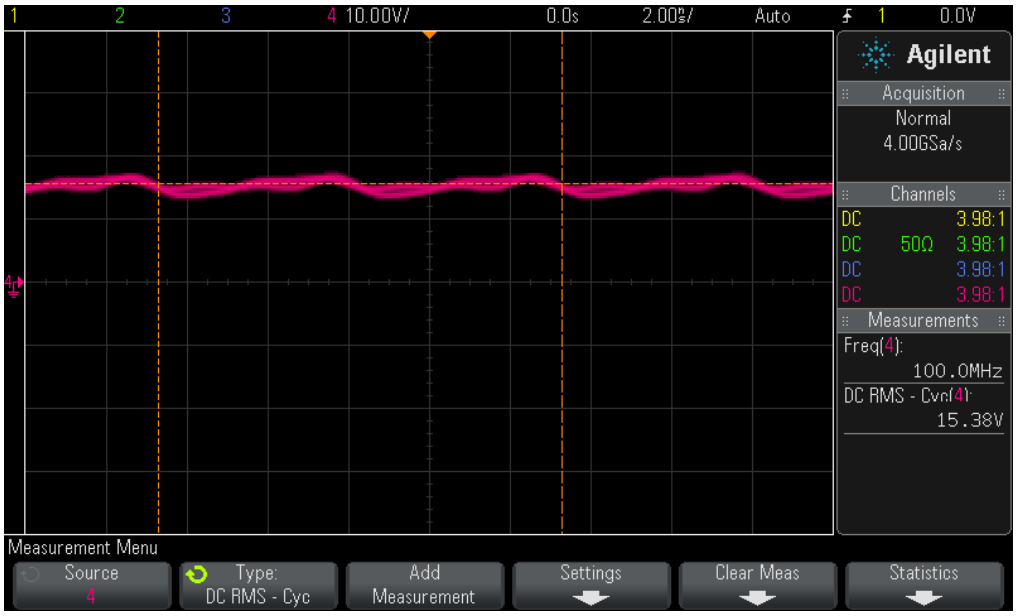

Figure 7.52: D= 37.5%- V_{IN}= 40V, V_{OUT}= 15V

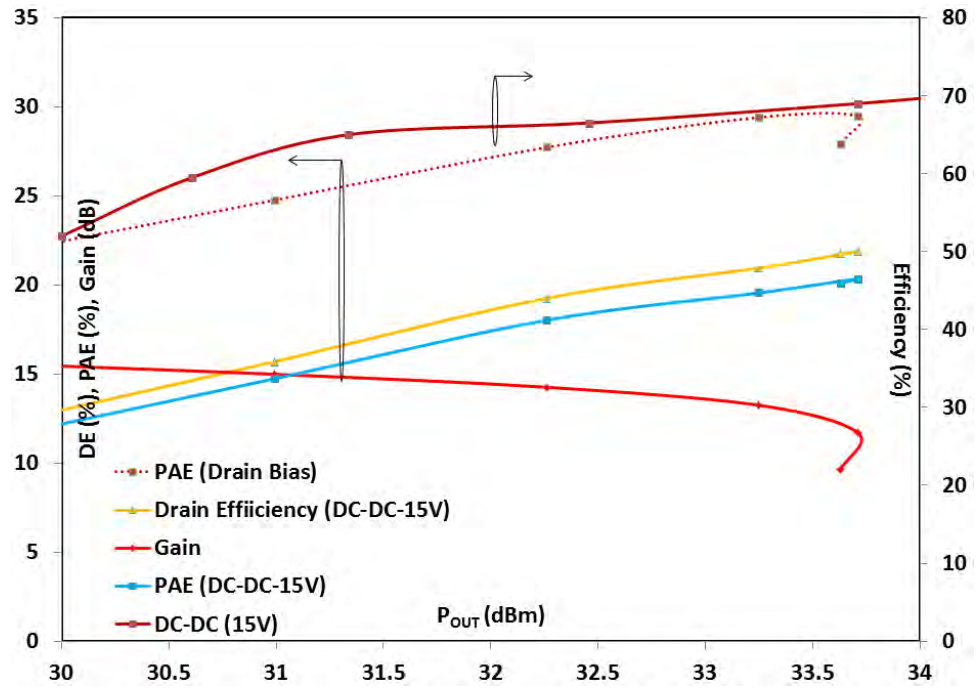

Figure 7.53: Cesar Power Sweep with DC-DC: 15V

For a drain bias of 15 V, the calculated DE and PAE of the HPA and supply modulator combination were 21.88% and 20.35% respectively, and it delivered an output power

of 33.71 dBm.

The broadband frequency characteristics of the HPA under supply modulator conditions were also measured for both 20 V and 15 V drain bias conditions. Figures 7.40 and 7.41 show the measured broadband performance of the supply modulated HPA. The DE was >13.26% , PAE > 11.98%, Gain > 10.37 dB and P $_{OUT}$ > 33.85 dBm at 20 V drain voltage biased through the supply modulator for the whole frequency range from 8-10 GHz.

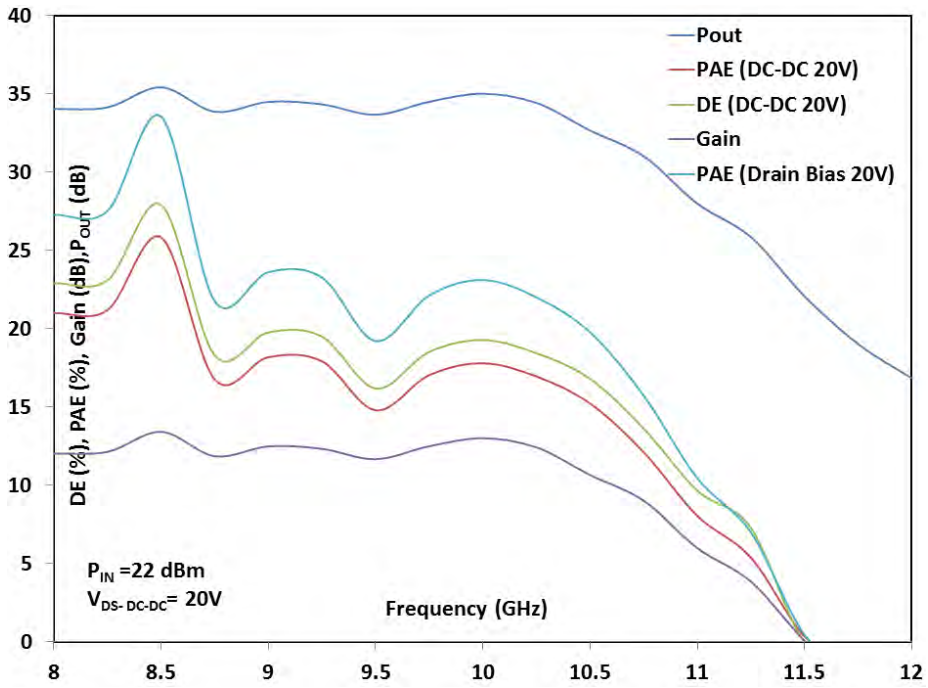

Figure 7.54: Power Sweep (SM: 20V)

Similarly the broadband frequency performance of the supply modulated HPA at 15 V drain bias had DE >31.16% , PAE> 14.78%, Gain> 11.85 dB and P$_{OUT}$ > 33.85 dBm for the 8-10 GHz bandwidth.

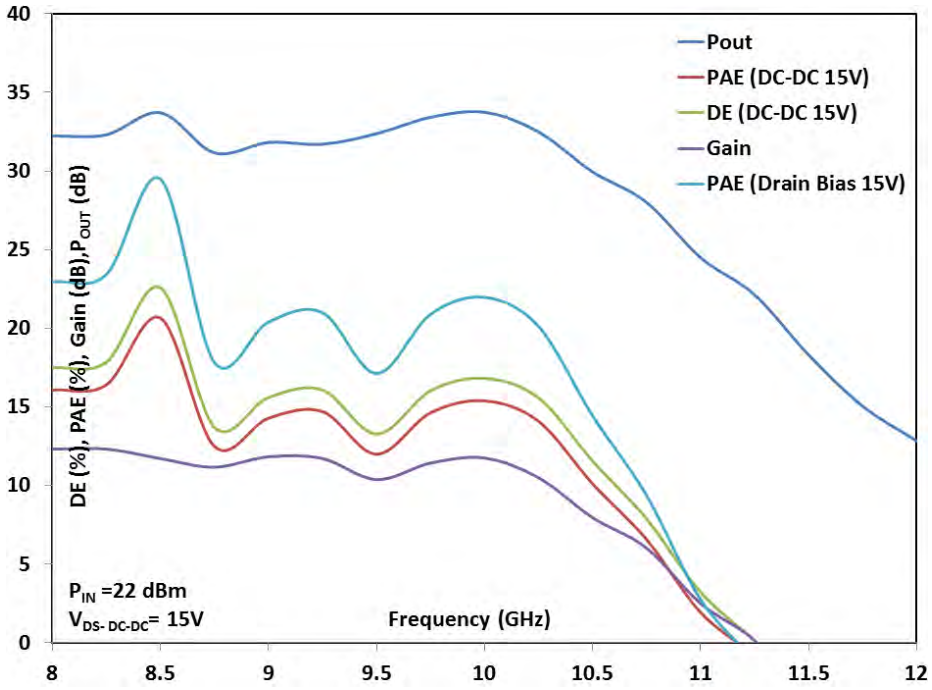

Figure 7.55: Power Sweep (SM: 15V)

7.8 Discussion

The work discussed in this chapter is the first reported supply modulator integrated HPA in GaN with a switching frequency of 100 MHz and efficiency of over 80% at a duty cycle of 75%.

The pcb prototype dual stage HPA delivers 38.14 dBm of output power with a PAE of 34.98%, with the drain biased at 28 V. The overall DE and PAE of the combined HPA and supply modulator were 28.80% and 26.65% at a drain voltage of 20 V (duty cycle = 50%) . With the drain bias of 15 V(duty cycle = 37.5%), the combined DE and PAE were measured as 21.88% and 20.34%. The delivered output powers were 34.98 dBm and 33.71 dBm. The supply modulator efficiency for a 20 V output peaks at 80%, while delivering over 36.43 dBm. The modulator was characterised to a maximum

ouput power of 40 dBm. The efficiency dips to less than 70% at an output power of 30.8 dBm.

The efficiency of the modulator at an output voltage of 15 V peaks at 72% for an output power of 35.79 dBm and it delivers a maximum output power of 39.03 dBm. The efficiency drops to less than 65% below 31.3 dBm of output power.

At lower power levels, the supply modulator efficiency is low (<70%) due to the fact that, even with optimised switch node connected ST-R-LT gate drivers, the power dissipation within the driver circuitry causes the overall efficiency to be low. However at higher RF input levels the combined efficiency of the RFPA and the modulator increases due to the increase in driver efficiency at higher modulator output power levels. Hence for an RFPA with integrated supply modulator targeting the 1-2W range, a GaAs implementation would be very competitive with GaN.

The supply modulator input supply voltage was set at 40 V, due to the fact that the bias voltages that set the level shifter operation are extremely challenging at higher voltages (> 40 V) and with as, with dead time setting done manually, the probability of destroying the power stage transistors due to accidental short-circuiting is greater due to the increased voltage levels. The use of an integrated level shifer incorporated within the gate driver circuitry will enable high voltage operation and interface to the PWM gate driver signal without the need for control voltages and an external bias tee. The integrated level shifter needs to be optimised to minimise power dissipation within the gate driver circuitry and to keep the efficiency of the total modulator high.

The modulator ouput voltage which biases the HPA was controlled by an external PWM signal. The PWM was adjusted manually, for the purpose of circuit demonstra-

tion in this chapter. In order to dynamically adjust the supply voltage, for RF input signals with complex modulation schemes, digital control of the PWM signal including the dead time control needs to be implemented [144].

Even though the supply modulator integrated HPA delivered 35.6 dBm of output power at an overall efficiency of 23.3%, the P_{IN} was varied linearly leading to a linear variation in the drain resistance with the input power. However, when presented with a complex modulation scheme like 20 MHz LTE-A, the drain presents itself as a dynamic and complex resistance plane which might lead to oscillations and problems with the stability of the amplifier. Hence a proper time-varying characterisation of the amplifier drain resistance with an appropriate modulation scheme needs to be fully understood for amplifier stability [128].

DC/DC converters can generate significant spurious noise in the Tx and Rx bands due to the switching action. In this work, the in-band spectrum was not explored to investigate the role of switching spurs affecting the RF signals. One way to minimise the switching spurs would be the use of a multiphase differential dc/dc converter [95]. Operating two parallel buck converters antiphase and into a common filter capacitor reduces the output voltage ripple by more than three times when compared to an equivalent-sized single-phase converter [145]. Moroever, the use of differential switching power converters will minimise odd mode stability problems within the HPA [95], [146].

Table 7.8 gives the maximum measured performance of the HPA with normal drain bias supplied by the power supply and a drain bias supplied by the supply modulator. Measurements done on both on-wafer and pcb prototypes was analysed to identify areas for efficiency improvement.

Table 7.8: Evaluation of HPA Max. Performance

	V_{DS} (V)	P_{OUT} (dBm)	DE (%)	PAE (%)	Gain dB
On Wafer	28	39.20	44.73	41.9	15.8
PCB Mounted	28	38.14	37.42	34.98	15.34
PCB Mounted	20	35.41	37.62	34.92	13.47
PCB Mounted	20 **SM**	34.98	28.80	26.65	13.41
PCB Mounted	15	33.87	32.28	29.49	11.55
PCB Mounted	15 **SM**	33.71	21.88	20.34	11.71

The on-wafer measurements delivered the maximum performance in terms of DE, PAE and P_{OUT} and gain. The measured values were 44.73%, 41.9%, 39.20 dBm and 15.8 dB. The prototype pcb measurements revealed DE, PAE, P_{OUT} and gain of 37.42%, 34.98%, 38.14 dBm and 15.34 dB. The reduction in P_{OUT} was -1.06 dBm, while the corresponding reductions in DE and PAE were -7.31% and -6.92%. This reduced performance was attributed to the fact that the back-side of the MMIC chip was glued onto the test jig with silver epoxy which did not form a good thermal interface between the two conducting surfaces, leading to increased thermal dissipation within the chip and hence a reduction in the output power that was delivered. Moreover, the effects of wire-bond inductances and package traces were not considered during the design phase. Hence the efficiency of the HPA can be optimised in the next chip run, by incorporating the package into the RF HPA simulations within the ADS simulator and, instead of epoxy, the chip should be soldered onto the test jig to maximize thermal conduction between the two interfaces.

The reduced operating voltage of 20 V had the critical impact of delivering lower out-

put power of 35.41 dBm, compared to 39.20 dBm measured in the on-wafer scenario. Thus, by the use of integrated level shifters and proper sizing of the transistors, high voltage supply modulator operation can be undertaken without much loss of efficiency. Moreover, adequate thermal management to cool the chips in high voltage, high current operation should ensure better efficiency.

Figure 7.56 shows the power sweep of the HPA at 8.5 GHz showing the calculated and estimated PAE at various drain bias conditions. The calculated PAE for the supply modulated RFPA at a drain bias of 20 V was 26.65% with an output power of around 34.9 dBm. At 15 V supply modulator bias, the PAE was 20.3% with P_{OUT} at 33.7 dBm.

The projected PAE for the design voltage of 28 V is also plotted. Two scenarios are given, a predicted PAE for PCB mounted as well as for on-wafer, which is the ideal scenario. The projected maximum performance for the pcb-mounted HPA was a PAE of 29.45% and an output power of 38.14%. The projected on-wafer performance delivers a PAE of around 34.14% with a P_{OUT} of 39.48 dBm. The projections were based on the efficiency of the supply modulator at a 75% duty cycle. However, due to the increased output power requirements, the size of the modulator power stage will have to be increased to deliver higher current at a much lower duty cycle. Hence a trade-off between efficiency and output power of the supply modulator with the requirements of the HPA needs to be undertaken to maximise the combined overall efficiency while delivering the maximum output power.

The potential for cost savings in terms of reduced weight/volume while delivering higher output powers is very promising, especially in a space-borne system which requires multiple back-up systems in case of failure in the primary system. Moreover, it also opens the possibilities for efficiency enhancement techniques with the drain bias

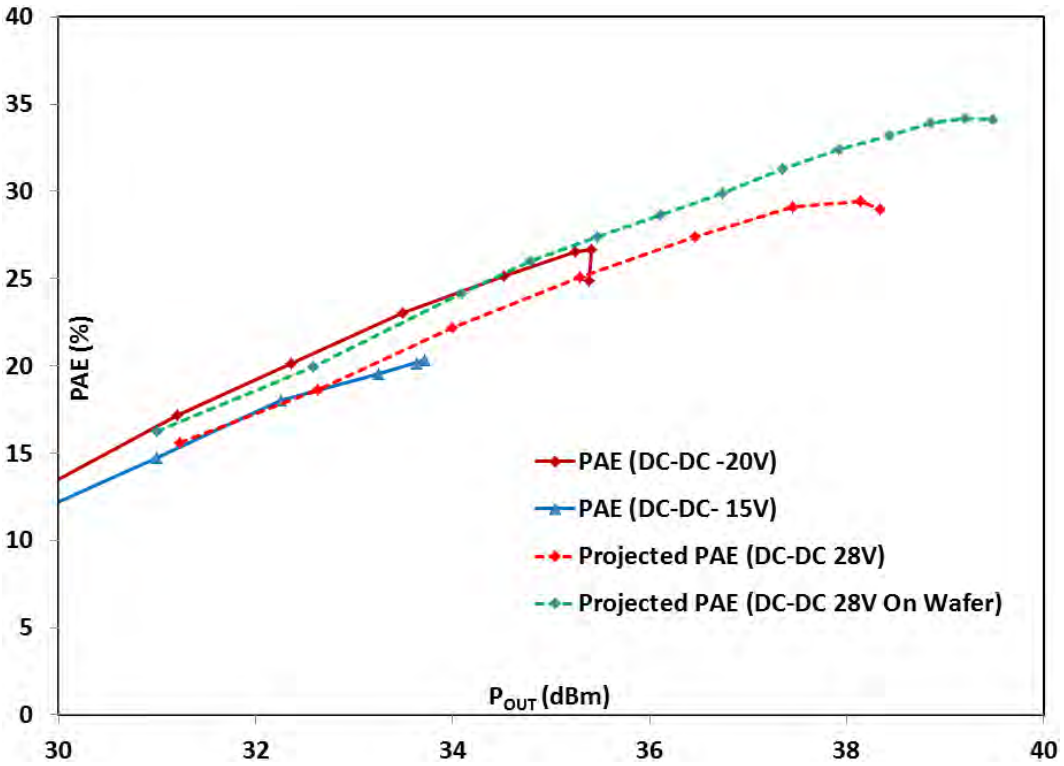

Figure 7.56: HPA PAE Comparisons

modulation techniques presented earlier.

Two supply modulated 0.15 μm X-Band PAs were demonstrated in [128] with a composite efficiency of 23.3% for the modulated supply with a peak output power of 40.3 dBm with a PAE of 65.4% and an output power of 36.5 dBm. The composite PAE was 34.8%. Here the linear stage and the switcher stage used pcb-mounted components, with a switching frequency of 5 MHz. In [129], the switching frequency was increased to 60 MHz, and an RF output power of 1.1 W at an overall PAE of 35.3% for a 20 MHz LTE-A signal was presented.

Table 7.9 shows the supply modulator integrated power amplifiers cited in the literature. The maximum output power for an RFPA integrated with a DC-DC converter was a GaAs design with an RF output power of 40 dBm in the S-Band. The integrated

Table 7.9: State of the Art: SMPS integrated HPA

Ref.	Process	HPA (dBm)	F_0 (GHz)	PAE (%)	SMPS (MHz)	SMPS P_{OUT} (W)	SMPS η(%)	PAE Overall (%)
[94]	0.50 μm GaAs	40	2.9-3.4	40	100	30	75	27
[147] [145]	0.50 μm IPMOS	36.7	0.85-0.95	61	1.6	5	90	55
[148]	0.18 μm SiGe BiCMOS	26 25.2	0.9 0.9	55 51	30 30	.63 .63	81 81	30
[150] [149]	0.35 μm SiGe BiCMOS	21	1.92-1.98	44	89	0.825	78.8	-
[151]	0.35 μm BiCMOS	31	1.95	60	130	2	83	49
This work	0.25 μm GaN	34.98	8-10	40	100	14	77	26.6

converter had an efficiency of 77% with a switching frequency of 100 MHz. The overall PAE was 23%.

A high voltage SOI based power converter integrated RFPA delivered 36.7 dBm in the 0.85-0.95 GHz frequency range. However the switching frequency was very low at 1.6 MHz [147], [145]. Two PA topologies in a SiGe process with a converter switching frequency of 30 MHz are given in [148]. Class E and F with efficiencies of 33% and 31% were used. The output power delivered was 26 dBm and 25.2 dBm respectively The power converter output was 28 dBm with an efficiency of 81%. A 0.35 μm BiCMOS fabricated PA integrated with a DC-DC converter was demonstrated in [149] and [150], with a reported efficiency improvement of 1.46× compared to constant dc bias. An integrated dc-dc converter switching at 130 MHz with a PA delivering 31 dBm was demonstrated in [151]. The chip was fabricated in BiCMOS, and the total efficiency was 49% with 27 dBm of output power for a WCDMA signal.

The work detailed in this chapter is the first reported supply modulator integrated HPA in GaN with a switching frequency of 100 MHz and an efficiency of over 80% at a duty cycle of 75%. The combined efficiency of the supply modulator integrated HPA was 26.6% and it delivered an output power of 34.98 dBm at 8.5 GHz.

7.9 Implications for Airborne/Space based Platforms

In a complex radar systems like the 1200 Tx/Rx element APG-81 Active Electronically Scanned Array [16], with thousands of radiating elements, on chip supply modulator would provide greater flexibility by offering the possibility to independently control individual radiating elements. These would allow improved beam formation, enhanced control and steering for adaptive beam forming. Even with a 1% efficiency improvement, the combined overall improvement would be significant considering the number of active elements in the array. A similar situation would be the case of a satellite like TerraSar-X [152] which provides SAR all-weather imaging capability; the use of distributed on-chip power conversion would enable greater flexibility and improve efficiency while minimising volume/weight which is invaluable in a space-constrained, energy limited system which demands rugged, reliable performance in harsh environments.

In airborne surveillance platforms like IAI's Heron [153] or Northrop Grumman's Global Hawk [20] with a hover time of over 30 hours, the reduced weight, enhanced performance and high temperature operation of supply modulator integrated HPA are very promising features that will improve the efficiency of the on board real-time communication and radar systems leading to efficient use of onboard power supplies.

To summarise, GaN offers a more than five fold power improvement compared to GaAs. A few high power GaN MMICs can be used to replace many low power GaAs MMICs/modules, reducing the overall cost while improving system reliability [5]. Hence by leveraging the inherent strengths of GaN, power conversion and power amplification circuit can be combined to design a supply modulator integrated HPA that would help improve the DC to RF conversion efficiency, reducing power consumption in mission- critical systems.

7.10 Next

Chapter 8, gives a summary of the major achievements of this thesis and gives directions for further research avenues.

8

Conclusions and Recommendations

8.1 Introduction

In this thesis, GaN RF HEMTs were investigated as power switches for integrated supply modulators. The investigation was conducted with a view to integrate a supply modulator and a high power GaN amplifier onto a single die. The work performed as part of this thesis is described in the following section, which and provide an overview of the important results. The background material and literature survery is introduced in chapter 2. Chapter 3 describe the pulsed IV investigation of commercial foundry RF GaN HEMTs as power switches. The role of on-resistance modulation was found to have an impact on the efficiency of the power switch. In chapter 4, a new trap model

was introduced to account for R_{ON} modulation in power switches.

A hybrid modulator topology was used to characterise the devices as power transistors in chapter 5. A new gate driver topology was introduced to minimize the current through the gate drivers. Two modified versions of gate driver topology were introduced in chapter 5 and fabricated in two 0.25 μm GaN process. The measured results have the highest reported output powers and efficiencies for a supply modulator operating at 100 MHz given in literature. Chapter 7 explores broadband RFPA designs in GaAs and GaN process. The X-Band GaAs PA has the highest reported PAE while the GaN supply modulator integrated RFPA is the first of its kind in the world.

Achieving a set of research results usually leads to interesting new questions. Therefore, further avenues for research are recommended.

8.2 Power Switch Pulsed IV Characterization

Trapping phenomena represent a major performance limitation factor for AlGaN/GaN HEMTs. It was observed that the output power measured at microwave frequencies was much lower than what was calculated from the DC parameters. This reduction in output power was attributed to to the presence of traps, and their manifestations have been described using various terms like dispersion, current compression, current collapse, gate/drain lag, power slump etc. In power switching applications, this reduction in output power due to the increase in the R_{ON} severely degrades the switch efficiency [116], [57].

Chapter 3 investigated pulsed IV characterisation of commercial foundry RF GaN

HEMTs to understand how traps affect the device performance when it is used as a power switch. Pulsed IV characterisation was conducted on commercial foundry GaN-on-SiC HEMTs using Diva 265 and Auriga 4750 systems. At high quiescent drain bias voltages, the test devices showed a significant increase in R_{ON} which dramatically reducing the output power.

8.3 Power Switch Trap Model

The integration of power amplifiers, driver amplifiers and LNAs within a space/satellite based Tx/Rx module onto a single die will lead to improvements in the cost, performance and size [2], [3], [4], [5].A recent trend is to integrate the power converter with the RFPA on the same die [95]. Pulsed IV characterisation presented in chapter 3, revealed the effect of traps in RF GaN HEMTs when used as power switches.

Thus, within a power converter integrated MMIC module the same transistors are to be used for different functions and the transistors operate in different quadrants in the I-V plane. Designing each of these functional blocks implies having accurate transistor models for that very specific function. It is very challenging to obtain a valid model that can predict the FET behaviour needed for all the functional blocks. For example, current GaN HEMT models available within the process design kits (PDK) of various foundries all cater for RFPA applications [120].

These models do not capture the quiescent drain bias dependent trap effects that cause a significant reduction in drain current leading to drastic reduction in the output power. When designing integrated power switches in GaN MMIC technologies, accurate simulation models that can predict quiescent bias dependent trapping effects;

in particular R_{ON} modulation becomes crucial for large periphery devices, as MMIC design is very expensive and once fabricated cannot be modified externally.

In chapter 4, a new power switch trap model based on SRH theory is introduced and a PS FET model isS used to simulate the trap model. The Spice simulation accurately predicted R_{ON} modulation and the corresponding current collapse seen in RF GaN HEMTs when used for power switching applications.

8.4 Hybrid Modulator

In this chapter 5, bare die GaN HEMTs manufactured by Cree devices were characterised as power transistors in a hybrid modulator topology. Results are presented for a 12 W and 14 W, 30 V synchronous buck converter prototype operating at 10 MHz. The measured power stage efficiencies peak above 93.1% and 95.8% at 10 MHz and remains above 90% over a wide range of operating conditions.

In order to acurately characterise the circuit for future integration, the driver circuits were also designed with GaN transistors. Due to the absence of p-type transistors in GaN process, the high side driver design is more complicated than that for the low side driver because the gate voltage for the high side must have a very large voltage swing, from below ground to pinch-off the HEMT, to approximately the full power supply voltage. Custom designed GaN Schottky barrier diodes were used as anti-parallel diodes in the power stage.

At a switching frequency of 10 MHz trapping within the power transistor had minimal impact on the overall performance. This is due to the fact that traps within the devices

Table 8.1: Comparison of Hybrid Modulators

Process	Topology	Efficiency(%)	P_{OUT}(W)	V_{DD}(V)
Cree 0.40 μm	ST-R-LT	93.1	12	30
Cree 0.25 μm	ST-R-LT	95.8	14	30

have a very limited time to react due to the high frequency of switching. Hence, the same device which showed trapping at high drain bias voltages and a switching frequency of 500 Hz showed minimal trapping effects when switched at 10 MHz.

It was revealed that the high side gate driver losses were the dominant contributer to the overall loss within the hybrid modulator. Hence minimizing the high side gate driver loss would significiantly improve the overall efficiency of the modulator. An ST-R-LT gate driver topology was introduced to minimize the gate driver current by adjusting the gate peripheries of the transistors and the size of the modulation resistor between them.

8.5 Integrated Modulator

In chapter 6, two supply modulator circuits based on modified ST-R-LT gate driver topologies were introduced and fabricated in a 0.25 μm GaN processes. A bootstrap topology with reduced high side gate driver voltage and a switch node connected high side driver which completely eliminated the need for a the high side driver bias voltage were presented. The modulators were fabricated in the Triquint Semiconductor 0.25μm process. The measured peak efficiencies of the modulators operating at switching frequency of 100 MHz were over 85% while delivering 8 W and 10 W of output power for the Triquint circuits. These modulators have the highest output powers among reported GaN supply modulators. The measured modulators can be used in

Table 8.2: Comparison of MMIC Modulators

Process	Topology	Efficiency(%)	P_{OUT}(W)	V_{DD}(V)
TQS	Bootstrap	81.5	39	30
TQS	Sw. Node	83.5	40	30

envelope amplifiers within an envelope tracking system to accurately track a 20 MHz bandwidth LTE envelope signal.

8.6 Supply Modulator Integrated HPA

In chapter 6, two broadband GaN PA designs in GaAs and GaN processes are explored. In Section I of this chapter an X-Band PA based on WIN Semiconductor's 0.10 μm GaAs technology was designed and fabricated for radar applications. A reactively matched Class-AB topology was chosen and both the input and output matching networks were optimised for highest PAE using commercially available CAD tools. Excellent performance was achieved with a maximum DE of 68.2%, PAE of 62.91%, P_{OUT} of 27 dBm and a corresponding gain of 12.89% , measured at 10 GHz.

The amplifier exhibited excellent broadband characteristics with DE over 50% between 7-13 GHz, a bandwidth of 6 GHz. The corresponding PAE remained over 45.31%, at the low end, while it was over 50% at 13 GHz. The corresponding output power remained over 23.86 dBm at 13 GHz, while between 7-12 GHz, the output power was over 25.79 dBm, peaking at 27 dBm at 10 GHz. The corresponding gain remained over 10.4 dB from 7-12 GHz, and falling to 9.23 dBm at 13 GHz.

The DE between 9-12 GHz frequency range was about 55.79% while PAE was above 51.02%. A review of the literature revealed that most of the published X-Band GaAs

MMIC amplifiers were fabricated in 0.25 μm or larger process. To the best of the author's knowledge, this work reports one of the highest drain and power added efficiencies for a GaAs PA in the 7-12 GHz frequency range.

In Section II, a two stage high power amplifier integrated with a DC-DC power converter was designed and fabricated in 0.25 μm GaN technology for an X-Band Satellite downlink. The X-band HPA had an efficiency of over 41% and delivered an output power of 39 dBm. The supply modulator was characterised over wide operating conditions and resistive loads. It delivered a maximum output power of 14.6 dBm with a peak efficiency of 88%. The combined efficiency of the HPA and supply modulator for a drain bias of 20 V was 26.65%, and delivered an output power of 34.98 dBm. This work reports the first, supply modulator integrated X-Band GaN HPA.

8.7 Future Research Avenues

Following are a couple of areas that can be subject to immediate investigation to fully understand the capabilities of the supply modulator integrated HPA.

8.7.1 Modulation Schemes

The supply modulator can be characterised for complex modulation schemes like 20 MHz LTE-A. A fully dedicated time-domain envelope test bench with digital control of pulse generation will enable the characterisation of the SM integrated HPA under real-time dynamic operation.

8.7.2 Functional blocks

With the availibility of both E-mode and D-mode devices, logic circuits can be implemented to form functional blocks like differential amplifiers, PWM generators, comparators etc [154], [155], [156], [157]. The ultimate goal will be to develop all the ET functional blocks in GaN for a fully integrated Tx/Rx chip that can be used with the appropriate modulation scheme. An integrated class-AB PA can be designed to provide the linear part of the envelope amplifier.

8.8 Conclusion

This work investigated the use of GaN RF HEMTs as power switches for supply modulators integrated with HPA. At the time of submission, this thesis reports the first reported supply modulator integrated X-Band GaN HPA integrated in 0.25 μm process. On-chip power conversion paves the way for new generation of highly efficient HPA for airborne and space based applications.

Appendix-A :

Pulsed I-V Characterization

The pulsed I-V characteristics of the test devices D7, D8 and D9 described in chapter 3 is given in this appendix. The effects of the R_{ON} modulation and current collapse is clearly visible with increasing quiescent bias voltages. The corresponding drain current waveforms (Figure A1 - A12) at three different values of V_{DS}, 1 V (very close to where dynamic R_{ON} was measured), 5 V (just after the V_{KNEE} and 10 V (steady state) clearly indicates the marked reduction in drain current with increasing quiescent drain bias voltages. The spike seen in the transient drain current measurement is due to the fact that the drain is already ON when the gate is pulsed.

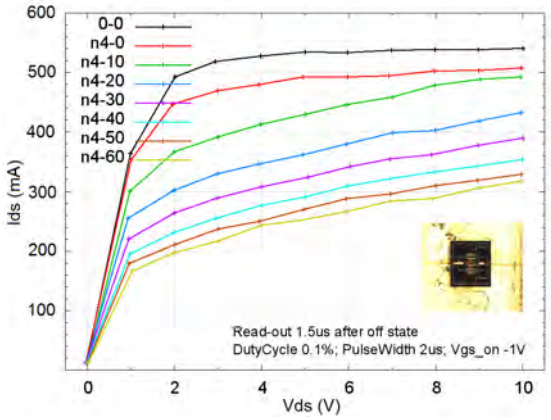

Figure A1: D7-V_{DS} =10V, V_{GS} =-1V

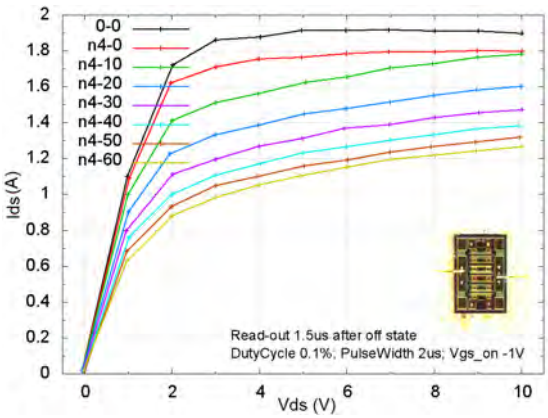

Figure A2: D8-V_{DS} =10V, V_{GS} =-1V

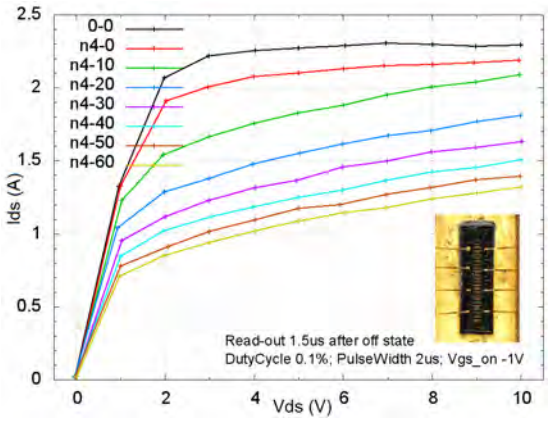

Figure A3: D9-V_{DS} =10V, V_{GS} =-1V

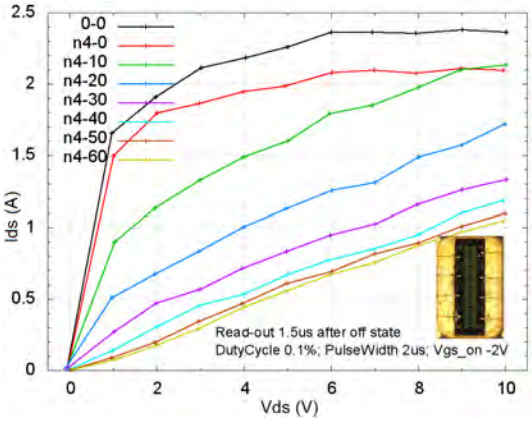

Figure A4: D10-V_{DS} =10V, V_{GS} =-2V

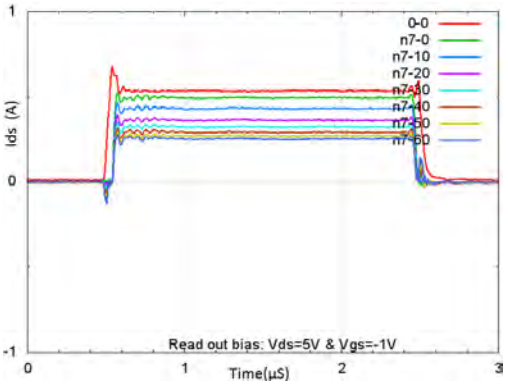

Figure A5: Transient Drain Current: Cree CGH0006, V_{DS} =5V, V_{GS} =-1V

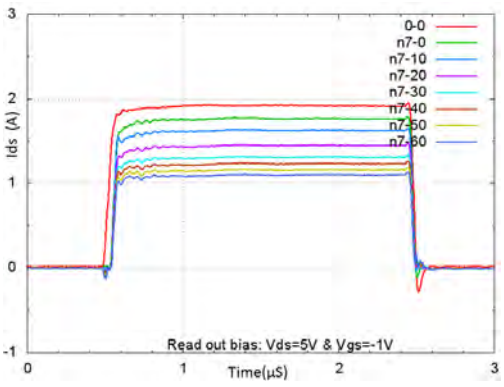

Figure A6: Transient Drain Current: Cree CGH0015, V_{DS} =5V, V_{GS} =-1V

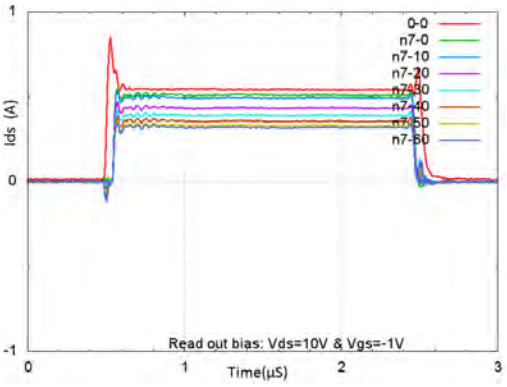

Figure A7: Transient Drain Current: CGH0006, V_{DS} =10V, V_{GS} =-1V

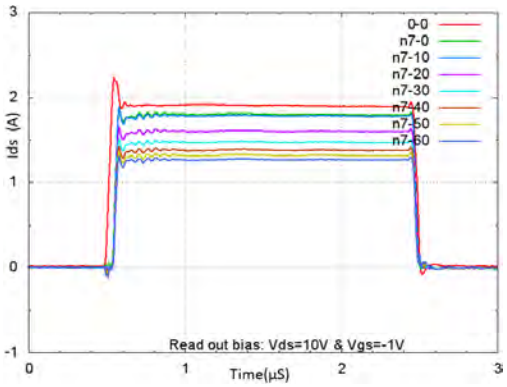

Figure A8: Transient Drain Current: CGH0015, V_{DS} =10V, V_{GS} =-1V

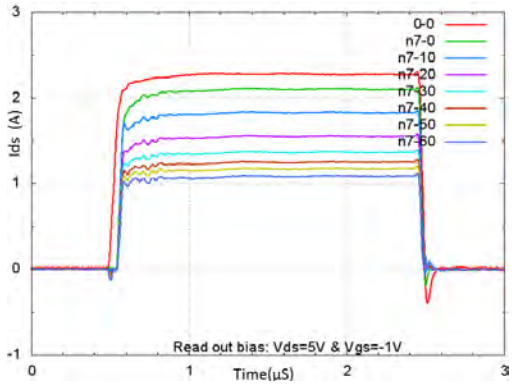

Figure A9: Transient Drain Current: Cree CGH0025,V_{DS} =5V, V_{GS} =-1V

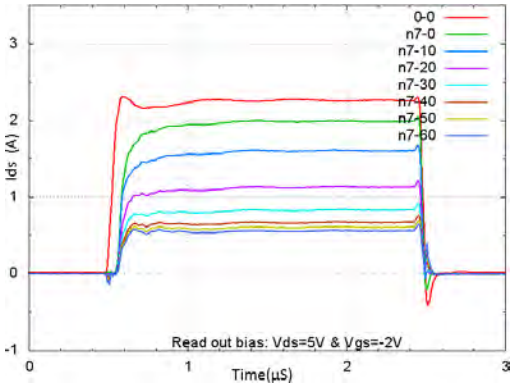

Figure A10: Transient Drain Current: Cree CGH0060,V_{DS} =5V, V_{GS} =-2V

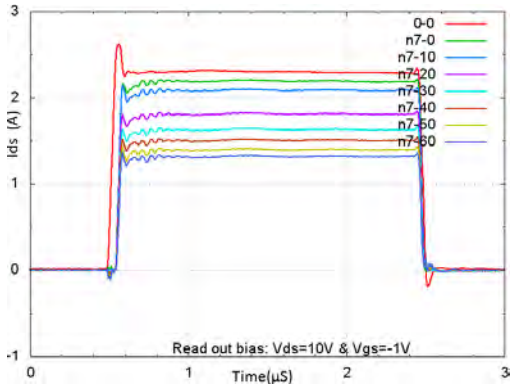

Figure A11: Transient Drain Current: CGH0025,V_{DS} =10V, V_{GS} =-1V

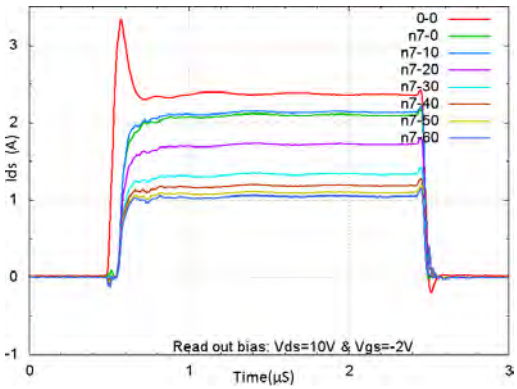

Figure A12: Transient Drain Current: CGH0060, V_{DS} =10V, V_{GS} =-2V

Appendix-B :

Spice Code

The spice code used for simulations in chapter 4 is given below.

Generic Trap-centre Model

.include subckts DES.cir

Thermal Coeffecients

.param n=0.5,fc$_t h$ = 8e9, $f\,o_t h$ = 1000, R_{th}=0.001

.param Tamb=25, DELTA=0.001

Trap Coeffecients

Bulk trapping: A = B

.param alpha=0

.param Vo=5, PHi=-5.5

.param Ai=0.1, Bi=0.1

.param Ci=+1

Note: Ci is either +1 or -1

B = 0

.param alpha=2.5

.param Vo=0.5, PHi=0.14

.param Ci=+1

.param Ai=0.15 Bi=0

FET Coeffecients

.param BETA=1.6, P=1.15, Po=2, GAMMA=0, VTO=-2

.param BETA=0.2, P=1.15, Po=2, GAMMA=0.000001, VTO=-2

.param BETA=0.09, P=0.98, Po=1, GAMMA=0.000001, VTO=-3.5

vtemp ambient 0 Tamb rtemp ambient 0 1e12 DC circuit

VgsDC Gate 0

VdsDC Drain 0

VgsDC Gate 0

VdsDC Drain 0

Viddx Drainx Drain 0

xfetDC Gate Drainx ambient HEMT

CONTROL

.control

destroy all

set DELMIN=1e-20

op

pause

rusage all

DC VgsDC -4.5 0.0 0.001 VdsDC 5 8 1

DC VgsDC -4.5 0.0 0.25 VdsDC 0 8 0.001

DC VdsDC 0 30 0.01 VgsDC -4.5 0.0 0.25

set color2 =lt$_b lue$

$*setcolor2 = lt_r ed$

$*setcolor2 = lt_g reen$

$*setcolor2 = black$

$plotdc1.xfetDC : vt$

$plotdc3.xfetDC : vt$

$plotdc1.i(Viddx)$

$plotdc3.i(Viddx)$

$printdc1.i(Viddx) > IV1d.txt$

$printdc2.i(Viddx) > IV2d.txt$

$.endc$

Subcircuit of thermal network

Thermal path for calculating temperature versus instantaneous power. Ref: Parker and Rathmell, "Broadband characterization of FET self-Heating," IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 7, pp. 2424-2429, July 2005.

Power is injected to node 'sink' at the rate of 1mA/mW.

Temperature is the voltage at node 'sink' in V/degC.

Ambient temperature is the voltage at node 'ambient' in V/degC

Parameters are:

Order of the thermal response 0 ¡ n ¡ 1

Characteristic freqnency of the response fo [Hz]

Ambient temperature Ta

The upper cutoff frequency is set to fc = 8GHz

.SUBCKT ThermalPath sink trap ambient n=0.4 fo=0.08 fc=8e9 Rth=20

.param pi = 3.141592654

.param M = 7

.param a = (((1+n)/(1-n))^(log(fc/fo))/(M + 1)))

$.paramro = (Rth * (a - 1)/(a^{M} + 1) - 1))$

$.paramco = (1/(2 * pi * fc * ro))$

$.paramc = (pow((fo/fc) * log(fc/fo) * (1 - a^M) * (a^M)/$

$+ (1 - a^(M + 1)), -1/M))$

$C0sink0co$

$C110co * c^1$

$C220co * c^2$

$C330co * c^3$

$C440co * c^4$

$C550co * c^5$

$C660co * c^6$

$C770co * c^7$

$R0sink1ro$

$R112ro * a^1$

$R223ro * a^2$

$R334ro * a^3$

$R445ro * a^4$

$R556ro * a^5$

$R667ro * a^6$

$R77ambientro * a^7$

$etraptrap0sink01$

$.ends$

Subcircuit of Trap center

core trap centre.

Charge in trap is that in Ctrap.

vi trap control voltage

Itrap current sink proportional to trap potential

Temperature [V/degC]

Parameters are:

Characteristic frequency of the trap centre fo [Hz]

Temperature at which fo is specified Ta [V/degC]

Fully ionized trap potential Vo [V]

Activation energy of the trap centre EG [eV]

Capacitance used for the trap model Cap [F]

```
.SUBCKT Trap vi Itrap Temperature fo=1000 Ta=20 Vo=1 EG=0.8
+ Cap=10e-6
.PARAM kbar=0.00008617097156814
.PARAM KELVIN=373.15
.PARAM kK= (KELVIN*kbar)
.PARAM EV=EG/(Ta*kbar+kK)
.PARAM LEM=GM/(GM+1)/LMM/SIG
Load for input current
RVi vi 0 1ohm
Primary charge storage element
Ctrap Vt 0 Cap
Temperature variation eliminated while v(vt) is non-physical to
prevent iteration runaways.
Bvh 0 Vh i=kbar*v(Temperature)
RVh 0 Vh 1ohm
```

Temperature corrected characteristic frequency [V/Hz]

Btrap vt 0 i=(v(vh)+kK)$^2 * Cap * fo * 6.28318530718/ + (Ta * kbar + kK)^2 * ($

$+ (exp(EV - EG/(v(vh) + kK))) * (v(vt) * (1 + exp(v(vi)$

$+ /(v(vh) + kK))) - Vo))$

$Outputcontrolingpotential$

$BvTrap0Itrapi = v(vt)$

$resistorstoensuremorethatonecomponentpernode$

$RmaxVt0vt1Tohm$

$RmaxTmTemperature01Tohm$

$.ends$

$Subcircuitoftransistor$

.SUBCKT HEMT g d ambient

+

* FET Coefficients:

+ BETA=0.33 P=1.3 Po=1 Gds=1 Gm=14.29

+ GAMMA=Gds/Gm VTO=-0.71

* Thermal Coefficients:

+ fc$_t h = 8e9 fo_t h = 5n = 0.25 Rth = 20$

+ $Tamb = 30 DELTA = 0.007$

$* TrapCoefficients:$

+ $fo_t rap = 1500 C_t rap = 10e - 6 EG = 0.8 Vo = +0.75 Alpha = 1$

+ $Ai = 0.01 Bi = 0.01 Ci = 1 Phi = 1$

+

Core drain current

jfet dd1 gg 0 fet

Rs dd dd1 R=0.001+alpha*v(vt)

bgg gg g v=GAMMA*v(dd)

edd dd idd d 0 1

vidd idd 0 0

bids d id i=i(vidd)*(1-DELTA*(v(temperature)-Tamb))

vid 0 id 0

.model fet njf level=2 beta=BETA vto=VTO q=P+1

+ p=P+Po xi=0.1

Thermal path

bheat 0 temperature i=(v(d)*i(vid)¡ 0 ? 0 : v(d)*i(vid))

xThermalPath temperature traptemperature ambient ThermalPath

+ n=n fo=fo$_t$$hfc = fc_thRth = Rth$

$Trap$

$bvi0vii = Phi + Ci * ((Ai - Bi) * v(g) + Bi * v(d))$

$xTrapvivttraptemperatureTrapfo = fo_trap + Ta = TambVo = VoEG = EGCap = C_trap$

$RmaxVtvt01ohm$

$resistorstoensuremorethatonecomponentpernode$

$Rmaxaambient01Tohm$

$Rmaxgg01Tohm$

$.ends$

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