MODELLING RADIO FREQUENCY GaN HEMT USING PHYSICS-BASED MODEL IN AWR

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STATEMENT OF CANDIDATE

I, Gajan Panuraj, declare that this report, submitted as part of the require-
ment for the award of Bachelor of Engineering in the Department of Electronic
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ABSTRACT

The modelling of an ASM-GaN HEMT in low cost and high durability with long life periods will definitely attract the industrial development in the semiconductor mass production activities. There are many companies involved in the mass production of GaN transistors; due to this reason GaN transistors are available in the common market with various brand names. The research on modelling Radio-Frequency GaN HEMT using physics based model in AWR to extract the DC parameters and RF parameters are widely analysed in this thesis research paper. The first portion of this research paper is giving background knowledge to the reader regarding the GaN transistor and RF Performance. Then the body of this research paper would contain the ASM-GaN-HEMT model, modelling, application of Verilog-A language, which will be incorporated with AWR in this project, simulation and tuned results of the DC parameter and RF parameter extraction with GaN model and AWR IV characteristics and S-parameters. Then the report will further discuss the results, future work on modelling and conclusion of the GaN HEMT modelling.

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Chapter 1

Introduction

1.1 Aim

This thesis project is the vision of Dr. Sourabh Khandelwal who is a supervisor of this project. I am tasked with modelling Radio-Frequency GaN HEMT Triquint 8x40 device using physics based simulation model in using Instruments Applied Wave Research (AWR) Microwave Office Software (MWO) to simulate and tune the GaN-HEMT model to build IV characteristics graph and S-parameters. The Verilog-A codes are applied in RF Power Amplifier Circuit and convert that codes to successfully simulate it on AWR.

The main scope of the research is to modelling the device to the measured data and ways and means to prolong the reliability of the GaN transistor, which is in the usage of modern technology. This will ensure the reliability, cost-effective and user-friendly of GaN HEMT that is going to be modelled during this research project.

1.2 Scope of thesis

I hope the favourable results of this research may be applied the modelled GaN transistor, which will be used in assemble of new equipment and appliances will be get benefitted in the future. I humbly request the readers to contribute me valuable ideas and comments for the favourable success of this project. It will not be able to complete the tasks without observation, investigation, modification, knowledge and experience in the design efforts of this research.

Chapter 2

Literature review

2.1 GaN Technology

2.1.1 Silicon Power MOSFETs

The cost and power management efficiency for more than last 30 years have proportionately increased due to the innovation of power metal oxide silicon field effect transistor (MOSFET) structures technology and circuit topology are relevant to the demand of electricity in the day to day life. The development of silicon power MOSFET used after the year 2000 closely approaches its theoretical values. Power MOSFETs replaced the bipolar transistors during 1976. The MOSFET is very faster, hardwearing and consists of higher current gain. These above aspects cause switching power conversion become a commercial. [10]

2.1.2 Properties of wide bandgap semiconductors

Highest electrical characteristics consist of the wide bandgap semiconductor materials related to Si. Related to other semiconductors, diamond is leading as the widest bandgap material. Therefore diamond should have a highest electric breakdown field. Semiconductors such as SiC and GaN consist of almost same bandgap and electric field values compared to other semiconductors. In order to function in greater temperatures, semiconductors should have wider bandgaps. This property of the diamond devices allows functioning in greater temperatures. Greater electric breakdown field is directly related to greater breakdown voltage in the power device. When the greater electric breakdown field is exerted on a material with the highest doping, then the gap will be widening among the upper breakdown voltage limits.

	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
JFM	1.0	1.8	277.8	215.1	215.1	81000
BFM	1.0	14.8	125.3	223.1	186.7	25106
FSFM	1.0	11.4	30.5	61.2	65.0	3595
BSFM	1.0	1.6	13.1	12.9	52.5	2402
FPFM	1.0	3.6	48.3	56.0	30.4	1476
FTFM	1.0	40.7	1470.5	3424.8	1973.6	5304459
BPFM	1.0	0.9	57.3	35.4	10.7	594
BTFM	1.0	1.4	748.9	458.1	560.5	1426711

JFM : Johnson's figure of merit is a measure of the ultimate high frequency capability of the material.	**FPFM :** FET power handling capacity figure of merit
BFM : Baliga's figure of merit is a measure of the specific on-resistance of the drift region of a vertical FET	**FTFM :** FET power switching product
FSFM : FET switching speed figure of merit	**BPFM :** Bipolar power handling capacity figure of merit
BSFM : Bipolar switching speed figure of merit	**BTFM :** Bipolar power switching product

Table 2.1: Wide bandgap semiconductors-Merits.

The next important parameter is the thermal conductivity. It is better to have a greater conductivity because when the higher conductivity will slower the temperature rise on a device. Diamond has a higher thermal conductivity and GaN has lower thermal conductivity. The merits performance depends on the number of merits, the larger number will give better performance on power electronics. Diamond has multiple times greater than other semiconductor materials compare to other semiconductors. The above Table 2.1: Wide bandgap semiconductors-Merits explains the merits number compare to Si. GaN and SiC have a similar number of merits that could lead both semiconductor materials to give the very similar performance. Si and GaA would give very poor performance compared to other semiconductors according to the Table 2.1 above. Semiconductor GaN would be used in optoelectronics and RF devices since it consists of direct bandgap and greater frequency performance. When GaN compared to SiC, GaN does not have oxide. The oxide is very important to use it in MOS devices. GaN substrates are less available in the industry, which makes it a bit more expensive than SiC. When we look at the future semiconductor technology growth, wider bandgap materials give more growth in future.

Diamond has good electrical properties and Research and development on this technology are still in early stages and it might be expensive to use the diamond on an electronic circuit. When we compare other semiconductors GaN and SiC have very similar electric properties and these two semiconductors are expect to grow and dominate the industry in near future. [13]

2.1.3 GaN

Gallium Nitride High Electron Mobility Transistor (HEMT) first produced during 2004 with depletion mode radio frequency (RF), transistor using GaN on Silicon Carbide (SiC) substrates rarely High Electron Mobility defined as a two-dimensional electron gas in the area of an Aluminium Gallium Nitride (AlGaN) and GaN heterostructure interface. Eudyna Corporation invented this technology in Japan, produced benchmark power gain in the multi-gigahertz frequency range in the year 2005.

The SIGNATIC®was invented by the Nitronex Corporation during the year of 2005 and they used the same technology first time to initiate the depletion-mode RF HEMT device consist with GaN grown Silicon wafers.

GaN RF transistors now use most of the RF applications. A lot of companies are involved in the manufacture of the GaN transistors therefore different brands are available in the market and the cost of the product varies according to the brand in the market. The disadvantage of depletion-mode operations, which needs a negative voltage on the gate to shut down the system. The initial enhancement-mode GaN on Silicon (eGaN®) FETs was introduced in June 2009 by the Efficient Power Conversion Corporation (EPC).

The newly produced eGaN FETs will function without using negative voltage to turn off. Mass production of eGaN FETs causes the product cost very low by utilizing standard silicon manufacturing technology. This is the main reasons for the replacement of power MOSFET.

Efficiency, reliability, controllability and cost effectiveness are very important factors for semiconductors, which are used in power conversion. These above factors of a row material in the manufacturing process for the semiconductors will be considered as an economically viable and profitable. It may have a lot of materials can be considering as a replacement to Silicon, Silicon Carbide and Gallium Nitride. We can analyze the characteristic performance of the different materials such as Silicon, Silicon Carbide and Gallium Nitride, which are utilized in the next generation of a power transistor. [10]

2.1.4 Advantage of Gallium Nitride

The influence of Silicon involved after 1950. The merits of Silicon compare to other semiconductors either Germanium or Selenium can be expressed as follows: Silicon entitled

new applications that were impossible with other materials, Reliability of Silicon is very high, Silicon can be easily used in various ways and most affordability of Silicon devices.

The above advantages supporting from the main physical properties of silicon joined with an extremely large venture in production infrastructure and engineering.

The following Table 2.2 is a comparison of electrical properties of 3 semiconductor materials such as Silicon, GaN and SiC:

Parameter		Silicon	GaN	SiC
Band Gap E_g	eV	1.12	3.39	3.26
Critical Field E_{Crit}	MV/cm	0.23	3.3	2.2
Electron Mobility μ_n	cm^2/V·s	1400	1500	950
Permittivity ϵ_r		11.8	9	9.7
Thermal Conductivity λ	W/cm·K	1.5	1.3	3.8

Table 2.2: Properties of Si, Gallium Nitride and Silicon Carbide.

2.2 RF Performance

The RF function of GaN transistors and in specific enhancement-mode transistors could be examined focusing particular RF applications, which could be an advantage from its acquisition.

GaN semiconductor material has been used to manufacture High electron mobility transistor (HEMT). This is a depletion-mode transistor and it can be used in RF power amplifier. The potential of device failure could occur due to the power raised because of the short condition and this can be reduced in the RF design. There is a disadvantage in enhancement mode device because negative gate voltage is needed to regulate the drain current, which needs extra circuitry for gate circuit biasing on depletion mode transistors.

GaN RF transistors are main rival in the operating range from 500MHz to 3GHz to the laterally diffused metal oxide semiconductor (LDMOS) FET that made out of Silicon. GaN RF transistors are strongly recommended compare to LDMOS transistors due to its remarkable RF performance especially with power density, frequency range (bandwidth) and noise figure. That initiates to develop in Radio-Frequency power efficiency from transistors within the very wide frequency range. Furthermore, higher impedance is caused by the lower input and output capacitance, which permits higher drains efficiencies and decreases impedance transformation ratios needed for matching. Thus increase the amplifier efficiency, reduction of size and the cost.

The initial stage in a pulsed-RF application the biased circuit should be functional before main power and RF are utilized to obstruct switching on with very high current, which causes possible damage to the circuit. Hence, RF circuits get advantages of utilizing enhancement-mode transistor.

V_{GSQ}	RF circuit gate voltage quiescent bias point
I_{DQ}	Drain current in the transistor at the quiescent operating point
P_{DQ}	Power losses at the quiescent operating point
P_{DC}	DC power delivered to the RF transistor
P_{RFout}	Output RF power
η_D	Drain efficiency – the ratio of P_{RFou}/P_{DC}
s_{11}	Input port reflection coefficient: the percentage of the input incident wave that is reflected back from the input port
s_{12}	Reverse gain: the percentage of the output port incident wave that is reflected to the input port
s_{21}	Forward gain: the percentage of the input port incident wave that is reflected to the output port
s_{22}	Output port reflection coefficient: the percentage of the output incident wave that is reflected back from the output port
K	Rollett stability factor
C_S	The source-side stability circle center on a Smith chart
C_L	The load-side stability circle center on a Smith chart
C_A	Constant available gain circle center on a Smith chart
R_S	The source-side stability circle radius on a Smith chart
R_L	The load-side stability circle radius on a Smith chart
R_A	The radius of the constant available gain circle on a Smith chart
Γ_{in}	Input reflection coefficient of the transistor
Γ_{out}	Output reflection coefficient of the transistor
Γ_S	Input-side matching reflection coefficient
Γ_L	Output-side matching reflection coefficient
G_T	Transducer power gain
G_{TU}	Unilateral transducer power gain
U	Unilateral figure of merit
g_u	Normalized unilateral transducer gain
G_A	Available gain
G_{MSG}	Maximum stable gain of the transistor
X	Matching network series reactance
B	Matching network shunt susceptance

Table 2.3: Table: Definition of phrases.

2.2.1 Characteristics of RF transistors

Radio Frequency transistors are produced to function ideal in the linear region of the transfer characteristics to increase the power gain of Radio Frequency and decrease the distortion of Radio-Frequency signal. The RF apparatus have assessment metrics such as drain efficiency, 1dB compression or linearity and power gain. The power gain finds out the input signal amount including power, which is amplified by the transistor. The maximum output power that can be passed by the transistor without distorting the signal can find out by the 1dB compression. The drain efficiency finds out the amplifying efficient and ability of the transistor.

RF signal is superimposed due to Radio Frequency device is biased within the limits of the operating point. In addition, the transistor can be biased by the drain-to-source current, which will set the voltage remains as a supply voltage.
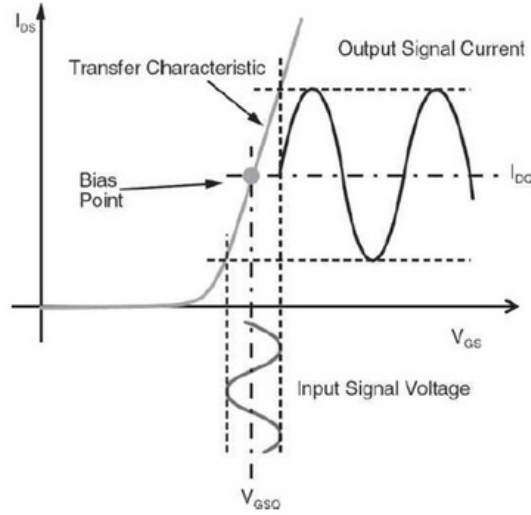
Figure 2.1: Relationship between Enhancement-Mode Transistor and Transfer characteristic.

Figure 2.1 layout about the transfer characteristic of the transistor. According to the Drain to source current $(I_{DS})Vs$. Supply voltage (V_{GS}) graph Bias point is a quiescent point or Q-Point of bias voltage (V_{GSQ}) and bias current (I_{DQ}).

The bias point can be related with losses $(P_{DQ} = I_{DQ}.V_{supply})$ may cause RF devices consumed higher operating power(P_{DQ}) loss ratio with relevant to the power delivered (P_{RFout}).

$$Drain efficiency(\eta_D) = \frac{power delivered(P_{RFout})}{DC power delivered to transistor P_{DC}}$$

Power loss ratio could reach up to theoretical maximum 50 percent when RF FET is used in Class A power amplifier. Therefore RF transistors have the capability to loose the thermal dissipation of power to the environment.

The S-parameters are the common metric utilized to define the Radio Frequency device. This is used to the caliber of reflection, incident, and transmission of electromagnetic waves. Furthermore, s-parameters can define GaN technology Radio Frequency transistors.
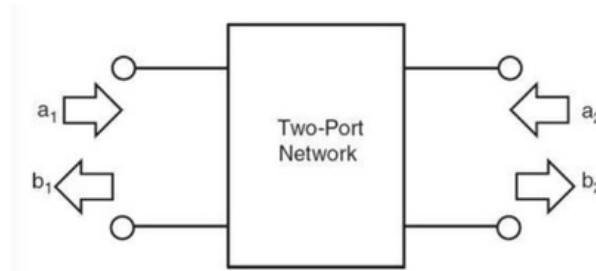
Figure 2.2: Incident waves (a) and reflected waves(b) in the two-pot network.

It is agreeable to explain a transistor Figure 2.2 express the two-port network simple diagram that is specifying the incident waves mentioned by a_1 and a_2 and then reflected waves mentioned by b_1 and b_2. In addition, each and every incident wave on a port could be reflected on both sides to the ports. This could be explained as an incident wave at port 1, which is referred as a_1, then it can be reflected from port 1 b_1 or it can be further infiltrated to port 2, reflected and referred as b_2.
The fraction between reflected (b_1 and b_2) and incident (a_1 and a_2) waves called as S-parameters. It is given by the equation below.

$$S_{nm} = \frac{b_n}{a_n},$$

Where S_{nm} is a general form complex number

$$S_{nm} = \Re(S_{nm}) + i.\Im m(S_{nm})$$

Port 1: Input port or gate.
Port 2: Output port or drain.
The two-port network characteristic for instance; impedance, gain, and isolation can be derived from the s-parameters.
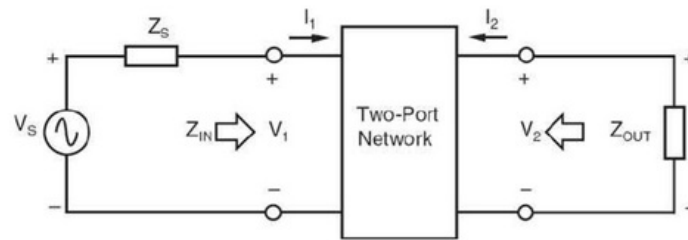
Figure 2.3: Source and load in the two-port network.

The technique is illustrated widely explained in Figure 2.3, which views the input and output impedance for the above ports are provided by the two port network linked to a source and load.

A Smith chart is an essential document that can be used change the s-parameters into impedance.

2.2.2 RF transistor metrics

The RF power gain is a primary metric for RF transistor performance assessment. The transistor's limit of linear performance can be defined by the maximum power gain.

The following Table 2.4 furnishes the detail of Nitronex NPT1012 datasheet for Radio Frequency metrics of the depletion-mode GaN on silicon HEMT in different operating status.

RF Specifications (CW, 3000 MHz): V_{DS} = 28V, I_{DQ} = 225mA, T_C = 25°C, Measured in Nitronex Test Fixture

Symbol	Parameter	Min	Typ	Max	Units
P_{3dB}	Average Output Power at 3 dB Gain Compression	43	44	-	dBm
P_{1dB}	Average Output Power at 1 dB Gain Compression	-	43	-	dBm
G_{SS}	Small Signal Gain	12	13	-	dB
η	Drain Efficiency at 3 dB Gain Compression	57	65	-	%
VSWR	10:1 VSWR at all phase angles	No damage to the device			

Figure 2.4: Radio Frequency metrics of the transistor data from Nitronex NPT1012 datasheet

RF power gain is calculated from the amount of power either increased or decreased

when the input current is fed to the port. Mathematically it can be written as follows:

$$G = \frac{P_{out}}{P_{in}}$$

The above equation can also logarithmically stated in decibel (dB) units as below:

$$G = 10.log(\frac{P_{out}}{P_{in}})$$

The linearity could be stated for an amplifier should have a set gain value. Linear correlation among the input and output power according to the gain definition define the set gain value. The amplification saturation may occur when there is a loss in gain at its limit. Linearity is referred as linear dynamic range, which has a limit of 1dB compression point. The value of gain can be a constant when the function of input power unit is up to exceeding a specific value for an RF transistor. The ideal forecasted power is varied by 1dB on measured output power amplifier; this point is specified as 1dB compression point. The output power can be indicated as a function of the input power according to the Figure (a). The gain as a function of input power is also specified the equivalent results as shown in Figure (b). The gain shall lead to reduce, then the output power would be non-linear towards the input power after a specific, on top of the input power level.
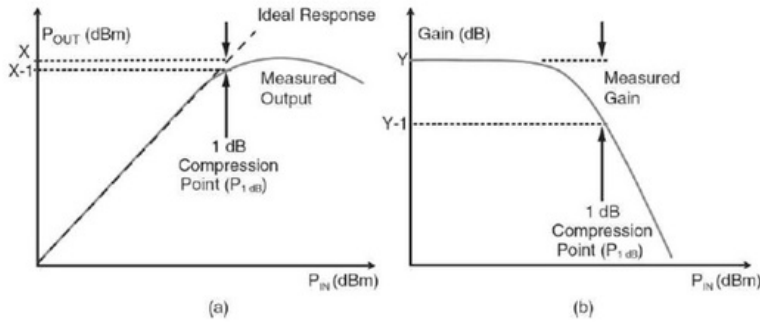
Figure 2.5: (a)1dB compression point and (b) Gain graph explain linearity

A datasheet of a transistor is specified at a precise frequency and biasing status. The power gain would depend on a frequency span and established as a precise bias setting. Class A RF power amplifier can be designed by using small-signal s-parameters, where as large signal s-parameters are required to forecast the power performance.

The transistor's Radio Frequency characteristics need some stages. The process is initiated with device's s-parameter measurements. The s-parameters can identify the type

of function of the device it is either unilateral (reverse gain can be negligible) or bilateral (reverse gain exceed high limit may affect stability). The design of amplifier depends on stability criteria, which is very important to design the type of amplifier either it is in class A or class AB. The vector network analyser is used to calibre the small-signal s-parameters to the transistor below specific biased conditions. Various measurements must be needed to define the bias condition, which turnout the maximum function metrics.

2.2.3 Testing of pulse for thermal consideration

The Radio Frequency devices consist of the large proportion of power dissipation for power output; hence it is needed significant cooling, in this instance power dissipation surpasses the capacity of the device, therefore pulse mode analysis could be used. The largest numbers of Radio Frequency amplifier is functioned with constant Radio Frequency signal and bias and it is called as continuous wave (CW) function. The average power dissipation in this device is reduced by the Pulse testing. Following Figure 2.6 indicates the pulsed testing by utilizing the bias pulse and pulsed Radio Frequency signal.
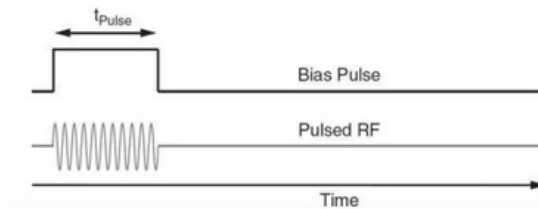
Figure 2.6: Pulsed Radio Frequency testing by using bias pulse Radio Frequency signal.

Error measurements could be reflected by unsteady drain bias current during the on-state of the pulse. It is very hard to carry out this task on Class A amplifier due to the increase the drain current in relevant to increase in RF power without identify the bias and the RF component. The oscillation and bias stability, which is triggered by an undesirable ringing of the drain that could cause by the quick variations in gate voltage. RF and bias requirement should be satisfied by the options of bias tees for pulse testing, it might be demanding due to the frequency response of the bias tees.

2.2.4 Analysing the s-parameter

It is very important to analyse the s-parameters and its data to be used to design an amplifier. The process consists of testing for stability concern and deciding the input and output reflection coefficients of the device.

2.2.5   Test for stability

It is essential to find out the stability of that device either it is conditional or unconditional. The device will not oscillate even though it was pronounced as unconditionally stable but remain stable during the oscillation. This is disregarding of the impedance connected to its gate or drain. Unconditional stability test can be referred as Rollett stability factor where K can denote it.

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2.|s_{12}s_{21}|} \geq 1 \, and |\Delta| \geq 1 \, where \Delta = (s_{11}.s_{12}) - (s_{12}.s_{21})$$

If this stability criterion for either K or $|\Delta|$ unsatisfied at that point. The transistor can be named as conditionally stable. The technique shows that each scheme utilizing the transistor should by pass the unstable region. Stability circle draws on a Smith chart can be used to identify the region of the unstable location. The following equations are used to calculate the stability circles.

$$C_s = \frac{(s_{11} - \Delta.s_{22}^*)^*}{|s_{11}|^2 - |\Delta|^2}$$

$$R_s = \frac{|s_{12}.s_{21}|}{|s_{11}|^2 - |\Delta|^2}$$

$$C_s = \frac{(s_{22} - \Delta.s_{11}^*)^*}{|s_{22}|^2 - |\Delta|^2}$$

$$C_s = \frac{|s_{12}.s_{21}|}{|s_{22}|^2 - |\Delta|^2}$$

The complex conjugate of the parameter is denoted as the superscript asterisk (*), which is also called as the reflection if the parameter.

Complex conjugate for S_{nm} can be written as below.

$$S_{nm}^* = \Re(S_{nm}) - i.\Im m(S_{nm})$$
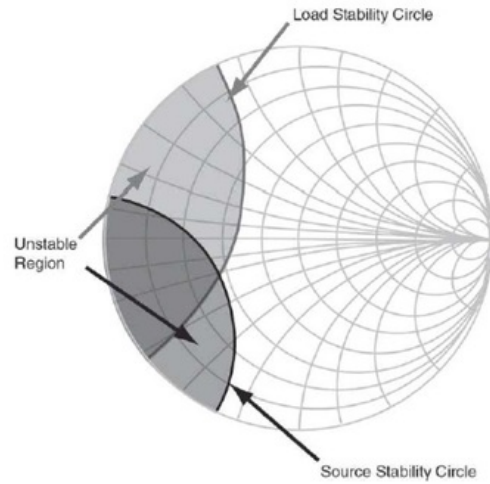
Figure 2.7: Characteristic of Stability circle

The stability circle would cover the unstable region inside it according to the Figure2.7.

2.2.6 Input and output reflection in a Transistor

The Radio Frequency transistor can be utilized in an amplifier design for input and output matching networks, which transform the standard source impedance (Z_o) and standard load impedance (Z_0) to desired values Γ_S and Γ_L.
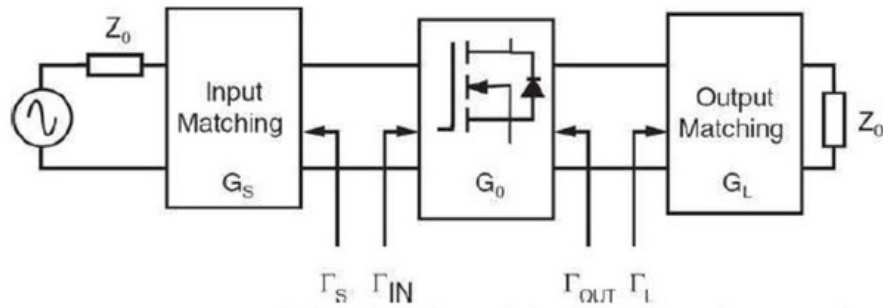
Figure 2.8: structure of Basic amplifier.

Despite the fact of view the similar codification the transistor input and output reflection coefficient are not directly specified by S_{11} and S_{22} but it is specified as input gate circuit (Γ_{in}) and output drain circuit (Γ_{out}). This is the outstanding effect of the

transmission coefficient S_{12} and S_{21} short impacts the input and output as load and source impedance respectively. This is referred in the equations as transistor input and output reflection. The load network referred as input reflection and the source network referred as output reflection.

$$\Gamma_{in} = S_{11} + \frac{S_{12}.S_{21}.\Gamma_L}{1 - S_{22}.\Gamma_L}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}.S_{21}.\Gamma_S}{1 - S_{11}.\Gamma_S}$$

2.2.7   Transducer Gain

Transducer power gain, which is denoted as the proportion of the power delivered to the load to the power offered from the source. There are three multiple gain components that are referred as follows: gain of the source side matching denoted as G_L , gain of the transistor denoted as G_0 and gain of the load side matching . All these components are formulating the transducer gain, which is denoted as G_T that can be referred as the following equation.

$$G_\Gamma = G_S.G_0.G_L$$

$$G_S = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{in}.\Gamma_S|^2}$$

$$G_0 = |S_{21}|^2$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{out}.\Gamma_L|^2}$$

2.2.8   Unilateral/bilateral transistor test

The unilateral transistor can be determined that its S_{12} parameter is considered to be very small compare to the parameters of S_{21}, where as physically a value of zero is not possible for S_{12} parameters. The results of the test will decide on the properties of the transistor whether it is bilateral or unilateral. The equation can be derived from substituting Γ_{in} and Γ_{out} by applying S_{11} and S_{22}correspondingly. A unilateral transducer gain (G_{TU}) could be derived from this equation. The ratio of the transducer gain should be used to define normalize unilateral transducer gain as below.

$$g_u = \frac{G_T}{G_{TU}}$$

which is bounded as below:

$$\frac{1}{(1+U)^2} < g_u < \frac{1}{(1-u)^2}$$

where as U is the unilateral figure of merit and given as follows:

$$U = \frac{|S_{11}|.|S_{12}|.|S_{21}|.|S_{22}|}{(1 - |S_{11}|^2).(1 - |S_{22}|^2)}$$

A transistor could be considered as unilateral if g_u is less than 10 percentage of unity, if not it should be considered as bilateral. Theoretically, unilateral transistor will be considered as stable by characterisation but the device efficiently might not have a feedback mechanism. The unilateral amplifier design is very clear and notable as Γ_{in} and Γ_{out} then it could be simplified to S_{11} and S_{22}. The same procedure is adopted to design an amplifier using a bilateral and unilateral transistor.

Chapter 3

Physics based GaN RF model

3.1 ASM-HEMT 1.0.0

The latest usage of Gallium Nitride created High Electron Mobility Transistor (GaN-HEMT) ensured as competing for technology for high frequency, high power and high voltage in the appliances. Precise and powerfully built circuit simulation is absolutely necessary, in order to make use of a maximum output of the device. The compact model utilised for GaN HEMT highly determined by the precise and merged simulations. The temperature and device geometry are relevant to the physics-based compact models, which are ideal benefits of exceptional model scalability. This model can elaborate about the device operation. This is an Advanced SPICE Model for GaN HEMT that is referred as ASM-GaN-HEMT. This model is very useful to designate terminal current, trapping effect, charges, thermal and flicker noise of the GaN device more precisely. ASM-GaN model is used in Radio Frequency and power electronics gadgets. This paper will cover more about ASM-HEMT model equations; drain current model, self-heating model, capacitance model and parameter extraction procedures in following subsections.

3.1.1 ASM-HEMT 1.0.0 model overview

The model can classify as three components such as core channel-charge, core terminal current and charge model. The HEMT device function is consisting of the creation to the 2-DEG, which is fundamental for the above. It was initially concentrated on establishing a physics-based model to 2-DEG charge density(n_s). The key threat in "modelling the 2-DEG charge density is caused by the complex or problematic differences of the Fermi-level(E_f) alongside (n_s) on the quantum well". While using Schrodinger and Poisson's equations onwards with the carrier statistics to GaN HEMT system that gives the results in the form of transcendental equations mentioned in [11]. Only considering a compact modelling, methodical clarifications would be anticipated because it will cause a sudden reduction in the circuit simulation velocity, which will be built on numerical methods. Analytical solution of this equation can be derived by dividing the differences of Fermi-level relevant to the gate voltage (V_g) in the different regions. The relevant regions are

located and depending on the point of Fermi-level corresponding to the energy levels of E_0 and E_1. The results of the analytical solutions consist of the entire region that can be connected as a single unified expression, which is very precise throughout entire regions. The fundamental model formations can be utilised to advance the model to the drain current (Id) for GaN HEMT. The model can be developed by using the current continuity and make the suitable incorporation outward potential with the channel below the gate. Thereafter the fundamental model has to be integrated with different actual devices. "These are the following effects of the actual devices such as velocity saturation effect, mobility field dependence, channel-length modulation, drain-induced barrier lowering, subthreshold-slope degradation, non-linear series resistances, self-heating effect and temperature dependence". Substantially connected parameters, which can keep the model analytical and these are highly beneficial for circuit simulation.

The capacitance has to be modeled accurately to ensure the perfectly simulated transient and frequency response to the device. The entire terminal charges with accurate charge model to the device are available in the ASM-GaN-HEMT model. Enable to get good merging properties, the charge model ensures from Ward-Dutton partitioning and remains to charge accumulation. Furthermore, gate current (I_g), flick noise and thermal consist in the ASM-GaN-HEMT model. In order to create the model entirely reliable consistent base calculations for the following gate current, noise and terminal charge are used in the model. In addition, RC network sub-circuits can be also utilized in the model for modeling the RF devices and trapping effects.

3.1.2 Model equations

Equations for Voltage calculation

$$V_{ds} = V_d - V_s$$

$$V_{gs} = V_g - V_s$$

$$V_{gd} = V_g - V_d$$

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.01}$$

$$V_{off,DIBL} = VOFF - (ETA0 - TRAPETA0 \cdot vcap + eta0_{trap}) \cdot \left(\frac{V_{dsx} \cdot VDSCALE}{\sqrt{V_{dsx}^2 + VDSCALE^2}} \right)$$

$$V_{gs,min} = V_{off,DIBL}(T) + V_{tv} \ln \left(\frac{L}{2Wq.DOS.V_{tv}^2} \right)$$

$$V_{gs,eff} = \frac{1}{2}\left((V_{gs} - V_{gs,min}) + \sqrt{(V_{gs} - V_{gs,min})^2 + 0.0001}\right)$$

$$V_{g0} = V_{gs,eff} - V_{off,DIBL}$$

$$V_{g0,eff} = \frac{1}{2}\left(V_{g0} + \sqrt{(V_{g0}^2 + 4ep_{psi^2})}\right)$$

$$V_{dsat} = \frac{(2VSAT(T)/\mu_{eff})\,L \cdot V_{g0,eff}}{(2VSAT(T)/\mu_{eff})\,L + V_{g0,eff}}$$

$$V_{d,eff} = V_{ds}\left(1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{DELTA}\right)^{\frac{-1}{DELTA}}$$

$$V_{gd0} = V_{g0} - V_{d,eff}$$

$$V_{gd,eff} = \frac{1}{2}\left(V_{gd0} + \sqrt{(V_{gd0}^2 + 4ep_{psi^2})}\right)$$

Equations for Bias Independent calculations

$$C_g = \frac{\epsilon_{AlGaN}}{TBAR}$$

$$C_{g,fp} = \frac{\epsilon_{AlGaN}}{DFP}$$

$$C_{g,sfp} = \frac{\epsilon_{AlGaN}}{DSEF}$$

$$\beta = \frac{C_g}{q \cdot DOS \cdot K_B.T_{dev}}$$

$$\alpha_n = \frac{e}{\beta}$$

$$\alpha_d = \frac{1}{\beta}$$

Temperature Dependence

$$T_{dev} = T + V_{rth}$$

$$cdsc = 1 + NFACTOR + (CDSCD + cdscd_{trap}) \cdot V_{dsx}$$

$$V_{tv} = KB \cdot T_{dev} cdsc$$

$$V_{off,DIBL}(T) = V_{off,DIBL} - \left(\frac{T_{dev}}{TNOM} - 1\right) \cdot KT1 + TRAPVOFF \cdot vcap + voff_{trap}$$

$$U0(T) = U0 \left(\frac{T_{dev}}{TNOM}\right)^{UTE}$$

$$VSAT(T) = VSAT \left(\frac{T_{dev}}{TNOM}\right)^{AT}$$

$$NS0ACCS(T) = NS0ACCS \left(1 - KNS0 \left(\frac{T_{dev}}{TNOM} - 1\right)\right) \cdot (1 + K0ACCS \cdot V_{g0,eff})$$

$$VSATACCS(T) = VSATACCS \left(\frac{T_{dev}}{TNOM}\right)^{ATS}$$

$$U0ACCS(T) = U0ACCS \left(\frac{T_{dev}}{TNOM}\right)^{UTES}$$

$$NS0ACCD(T) = NS0ACCS \left(1 - KNS0 \left(\frac{T_{dev}}{TNOM} - 1\right)\right) \cdot (1 + K0ACCD \cdot V_{g0,eff})$$

$$U0ACCD(T) = U0ACCD \left(\frac{T_{dev}}{TNOM}\right)^{UTES}$$

$$RSC(T) = RSC \left(1 + KRSC \left(\frac{T_{dev}}{TNOM} - 1\right)\right)$$

$$RDC(T) = RDS \left(1 + KRSC \left(\frac{T_{dev}}{TNOM} - 1\right)\right)$$

$$VBI(T) = VBI - \left(\frac{T_{dev}}{TNOM} - 1\right) KTVBI$$

$$CFG(T) = CFG - \left(\frac{T_{dev}}{TNOM} - 1\right) KTCFG$$

3.1.3 Drain Current model

"The drain current at any point x along the channel under the gradual channel approximation with drift diffusion model can be expressed as?.

$$I_d = -\mu W Q_{ch} \frac{d\psi}{dx} + \mu W V_{th} \frac{dQ_{ch}}{dx}$$

$$I_d = \frac{W}{L} \mu C_g \left(V_g 0 - \psi_m + V_{th}\right) \psi_{ds}$$

Where

$$\psi_m = (\psi_d + \psi_s)/2, \psi_d s = (\psi_d - \psi_s)$$

3.1.4 Self Heating model

An RC network can have self-heating effect and it contains thermal resistance, which is denoted as RTH and thermal capacitance that is denoted as CTH. The increase in temperature can be put into the die temperature that is caused by the thermal node voltage.
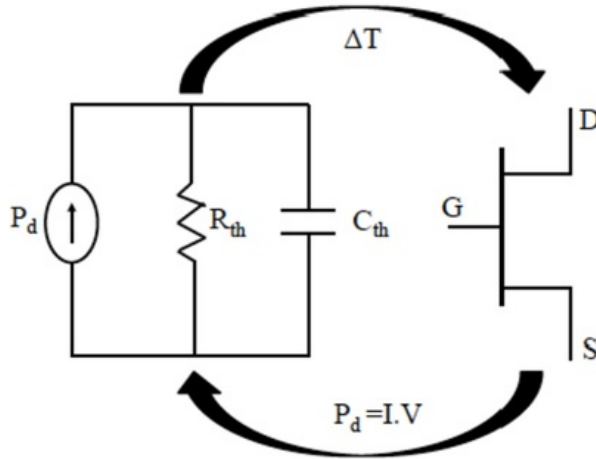

Figure 3.1: RC thermal network

3.1.5 Parasitic Capacitance

Access region capacitance should function at the drain part of the device that appears in drain-source capacitance, which is denoted as C_{ds}.

The following capacitance parameters such as CGSO, CGDL, CDSO and CGDO are model to overlap capacitance outcomes.

In order to get the effects of fringing capacitance, model parameters such as CFD and CFG are used.

3.1.6 Parameter extraction procedure

The following steps explain the procedures about the parameter extraction on ASM-GaN-HEMT model.

The following physical parameters should be set as LDG, W, LSG, NF, L and TBAR in the ASM-GaN-HEMT model. Usually these parameters are accessible to the device technician or engineer.

The next extraction step would be concentrated on obtaining the linear VD condition parameters. These are the following bias condition for a linear drain current with respect to VD is 50 - 100mV and ID-VG characteristics. After that extract the parameters of VOFF (cut-off voltage, which is an incredibly essential parameter) and NFACTOR. Considering the ID - VG plot, VOFF is approximately equal to VG when ID increases. The following estimated approximate values could be tuned as an instance within the parameter extraction with the flow that perfects fits. The sub-threshold slope of the device is influenced by the NFACTOR, which might be extracted along with the ASM-GaN-HEMT model to match the "linear condition ID - VG characteristics" on a log scale.

"Subsequently carrier low-field mobility denoted as U0 and mobility vertical-field dependence parameters such as UA and UB must be able to extracted from linear VD condition in the ID - VD characteristics". Parameters U0, UA and UB can be used to precisely modelled Trans-conductance GM and it's first derivate GM' and second derivate GM" within the linear VD condition. Series resistance can significantly impact the linear ID - VG. The following series resistance parameters such as RSC, D, NS0ACCS and MEXPACSS values can be useful to maintain the values but parameter D has to be a sensible value for this stage. The initial value for series resistance parameter during fine-tuning could be from exceptional measurements such as TLM structures or intimate to a formerly extracted device.

The parameter for the high VD conditions must be able to extracted same as before and linear VD condition can be matched. "Repeat the process as above, initially focused on ID-VG characteristics to enable to get high VD conditions then extract the sub-Voff or low current region of the parameters. The cut-off voltage in the high VD condition decline because of the drain-induced barrier lowering effect, which is modelled along with the extraction of DIBL parameters such as ETA0 and VDSCALE. Parameter CDSCD

should be able to modelled the sub-threshold slope and reduces the high VD conditions in the model".

The next level of this parameter extraction procedure is doing the V0ff fitting for high VD ID - VG. Then following parameters are the important parameters in this process are channel-length modulation parameter denoted as LAMBDA, velocity saturation parameters denoted as VSAT, non-linear series resistance parameters such as NS0ACCS, D, S, MEXPACCS and U0ACCS. This process could be done with matching the high VD ID - VG on a linear scale. VSAT can be extracted by using intermediate current levels with GM along with the high VD condition that keeps increasing with VG. Due to non-linear series resistance, GM can be reduced relevant to VG and relevant parameters can be tuned to match the following region. The self-heating aspect of this device would influence the high current and high drain-voltage regions. Therefore the thermal resistance for this device could be adjusted to a sensible value through calibrations, past experience of the device and TCAD simulations. The parameters shown in this step explains the precise modelling of trans-conductance aimed at various VD settings should be accomplished. After finishing with all these steps, it is advisable to recheck the linear IDVG and do the bit more tuning if is it necessary to make it perfectly fits.

After the above steps, output characteristics of ID - VD needs to be considered to go forward in this process, especially with IDVG has to be matched with various VD conditions. The precisely modelled IDVD must be matched beforehand. If it is not perfectly matched then parameters can be tuned to match perfectly.

All these above processes have been supposed to undergo in the room temperature for DC parameter extraction for this model. If there is a variation of temperature in DC IV's, the application of temperature scaling equation is to convert to match with main model parameters for modelling. The different temperatures are modelled by utilising the temperature parameters DC I-V.

The next main section with the parameter extraction process would be S-parameter modelling after the DC parameter modelling in this ASM-GaN-HEMT model. A sub-circuit must be designed by utilising all the models of parasitic capacitances and inductances to enable to symbolise for parasitic components.

During this scenario, the intrinsic region device capacitances might have been already forecasted by the model through the core formulation. The parameters CGSO, CGDL, CGDO and VDSATCV might be used to obtain by well tune the capacitance such as CGS and CGD. The gate-resistance parameters such as RSHG and XGW could be able to modelled and met its impact on the high frequency of the gate-resistance. The following steps would be used for S-parameters in various DC bias conditions, for all these parameters into a single set of this model. Enormous signal RF modelling measurements could be obtained subsequently modelling the S-parameters in various DC bias conditions. [4]
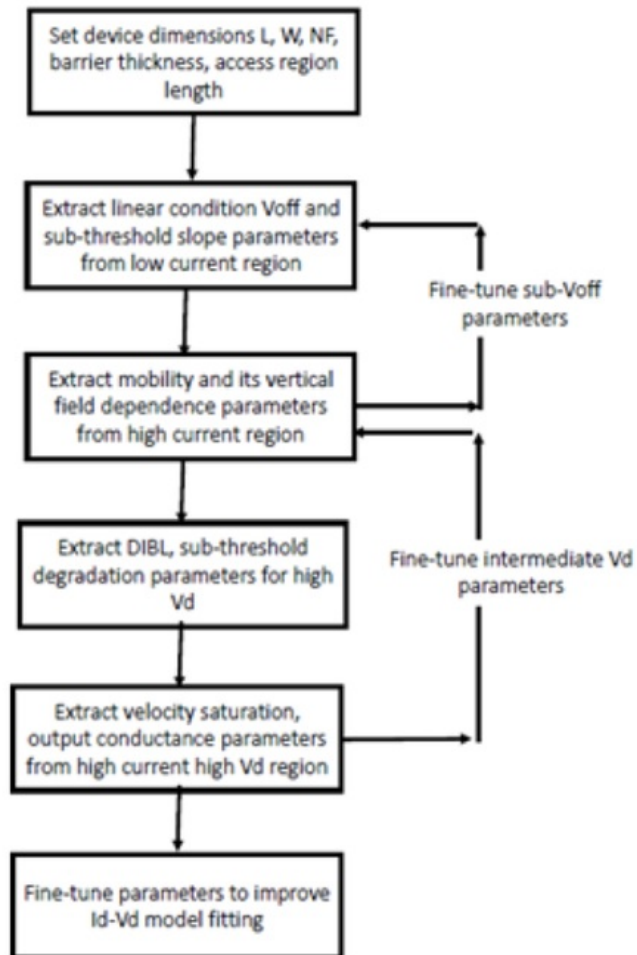
Figure 3.2: Process of Parameter extraction [4]

Chapter 4

Modeling and Simulations

4.1 Verilog-A

The Verilog-A is a subset analogue language of Verilog-AMS, which is a hardware description language. This is one of the greater support software languages for compact gmodelling. Verilog-A is very quick and reliable when compared to hand-coded in C. The next generation of MOSFET model standardisation is developed from the Verilog-A source code. MATLAB is very regularly utilised for compact model development because of the user-friendly capability, great data control and planning procedures. Anyhow, MATLAB could not be utilized for circuit simulation. Verilog-A is very user-friendly as MATLAB and this could be utilized in circuit simulators and parameter extraction software directly. Parameter extracting software gives methods to take care the measured data.

An excellent Verilog-A compiler can make great outcome and more efficient code, which will be better than an individual's hand code especially if the person intensifies on expanding the perfect equation of the model. The fundamental purpose for chooses Verilog-A for compact modelling over common purpose programming languages is that if exempts the model designer from the hardship the carry on the simulator interfaces. The undermentioned multitasks are carried out by the simulator interface specified as evaluate the model parameters, checking the topology, allocating memory, initializing values or recomputing them for a new temperature, loading the Jacobian matrix and right hand side vector, all of the above are individual functions in Spice, which is referred as specific time during a simulation. The partial derivatives of the current and charges in a compact model can be spontaneously calculated by the Verilog-A simulators. This can be lead to a suitable inclusion of the values within the Jacobian matrix for Newton's method. The default values and range of the credible values would be mentioned in a declaration statement. The default value also possibly has a high chance to be a function of already declared parameters.

The primitive of spice is substituted by modules on Verilog-A. A module could be represented in a Spice netlist while if it is a primitive or sub-circuit on a simulator, which

supports Verilog-A, but there are still some simulators that do not support spice model cards on Verilog-A modules. Modules can accommodate another module, which can create as hybrid among primitive and sub-circuit.

Verilog-A would be referring the device's terminal as 'a' and 'b' in pons. The Inout has been declared as terminals of compact models and fundamentally Verilog-A is a language for modelling digital logic where the directions designate the signal flow and the terminals have been mentioned as electrical.

The included files 'diciplines.vams' that consist of definitions of disciplines derives from the definition of electrical. The electrical is the main discipline of concern for compact modelling, which have the variable V across and the variable I through. Self-heating modules refer as a thermal discipline. Declaring its disciplines could be determined as an internal node, but excluded in the post list under mention the module name that is done here for int. The res and dio affirm as two portions of the module. The port and branch declaration should also be included within the parameter declaration. The default value should be included by the parameter interpretation; it can be a simple number that contains exponential notation or standard scale factors. The parameter could be stated in the disclosure that equivalent as **0;inf.** The undermentioned basic mathematical notations brackets [] demonstrate that the spectrum includes the endpoints but parenthesis ()is not included the endpoints. An error message can be automatically created by the simulators when the parameter is out of range. An extension of the compact modelling delivers for parameter aliases and the simulator that aids the extension might permit *vj* to mention as phi for this module. The top-level variable could be stated and might be stated inside the named blocks similar to C that declaration should take place at the top of the block.

The attitude of the module is incorporated in the analogue block, then the module could accommodate only one analogue block that can have arbitrarily many statements. Blocks can be written as begin and end in Verilog-A, where it is written as curly braces **{}** in C. Verilog-A denoted $<+$ to specify an input to the voltage or current of a section. The parasitic resistance refers the voltage formulation V(res) $<+$ I (res)*rs to consent rs is equal to 0. The dc capacitive current consumes distinct input for the diode section. The total current of the branch produces by adding the above values. The fundamental mathematical notations, which are used in C has been used in Verilog-A as well. These are the following mathematical abbreviations: $+$-*/ and functions of **sqrt** ,**pow** ,**In**, **exp** and **abs**. The **limexp** is replaced by **exp** on upgraded convergence for semiconductor junctions. The time derivatives charge with the **ddt** operator that was determined by the capacitive current. The partial derivative operator **ddx** consists of compact modelling extension. This would be very beneficial for operating point information just as capacitance and conductance. The thermal noise would be measured out by using these partial derivatives. The simulation temperature would be desired as *$temperature* and thermal voltage is desired as *$vt*. A mechanism of demanding other significant values from the simulator is called as the compact modelling extension just as the minimum conductance

$simparam ('gmin'). The $ denoted a system function. The if and else statements are used in conditional statement in Verilog-A. The usual logical operators such as &&,||,!, the relational operators $>, >=, <=, <$ and the equality operators $==,!=$ could be utilised as the conditional expressions in Verilog-A. The case statements and for loop can be used in Verilog-A even though there are other compact modelling programs, which do not use them. The incidental of the model developer creating derivative errors eliminated in Verilog-A due to the automatic derivative calculations.

Debugging is one of the toughest processes due to unable to access lower level of data processing just as derivatives or values in Newtons-Raphson iterations. The system task *$debug* that print its arguments on every iteration and also the **ddx** function to need the information contained in the compact modelling. The hierarchical name of the module could be printed by the format specifier *%m*.
Model developer causing derivatives errors can be eradicated by automatic derivative calculation of Verilog-A. Therefore Verilog-A is one of the preferred languages in compact modelling. [3]

4.2   AWR Microwave Office

Microwave Office is a software simulation tool, which is very useful to innovative designers and engineers. The simulation of harmonic balance circuit can be carried out in NI AWR design environment platform. This NI AWR design environment platform contains microwave office, Visual system simulator, analyst and AXIEM. All these platforms help engineers to overcome design Radio Frequency and microwave circuits in these competitive and challenging circumstances.

There are some advantages with using this software simulation tool. These are the following advantages: This application is very user-friendly and easy to navigate around even though the complicated problems can be solved with powerful solvers are handled by the software tool and able to access and achieve accurate results without working out manually by the user, the end user outcome is very transparent and able to synchronized data at the beginning state to finish then directly send the simulation results to manufacturing phase and finally NI AWR simulation environment support to incorporate the third party vendor software along with this simulation software tool that allows user to maximise the outcome of their work. Those above reasons made NI AWR Microwave Office as a best high-frequency software simulation tool in the industry.

This NI AWR Microwave Office simulation software tool can be used in following applications such as amplifiers including power and low-noise amplifiers, passive circuits (couplers, splitters/combiners, attenuators), filters, oscillators, antennas, mixers, multipliers, frequency converters, switches and control circuits. AWR supports with following technologies including Monolithic microwave integrated circuits denoted as MMIC,

Printed circuits boards denoted as PCB, Radio frequency integrated circuits denoted as RFIC, Modules and systems. This thesis is required to using MMIC since it has design flows and process tool kit (PDK) for GaN technology.

There are so many features in this product that would inspire the user as follows: design schematic process including the tuning tool, APLAC which consist of linear and non-linear circuit simulation, EM analysis, load pull, stability that consists linear and non-linear stability analysis, synthesis, DRC/LVS and PDKs for multiple collection of MMIC and RFIC. [1]

Macquarie University engineering department uses this AWR Microwave Office software simulation tools in the laboratory sessions for circuit design and simulation educational purposes.

4.3   Incorporate Verilog A with AWR

This is the main part of my thesis project to incorporate Verilog-A with AWR. My supervisor Dr. Sourabh Khandelwal has already developed the Verilog-A codes for ASM-GaN-HEMT model, and then my task is to convert that code and successfully simulate it on AWR. My supervisor is contacted with AWR staffs to seek some assistant to incorporate Verilog-A with AWR since it does not automatically support and Verilog-A to run the simulation. Therefore some manual adjustment should be made to incorporate Verilog-A code with NI AWR Microwave Office simulation tool. AWR support staffs helped us to incorporate the Verilog-A code with AWR simulation tool.

4.4   Modelling

Measurements and modeling are quite different to each other but both needs each other to understand the real understanding of each other. There are different type of modelling such as electrical modeling and thermal modeling. This section will cover about the modeling on GaN device and its circuit behaviour will totally depends on requirements and limitations. It is not very easy to get exact electrical modeling for the behaviour of GaN transistor. In addition to the active device characteristics the following high frequency elements including layout inductance, consists of skin and proximity effects. The above conditions could not be modelled in GaN transistor.

There are several electrical elements consisting of current sources, capacitors, resistors and inductors utilized in the SPICE model in order to match the real circuit device performance [10]. Our GaN-HEMT model needs to be measured and tuned IDVG and IDVD in order to measure and tune the DC parameters and Capacitance parameters have to be tuned in order to model the S-parameters and fit our plot with measured data of the

device. This section will be further discussed in next sections.

Some models such as Curtice FET (CFET) cannot be fitted with the measured data. GaN-HEMT has capability of working in greater voltage-current appliances, which make it necessary to get precise electro thermal modelling. The criteria for decent power transistor models are based on the following factors: precise measurement, appropriate model and sort of validations performed testing methods to improve the model. Then the model should be calibrated to get the accurate data. Thus force the compact model precision is totally depends on the data precision. Non-linear modelling techniques can be forecasted and study the characteristics of GaN devices. Most of the microwave devices are designed in the region of non-linear modelling of GaN-HEMT usage. This can be very precisely calibrated and established especially for design purpose. There are some coding approaches can be taken to program and simulate the device in different applications such as C-code, Verilog-A and symbolically defined devices denoted as SDD. Metal-semiconductor field-effect transistor denoted as MESFETs and HEMTs are straightforward compact models, which were developed on GaAs wafer can be used for better understanding the GaN-HEMT model. The Essof GaAs HEMT denoted, as EEHEMT model is an addition of Curtice model. The characteristics of a simpler model extraction divide the AC and DC to this EEHEMT model.

Radio Frequency Micro Devices is denoted as RFMD, which is a GaN device with EEHEMT model has a good history of performance for modelling. Curtice is developed remarkably from the old version to the present model difference is named as CFET and C_HEMT then referred as C_HEMT3. Those models could have specific improvements and assistance along GaN modelling.
Changes in the design are periodically made to the original Angelov model and it can be seen as a GaN-specific model is referred as Angelov_GaN usable in Verilog-A code. The Angelov_GaN type consists the conversion of Ids model to concentrate on forecasting of harmonics together with the dispersion. Conversions are making better convince charge preservation of capacitance in its function. The symbolic trapping properties consist of GaN HEMT furthermore numerical access. The drain lack model is discussed by Jardel et al, likewise, the analysis of Baylis which converted the Angelov current formation concentrate quiescent-bias reliant trapping properties fundamental of the physics which consists of numerical access have acknowledged more new capability demand convenient consideration acting as breakdown action with nonlinearity in the GaN HEMT source resistance.

The model that contains the larger amount of parameters does not essentially mean to give expected assigned task. The required task can be achieved by feeding additional parameters to either link the model very intimately to physical action effects, referring to the Berkeley short-channel IGFET model denoted also as BSIM brand of model or keep expanded flexibility in modelling with limited AC and DC condition of this device characteristics, as in the concern of EEHEMT model. The undermentioned are the purpose of using less number of parameters preferable.

The model parameter extraction period rises relevant to an amount of parameters. A hundred parameter model will get extensively larger duration when compare to fifty parameter model. Among the parameters, a large parameter fixed model tries to be experimental and less physical. If the amount of parameters raises and uncertainty in parameters also rises, which will cause lesser conjunction in the optimisation procedures.

It is notable all the models have indicated temperature created into stability formulas, very few have electrothermal models, which tackles self-heating. The self-heating is generated by moderate power dissipation occurred from the device. The self-heating is differed from DC bias and during high power along RF signal levels. The models are available in the market and able to incorporate with Microwave circuit simulators such as ADS and AWR. Angelov model is obtainable on Verilog-A format as 2 different versions named as Original and Angelov_GaN. In terms of our model ASM-GaN-HEMT is not automatically supported on AWR Microwave office simulation tool. Therefore ASM-GaN-HEMT model has to manually incorporate with AWR.

The extraction of Angelov model parameter considered being more time taking process-comparing to EEHEMT and CFET during the extraction process IC-CAP sequences are immediately available to assists. The nonlinear categorization and modelling procedure in the situation of sending certain specialised problems related to GaN modelling.

A symbolic test station utilised to collect data as model coefficient extraction subsist of a wafer inquiry station, broadband vector network analyser denoted as VNA. Direct Current and Pulsed current voltage denoted, as I-V analysers and running software of the computer are ease to control the instrument and data gain, if not happen then the model extraction will be there. The following Figure 4.1: Non-linear modelling process explains all the steps of the modelling process.
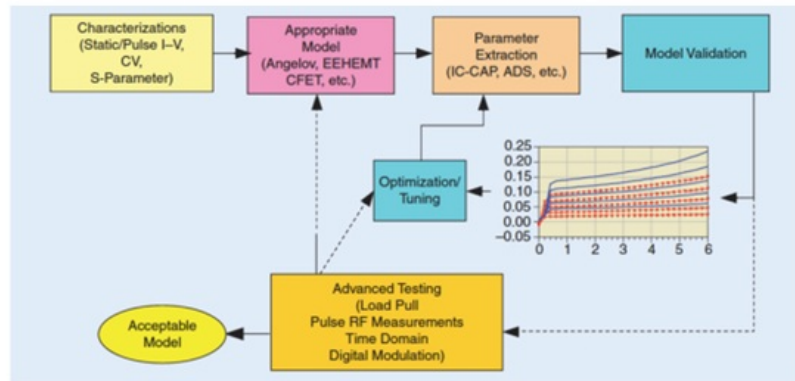

Figure 4.1: Non-linear modelling process

The first instance, I-V and multi-bias S-parameter calibrations are executed. It is very important trapping properties and its bias dependence is necessary for effective GaN-HEMT modelling. [5]

4.5   Parameter extractions for the project

This is a generic ASM-GaN-HEMT device. Generic means device that does not represent any industrial device. This device can be converted and changed by adding some suitable parameters for capable to become an industrial device. The parameter values should be determined and calibrated in this research thesis paper. Then the next step for this parameter extraction would be adding the manifolds to the ASM-GaN-HEMT Triquint 8x40 device. Manifolds are kind of network. ASM-GaN-HEMT device has 5 nodes, which includes as follows: drain node, gate node, source node, substrate and temperature node. Then temperature node is always connected with a resistor.

Each node has its own manifold circuits to be added. Finally, drain and gate voltage sources need to be connected to the drain and gate manifolds circuits through bias tees. Bias gate should be connected with DC bias, then the way it is connected to this ASM-HEMT device through DC feed. DC feed could be a very high-value inductor. The DC feed and DC block is integrated as one element, which is called as a bias tee in the AWR. The AWR simulator also has the ideal bias feed or bias tee. Therefore bias tee has been used in this project for AWR simulations. The bias tee from the one end is connected to the DC source and the other end is connected to the RF source. Bias Tee has three ports, which consists of two inputs (DC source and RF source) and an output port in the AWR simulation. Bias Tee must be connected to the gate manifold. The same procedure also should be repeated for the drain side as well.

Parameters are fed by double click on the ASM-HEMT model and the parameter values are also fed on the model by using the same method. This has been done to calibrate the model to the data.

The following tuning process has been done to tune the RF device from Triquint. I have figured out how to embed measured data on AWR and do the tuning. I have used tuner tool on NI AWR Microwave Office simulation tool to adjust the parameter to fit the measured data. My supervisor Dr.Sourabh Khandelwal has provided me readings of the measured data compare and tune the device to measured data. I was tasked to fit the model with DC and RF measured data. This project based on parameter extraction in AWR for high-frequency GaN device. Measured data is incorporated in AWR very easily since it has an option to feed the data. There are two ways to do the parameter extractions. First one is for DC parameters and the second one is S-parameters then measured data for both of them was given. The first step would be starting with DC parameter extraction and modelling. No need to include the manifolds for DC parameter

modelling. For this, IdVd type simulations must be run without manifolds and nodes were directly connected to the voltage sources. DC modelling required adding simulations for IdVg and IdVd curves. RF modelling requires adding manifolds. The SP2 files are measured S-Parameters files and there are ways to include the files in AWR. I managed to match my simulations with the SP2 file in AWR then I turned the device for the best fit. Picked 3 or 4 bias conditions for DC parameters and done S-Parameter for 20V and 32mA bias condition. First measured data will have the range of VgVds. This is the range where the measurements were done.

4.6 DC Parameter extractions

The DC parameters are shown in the Appendix B, which I initially fed the parameters and values in the ASM-GaN-HEMT model. I adjusted the values after plotting IdVd and IdVgs plot to match the device. I have also removed some parameters since it was not necessary and did not make any difference for an example U0ACCS and U0ACCS were given twice. Therefore I needed to remove one of them. The following parameter values were changed according to the Table 4.1: Adjusted parameter values.

Parameters	Initial values	Adjusted value
NS0ACCS	9.3e16	9.0e17
NS0ACCD	9.3e16	9.0e17
U0ACCS	100.0e-3	9.0e-3
U0ACCD	100.0e-3	9.0e-3

Table 4.1: Adjusted parameter values

The parameters for ASM-GaN-HEMT model can be found in the ASM-GaN-HEMT model manual [4]. I did not feed all the parameters, which was given in the manual on my model. My schematic started to run without any errors after following changes were made on parameters values.

Then the following DC parameters were tuned to fit the ASM-GaN-HEMT model device with the already measured data: CDSCD, ETA0, UA, UB, UOFF and VSAT. I only tuned the main DC parameters, which were given above and did not tune other DC parameters values except those five, which was given above for DC parameter extraction.

4.6.1 IdVd

Figure 4.2 is simulated for IdVds graph to Id_Vds_25C generic device and VoutQ vs IoutQ measured data from EGO490 8x40 device. Then Figure 4.3 is shows that Id_Vds_25C generic device is tuned for measured data. This has been tuned by tuning the DC parameters. Table 4.2 shows the tuned DC parameters values.
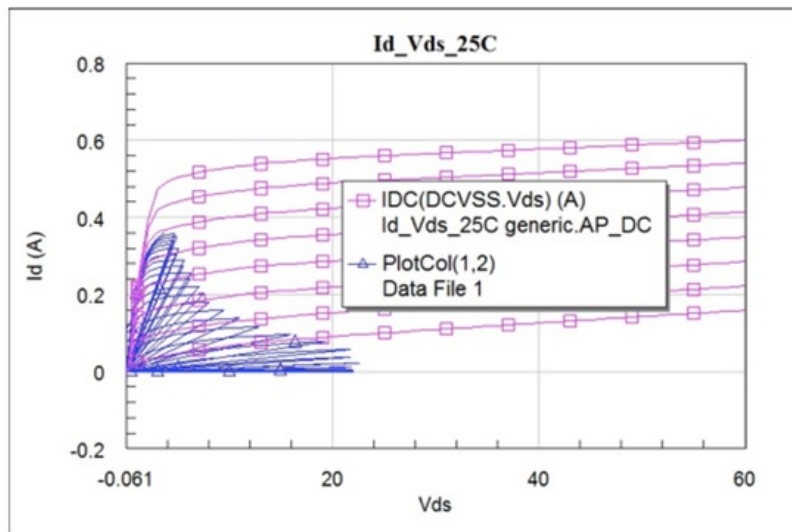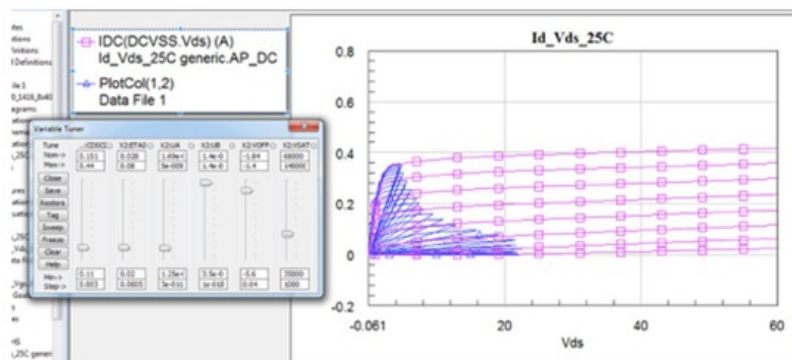
Figure 4.2: IdVd before tuning

Figure 4.3: Tuned IdVd plot

	VOFF	UA	UB	ETA0	CDSCD	VSAT
Norm	-1.86	1.51E-09	1.16E-16	0.0348	0.181	68000

Table 4.2: Tuned Results for IdVd output 1.0

Figure 4.4 is a schematic simulation for IdVd New_Output schematic to bias condition of 1V. Figure 4.5 is an IdVds plot for Figure 4.4 schematic and Table 4.3 is a tuned DC parameter values for Figure 4.4 schematics circuit.
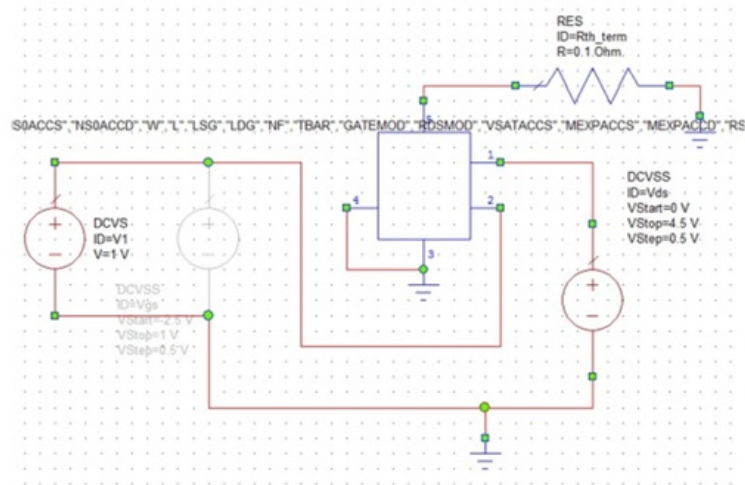
Figure 4.4: IdVd New_Output Schematic for bias condition 1V
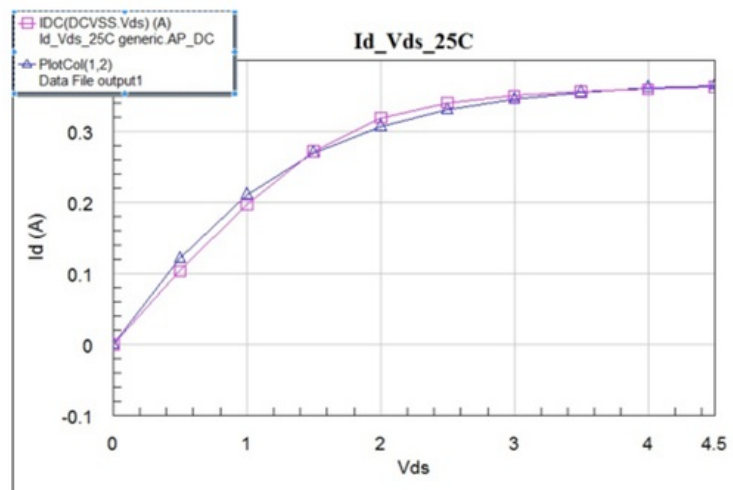
Figure 4.5: IdVd New_Output graph for bias condition 1V

	CDSCD	ETA0	UA	UB	VOFF	VSAT
Norm	0.277	0.0384	4.13E-09	2.13E-16	-2.68	56300

Table 4.3: Tuned Results for IdVd New_Output for bias condition 1V

Figure 4.6 is a schematic simulation for IdVd New_Output schematic to bias condition of $-2V$. Figure 4.7 is an IdVds plot for Figure 4.6 schematic and Table 4.4 is a tuned DC parameter values for Figure 4.6 schematics circuit.
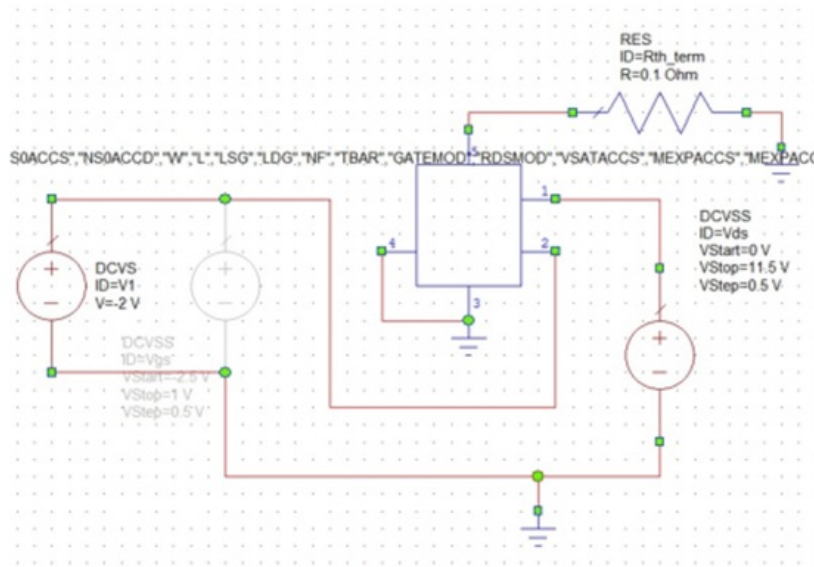
Figure 4.6: IdVd New_Output Schematic for bias condition -2V
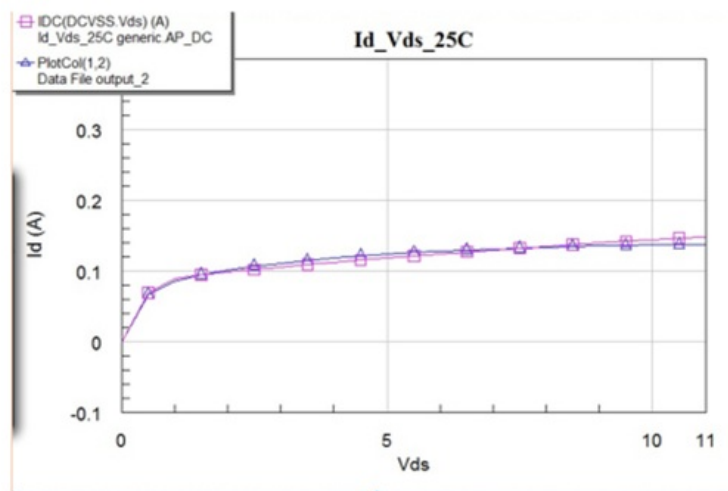
Figure 4.7: IdVd New_Output graph for bias condition -2V

	CDSCD	ETA0	UA	UB	VOFF	VSAT
Norm	0.278	0.0319	2.45E-09	3.00E-16	-2.68	108300

Table 4.4: Tuned Results for IdVd New_Output for bias condition -2V

Figure 4.8 is a schematic simulation for IdVd New_Output schematic to bias condition of -5V. Figure 4.9 is an IdVds plot for Figure 4.8 schematic and Table 4.5 is a tuned DC parameter values for Figure 4.8 schematics circuit.
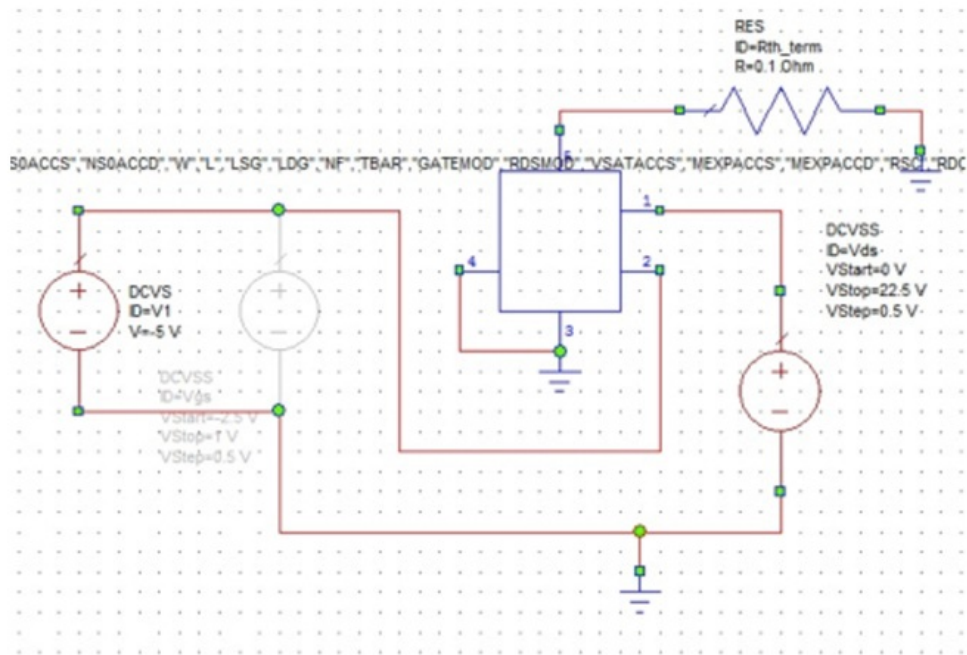
**Figure 4.8:** IdVd New_Output Schematic for bias condition -5V
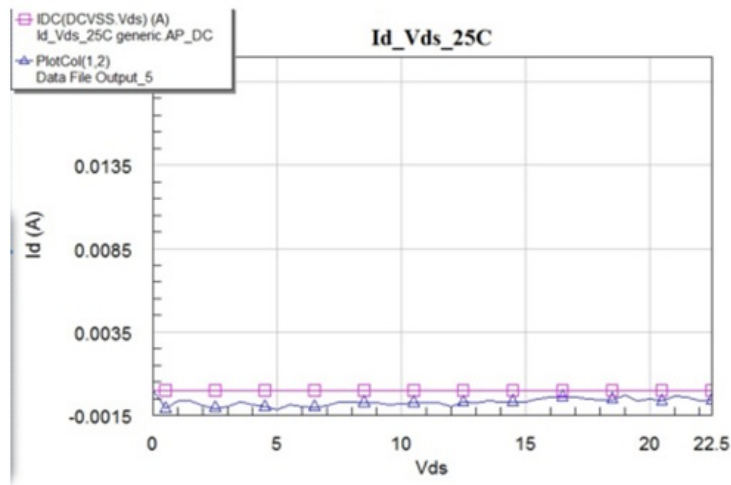
Figure 4.9: IdVd New_Output graph for bias condition -5V

	CDSCD	ETA0	UA	UB	VOFF	VSAT
Norm	0.286	0.0549	2.45E-09	2.57E-16	-2.26	112600

Table 4.5: Tuned Results for IdVd New_Output for bias condition -5V

Figure 4.10 shows that IdVd plot to all 3 bias conditions (1V, -2V and -5V) in one and the same plot. Table 4.6 states that all three bias conditions were tuned to one DC parameter values.
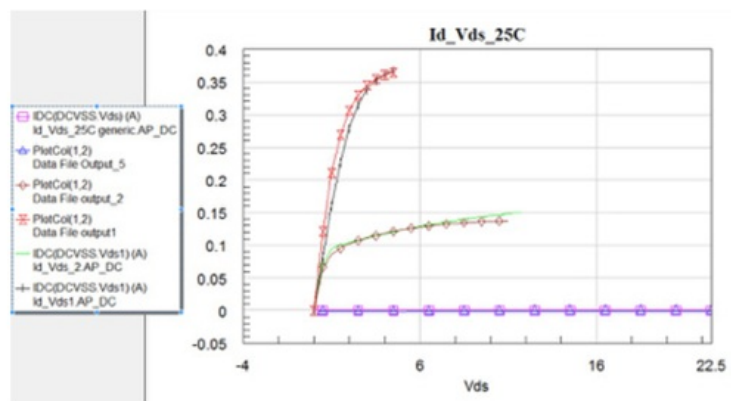
Figure 4.10: IDVD New_Output Tuned plot for all 3 bias condition

	CDSCD	ETA0	UA	UB	VOFF	VSAT
Norm	0.143	5.17E-02	4.90E-09	3.68E-16	-2.89	72600

Table 4.6: Tuned Results for IdVd New_Output for for all 3 bias condition

The simulation should be plotted until the actual measured data plot. Ran the simulation till the measurements; it is not required to run the simulation way beyond that.

IdVd needs to be tuned on one plot for all the bias conditions, which will result in the one DC parameter extraction values for IdVd for all the bias conditions. This procedure should be followed to IdVg part as well. IdVd should be plotted only on linear scale.

4.6.2 IdVgs

Figure 4.11 shows the schematic simulation for IdVg New_Transfer schematic to the bias condition of 7.5V. Figure 4.12 is an IdVds plot for Figure 4.11 schematic and Table 4.7 is a tuned DC parameter values for Figure 4.11 schematics circuit.
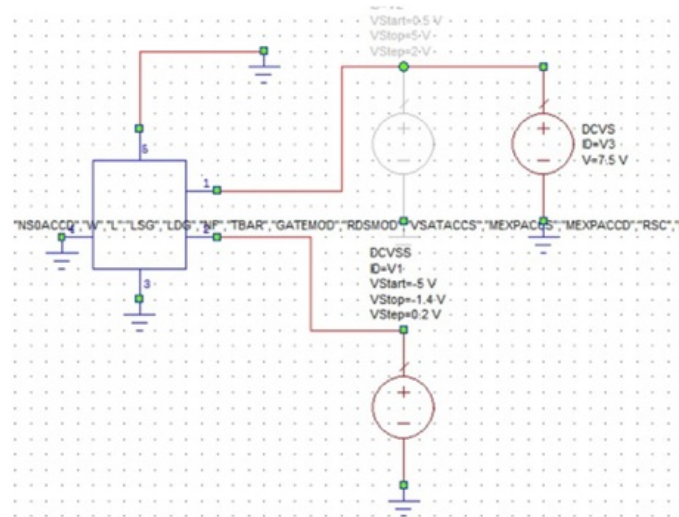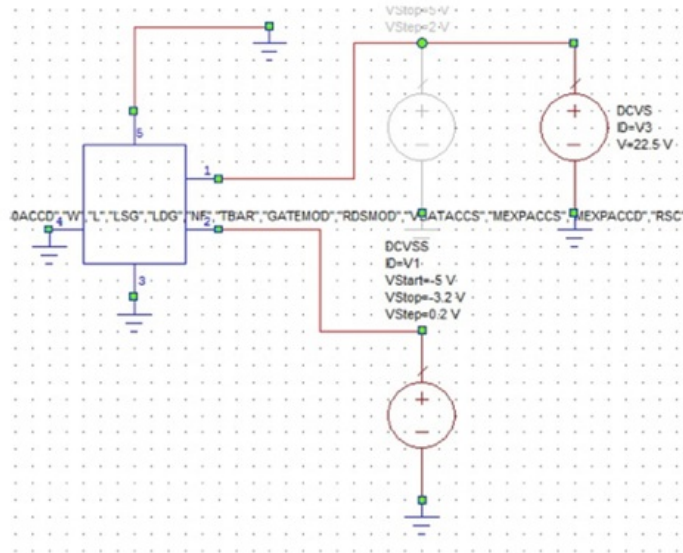

Figure 4.11: IdVg New_Transfer schematic for bias condition 7.5V
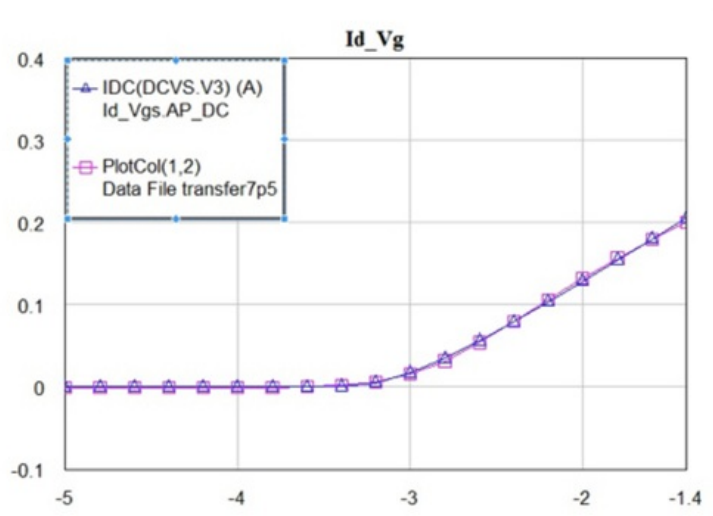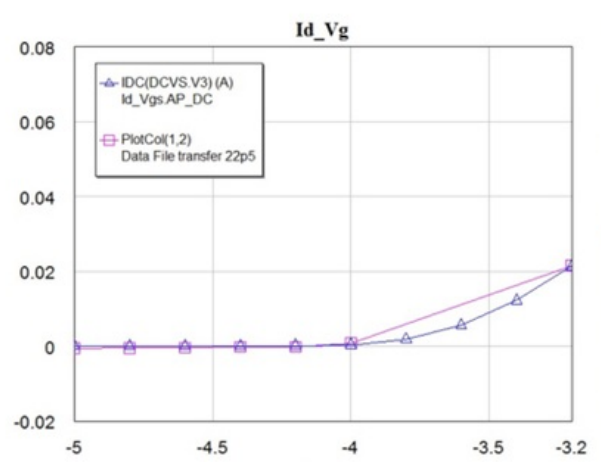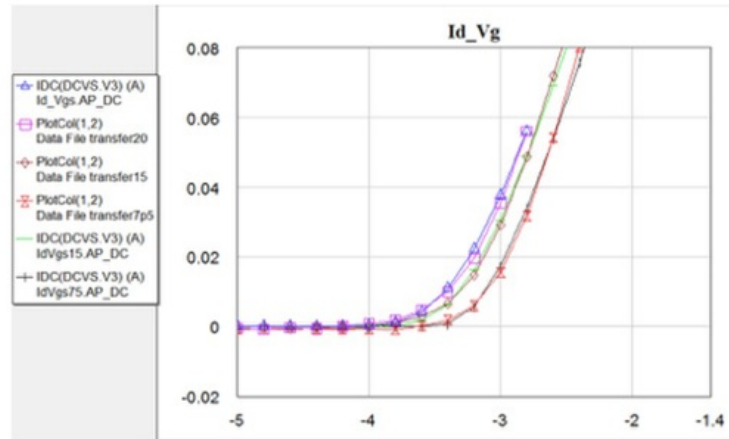
Figure 4.12: IdVg New_Transfer graph for bias condition 7.5V

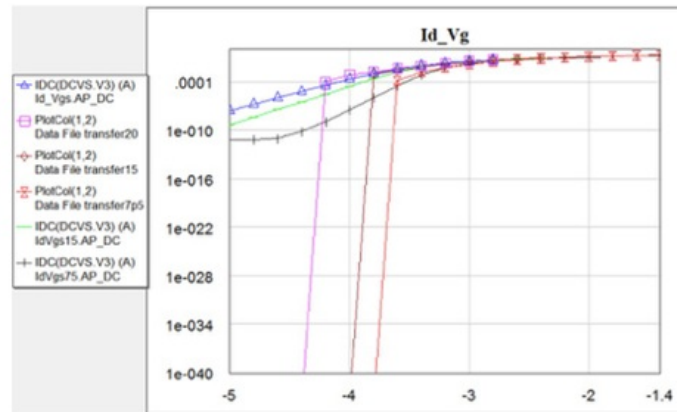|	CDSCD	ETA0	UA	UB	VOFF	VSAT
Norm	0.1235	3.58E-02	6.01E-09	1.56E-16	-2.95	69000

Table 4.7: Tuned Results for IdVg New_Transfer for bias condition 7.5V

Figure 4.13 shows the schematic simulation for IdVg New_Transfer schematic to the bias condition of 15V. Figure 4.14 is an IdVds plot for Figure 4.13 schematic and Table 4.8 is a tuned DC parameter values for Figure 4.13 schematics circuit.
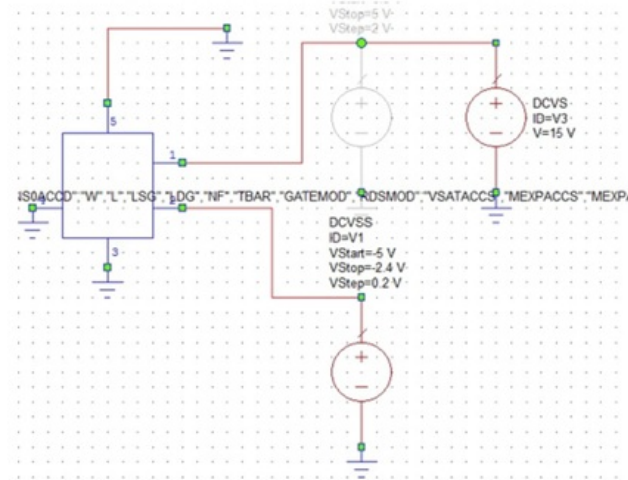
Figure 4.13: IdVg New_Transfer schematic for bias condition 15V
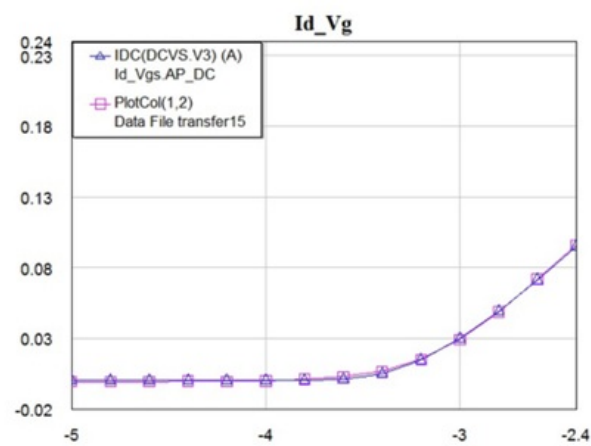
Figure 4.14: IdVg New_Transfer graph for bias condition 15V

	CDSCD	ETA0	UA	UB	VOFF	VSAT
Norm	0.1325	4.43E-02	4.57E-09	1.16E-16	-2.87	69000

Table 4.8: Tuned Results for IdVg New_Transfer for bias condition 15V

Figure 4.15 shows the schematic simulation for IdVg New_Transfer schematic to the

bias condition of 22.5V. Figure 4.16 is an IdVds plot for Figure 4.15 schematic and Table 4.9 is a tuned DC parameter values for Figure 4.15 schematics circuit.

Figure 4.15: IdVg New_Transfer schematic for bias condition 22.5V

Figure 4.16: IdVg New_Transfer graph for bias condition 22.5V

	CDSCD	ETA0	UA	UB	VOFF	VSAT
Norm	0.1325	6.05E-02	4.69E-09	1.00E-16	-2.87	34500

Table 4.9: Tuned Results for IdVg New_Transfer for bias condition 22.5V

Figure 4.17 shows that IdVg plot to all 3 bias conditions (7.5V, 15V and 22.5V) in one and the same linear plot. Figure 4.18 shows that IdVg plot to all 3 bias conditions (7.5V, 15V and 22.5V) in one and the same log plot. Table 4.10 states that all three bias conditions were tuned to one DC parameter values.

Figure 4.17: IdVg New_Transfer graph in linear scale for all 3 bias conditions in one plot

Figure 4.18: IdVg New_Transfer graph in log scale for all 3 bias conditions in one plot

	CDSCD	ETA0	UA	UB	VOFF	VSAT
Norm	0.1325	6.05E-02	4.69E-09	1.00E-16	-2.87	34500

Table 4.10: Tuned Results for IdVg New_Transfer for all 3 bias conditions

Any random measured data bias conditions can be picked for IdVg in order to tune the device. For an example, bias conditions for IdVg vary from 0V to 22.5V. I have chosen 3 bias conditions as follows: 7.5V, 15V and 22.5V. I may have chosen 20V instead of 22.5V, not necessarily stick with the maximum voltage bias condition so bias conditions can be randomly picked. DC parameter extraction can be done it for all the measured bias condition as well but I have chosen to pick only a few conditions just to save time in this thesis with my supervisor Dr.Sourabh Khandelwal's advise. IdVg needs to be tuned on one plot for all the bias conditions, which will result in the one DC parameter extraction values for IdVg for all the bias conditions.

When drain voltage is zero then drain current is also zero. When it says transfer 7.5, which means drain voltage is 7.5V. If the drain voltage is not changed then something is wrong according to the measured data. We are trying to match the simulations with the measured data. Therefore same conditions need to be used in order to fit the data.

It is preferred to have the graph in the linear and log scale. Id has to be set in Left 1 on AWR Rectangular plot option. Log scale should be selected for Left 1, not for x. Please review the Figure 4.19 below.
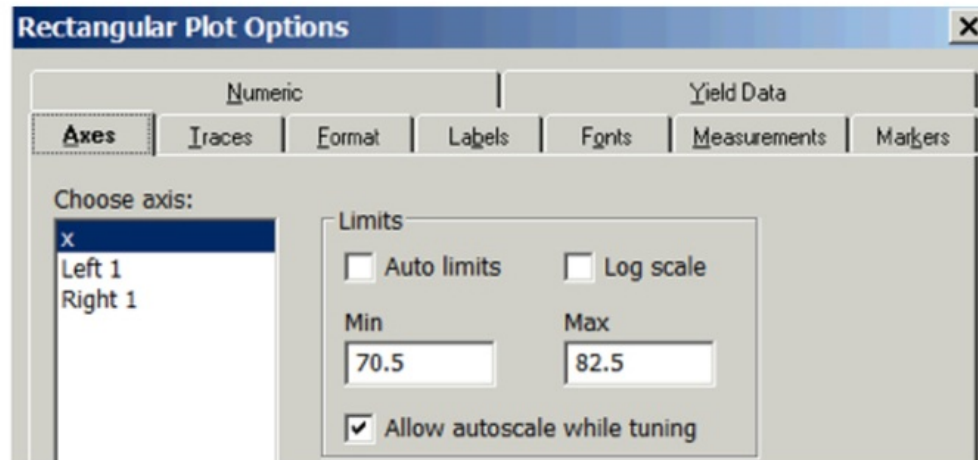
Figure 4.19: Linear and log scale should be plotted only for IdVg, not for IdVd

4.7 RF Parameter extractions

Capacitance parameters, which are given in the ASM-GaN-HEMT model manual, are given below on Table 4.11: Capacitance parameters [4]. I did not feed all the capacitance parameters that are given in the Table 4.11 on ASM-GaN-HEMT model for this project. Only four capacitance parameters were fed in the model. These are the following capacitance parameters such as CDSC, CGDL, CGDC and CGSC. The above capacitance parameters were used to tune the model S-parameters to fit the measured data S-parameters in order to get the RF parameter extractions including magnitude of S-parameters tuning and phase of S-parameter tuning. Only two ports are assigned with the model circuit with manifolds. More ports will unnecessarily absorb more current into them since port has some resistance about 50ohms each. More ports on manifolds will affect the results of getting 32mA drain voltage. Figure 4.20 shows the ASM-HEMT model circuit schematic added with all manifolds, bias tee, ports and voltage source for RF parameter extractions.

Name	Unit	Default	Min	Max	Description
CGSO	F	1e-18	-	-	Gate-Source overlap capacitance parameter
CGDO	F	1e-18	-	-	Gate-Drain overlap capacitance parameter
CDSO	F	1e-18	-	-	Drain-Source capacitance parameter
CGDL	F	0e-15	-	-	Parameter for bias V_{ds} dependence in CGDO
VDSATCV	V	100	-	-	Saturation voltage at drain side in CV model
CFG	F	0e-18	-	-	Gate fringing capacitance parameter
CFD	F	0e-12	-	-	Drain fringing capacitance parameter
CJ0	F	0e-12	-	-	Zero V_{ds} access region capacitance parameter
VBI	V	0.9	-	-	Drain end built-in potential parameter
MZ	-	0.5	-	-	Parameter governing decay of C_{aced} for high V_{ds}
AJ	-	115e-3	-	-	Parameter for governing bias independent value of C_{ds} at low V_{ds}
DJ	-	1	-	-	Parameter governing decay of C_{aced} for high V_{ds}

ADOS	-	1	0	∞	Quantum mechanical effect pre-factor or switch in inversion
BDOS	-	1	0	∞	Charge centroid parameter - slope of CV curve under QME in inversion
QM0	-	1e-3	0	∞	Charge centroid parameter - starting point for QME in inversion
ADOSFP	-	1	0	∞	Quantum mechanical effect pre-factor and switch in inversion
BDOSFP	-	1	0	∞	Charge centroid parameter - slope of CV curve under QME in inversion
QM0SFP	-	1e-3	0	∞	Charge centroid parameter - starting point for QME in inversion
ADOSI	-	0	0	∞	Quantum mechanical effect prefactor cum switch in inversion
BDOSI	-	1	0	∞	Charge centroid parameter - slope of CV curve under QME in inversion
QM0I	-	1e-3	0	∞	Charge centroid parameter - starting point for QME in inversion

Table 4.11: Capacitance Parameters
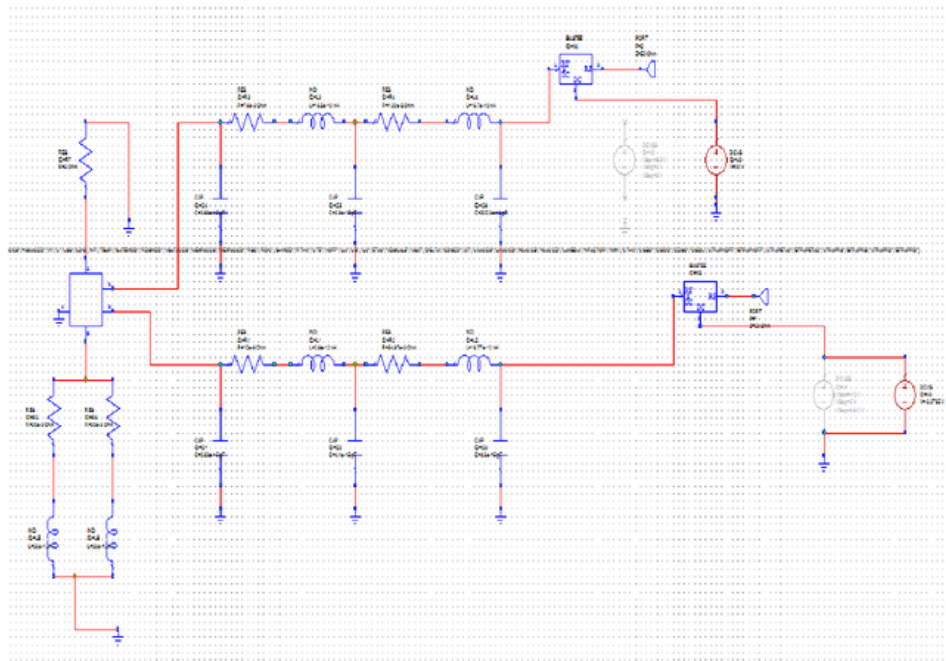
Figure 4.20: ASM-HEMT model-RF Parameter extraction Schematic

4.7.1 S-Parameter

S-Parameters are usually specified as 20log of voltage ratio at the waves at the ports in dB. The S_{11} and S_{22} can be plotted on Smith chart [12]. Impedance matching can be plotted on smith chart. Usually a smith chart includes all the impedance, real and imaginary in one circle. [2]

S_{11} means forward reflection (input match - impedance)
S_{22} means reverse reflection (output match - impedance)
S_{12} means forward transmission (gain or loss)
S_{21} means reverse transmission (leakage or isolation) [12]

Figure 4.21 shows the tuned ASM-HEMT model with a measured data for magnitude of S_{11}. Figure 4.22 shows a S_{11} Smith chart for ASM-HEMT model and Figure 4.23 shows a S_{11} Smith chart for measured data on excel.
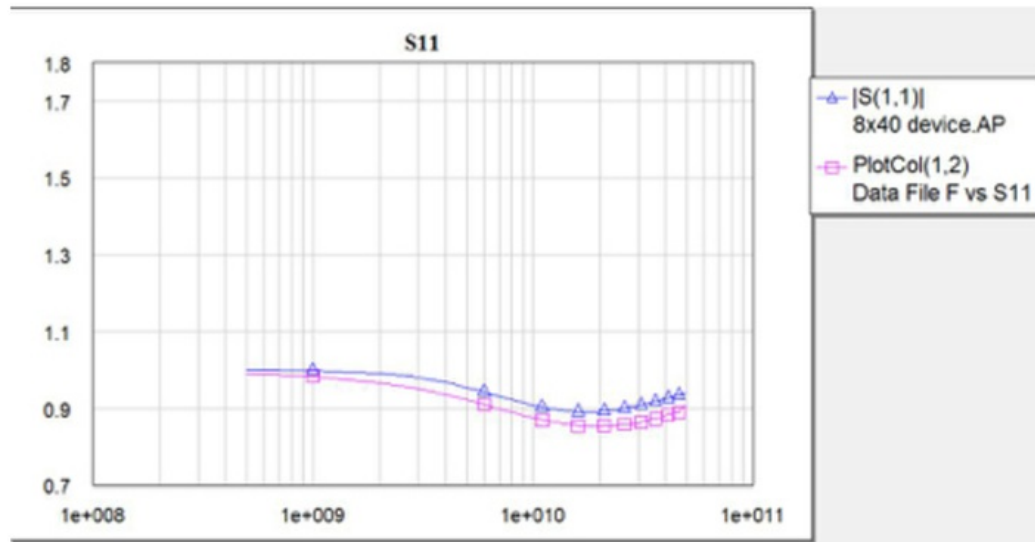
**Figure 4.21:** Tuned Magnitude of S11 results for ASM-HEMT model

S11_smith chart

m1:
50 GHz
r 0.0303915
x -0.169772

Swp Max
50GHz

S(1,1)
8x40 device.AP

Swp Min
0.5GHz
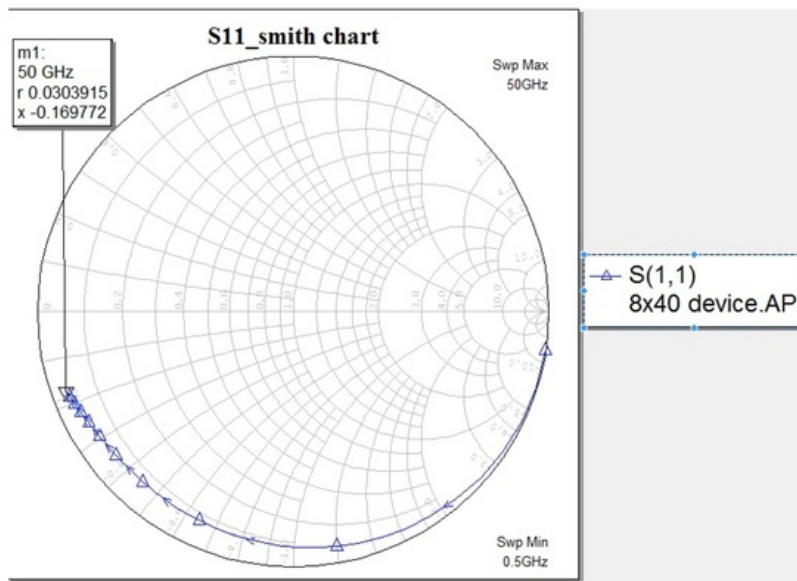
Figure 4.22: Model S11 on Smith Chart

S11

Enter name
1+j0
-1+j0
0-j1
0+j1
0+0

Plot Area

RF Cafe
2002
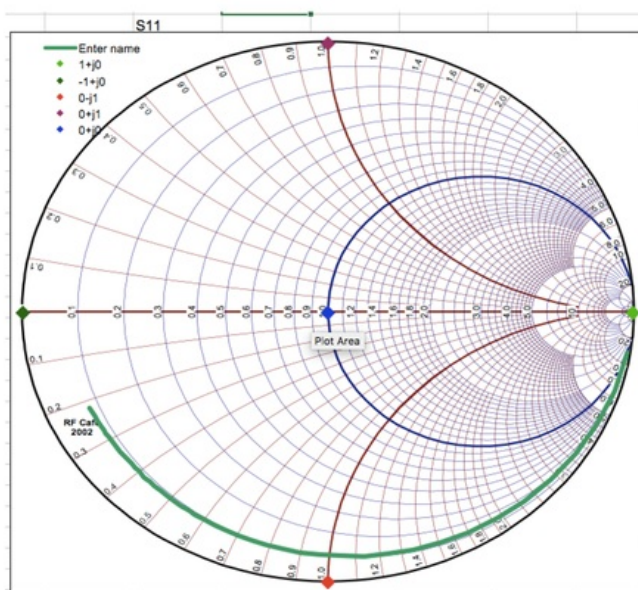
Figure 4.23: Measured data S11 on Smith Chart

Figure 4.24 shows the tuned ASM-HEMT model with a measured data for magnitude of S_{12}.
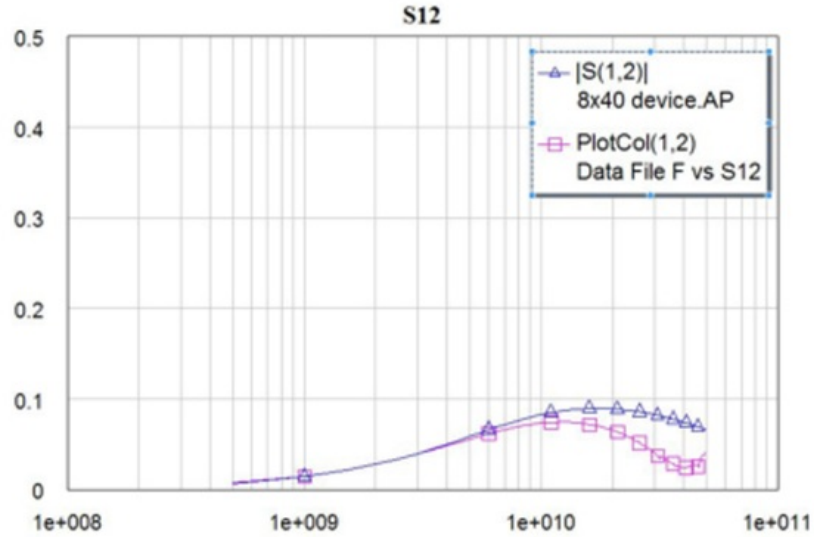
Figure 4.24: Tuned Magnitude of S12 results for ASM-HEMT model

Figure 4.25 shows a magnitude of for ASM-HEMT model with a measured data for magnitude of S_{21} .
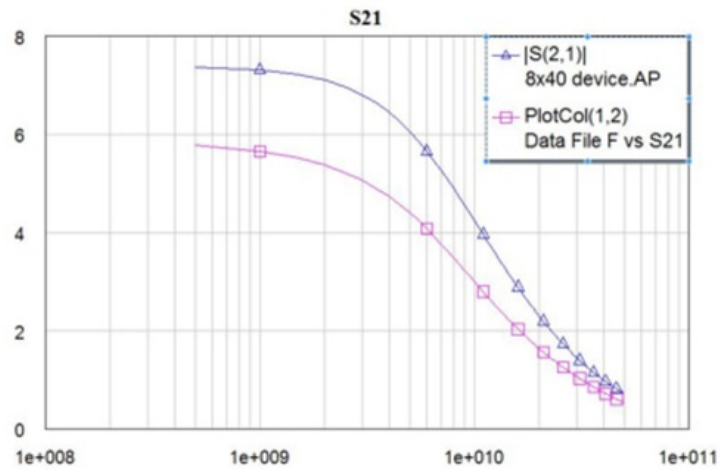
Figure 4.25: Tuned Magnitude of S21 results for ASM-HEMT model

Figure 4.26 shows the tuned ASM-HEMT model with a measured data for magnitude of S_{22}. Figure 4.27 shows a S_{22} Smith chart for ASM-HEMT model and Figure 4.28 shows a S_{22} Smith chart for measured data on excel.
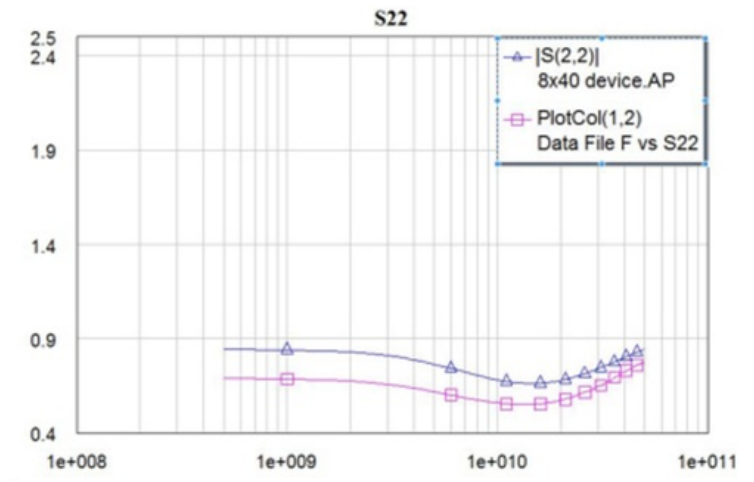
Figure 4.26: Tuned Magnitude of S22 results for ASM-HEMT model
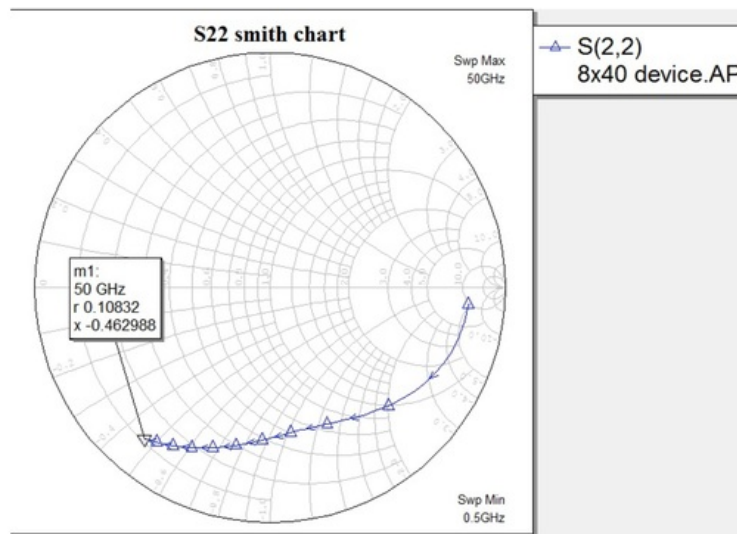
Figure 4.27: Model S22 on Smith Chart
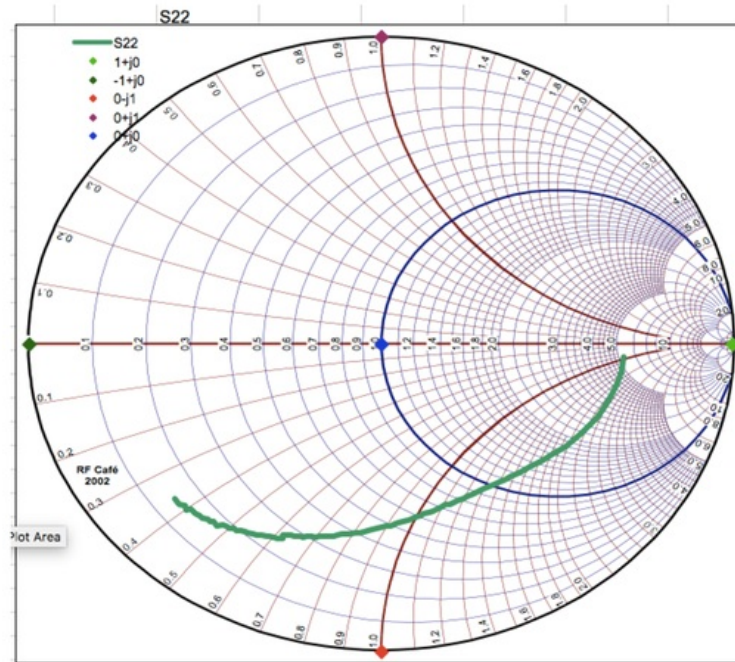
Figure 4.28: Measured data S22 on Smith Chart

Table 4.12 is a tuned capacitance parameter values for magnitude S-parameter of the ASM-HEMT model with measured data.

	X1:CDSC	X1:CGDL	X1:CGDC	X1:CGSC
Norm: Mag-nitude of S-Parameter	1.04E-13	9.38E-16	6.61E-14	1.50E-13

Table 4.12: Tuned Magnitude of S-parameter results for ASM-HEMT model

S-parameter simulations do not require to sweep for the DC. Instead of sweeping it, this can be done for the fixed bias condition 20V and 32mA so this bias condition is used to simulate the S-parameters and frequencies are swept. First of all my simulation had results of so many s-parameters when I was changing bias for each curve, which is not needed. Then I figured out using one fixed bias point varies the frequency to simulate this.

Magnitudes of the S-parameters are different to IdVd or IdVg parameters. Capacitance parameters should be adjusted in order to tune the S-parameter for RF parameters modelling. DC part may have to be tuned slightly but not that much and main tuning would be on capacitance parameters. All the capacitance parameters were given in the

ASM-HEMT model manual [4]. Same values from the Simulation Setup: RF Triquint-ASM-GaN-HEMT documents has been used for manifolds, which includes capacitor values and inductor values [8]. It is observed in S-parameters things are the little bit different and it can be viewed in many different ways such as Smith chart, phase plot, linear plot and etc. My RF parameters plots are matching the shape of the plots that are given in ASM-GaN-HEMT: Advanced SPICE model for GaN HEMTs paper [9] . It is preferable to plot the S_{11} and S_{22} on a Smith chart and S_{12} and S_{21} on a regular Magnitude vs Frequency plot for a bias condition 20V and 32mA. This 20V in this bias condition would be the drain voltage and 32mA is a drain current. Using the imported data cannot plot Smith chart. Therefore I have used excel template to plot the smith chart for measured S_{11} and S_{22} so I can compare the measured plot and model plot simulation shape.

The following plots are expected for RF parameter modelling: Magnitudes of S-Parameters, the phase of S-Parameters, K and Max gain. S-parameter simulation must be plotted for S-parameters vs Frequency graph, not with bias condition. Bias voltages are fixed and only frequency is sweeping here at RF modelling.

In order to get fixed drain voltage, adjust the gate voltage till achieving 32mA current flowing through the drain voltage source for 20V and 32mA bias condition. The frequency range can be found in the measured data spreadsheet to plot the S-Parameters on AWR. Frequency is given in the first column, real and imaginary S-parameters values were given in following columns on measured data spreadsheet. The magnitude of S-parameter is needed for the simulation. Therefore it needs to be calculated from the real and imaginary data. Complex numbers knowledge is essential to get the magnitude. Magnitude can be calculated by using following equation.

Magnitude of S-Parameters= $|S\text{-}Parameter|$

$$|S\text{-}Parameter|=\sqrt{Real\ S\ Parameter^2 + Imaginary\ S\ Parameter^2}$$

4.7.2 Phase S-Parameter

The following figures show the frequency vs phase of S-parameters plots: Figure 4.29 is a tuned data for P_{11} ASM-HEMT model with measured data. Figure 4.30 is a tuned data for P_{12} ASM-HEMT model with measured data and Figure 4.31 is a tuned data for P_{22} ASM-HEMT model with measured data. Table 4.13 is a tuned capacitance parameter values for phase S-parameter of the ASM-HEMT model with measured data
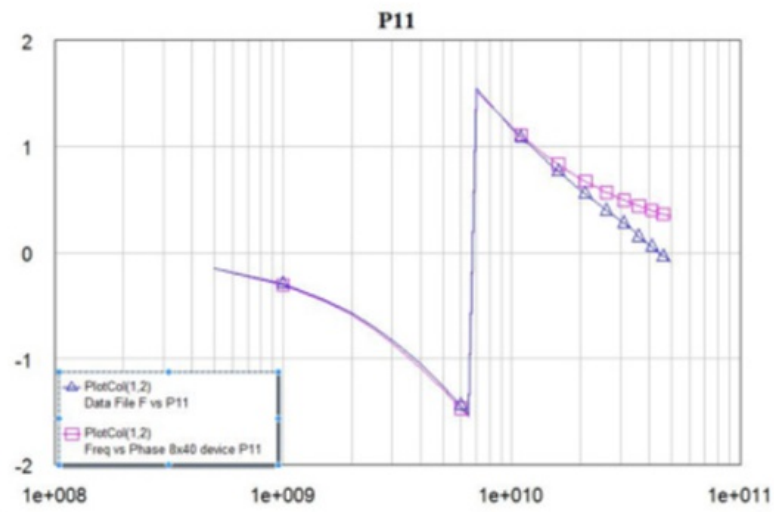
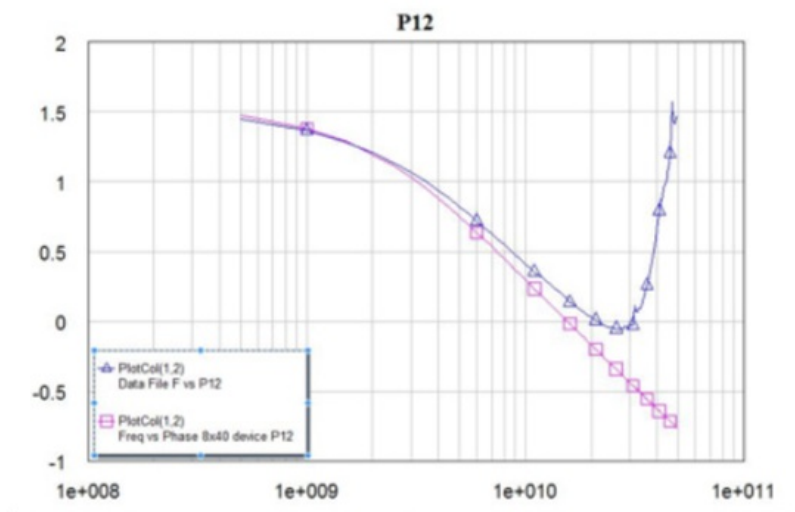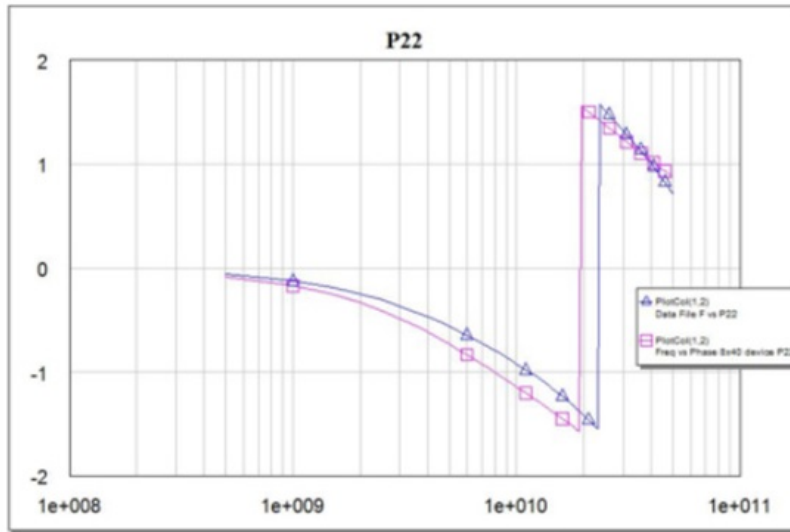**Figure 4.29:** Tuned P11 results for ASM-HEMT model

Figure 4.30: Tuned P12 results for ASM-HEMT model

Figure 4.31: Tuned P22 results for ASM-HEMT model

	X1:CDSC	X1:CGDL	X1:CGDC	X1:CGSC
Norm: Phase of S-Parameter	1.01E-13	1.01E-15	7.83E-14	2.00E-13

Table 4.13: Tuned Phasse of S-parameter results for ASM-HEMT model

The phase of S-Parameter is needed for the simulation for RF parameter extraction. Phase can be calculated by using the complex numbers. Phase can be calculated from the following equation.

$$Phase\ of\ S\ Parameter = tan^{-1}\frac{Imaginary\ S\ Parameter}{Real\ S\ Parameter}$$

I have used the Excel tool to calculate the magnitude and phase of the S-parameters. Then I have imported that data into AWR to simulate the graph. I was unable to plot the phase of S-parameter for ASM-GaN-HEMT model on AWR due to non-availability of feature to simulate phase of s-parameter. Therefore I have exported the S-parameter real and imaginary values for ASM-GaN-HEMT model from AWR. Then I have used the same method, which I used to calculate the phase s-parameter for measured data on excel to calculate the model. Then I have incorporated that data into AWR simulation tool to plot the model and measured data phase S-parameter on one plot to tune. I?m unable to plot the Smith chart for phase S-parameters due to non-availability of feature that could draw a Smith chart by using imported data on AWR.

4.7.3   K

K is a Rollett stability factor, which is mostly used to measure the stability of power amplifier. K has to be $>$ or $=$ to 1 for unconditional stability. According to our simulation below K factor is less than 1 for ASM-GaN-HEMT model. Therefore our model is unstable at the moment. [6]
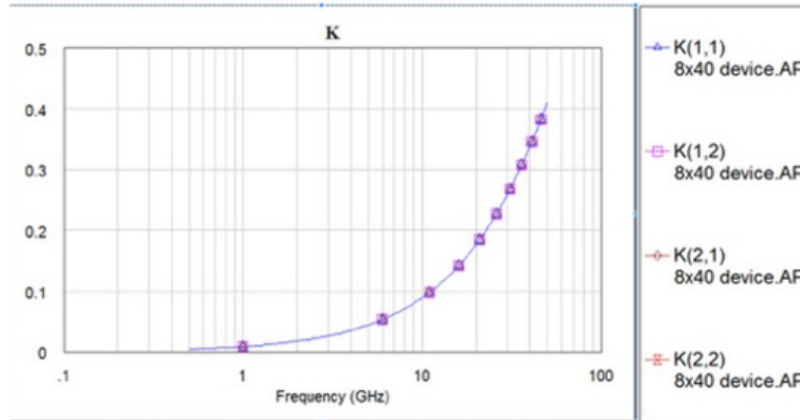
Figure 4.32: K plot for ASM-GaN-HEMT model

4.7.4   Max Gain
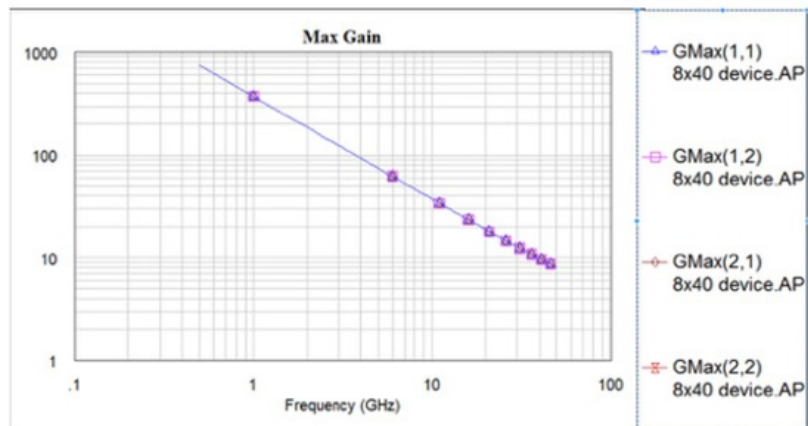
Figure 4.33: Max Gain plot for ASM-GaN-HEMT model

Chapter 5

Futurework on RF GaN HEMT modeling

There are some following sections can be worked in future such as modelling at multiple temperatures and load pull measurements.

5.1 Modelling at multiple temperatures

The possible next future work on this project would be modelling the GaN-HEMT at multiple temperatures. The main purpose of this study would be to extend the lifespan of the ASM-GaN-HEMT model and ensure the stability condition of the device. Analysing the thermal circuit parameters and thermal dependenceies can make the above achievement. The following example, which was conducted in different GaN device, is used to explain the modelling at multiple temperature future task. Meeting the hotspot temperature transient attained by finite element simulation tool can attain the thermal circuit. The following Figure 5.1: Extraction of the thermal impedance vs time of modelled device shows that this model is gained self-heating by dissipation power and fitted by modelling it with five RC cells.
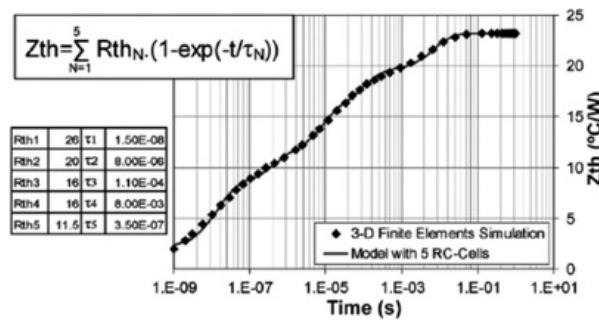
Figure 5.1: Extraction of the thermal impedance vs time of modelled device
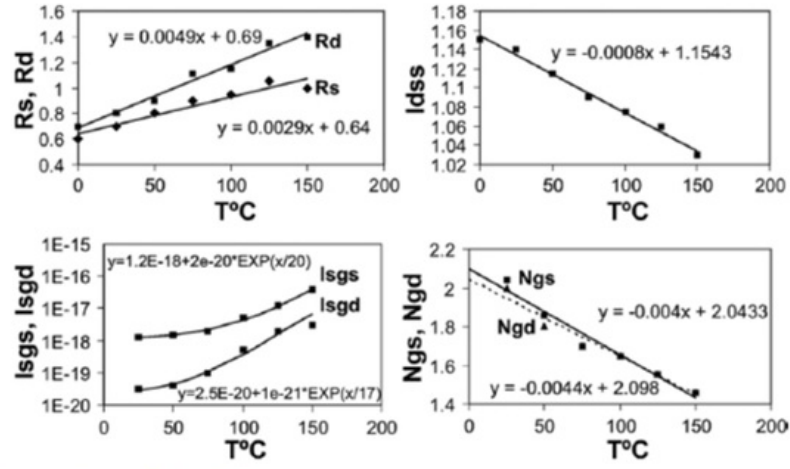
Figure 5.2: Thermal dependence on parameters

The above Figure 5.2: Thermal dependence on parameters explains about the several temperatures has been used from $0°C$ to $200°C$ to fit the quasi-isothermal pulsed I(V) to attain the thermal reliance of the current source parameter. Most of the parameter values were unchanged when it was tested with different temperatures but compel to change for some of them. The interrelations confirm the method of thermal modelling even though the approximation is made. The GaN HEMT temperature does not reflect the hot spot temperature of the model. When extracting through the simulator to enable to get self-heating, which is a very practical easy way to get in time.

5.2 Load-Pull Measurements/Simulations

The load-pull measurements/simulations will be utilised to validate the planned GaN HEMT model. This has to be accomplished in two different frequencies for different load impedance at high voltage standing wave ratio denoted as VSWR. The consequence of trapping effects on the average current is clearly noticeable. The current reduced relevant to the power rise, which is an important outcome of the asymmetric nature. The traps capture and emission method could not be accredited to the thermal outcomes. These thermal outcomes also modelled and the traps state is resolved by the peak values of V_{gs} and V_{ds}. These peak values increased during the increases of input power. [7]

Chapter 6

Conclusion

he GaN-HEMT device is a growing technology, which has a higher possibility in dominating semiconductor industry in the future. This research thesis is mainly conducted on NI AWR Microwave Office simulation tool, which did not automatically supported the Verilog-A codes so Verilog-A was manually incorporated with NI AWR Microwave Office simulation tool with the help of their staff. The research paper further examined the modelling on ASM-GaN-HEMT Triquint 8x40 device, which is further experimented into DC parameter extraction and RF parameter extraction by tuning the ASM-GaN HEMT model with the measured data. The simulations mainly focused on IdVd, IdVg, the magnitude of S-parameters, the phase of S-parameters and Smith charts in order to tune the device with measured data. DC parameter extraction was done in multiple bias conditions, then tuned the different bias condition as a single value on a simulation plot for IdVd and IdVg that causes the outcome of one DC parameter values reflected in the results for multiple bias conditions. RF parameter extraction was done for 20V and 32mA bias condition. Using magnitude of S-parameters and phase of S-parameters modelled RF parameter extractions. The overall outcome of this research is pretty successful and was able to successfully modelled the device with measured data and fit the device simulations with the measured data simulation. There are some future work can be done with this projects on modelling at multiple temperatures, large signal load pull simulations and RF power simulations. GaN HEMT consists of a lot of properties, which can be identified through research and make use of this semiconductor in the designing of new devices.

Appendix A

Abbreviations

HEMT	High Electronics Mobility Transistor
RF	Radio Frequency
GaN	Gallium Nitride
eGaN	Enhancement-mode Gallium Nitride
PA	Power Amplifier
RHP	Right-Hand-Plane
MOSFET	The Metal-Oxide-Semiconductor Field-Effect Transistor
LDMOS	The Laterally Diffused MOSFECT
FET	Field-Effect Transistor
CW	Continuous Wave
NI AWR	National Instruments Applied Wave Research

Appendix B

Initial DC Parameters and values

W = 40.00u
L = 125.0n
LSG = 200.0n
LDG = 1.700u
NF = 8.000
TBAR = 20.00n
GATEMOD = 0.000
RDSMOD = 1.000
VSATACCS = 90.00K
MEXPACCS = 900.0m
MEXPACCD = 900.0m
RSC = 1.000n
RDC = 1.000n
SHMOD = 1.000
RTH0 = 28.00
UTE =-1.100
VOFF =-2.800
UA = 2.500n
UB = 70.00a
U0 = 125.0m
ETA0 = 40.00m
VDSCALE = 10.00
VSAT = 70.00K
DELTA = 2.000
CDSCD = 220.0m
AT = 0.000
U0ACCS = 100.0m
U0ACCD = 100.0m
NS0ACCS = 9.300E+16
NS0ACCD = 9.300E+16
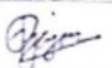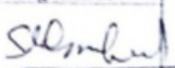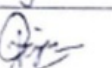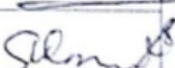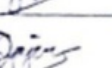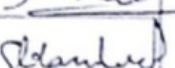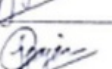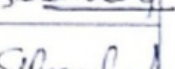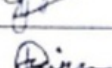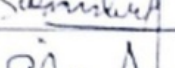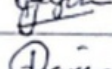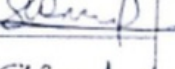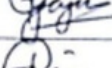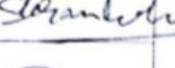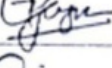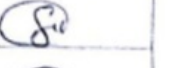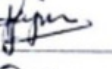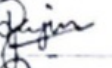
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U0ACCD = 140.0m
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K0ACCD = 90.00m
TRAPMOD = 0.000
LAMBDA = 0.0
NFACTOR = 0.0
IMIN = 100e-18
CTH0 = 1e-6
CGSO = 180e-15
CGDO = 74e-15
CDSO = 80e-15
CGDL = 1.145e-15
ATRAPVOFF = 0.1
BTRAPVOFF = 0.3
ATRAPETA0 = 0
BTRAPETA0 = 0.05
ATRAPRS = 0.1
BTRAPRS = 0.6
ATRAPRD = 0.1
BTRAPRD = 0.6
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Bibliography

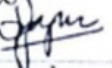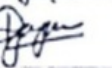[1] (2017, may). [Online]. Available: http://www.awrcorp.com/products/ni-awr-design-environment/microwave-office

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Consultation Meetings Attendance Form

Week	Date	Comments (if applicable)	Student's Signature	Supervisor's Signature
	7/3/2017	Introduction		
	14/3/2017	RF, GaN, Verilog		
	21/3/2017	Simulations		
	28/3/2017	Stability analysis ECP, simulations		
	04/04/2017	Stability analysis, matching network		
	11/04/2017	Power in Vs Power out graph for 500mA		
	18/04/2017	Parameters. Process of the Project		
	26/04/2017	DC Parameters. Manifolds		
	2/05/2017	Parameter extraction & new goals of the project.		
	9/05/2017	DC Parameter extraction.		
	12/05/2017	Parameter extraction for S-parameter.		
	15/05/2017	IDVG1 & IDVD		

Consultation Meetings Attendance Form

Week	Date	Comments (if applicable)	Student's Signature	Supervisor's Signature
	16|5|2017	Phase S-parameters		
	23|5|2017	Capacitance parameters		
	25|5|2017	Smith chart, Phase thesis structure.		
	30|5|2017	Thesis structure & Results Simulations		