PHASE NOISE PREDICTION IN NONLINEAR MIXER CIRCUITS

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STATEMENT OF CANDIDATE

I, Tiernan Vanecek, declare that this report, submitted as part of the requirement for the award of Bachelor of Engineering in the Department of Electronic Engineering, Macquarie University, is entirely my own work unless otherwise referenced or acknowledged. This document has not been submitted for qualification or assessment an any academic institution.

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ABSTRACT

The double balance mixer is a versatile component that is widely used in various electronic applications. As a result, acquiring correct measurements means that it is not trivial to calculate it's phase noise contribution. A 5 MHz double balance mixer from Barnes et al will be studied. The mixer is comprised of commercial off-the-shelf components where the transformers contain a 1:5 impedance ratio that holds the ports at 50 Ω . It will utilise four 2N2222A transistors that operates as it's diode ring where the collector and base ports are shorted. The mixer is explored in it's conversion loss and phase noise contribution. The research will start from a simulation process using National Instruments Microwave Office then a measurement process using those off-the-shelf components. This mixer will be constructed and measured using Macquarie University's laboratory equipment. The aim is to acquire similar results of conversion loss and phase noise to the literature report and to evaluate them. This leads to the research question of can; phase noise be correctly simulated in nonlinear mixer circuits.



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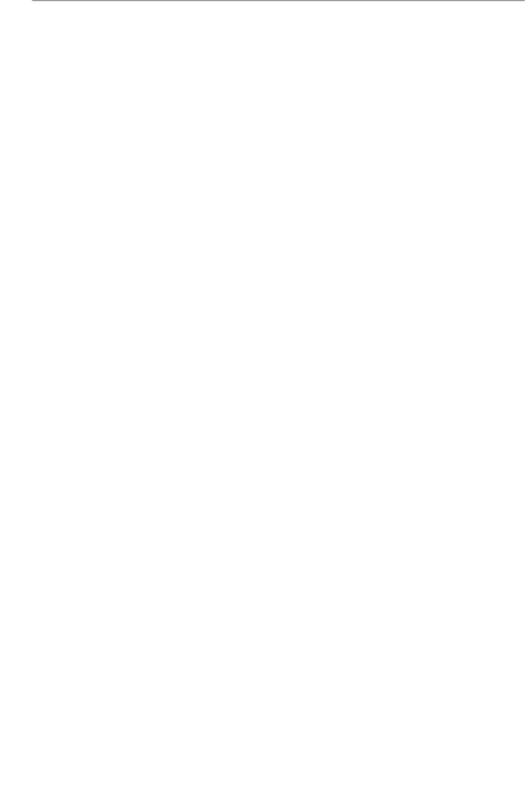
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Abbreviations

3D	Three-dimensional
AF	Flicker-noise exponent
AM	Amplitude Modulation
BJT	Bipolar Junction Transistor
CL	Conversion Loss
$^{\mathrm{dB}}$	Decibels
dBm	Decibel-millwatt
DBM	Double Balance Mixer
DSP	Digital Signal Processing
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
KF	Flicker-noise coefficient
LNA	Low-Noise Amplifier
LO	Local Oscillator
NI	National Instruments
PCB	Printed Circuit Board
\mathbf{PM}	Phase Modulation
PN	Phase Noise
RBW	Resolution Bandwidth
\mathbf{RF}	Radio-frequency
SPICE	Simulation Program with Integrated Circuit Emphasis
SSB	Single Sideband
SWT	Sweep Time
VBW	Video Bandwidth

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Chapter 0. Abbreviations



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Chapter 1 Introduction

Phase noise (PN) is one of the major limiting factors that affects the performance of equipment and systems. It has challenged radio frequency (RF) engineers and technicians since the earliest days as it is a characteristic that limits system performance [25]. When engineers design these telecommunication devices, measurements of PN are gathered from various sources of literature in order to get a good idea of what noise values you may acquire for their design. However, this design process is deemed incapable of predicting PN in mixers.

Double balance mixers are widely used as phase detectors for phase modulation (PM) noise detection at several carrier frequencies [6]. In typical measurement systems, phase detectors are used to remove the carrier and to downconvert the noise sidebands into basebands. Currently there is little literature on the understanding of the PN generated inside this type of mixer. Specifically, the mixer's diode ring utilises bipolar junction transistors (BJT) that intrinsically contain noise attributes [25] [21] [23]. Additionally, the local oscillator (LO) contains at least an active device that contributes to the total noise measured at the output [25]. The report will investigate this type of double balance mixer from Barnes et al, that is rated at 5 MHz. It will be built for simulation and measurement purposes where the sources of noise are investigated from the mixer's diode ring and LO source.

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1.1 Project Goal

The aim is to build the mixer circuit using simulation software for the purposes of conversion loss (CL) and PN contribution. Off-the-shelf components in terms of the BJTs and transformers will be modelled in the software in order to acquire accurate results. These results are aimed to be similar to the acquired measurements found in "5 MHz phase detector with low residual flicker". In the prescribed article, Barnes et al measured the mixers characterisation in it's CL and it's residual PM noise. As a result, there are four main deliverables of the research project. These include:

- Simulation schematic,
- Breadboard prototype,
- Printed Circuit Board (PCB),
- Measurements.

The simulation schematic will use National Instruments (NI) RF/Microwave Circuit Design Software that will produce a schematic of the mixer. This will simulate the measurements and hopefully provide insight of how PN is generated inside the mixer and other sources involved. The breadboard prototype will utilise the off-the-shelf components and use the laboratory equipment to measure the two parameters. These components will be match to the specifications of the schematic as the component identities were not given. Two Rohde Schwarz signal generators (rated at 5 kHz - 6 GHz) will input the signals where the output will be measured using a Rohde Schwarz Spectrum Analyzer (rated at 20 Hz - 67 Ghz).

The PCB will be designed using CircuitMaker that is a open source design software by Altium. The board will be manufactured and measured using the same equipment as mentioned above. This will have it's CL and PM noise contributions explored where a comparison between the deliverables will be investigated. Through the three deliverables, an analysis is conducted in comparing the results acquired and reasons for their discrepancies.

1.2 Project Planning

A project plan for any project is critical for it's development over a set time frame. This section will look into the project's scope, time frame and cost.

1.2.1 Scope

The initial scope is described through the deliverables outlined in section 1.1. Though it is clear that are four stages of the project; the simulations, breadboard prototype, the PCB and measurements, there is a minimal expectation from the research. CL simulations and measurements from the breadboard prototype or PCB are required. Given the time frame of the project, completing all deliverables is feasible.

1.2.2 Time

To ensure the deliverables would be completed on time, a schedule was developed during the previous semester in ENGG460. Given approval by the project supervisor, the schedule is subject to change due to unforeseen difficulties. This was the case in the simulation stage where there was great difficulty correctly simulation the CL and PN due to incorrect transistor modelling. There were also set backs in the breadboard measurements and simulation process as the components were not delivered until week five into the semester.

1.2.3 Cost

Final year thesis students are allocated a base amount of \$300 of financial aid in conducting their research. The off-the-shelf components totalled \$166.74 and the PCB design was a total cost of \$47.99 leaving a \$85.27 surplus. The total amount was above the estimated costs as the transformers were sourced from an overseas manufacturer that generally only supply in large quantities. As a result, a minimum cost benefit amount was charged on top of the component prices. All the other components and equipment required were supplied and are owned by Macquarie University.

Chapter 1. Introduction



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Chapter 2

Background

2.1 Frequency Mixers

RF mixers or in simple terms mixers, are frequency converters used in many RF applications [4] [23]. Mixers change the frequency of an electronic signal while preserving it's characteristics (phase and amplitude) through a process of modulation or demodulation [18]. These devices generally has two input signals, one of which is aimed to be modified in it's frequency. These two input signals are combined together that produces an output signal. This combination of the two input signals creates a nonlinear response [18]. Here the output signal contains harmonics as it is the sum and difference of the two inputs, depending on the type of mixer being used. For this case, the output can be represented by the following equation:

$$f_{IF} = m f_{LO} \pm n f_{RF} \tag{2.1}$$

where f_{LO} as the frequency of the LO, f_{RF} as the RF, f_{IF} as the intermediate frequency (IF) and *m* and *n* are the order of the harmonics from fundamental to infinity [4] [5]. The LO port is typically driven by either a fixed amplitude square wave signal or a sinusoidal wave signal [19]. This unmodulated signal determines the frequency difference between the output and input signals [4]. Depending on the application of the mixer, the f_{RF} and f_{IF} can be interchanged as an input or an output. Downconverting mixers are used in receiver channels where f_{LO} is lower than f_{RF} [4]. This is called a low-side injection and the mixer is a low-side downconverter. When f_{LO} is greater than f_{RF} it is called a high-side injection and the mixer a high-side downconverter. This type of conversion mixer ultimately depends on the output f_{IF} . If the desired frequency is lower than the input f_{RF} then the process is a downconversion and opposite applies to a upconversion mixer [3]. In other words for downconversion mixers, it is:

$$f_{IF} = |f_{LO} - f_{RF}|$$
 or $|f_{RF} - f_{LO}|$ (2.2)

Upconversion or double sideband conversion is shown by:

$$f_{RF1} = f_{LO} - f_{IF}$$
 and $f_{RF2} = f_{LO} + f_{IF}$ (2.3)

 $[\]mathbf{5}$

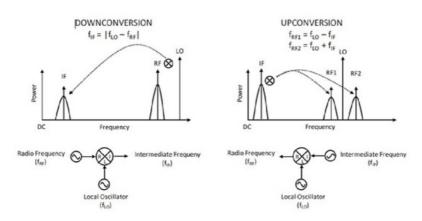


Figure 2.1: Definition of downconverting and upconverting mixers. [18]

where the sum and differences are close together and can imply that both are available at the RF port [3].

Mixing by Nonlinear

If there are two incoming signals into a nonlinear transfer function (i.e. some nonlinear circuit), there will be an inherent blend of intermodulations in that nonlinear element [18] [19] [3]. When performing the Taylor expansion, there is a second ordered term that expands into it's trignonmetric identities that ultimately leads to a sum and difference term. We are interested in the desired mixing aspect of the second order term aside from the DC and second harmonic [3]. These type of mixers are often known as square law mixers that are narrow band and are sensitive in terms of the impedance that are shown around them [4] [5].

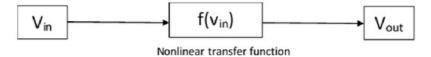


Figure 2.2: Mixing by a nonlinear element [18].

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + \dots$$
(2.4)

Given an input signal:

$$v_{in} = v_{RF} cos(w_{RF}t) + v_{LO} cos(w_{LO}t)$$

$$(2.5)$$

Second Order Term:

$$v_2 = a_2 v_{RF} v_{LO} [\cos((w_{RF} - w_{LO})t) + \cos((w_{RF} + w_{LO})t))]$$
(2.6)

Mixing by Switching

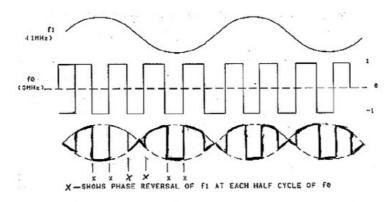


Figure 2.3: Double Balanced Diode Mixer commutation showing a phase reversal at each 50% duty cycle. [5]

Switching mixers contain a strong switching LO signal where a RF is injected into the device. The fast switching LO chops that incoming small signal RF, to create some output waveform as IF. The IF waveform can be mathematically computed as a fourier transform that is represented by the following equation [18].

$$v_{IF} = 2/\pi [sin((w_{RF} + w_{LO})t + sin((w_{RF} - w_{LO})t] - 2/3\pi [sin((w_{RF} + 3w_{LO})t + sin((w_{RF} - 3w_{LO})t] + 2/5\pi [sin((w_{RF} + 5w_{LO})t + sin((w_{RF} - 5w_{LO})t] - ...$$

$$(2.7)$$

or simply

$$v_{IF} = 2/\pi [sin(w_{RF} + w_{LO})t + sin(w_{RF} - w_{LO})t + harmonics]$$
(2.8)

This v_{IF} equation can be seen as the IF signal in figure 2.3. Upon inspecting this equation you can see that the 50% duty cycle, the square wave chopping creates only one RF by odd LO tones [3]. This ends up in the output as one by one, one by three, one by five and so forth. In this particular mixer, the $2/\pi$ term has a minimum 3.92 dB conversion efficiency in the absence of any gain [18]. These type of mxiers can be extremely broadband with it's linearity dependent on the switching speed. A higher linearity is present if the switching speed is increased. If the switching speed of the device is infinitely increased then there no generation of intermodulation distortion. Only odd LO tones by one RF's are generated due to equation 2.7. If two small signal RF are injected, the device cannot intermodulate that switch, to create multi-tone distortion. The broadband feature of the device is dependent on it's operating speed and the surrounding circuits in connection. If the mixer contains very high frequency diodes, for instance to terahertz, then the mixer can switch at a extremely high rate.

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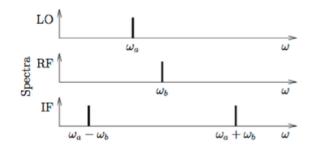


Figure 2.4: Frequency conversion in the spectrum. [6]

The Dirac delta function $\delta(\omega - \omega_0)$ and $\delta(\omega + \omega_0)$ can be used to describe the sinusoidal signal and products in the spectrum. [23]

2.2 Double Balance Mixers

The schematic in figure 2.5 demonstrates what a typical double balance mixer inherently contains. At either side of the schematic are the two input signals with the RF source being the signal that is aimed to be modulated. These inputs are connected at the primary side of the transformers that are stepped up at a certain impedance ratio. At the secondary side of the right transformer which is also connected into the primary of the RF, the output or IF port is connected.

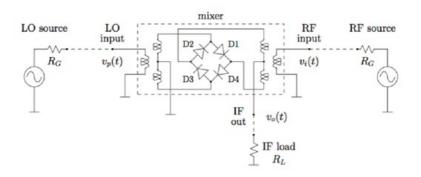


Figure 2.5: Double balance mixer with switch-network equivalence [23]

At the centre of the mixer, there is a diode ring that acts as a switching circuit [19] [23] [7]. This occurs as $v_p(t)$, where the LO input is large against the diode threshold and $v_i(t)$ is small at the RF input. When $v_p(t)$ is at it's positive half-period, two diodes are forward biased to saturation and two diodes to be reversed biased. At the negative half-period of $v_p(t)$, the diode biasing reverses, causing the IF signal $v_o(t)$ to switch between $\pm v_p(t)$ depending on the half-period sign of $v_i(t)$ [23]. The baluns operating at the LO and RF inputs are required in order to convert the unbalanced inputs into balanced signals. This allows for the diode ring to operate as a switching circuit [23] [7]. This switching rate is equal to the frequency at the input LO port [18]. The level of instantaneous $v_o(t)$ is dependent on the level and polarity at the RF secondary winding and what term of that secondary is at a ground potential. The output at the IF port removes even order non-linearities as this is due to the differential output. Furthermore, if the RF and LO frequencies are equal, the difference is a zero frequency DC [15].

The use of two baluns increases the complexity and cost of the mixer and compared to a single balanced mixer, a higher LO drive level is needed. A higher LO drive is needed in order to pump the diodes to the same degree when compared to single-balanced mixers and also to ensure correct diode conductance [7]. A strong conductance is required in order to achieve low noise and to correct converting of large signals without excessively being nonlinear and spurious [7]. In addition, the benefits of this schematic is high isolation of all ports particularly the frequency independence between LO and RF, high conversion efficiency with increased linearity since half of the signal is processed by each side and better suppression of harmonics spurs at the IF port. The higher suppression of harmonics spurs is due only the odd n and m order products of RF and LO surviving at the IF port. Therefore, the double balancing at each source has the benefit of reducing around 75% of spurious interferers [18]. There are some aspects that should be noted concerning the diode ring. When the LO is over-driven i.e. increased to higher V_{LO} , it generates more DC retified current that circulates in the diodes. This DC retified current forward biases the diodes causing them to never going to a fully OFF to a fully ON state; generally in a always ON state. Furthermore, this can reverse breakdown the diodes which comprimises the switching behaviour [23]. The diode ring decreases it's linearity as the V_{LO} is over driven and only improves with large V_f .

2.2.1 Mixer relevant operating modes

In PM noise measurements, the mixer being studied was operated in linear and saturation modes. Each parameter highlights the different effects of manipulating the input signal levels.

Linear Mode

In the report, the mixer is operating as a Linear frequency converter in the first PM noise measurements. This is typically known as a typical superheterodyne receiver. For linear operation:

$$v_i \neq v_l \quad \text{and} \quad P_i \ll P_S \tag{2.9}$$

where the input RF voltage is not equal to the internal LO signal and the input power is much-less-than the internal LO saturation power [23]. Linear operation requires the LO port to be saturated by a sinusoidal signal, a small (narrowband) signal at the RF input and the RF and LO signals are at separate frequencies. In the PM noise measurement, LO = +11 dBm and RF = +5 dBm [6] which affirms equation 2.9.

Phase detector Mode

When LO and RF inputs are saturated, the mixer's behaviour changes. Instead of the switching action of the RF signal depending on the LO sign, the largest signal at that instant, controls the switch. This therefore sets the polarity of the other signal. These roles interchange between the signals and change continuously. There is inherent PN multiplication due to harmonic generation [22]. Here the multiplication takes place in the RF and LO signals and amplitude has little effect on the output IF.

Phase detector mode is a saturated operation of the mixer [23]. Phase detectors output the difference in phase between two signals inputs as a voltage signal. Mixers, particulary a double balance mixer, can be used in this way. From Barnes et al, the mixer schematic was used a phase detector for various carrier frequencies [6]. This type of mixer can have several types of operating modes that depend on several conditions. These include the amount of power (P), voltage(V) and current (I) at the ports [23]. In the report, the

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2.2 Double Balance Mixers

double balance mixer is used as a phase detector rated at 5 MHz. For operating as a phase detector:

$$v_i = v_l$$
 and $P_i \ge P_S$ (2.10)

where the input RF voltage is equal to the internal LO signal and the input power is equal to the internal LO saturation power [23]. In the PM measurements, the port specifications were LO = RF = +11 dBm [6]. Given that RF and LO are at the same frequency, this cancels the w_{LO} and w_{RF} for each term leaving only the amplitude and phase difference signals. The output signal of a actual phase detector mixer is the distorted sinusoidal of second order plus a DC term [23]. This can be approximated by

$$v_o(t) = a_2 \sin(2w_0 t + \phi) - a_0 \sin(\phi) \tag{2.11}$$

where the input voltage is equal to the internal LO signal and the input power is greater than equal to the internal LO saturation power [23] [15]. The experimental parameters a_2 and a_0 , depend on the specific mixer and power level. RF and LO port are saturated by sinusoidal signals and are to be in quadrature, i.e. separated in phase by 90° [17]. Important specifications of a phase detector include the DC offset, isolation between ports, the maximum DC output, the polarity of output voltage and the frequency response (i.e the input frequency with varying maximum DC output) [15].

2.3 Noise

In many small signal applications, it is essential to minimize the degrading effects of noise. Unwanted signals obscure the desired signal as they set the ultimate limit of detectability of weak signals [12]. In the absence of weak signals, this degrades the measurement accuracy [8].

Noise is a characteristic of all electronic circuits and must be accounted for in many RF applications [21]. There are some forms of noise that can not be avoided such as measured quantity fluctuations (which have to overcome by a process of bandwidth narrowing), and signal averaging. Other types such as "ground loops" and RF interference can be reduced/eliminated by filtering, careful component location, wiring configuration and use of low-noise amplifiers (LNA) [2].

Chief offenders of noise can be classified as Johnson (Nyquist) noise, shot noise, 1/f flicker noise and burst noise. [22] [2] [12]. The first two listed types of noise are irreducible forms as they are based on the physical properties. Johnson noise or (Nyquist noise) relates to the thermal agitation of free electrons as current passes through some conductor. It has a flat frequency spectrum meaning the noise power is the same for each hertz of frequency. Flat frequency noise is also called "white noise". Shot noise is the random nature of current flow that is independent to frequency and temperature factors. This type of noise is white and follows a Gaussian distribution, like Johnson noise [21].

1/f Flicker noise or sometimes called "pink noise" is a signal that changes in amplitude over the frequency. When plotted against current or voltage, the amplitude falls at a $1/\sqrt{f}$ rate. The corner frequency f_c is found as the 1/f noise transitions to white noise. Here the power spectral density is inversely proportional to the frequency band. This means that flicker noise decreases with frequency which is a 1/f characteristic. There are some noise sources that are not characterized by gaussian distribution. Burst noise or "popcorn" noise, consists of random jumps between voltage levels in the frequency domain. These occur in the scales of tens of milliseconds where portions spike without any notable spectral peaks [21] [2].

Noise in Mixers

Noise is inherentely contained in mixer circuits as a result of the components used in the design. Given a passive mixer that only has loss and no gain, the noise figure is almost equal to the insertion loss [20]. A study performed by Marki Microwaves found that the noise addition from passive mixers (using Schottky diodes), is negligible [14]. For each harmonic of LO, the noise is replicated and translated where this is known as Noise Folding [13]. The study did affirm the attunuation of the signal but the amount is equal to the CL.

Mixers are used in the amplifier stages where noise becomes a bigger issue. LO noise is amplified by the various subsequent stages that can be fed with the carrier signal. The desired signal is then surrounded by this band of noise. This complication increases in the mixing stages where if a modulated RF signal is mixed with some clean LO source,

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2.3 Noise

the IF is modulated. However, if a modulated LO source is mixed with some clean RF signal then again the IF is modulated. The total noise is the sum of an infinite number of components over a range of frequencies [22].

Noise Modelling

The key elements in our mixer are the transistors in the diode ring. Transistors contains thermal, shot and 1/f flicker noise [21]. Noise modelling is incrediblely important as we can predict the noise behaviour of the system. This requires accurate noise models which without these models, cannot perform the design and optimisation stages of a system [10].

More related, we look at the 1/f noise exhibited by the transistors. The current dependency of the 1/f is given by this equation:

$$F_{1/f} = KF \cdot \frac{I^{AF}}{F_c} \tag{2.12}$$

where KF = flicker-noise coefficient and AF = flicker exponent [1] [10]. In saying this, the equation does not take into account the thermal noise and shot noise by the base and collector currents.

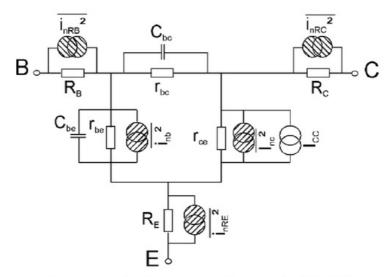


Figure 2.6: Simulation noise schematic of a BJT [10].

In figure 2.6, this represents the noise schematic utilised in Simulation Program with Integrated Circuit Emphasis (SPICE) and other simulators. At each port of the transistor, the sources of noise is contained in the various elements. For each resistor, the thermal noise is represented by:

$$i_{R,I}^2 = 4 \cdot k \cdot T \cdot \frac{1}{R_i} \Delta f$$
 and $i = b, c, e$ (2.13)

where k = Boltzmann's Constant [10]. In the schematic the current at the base and collector are considered independent. The shot noise can be represented by:

$$i_{b,S}^2 = 2 \cdot e \cdot I_b \cdot \Delta f \tag{2.14}$$

for the base where $\Delta f = 1$ Hz. And the collector as:

$$i_{c,S}^2 = 2 \cdot e \cdot I_c \cdot \Delta f \tag{2.15}$$

The base-emitter ports are in parallel by a noise source. This related to the total 1/f noise of the BJT [10]. This leads to the total 1/f noise as:

$$i_{nb}^2 = 2 \cdot e \cdot I_b \cdot \Delta f + KF \cdot \frac{I_b{}^{AF}}{f} \Delta f$$
(2.16)

being the combination of it's shot noise and flicker noise [10]. The resistors are modelled by white noise where as the inductor, capacitors and transmission lines are considered noise free. This is only the case for given ideal components. The BJT models in the simulation chapter have defined parameters for all values from figure 2.6. The amount of noise contribution originate from the parasictic resistors used for biasing the BJT [1]. 2.3 Noise

2.3.1 Phase Noise

Stability in the frequency domain is commonly known in terms of spectral densities. This is referred to as an ideal signal and can be represented in a signal spectral line. For example:

$$v(t) = a_o \sin(\omega_o t) \tag{2.17}$$

where $a_o =$ nominal amplitude and $w_o =$ nominal frequency [11]. However in a real-world application, the signal will always contain unwanted phase and amplitude and phase fluctuation due to inherent noise sources [11] [22]. This can be defined as:

$$v(t) = (a_o + \epsilon(t))sin(\omega_o t + \phi(t))$$
(2.18)

where $\epsilon(t) =$ random amplitude changes and $\phi =$ random phase changes [11]. In the frequency domain, there is a spread of spectral lines that are greater and lower than the nominal signal frequency. This can be seen as modulation sidebands due to the random phase and amplitude fluctuations. As a signal experiences frequency variations or fluctuations, we can relate this as a measurable quantity in terms of it's phase fluctuation. This is what is known as phase noise; revolving around the frequency stability of a signal [11]. The stability of the signal can be categorised in its long-term frequency stability or short-term frequency stability [22] [12]. Long-term frequency stability are the variations measures over periods of hours and above. Short-term frequency stability are the changes over periods of seconds and less. In relation to the mixer studied, the LO variations will be focused on the short-term frequency. Figure 2.6 demonstrates the comparison from ideal to real signals in the time and frequency domains. The top images are an representation of ideal signals. The bottom images are real-world signals. This is due to equation 2.13 where the added ϕ causes phase jitter that translates into the frequency domain as the modulation sidebands.

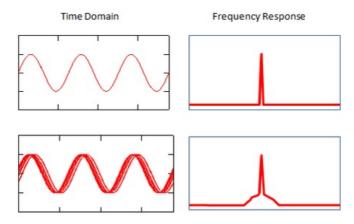


Figure 2.7: Ideal and real signals in the time and frequency domain [24].

Equation 2.13 can be broken down into it's Fourier frequency components of different amplitudes and phases [22]. Through a power spectrum, it is the combination of the power level on the carrier signal and all other components from the result of its amplitude and phase fluctuations. From the amplitude modulation (AM) and PM power spectras, the later of the fluctuations can be called $S_{\phi}(f)$ where the rms phase deviation can be determined at the Fourier frequency f relative to (or offset from) to the fundamental carrier f_c . From figure 2.6 the f_c signal is the peak point of the real-world signal in the frequency domain where the offset is a frequency away from f_c [11].

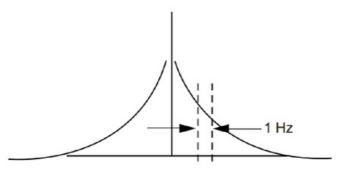


Figure 2.8: Single sideband PN. [1].

The surrounding PM around the carrier can be measured as a one-sided spectral density or single sideband phase noise (SSB) phase noise. The spectral desnity is twice of SSB as this relates to the total phase change. SSB phase noise relates to the relative level of one sideband. Under formal definition, the Institute of Electrical and Electronics Engineers (IEEE) defines PN as:

$$\mathcal{L}(f) = S_{\phi}(f)/2 \tag{2.19}$$

where $S_{\phi}(f)$ is the one-sided spectral density for it's phase instability [11] [12] [26]. This has the units of dBc/Hz as decibels relative to the carrier power per hertz of bandwidth. Measurements of the offset frequency are on a log base 10 format:

$$\mathcal{L}(f) = 10\log[S_{\phi}(f)/2] \tag{2.20}$$

 $\mathcal{L}(f)$ is defined as the SSB that is due to the phase fluctuations in reference to the total power [22];

$$\mathcal{L}(f) = \frac{\text{Noise power in a 1 Hz bandwidth}}{\text{total signal power}}$$
(2.21)

What this means is that given the main carrier, we can measure the power at a desired offset frequency. This can be thought as taking a frequency window on the side-band and measuring the power at some offset frequency away in reference to the carrer frequency 2.3 Noise

power within a 1 Hz bandwidth. Through a spectrum analyzer this is performed as taking the difference of:

$$P_n(dBm/Hz) - P_s(dBm) \tag{2.22}$$

at the carrier. P_n as the power at some offset frequency and P_s as the carrier power [11]. The 1 Hz bandwidth is most convenient as it can easily related to other bandwidths however this requires a very narrow filter bandwidth. Current signal processing technology can widen the bandwidth and mathematically adjust the power level relative to 1 Hz.

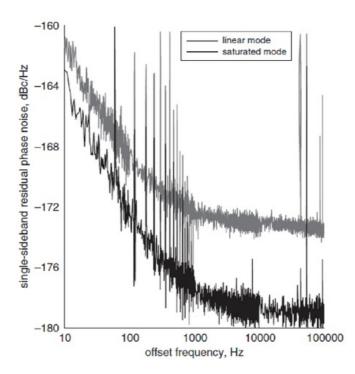


Figure 2.9: PM noise floor of the DBM being studied in linear and saturation operation [6].

In figure 2.7 shows the residual PM noise of the DBM being investigated [6] and how PN is represented. As the offset frequency increases, the 1/f flicker noise dominates most of the graph. After the corner frequency, other noise sources dominate the results which occurs at +1000 Hz. In linear operation, $\mathcal{L}(10Hz) = -161dBc/Hz$ when LO = +11dBmand RF = +5dBm. In saturation mode where LO = RF = +11dBm, $\mathcal{L}(10Hz) = -163dBc/Hz$, the 10Hz noise has improved [6].

Measuring using RBW, VBW and SWT

The resolution bandwidth (RBW) can relate as being the eyes of the spectrum analyzer. It determines that frequencies can be resolved on the screen [8]. For example, given two frequencies are expected at the output, F_1 and F_2 at two difference frequencies. If a large RBW is used, the two signals can be masked a signal broadband carrier. When the bandwidth is reduced, the noise floor is lowered and two frequencies can be resolved. All measurements for conversion loss were maintained at the same RBW frequency.

Video bandwidth (VBW) is a low pass filter that aims to filter out high frequency components [8]. It does not change the noise floor but filters the noise and changes the signal amplitude. Given two signals F_1 and F_2 with a predominant noise floor, the VBW can smooth the amplitude of the noise values. The sweep time (SWT) is the refresh rate of the detector output. Decreasing the SWT changes how often the output is measured. The SWT value however, must be sufficiently slowed in order to allow the detector to properly charge and output correct amplitudes.

Oscillator Phase Noise

Oscillators play an important role of any RF device. They are required for the purpose of mixing, frequency synthesis and operation of phase-locked loops [25]. PN is additive depending on the number of oscillators in the system, and will have a detrimental effect on frequency stability and local channel signals. The origin of PN is inherent in the active devices of the system. In the mixer being studied, this is contained in the four BJTs, due to the Johnson (Nyquist) noise, shot noise, 1/f flicker noise and burst noise. The switching action of the BJT's from their off/on states is dependent on the current pulse duration. If the pulse is constricted to a more narrow width, there will be less PN generated. When the pulse width is increased, more PN is generated in the osciallator [25]. Controlling the pulse width of the oscillator through nonlinear design techniques would control the level of BJT noise contributing PN at the IF.

Noise prediction in oscillators can be expressed through Leeson's model [16]. Designing their oscillator around this parameter has helped engineers control how much noise is reduced in their device. The expression only applies between the 1/f flicker noise frequency down to a dominating white noise frequency [25]. As a result Leesons model equation shows that the PN increases by 6 dB when doubling the loaded-Q and that a 6 dB PN degradation occurs when doubling the operational frequency [16].

2.4 Conversion Loss In Mixers

Conversion loss is an important parameter that must be considered and measured in mixers. From the Barnes et al report, it highlights that the mixer's characterisation from measuring the conversion loss is required before measuring the PM noise [6]. It is the difference between the input P_{RF} and the desired output P_{IF} [18]. In other words,

$$CL = P_{RF} - P_{IF} \tag{2.23}$$

where CL is in dB and P_{RF} and P_{IF} are in dBm. The level of CL is dependent on factors of transmission line losses, mixer (im)balance, balun mismatching and inherent operating device resistances [18]. Figure 2.10 depicts the measured CL for RF and LOs for the Barnes et al report. In the process of downconverting where a higher input dBm signal results in a lower dBm output signal, the difference between the two is the conversion loss. In the process of unconverting, a higher dBm output signal is known as the conversion gain [3].

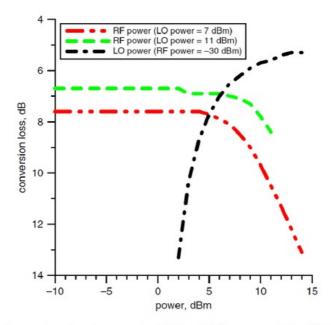


Figure 2.10: Conversion loss from against LO and RF powers of the DBM being studied [6].

Chapter 2. Background



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Chapter 3

Simulating Conversion Loss and Phase Noise

The simulation stage started with gathering SPICE models of the relative components. Specifically, the 2N2222A BJT was acquired from the two only available sources online. One model from Zetex Semiconductors plc and a model from Symmetry Design Systems. The Zetex Semiconductors plc model, dates back to 1992 and represents a Gummel-Poon model. It does not contain a KF or AF parameters when compared to the later SPICE model. Symmetry's Gummel-Poon model does contain Flicker noise parameters that set to defaults values of KF = 0 and AF = 1.

The transformer components were not acquired until week five for the semester. The transformers were measured for their inductance and capacitance. These values were sited into a coupled inductor model in order to correctly represent the T5-1T X65+ transformer.

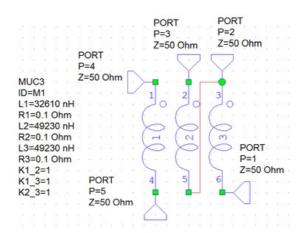


Figure 3.1: T5-1T transformer represented as coupled inductors.

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The transistors were imported as SPICE models and translated into AWR. There are three models that were investigated. Aside the two imported models from online, a third model was created. This used a AWR Gummel-Poon NPN transistor where the parameters from the 1992 model were used. Each of the BJT models were measured for their I-V characteristics where the 1992 model correlated similarly to it's datasheet specified beta ratio.

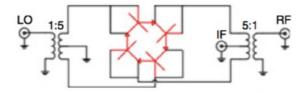


Figure 3.2: Mixer to be simulated. [6]

Figure 3.2 is the schematic that will be simulated. In the design, there are BJTs that will form the diode ring. The base to collector is shorted in order for them to operate as diodes. Figure 3.3 is the schematic used for all simulations. Subcircuits were used in the

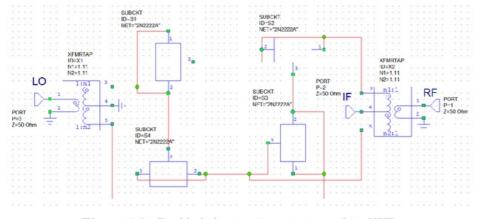


Figure 3.3: Double balance mixer constructed in AWR.

diode ring where each BJT can be selected and simulated. The ideal transformers and the modeled inductors were swapped at various stages. For the ideal transformers, each inductor was given a turn ratio of 1.11. This is about half the square root of five, that is the turn ratio of the prescribed mixer. This is due to:

$$\sqrt{\frac{Z_P}{Z_S}} = \frac{N_P}{N_S} \tag{3.1}$$

where Z_P is the impedance of the primary, Z_S as the secondary impedance, N_P as the primary number of turns and N_S as the secondary number of turns [9]. This ensures that

the input impedances of RF and LO ports are nearly 50Ω at 5MHz. The transformers have two input to output turn ratios where the combination is the total ratio for that side.

3.1 Mixer characteristion

Great difficulty was initially found in gathering all results found in this section. The AWR software provides various example simulation files. Specifically under the name Diode_Mixer, this formed the basis for the CL and PN simulations. This Diode_Mixer file was manipulated for purpose of this double balance mixer simulation as the original file simulated the CL and PN of diode mixer utilising a Lange coupler.

There are various stages of the simulation process. For work efficiency and removing the room for error between different simulations, the schematic in figure 3.3 was made as a subcircuit. For all results shown in this chapter and following two subsections, an **ideal BJT with Zetex Semiconductors plc (1992) model parameters** was used. When the SPICE models were imported and used directly in the schematic, simulations did not correlate well to the literature results and were deemed incorrect. **The hybrid model produced the best results for all simulations.**

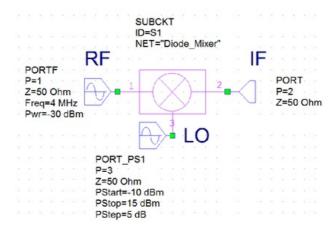


Figure 3.4: Conversion loss simulation bench for LO.

The schematic in figure 3.4 forms the basis for simulating the LO power. A varied power of a 5 MHz signal is applied to the RF port while a 4 MHz signal at -30 dBm is applied at the RF port. The LO port uses a power sweep of -10 dBm to 15 dBm that is rerepresented as the x-axis. The power ratio is taken from the IF port at a 1 MHz beat to the RF port. The type of measurement was a large signal S parameter at harmonic. Measurement went from Port 1 to Port 2, harmonic index of 1 MHz as this is our f_{IF} and second Harmonic index at 4 MHz.

$\mathbf{24}$

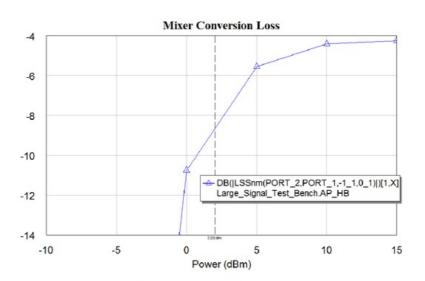


Figure 3.5: Conversion loss for schematic LO power(RF power = -30 dBm).

The output of the LO power simulation follows similarly to the literature trend and values found in figure 2.10. The simulation saturates around 4.5 dB loss with the 1 dB compression point at +5 dBm.

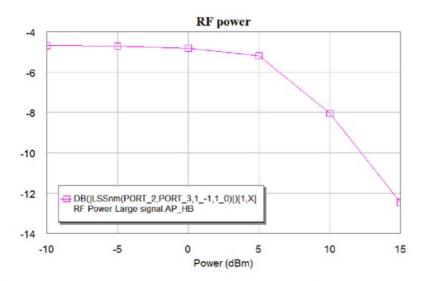


Figure 3.6: Simulated conversion loss aganst RF power(LO power = 7 dBm).

 $\mathbf{25}$

The simulation schematic for against RF signal power is the same as in figure 3.4. LO and RF ports were swapped with LO is set to 4 MHz and RF at 5 MHz at constant LO drive powers. The RF powers were simulated for LO power = 7 dBm and LO power = 11 dBm. The type of measurment was kept the same with it's properties adjusted accordingly. The overall results for the RF powers followed a similar trend when compared to figure 2.10. RF power at 7 dBm drive has a short saturation that consists of 1 dB compression point of +6 dBm. The loss is around 3 dB higher at saturation which improves to a 1 dB difference at +10 dBm.

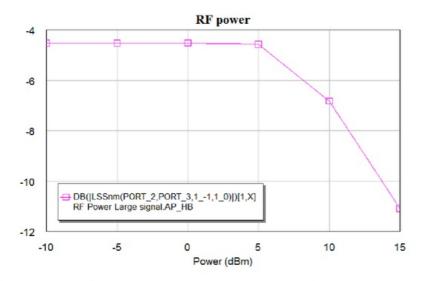


Figure 3.7: Simulated conversion loss aganst RF power(LO power = 11 dBm).

The drive at 11 dBm is more correlated to the literature with a CL difference of 2 dB and a 1 dB compression point around +7 dBm. All CL simulations were higher than expected meaning these actually had better performance than the report. The hybrid BJT model works and the overal mixer works as expected. In order to increase the CL of the schematic, the coupled inductors in figure 3.1 should be used and simulated. Since it is modelled without the modelled transformers, these should return high dB results given it's real-world characteristics. Due to time constraints this was not simulated and will be noted as a task in future work.

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3.2 Phase noise simulation

The PN test bench is found in figure 3.8. This has been setup to simulate the PN out of the mixer while providing PN at the LO port. The output PN will be represented as a SSB of simulated noise contributions of the schematic. In this section, two simulations were recorded. One represents the mixer operating in linear mode and the other operating in saturaton. A NLNOISE block is used to specify what frequencies are to be simulated for the PN and also directs the PN by specifying the input and output ports. A V_NSMTR element is used to identify the output node for noise contributor measurements. This is connected from the output to ground.

Following the same specifications as the literature, the noise frequency starts at 1e-5 MHz and ends at 0.1 MHz at log10 increments. All noise contributions at the output is detailed by Source. A oscillator called OSC_W_PH_Noise is connected from the LO port to ground. OSC_W_PH_Noise specifies the frequency, power, PN vs offset frequency and impedance. It is these vectors that set the shape of a SSB graph. The AF parameter intially started at 1e-004 and adjusted to a smaller value to 1e-008 as this gave the most improved PN without saturating the results. The AF was set to 2 and stayed at this value for all PN simulations.

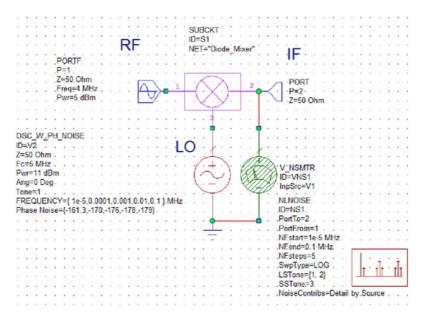


Figure 3.8: Phase noise simulation bench for linear mode.

(3.2)

3.2.1 Linear Mode

For operation of the linear mode, LO = +11 dBm at 5 MHz and RF = +5 dBm at 4 MHz. Output equations were used to plot the PN measurements. The PN equations are as follows.

 PN_dB is equal to:

 $Phase_Noise_Test_Bench.AP_HB.\$F_SPEC : DB(PH_NOISE_NL(-1_1))[*, X]$

 $Phase_NOISE_dB$ is equal to:

 $assign_swpunit(plot_vs(PN_dB, 1e6 - swpvals(PN_dB)), 1)$ (3.3)

Equation 3.2 for PN_dB is the nonlinear noise measurement utilising the NLNOISE block. This outputs the large-signal harmonic that is set to 1 MHz. Equation 3.3 is used to subtract the IF from the x-axis which allows the results to be plotted against the offset frequency. A large amount of difficulty was found here in using output equations in setting the correct offset frequency.

The results were achieved through a process of reverse engineering the model parameters for their flicker coefficient and the level of oscillator PN contribution. The approach for both mixers was the same. Initially, the oscillator PN values ranged from 140 dBc/Hz in 20 dBc/Hz increments; up to a max level of 220 dBc/Hz for 0.1 MHz. The KF value was adjusted where as the coefficient becomes smaller, the 10 Hz noise improves. When the KF exponent cannot improve the 10 Hz noise anymore, the oscillator PN values were adjusted according to the literature graph.

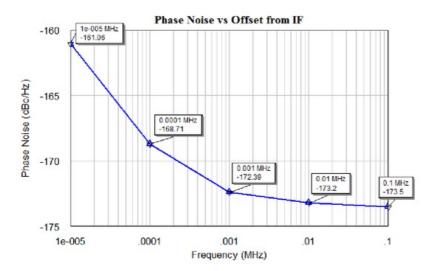


Figure 3.9: PM noise floor of mixer in linear mode.

The flicker noise of the mixer at $\mathcal{L}(10 \text{ Hz}) = 161.06 \text{ dBc/Hz}$. The frequency that is relatively close to the carrier is primarily defined by the LO and is also known as the flicker FM. At 10 Hz on OSC_W_PH_Noise element defines the PN as -161.3 dBc/Hz. The difference between the two is 0.24 dBc/Hz. This may be the mixer's PN contribution due to it's inherent active devices. As the frequency offset increases, the oscillators PN influence decreases. This is also the case with the BJT's KF values where beyond KF = 1e-009 as a smaller value, there is little improvement to the PN simulations.

3.2.2 Saturation Mode

Saturation saw the input powers being equivalent where LO = RF = +11 dBm.

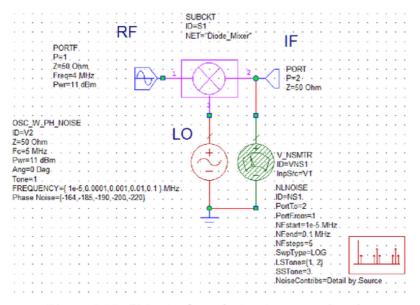


Figure 3.10: PM noise floor of mixer in saturated mode.

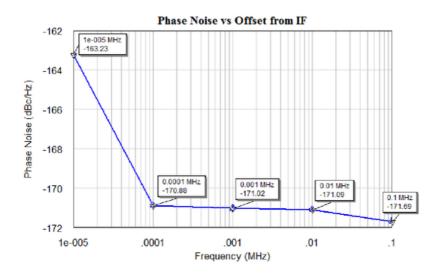


Figure 3.11: PM noise of mixer in saturation mode.

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From figure 3.11 the 10 Hz noise is improved to $\mathcal{L}(10 \text{ Hz}) = 163.23 \text{ dBc/Hz}$. This is a very similar result to the literature where at $\mathcal{L}(10 \text{ Hz}) = 163 \text{ dBc/Hz}$. At the corner frequency, this point almost leads to white noise as the 100 Hz point completely saturates the SSB noise values. The rest of the graph is far too saturated with the 10 Hz offset frequency being primarily defined by the LO. Using the same process for linear operation, this is the most improvement this schematic can produce. At KF = 1e-0014 and reducing it to smaller values, there no improved flicker noise. The PN values of the oscillator also do not further improve the flicker noise.

The amount of PN discrepancy between the OSC_W_PH_Noise element and the simulations are larger compared to linear operation. At 100 Hz there is a difference of 9.12 dBc/Hz that increases with the offset frequencies. Under the assumption that the added noise is due to the mixer, the level of PN is multiplied due to harmonic generation. Specifically in saturation mode, the multiplication occurs in LO and RF. This may be the reason why the level of PN is much larger compared to linear operation.

Chapter 3. Simulating Conversion Loss and Phase Noise

Chapter 4

Measuring the mixer

Measuring CL and PN is the second part of this research. This section investigates the design process of the breadboard and PCB through to the measurement stages. Both mixer boards were measured as well as some of the components. Some of this data aided the simulation process as ideal components were required in order to provide correct simulation results. Such data gathered in this section will hope to generate a better understanding of the residual PM noise of the mixer and provide solid grounds for further research.

The spectrum analyzer in the laboratory has been flagged for producing incorrect PN measurements and is currently scheduled for repair. As a result, **the mixer PM noise measurements have not been conducted** in the labs due to time constraints and the inability of performing the measurement.

4.1 Double balance mixer design

The double balance mixer was designed into it's breadboard prototype and then to it's PCB design. The PCB was pushed for design as there was doubt in the results acquired due to it's unprofessional finish and it's high sensitivity.

4.1.1 Breadboard Prototype

The components were ordered from Mini-Circuits and element14 where they arrived in week five of the semester. The board was constructed using student level parts such as the wires and breadboards. This can be seen in figure 4.1 where the board is under test. The transformers are on the left breadboard with the BJTs on the right side. All grounds were connected on the left negative rail.

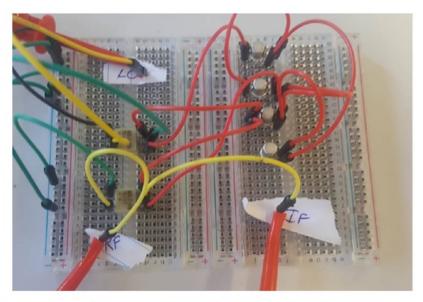


Figure 4.1: Breadboard mixer under test.

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4.1.2 Printed Circuit Board Design

The PCB design and manufacture process took up to two weeks for completion. The design process started with the components. The component footprints can either be created manually or sourced from Altium's online library. Given the 2N2222A is a common component, a symbol and footprint were already made and was accessible to the public. The footprint was thoroughly checked in terms of their footprint dimensions when compared to it's data sheet. Unfortunately the T5-1T transformer was not listed in the component library which meant it had to be constructed. The symbol used a basic DIP-6 format where the centertap was removed on the left side. By following the datasheet of the transformer, the configuration of the pins were formatted and were throughly checked over. Correct pin configuration directly links to the routing procedure for the PCB. This can be seen in figure 4.2.

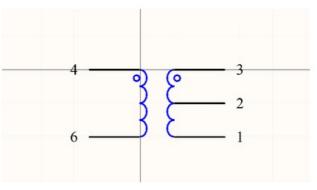


Figure 4.2: T5-1T Symbol used for the schematic.

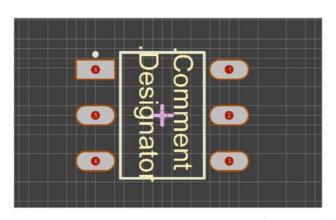


Figure 4.3: T5-1T with a X65+ case footprint used for the schematic.

As the pins were finalised, the footprint needs to be configured. Utilising a generic DIP-6 format, the horizontal and vertical distances between the pins were adjusted accordingly to it's datasheet. Hole sizes were set to 0.6mm set with a 2.5mm by 1.2mm solder bases. A rectangle shape was placed on the assembly text top for placement purposes. This is seen in figure 4.3 with pin 6, represented as a dot symbolising the top orientation for the transformer.

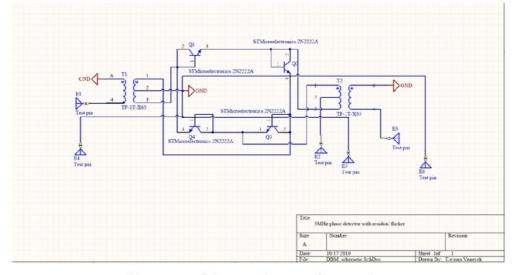


Figure 4.4: Schematic drawn in Circuitmaker.

The schematic can be summarised in figure 4.4. Tests pins were created to allow routing to a hole connection in the PCB document. These are represented as E1 - E6 with input/output dummy antennas.

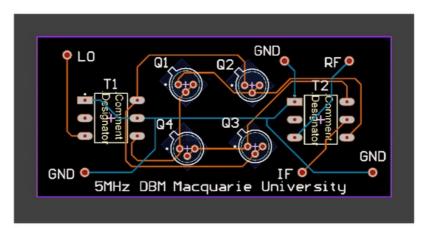


Figure 4.5: PCB document of the mixer being studied.

The PCB design follows the same layout as the other schematics seen in this report. With LO on the left and RF and IF on the right. The board was set to 60mm by 27mm to reduce board manufacturing costs and reduce routing distances. Test pin pads were set with a hole size of 1mm diameter with a standard drilled type and size of 1.5mm by 1.5mm. This increases the ease of soldering and reduces room for error, if the test pins were micrometers larger. Routing tracks were defined and locked as what was specified in the schematic document. These tracks were manually done as auto-routing was not recommended and given the size of the schematic, is most manageable. Most routes were made on the top layer with the exception of the GND tracks and a track for the RF port. Top layer tracks are represented as the orange routes and bottom layer tracks are in blue. These were placed on the bottom layer to overcome routing issues. Tracks were at a default size of 0.25mm in width however, these should of been increased as advised by the supervisor. The total thickness of the board is 1.12mm with the dielectric set to 1mm, solder masks were set to 0.025mm and signal layers set to 0.035mm.

Layer Name	Туре	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation
 Top Overlay	Overlay						
 Top Solder	Solder Mask/Co	Surface Material	0.0254	Solder Resist	3.5		
 Top Layer	Signal	Copper	0.03556				Тор
Dielectric 1	Dielectric	Core	1	FR-4	4.6		
 Bottom Layer	Signal	Copper	0.03556				Bottom
 Bottom Solder	Solder Mask/Co	Surface Material	0.0254	Solder Resist	3.5		
 Bottom Overlay	Overlay						

Figure 4.6: PCB physical layers and their sizes.



Figure 4.7: 3D representation of the mixer in CircuitMaker.



Figure 4.8: Mixer under test with the PCB containing soldered components.

The board was chosen from series of recommended manufacturers that are based overseas. The company PCBWAY was used due to it's fast manufacturing time and of it's low cost. When sending the files off for manufacture, there were issues of the board not containing a keepout/board outline. This was corrected when given advice on the Circuitmaker forums where a track was made on the keepout and outline layers. Rubber feet were positioned at each corner of the board in order to isolate the board when placed on a table and create a more static board that keeps it from sliding due to the long measuring cables. When soldering the components onto the board, there were difficulties with the T5-1T transformers. The pins had to be slightly bent away from each other in order to be placed in the holes. This was because the DIP-6 footprint pin holes are slightly too far apart from each other. Another slight error in the PCB design is found next to the transformer on the right (T2). Here the connection from pin 3, there is a right-angled track, which should be a minimum 45° . Given the use of the mixer, this shouldn't be of concern and should not affect the measurement results.

4.2 Experimental Results

4.2.1 Literature graphing

The CL of the 5 MHz mixer from Barnes et al was replotted into the same scaled graphs as the measurements acquired. This allows a proper comparison between the results. These values are the closest approximation from what the report presents as the graph is 5cm by 5cm in size. In figure 4.9, the 1 dB compression point of the LO drive is found to occur at a level of +8 dBm. A second measurement of CL against RF power at a selected LO power (11 dBm) has a 1 dB compression point occuring at +5 dbm. This characteristation was found in order find the nominal operating powers for the mixer when performing PM noise measurements.

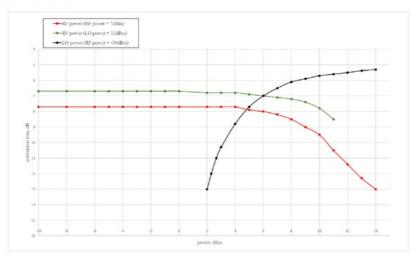


Figure 4.9: Literature mixer's conversion loss.

4.2.2 Breadboard measurements

Before any PM noise measurements, the breadboard and PCB models are measured for their CL. As the components are rated at 5 MHz, the ports in the breadboard and PCB should be impedance match at 50 Ω [6]. The set up for the breadboard used the classroom graded cables and measuring hooks. These can be seen in figure 4.8. These cables are very long and had to be sticky-taped to the table. This decreased the precision of recording the results as the cable's sensitivity produced additional jitter noise which caused the measurement values to fluctuate. There was a concern for the cable loss given the length and how they would affect the total CL of the mixer. Since there would be a total of three used, a calibration test was made with the signal source connected directly to the

4.2 Experimental Results

spectrum analyzer. The cable loss was found to be roughly 0.5 db that totals roughly 1 db given:

$$CG = IF - RF$$
 or $CL = RF - IF$ (4.1)

for the conversion gain where - 0.5 dBm - 0.5 dBm is made on the RF side or vice versa. In order to ensure consistent measurements across the two mixer models, the RBW, VBW and SWT were set to the same values for different operating powers and experiments. Spectrum analyzer measurements were set as RBW = 10 kHz, VBW = 3 kHz and SWT = 10ms. A capacitor specified SMA plug was connected at the spectrum analyzer input. This ment that a capacitor is essentially connected across the IF port that blocks any DC to the spectrum analyzer. This is a precaution measure in order to protect the spectrum analyzer as no DC should be allowed into the unit, as Mixer's can output a DC component. Measurements were taken at the input ports LO and RF ports that were either set at 5 MHz and 4 MHz, depending what nominal operating power was being found.

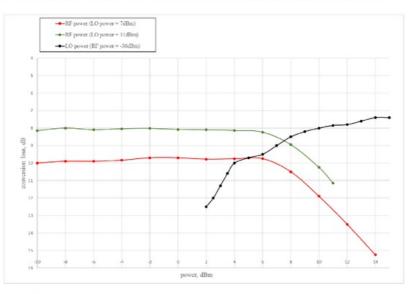


Figure 4.10: Breadboard prototype measured conversion loss.

The results acquired can be seen in Appendix E where the CL was calculated using equation 2.22. The breadboard prototype had roughly a 2 dB lower loss that with the literature. The LO power suffered the most with inconsistent linearity from throughout the range. This was also the case with the RF powers, where the increase of RF power sweep, caused the mixer to suffer higher losses with LO power = 11 dBm presenting a maximum 15 dB conversion loss. The 1 dB compression point of the LO drive is found to occur at a level of +10 dBm and the compression point of conversion loss at the RF port is found to occur at +7 dBm. The graphs followed similarly to the literature however

were deemed not very precise. The use of large mesuring cables and a messy breadboard setup, added the additional losses to the results.

4.2.3 Printed circuit board measurements

The results acquired corellated very well when compared to the literature results, with the RF powers showing the most promising results.

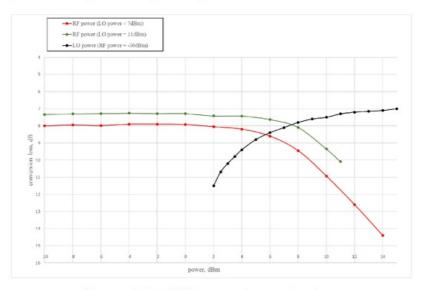


Figure 4.11: PCB measured conversion loss.

The connection inefficiency and sensitivity between components was overcome with the PCB. The same measuring cables were used in the process with the same spectrum analyzer setup. There is a descrepancy of roughly 0.3 dB across the RF power band for LO drives of 7 dBm and 11 dBm. Here the 1 dB compression point found at the RF port occurs at +5 dBm. For the measurments of the LO power, there is better conversion loss at lower LO powers however worse CL values at higher LO powers. Here the 1 dB compression point is found to occur at a level of +8.5 dBm. Such differences may be due to the measuring cables used and the spectrum analyzer's inherent specifications. The spectrum analyser is scheduled for a service which may contribute to this difference. As this is only available unit at the time being, the measurement process proceeded ahead. All results for the breadboard and PCB were repeated several times for reliability purposes. These measured results can be see in Appendix E.

Chapter 5 Conclusions

In RF applications, PN is a key parameter that must always be accounted for. As we delve deeper into very complex modulator schemes, noise levels become even more critical. For decades, we have used noise modelling technquies in order to predict the level noise. This simulation process allows engineers to predict the behaviour through design and optimizing stages for their system. However, we do not fully understand the level of PN contribution a mixer adds.

Recently, Barnes et al developed and measured a phase detector with a flicker noise floor at levels of $\mathcal{L}(10 \text{ Hz}) = -163 \text{ dBc/Hz}$. In the interest for Macquarie University's research department, this thesis focused on the area of PN in nonlinear mixer circuits. From the simulation, the mixer operating in linear mode produced results that correlate very well to the report. However, in saturation mode, this was not correctly simulated due to incorrect 1/f modelling. Therefore, it is neccessary to develop new a BJT model that will allow the mixer whether it is linear or saturation mode, to output correct levels of PN. The various deliverables that have been completed from this semester form a solid ground for further research. Given linear operation of the mixer produced very similar results to the literature, it can be concluded that it is possible to correctly simulate PN in nonlinear mixer circuits.

Future Work

It is recommended that the work carried out in this thesis, be put forward for further research. These areas include correctly simulating PN levels for both linear and saturation modes and measuring the PN for the breadboard/PCB. The schematics developed in AWR use alot of subcircuits, due to the amount of testing comparison between the various BJT models. The mixer characterisation stage used ideal transformers, therefore, these should be simulated again using the modelled T5-1T coupled inductors. Future students or researches can easily adapt and manipulate the circuit as the schematic development process was very time-consuming.



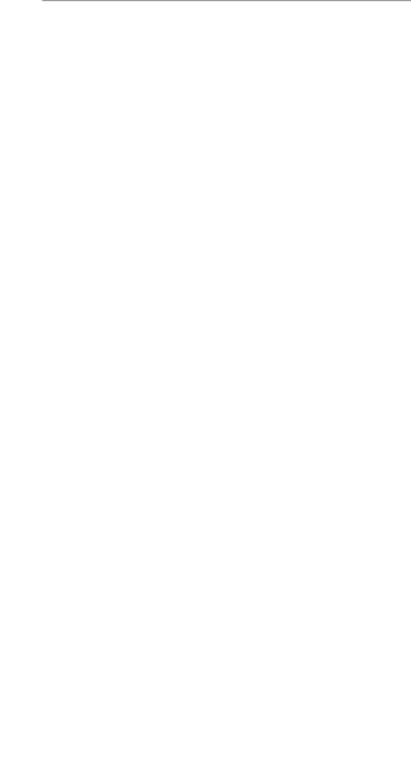
Appendix A Project Timeline

This project plan was designed in the previous semester. As a requirement of ENGG460, this plan was approved by the supervisor. Given the several difficulties encountered throughout the semester, the plan was modified in order to accomplish nearly all deliverables.

	Task	Location	Week 1	Week 2	Week 3	Week 4	Week 5	Week 6	Recess	Week 7	Week 8	Week 9	Week 1	Week 1	1 Week 3	2 Week 1	13 Exams Wk	Exams Wk2
1	Order BJT components	University																
2	Design AWR Schematic	Home	1000															
3	Simulate AWR Schematic	Home	1															
4	Review Laboratory Equipment	University Labs	1															
5	ENGG411 Progress Report	Home																
6	Construct Breadboard Prototype	University Labs	1															
7	Measure Breadboard Prototype	University Labs	1															
8	PCB design*	Home/University																
5	Order PCB from manufactuer	University	1															
10	Construct/Measure PCB	University Labs	1															
11	Final Report	Home/University											1					
12	Seminar Abstract	Home/University	-															
13	Demonstration & Poster	Home/University																

Figure A.1: Project timeline

Chapter A. Project Timeline



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Appendix B Attendence Form

This appendix contains the consultation meetings attendence form. These were held on a weekly basis where the research progress would be discussed. Both student and supervisor must sign off consultation meetings as a requirement of ENGG411.

Week	Date	Comments (if applicable)	Student's Signature	Supervisor's Signature
1	3/8/16	Project Scripe Lab induction	and	Oyabril.
2	10/8/16	MACOM meeting Nih SYD Bign sugget reference [2] for impedance mismeth with applified	1 Min	Oyalinh:
3	17/8/16.	KF, OF, BJT model, Skurn Mare resemb popers, Topsforme results, resuscence	Cull	Oyabinh:
4	31/8/16	Schemitic changes, Auguss urport, parts arrived	and	Oyabine
5	30/87/9/16	Transfor and miver simulations	and	Oyalinhi
6	14/9/16		end	Oyafinli
7	21/9/16	Simulations, Croph measurements in small, pers dessign	and	Oyaline:
8	28/9/16.	Simulations, transformers, Di BJ B comparison, add michisdo (DO 13 5.000.	Lesm	Oyalinh:
9	5/10/16	PLB Jesign, Transformer test, Simulations.	and	Dy adiala
10	12/10/16	Stimulations, PCD, Nose mobiling sim	althe	Dyasimle
11	19/10/16	Simuthans, Noize modelling sum	1	Oyabind.
12.	26/10/16	Simulations, report feedback.	and	Oyasemh

Consultation Meetings Attendance Form

Appendix C Relevant paper

The research project is based on the research article shown below.

5 MHz phase detector with low residual flicker

C.A. Barnes, A. Hati, C.W. Nelson and D.A. Howe

The measurement of close-to-carrier phase modulation (PM) noise of state-of-the-art oscillators is always challenging. Quite often the residual noise of the phase detector used in these measurements is higher than the noise of the source at Fourier offset frequencies between 5 and 1001Rz. A conventional double balanced mixer using 2N2222A transistors as the nonlinear components of a diode ring was constructed for use as a phase detector. Residual single-sideband PM noise measurements at 5 MHz for this device have shown a low flicker noise floor of L(10 Hz) = -163 dBc/Hz. When this mixer design is implemented in a dual-channel measurement system, a cross-correlated PM noise floor of better than L(10 Hz) = -170 dBc/Hz is expected.

Introduction: The double balanced mixer (DBM) is the most widely used phase detector for high-resolution phase modulation (PM) noise detection at most carrier frequencies. Often, the measurement of PM noise is difficult owing to the high dynamic range that exists between the carrier and the modulated sidebands. In typical measurement systems, a phase detector is used to remove the carrier and downconvert noise sidebands to baseband. For offset frequencies close to the carrier, the residual flicker noise of the DBM is often the limiting factor of a phase noise measurement system. The most difficult range of offset frequencies to measure is between 5 and 100 Hz, where the oscillator noise has a slope of f^{-3} , while the measurement system noise floor follows f^{-1} . The 2N2222A bipolar junction transistor (BJT) has been successfully used in low-flicker PM noise circuits [1, 2] and is chosen as the low noise nonlinear element in a custon-built DBM design. A pair of mixers using this design can be used to construct a cross-correlation PM measurement system to reduce the PM residual noise floor further.

Proposed DBM design: Fig. 1 shows the general topology of the DBM. In this design there are four 2N222A BJTs used to construct a conventional double balanced diode ring. By shorting the base to the collector these BJTs will operate as diodes. The transformers used for this design are commercial off-the-shelf parts and have a 1:5 impedance ratio. This impedance ratio is chosen so that the input impedances of the reference frequency (RF) and local oscillator (LO) ports are nearly 50 Ω at 5 MHz. The mixer's input impedances are measured using the Smith chart display of a vector network analyser.



Fig. 1 Double balanced mixer schematic Diode ring in this double balanced mixer is constructed by use of transistors with collector input tied to base

Mixer characterisation: To measure the PM noise of the DBM the nominal operating powers need to be found [3]. To determine the nominal LO power, a 4 MHz sinusoidal signal at -30 dBm is applied to the RF port of the mixer while the power of a 5 MHz signal at the LO port is varied. Conversion loss of the mixer is calculated by taking the power ratio of the 1 MHz beat at the intermediate frequency (IF) port to the RF signal at 5 MHz. A plot of conversion loss against LO power is shown in Fig. 2. By use of this plot, the 1 dB compression point of the LO drive is found to occur at a level of +8 dBm. Operating the LO port in saturation is desired to reduce LO power fluctuation sensitivity. Taking the maximum allowed operating specifications of the transistors and transformers into account, a nominal LO drive of +11 dBm is selected. An additional measurement of conversion loss against RF power at the selected nominal LO was made and is plotted in Fig. 2. The 1 dB compression point of conversion loss, at the RF port, occurs at +5 dBm. All conversion loss tests for the mixer were conducted with a 50 Ω load at the IF port.

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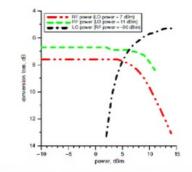


Fig. 2 Conversion loss against LO power of mixer with a = 30 dBm RFpower level (RF at 4 MHz, LO at 5 MHz, 50 Ω input impedance to FFT); and conversion loss against RF signal power at constant LO drive powers (LO at 4 MHz, RF at 5 MHz, 50 Ω input impedance to FFT)

Mixer PM noise measurements: Residual PM noise of the DBM was measured by use of a cross-correlated homodyne measurement system [4]. In phase quadrature, the common mode phase noise of the oscillator and the power amplifier used in this measurement system will cancel out at the mixer. A diplexer terminates the high frequency products of the mixing while still maintaining a high phase-to-voltage conversion at baseband. This diplexer also allows for the baseband signals to be amplified without saturating the IF amplifiers with the 5 and 10 MHz signals from the mixing process. The topology of the diplexer used at the output of the phase detector can play an important role in the mixer's performance [5, 6]. The pair of baseband IF amplifiers mise the residual PM noise of the DBM above the noise floor of the fast Fourier transform (FFT) analyser. The uncorrelated input voltage noise of each IF amplifier can be minimised by the use of cross-correlation, allowing measurement of the thermal residual noise in the mixer.

of the thermal residual noise in the mixer. Fig. 3 shows the results of the residual PM noise of this DBM design used as a phase detector. From this data it can be seen that the flicker noise of this device is L(10 Hz) = -161 dBc/Hz (L = single-sideband PM noise) when the DBM is operated at LO = +11 dBm and RF = +5 dBm. In deep saturation (LO = RF = +11 dBm) the 10 Hz noise is improved to L(10 Hz) = -163 dBc/Hz. Both these measurements show that this DBM has very low flicker noise as a phase detector.

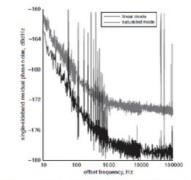


Fig. 3 Cross-correlated residual PM noise floor of 2N2222A based mixer in linear and saturated operation

Conclusions: A DBM mixer design using diode-connected 2N2222A BJT ransistors is presented. The phase detector design in this Letter has shown a residual PM flicker noise floor at levels of L(10 Hz) = -163 dBc/Hz. As compared to many commercially available DBMs used for phase detection at 5 MHz, this design performs among the best. Furthermore, this phase detector will be useful for the measurement

of state-of-the-art oscillators where the phase noise at 10 Hz offset can be difficult to measure with currently available detectors. In the future we will use this detector design in a cross-correlation measurement system and expect the residual noise levels to reach $L(10\mbox{ Hz}) = -\,170\mbox{ dBc/Hz}$ or better.

Acknowledgments: The authors thank J. Searle for the idea of constructing their own mixers; E. Rubiola for an IF amplifier design used in the noise floor measurements described in this Letter [7]; and J. DeSalvo for theoretical discussion regarding measurement systems.

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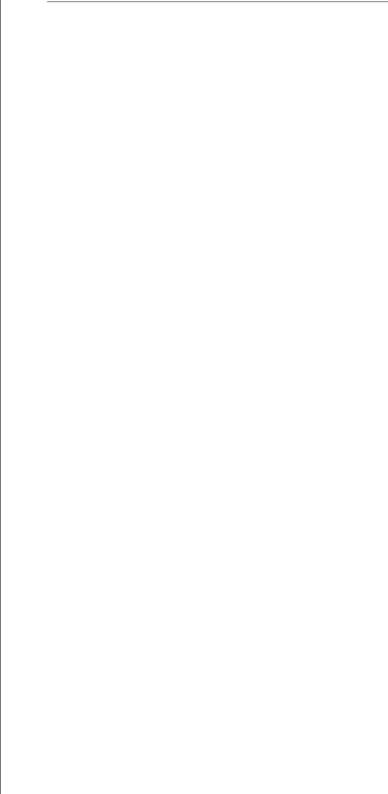
One or more of the Figures in this Letter are available in colour online. C.A. Barnes, A. Hati, C.W. Nelson and D.A. Howe (Department of Commerce, National Institute of Standards and Technology, Time and Frequency Metrology, 325 Broadway, Mailcode 847.30, Boulder, CO words 2327 University 80305-3337, USA)

E-mail: corey.bames@nist.gov

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 Rubiola, E., and Lardet-Vieudrin, F.: 'Low flicker-noise amplifier for 50 Ω sources', *Rev. Sci. Instrum.*, 2004, 75, (5), p. 1323

Chapter C. Relevant paper



Appendix D Off-the-shelf Components

The off-the-shelf component datasheets are shown below. These were acquired from the supplier's website.

2N2222A

Small Signal Switching Transistor

NPN Silicon

Features

- MIL–PRF–19500/255 Qualified
- Available as JAN, JANTX, and JANTXV

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Collector-Emitter Voltage	VCEO	50	Vdc
Collector-Base Voltage	VCBO	75	Vdc
Emitter-Base Voltage	VEBO	6.0	Vdc
Collector Current – Continuous	lc	800	mAdo
Total Device Dissipation @ T _A = 25°C	PT	500	mW
Total Device Dissipation @ T _C = 25°C	PT	1.0	w
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance. Junction to Ambient	R _{BUA}	325	°C/W
Thermal Resistance, Junction to Case	R _{euc}	150	°C/W
Stresses exceeding those listed in the Maxim device. If any of these limits are exceeded, assumed, damage may occur and reliability n	device functio	nality sho	



ON Semiconductor®

http://onsemi.com





TO-18 CASE 206AA STYLE 1

ORDER	ORDERING INFORMATION						
Device	Package	Shipping					
JAN2N2222A							
JANTX2N2222A	TO-18	Bulk					

JANTXV2N2222A

D Semiconductor Components Industries, LLC, 2013 November, 2013 - Rev. 2 Publication Order Number: 2N2222A/D

Figure D.1: 2N2222A datasheet.

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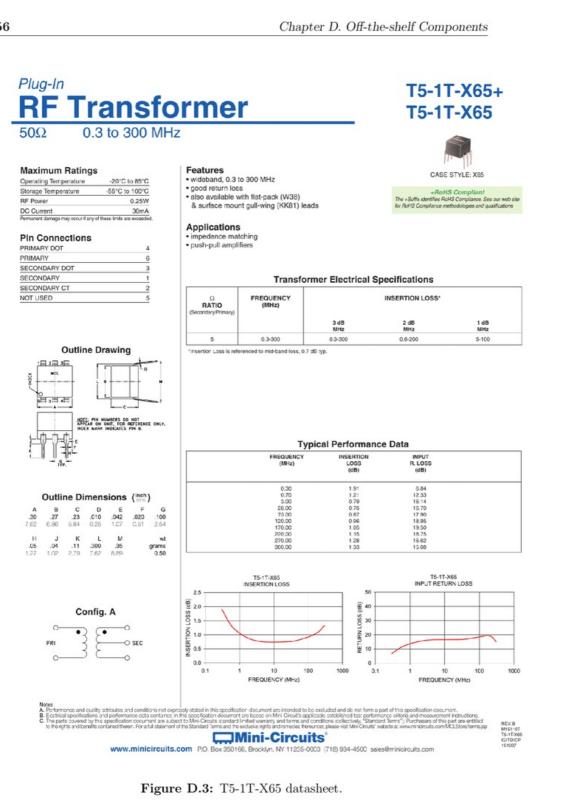
2N2222A

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I _C = 10 mAdc)	V _{(BR)CEO}	50	-	Vdc
	Гсво	-	10 10	µAdc nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0 \text{ Vdc}$) ($V_{EB} = 4.0 \text{ Vdc}$)	IEBO		10 10	µAdc nAdc
Collector-Emitter Cutoff Current (V _{CE} = 50 Vdc)	ICES	-	50	nAdc
ON CHARACTERISTICS (Note 1)				
$ \begin{array}{l} \text{DC Current Gain} \\ (l_{C}=0.1 \text{ mAdc}, V_{CE}=10 \text{ Vdc}) \\ (l_{C}=1.0 \text{ mAdc}, V_{CE}=10 \text{ Vdc}) \\ (l_{C}=10 \text{ mAdc}, V_{CE}=10 \text{ Vdc}) \\ (l_{C}=150 \text{ mAdc}, V_{CE}=10 \text{ Vdc}) \\ (l_{C}=500 \text{ mAdc}, V_{CE}=10 \text{ Vdc}) \end{array} $	hre	50 75 100 100 30	325 300	-
$\begin{array}{l} \text{Collector}-\text{Emitter Saturation Voltage} \\ (I_C=150 \text{ mAdc}, I_B=15 \text{ mAdc}) \\ (I_C=500 \text{ mAdc}, I_B=50 \text{ mAdc}) \end{array}$	V _{CE(set)}	-	0.3 1.0	Vdc
$\begin{array}{l} Base-Emitter Saturation Voltage \\ (I_C=150 \mbox{ mAdc}, I_B=15 \mbox{ mAdc}) \\ (I_C=500 \mbox{ mAdc}, I_B=50 \mbox{ mAdc}) \end{array}$	V _{BE(sot)}	0.6	1.2 2.0	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Magnitude of Small–Signal Current Gain (I _C = 20 mAdc, V _{CE} = 20 Vdc, f = 100 MHz)	h _{fo}	2.5	-	-
Small-Signal Current Gain (I _C = 1.0 mAdc, V _{CE} = 10 Vdc, f = 1 kHz)	h _{fe}	50	-	-
Input Capacitance (V_EB = 0.5 Vdc, I_C = 0, 100 kHz $\leq f \leq$ 1.0 MHz)	Cito	-	25	pF
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0,100 kHz \leq f \leq 1.0 MHz)	C _{obo}	-	8.0	pF
SWITCHING (SATURATED) CHARACTERISTICS				
Turn-On Time (Reference Figure in MIL-PRF-19500/255)	ton	-	35	ns
Turn-Off Time (Reference Figure in MIL-PRF-19500/255)	t _{off}	-	300	ns
and a transmitter of an analytic for the first of the fir				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

http://onsemi.com 2

Figure D.2: 2N2222A datasheet.



Appendix E Conversion Loss Values

This chapter contains the values of the conversion loss graphs found in the measurements chapter. It is important to note that the values found in Table E.1 are found by line of sight on the research paper and are therefore approximations. This was because there were no supplied values by the authors.

	Conve	rsion Loss Literature	Measurem	nents	
LO (RF=-30dBm)	CL (dB)	RF (LO=11dBm)	CL (dB)	RF (LO=7dBm)	CL (db)
2	13	-10	6.7	-10	7.7
2.3	12	-8	6.7	-8	7.7
2.65	11	-6	6.7	-6	7.7
3	10.3	-5	6.7	-5	7.7
4	8.8	-4	6.7	-4	7.7
5	7.7	-3	6.7	-3	7.7
6	7	-2	6.7	-2	7.7
7	6.5	-1	6.7	0	7.7
8	6.1	0	6.7	2	7.7
9	5.9	2	6.8	3	7.7
10	5.7	3	6.8	4	7.7
11	5.6	4	6.8	5	7.9
12	5.5	5	6.9	6	8
13	5.38	6	7	7	8.2
14	5.3	7	7.1	8	8.5
		8	7.2	9	9
		9	7.4	10	9.5
		10	7.8	11	10.5
		11	8.5	12	11.4
				13	12.3
				14	13

 Table E.1: Measured conversion loss from Barnes et al literature.

Chapter E	E. Conversion	Loss	Values
-----------	---------------	------	--------

	Conver	sion Loss Breadboar	d Measurer	nents	
LO (RF=-30dBm)	CL (dB)	RF (LO=11dBm)	CL (dB)	RF (LO=7dBm)	CL (db)
2	12.5	-10	8.15	-10	10
2.5	12	-8	8	-8	9.9
3	11.3	-6	8.1	-6	9.9
3.5	10.6	-4	8.04	-4	9.84
4	10	-2	8.02	-2	9.7
5	9.7	0	8.08	0	9.7
6	9.5	2	8.1	2	9.78
7	9	4	8.14	4	9.76
8	8.5	6	8.24	6	9.75
9	8.2	8	8.95	8	10.5
10	8	10	10.25	10	11.9
11	7.85	11	11.15	12	13.5
12	7.8			14	15.85
13	7.6				
14	7.4				
15	7.4				

Table E.2:	Measured	conversion	loss from	breadboard	prototype.
------------	----------	------------	-----------	------------	------------

	Con	version Loss PCB M	leasuremen	ts	
LO (RF=-30dBm)	CL (dB)	RF (LO=11dBm)	CL (dB)	RF (LO=7dBm)	CL (db)
2	11.5	-10	7.33	-10	8
2.5	10.7	-8	7.3	-8	7.95
3	10.2	-6	7.29	-6	7.98
3.5	9.8	-4	7.26	-4	7.9
4	9.4	-2	7.29	-2	7.9
5	8.8	0	7.29	0	7.92
6	8.4	2	7.42	2	8.05
7	8.1	4	7.43	4	8.19
8	7.8	6	7.63	6	8.6
9	7.6	8	8.09	8	9.45
10	7.5	10	9.35	10	10.93
11	7.3	11	10.09	12	12.6
12	7.2			14	14.4
13	7.15				
14	7.1				
15	7				

 Table E.3: Measured conversion loss from PCB.

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Appendix F Transistor Simulation models

This chapter contains the three transistor simulation models. The new transistor model using Zetex parameters, produced the most accurate simulations.

Chapter F. Transistor Simulation models

Name	Value	Unit	Tune	Opt	Limit	Upper	Description
M ID	2N2222A_GBJT1						Device ID
B IS	3.0611e-11	mA					Saturation current
B IBE		mA					Reverse BE saturation current
B IBC		mA					Reverse BC saturation current
B BF	220						Fwd current gain
BINE	1.00124						Fwd ideality factor
B VAF	104	V					Fwd Early voltage
B IKF	520	mA					Fwd current knee
R ISE	7.5e-12	mA					BE leakage current param
B NE	1.41						BE leakage ideality factor
BR	4						Rev current gain
BINR	1.005						Rev ideality factor
VAR	28	V	Ē	Π	Ē		Rev Early voltage
IKR IKR	240	mA	Π	Ē			Rev current knee
E ISC	1.06525e-8	mA		Ē			BC leakage current param
BINC	1.3728		Ē	Ē	Ē		BC leakage ideality factor
E RB	0.13	Ohm	_	Ē.			Base resistance
IRB IRB	1e18	mA	Ē	Ē			Current where RB falls halfway to min
RBM	0.01	Ohm	Π	Ē.			Minimum high-current base resistance
RE	0.22	Ohm	Π.	Ë.	Ë.		Emitter resistance
RC	0.012	Ohm	Π.	Ë.	Ē.		Collector resistance
	27.01	pF	Ξ.	Ë.	Ë.		CJ0 for BE junction
	0.75	V	Π.	Ë.	Ë.		BE built-in potential
BIMJE	0.33		Ξ.	Ξ.	Π		BE grading coefficient
E TF	0.000325	us	Π.	Ξ.	Ē		Fwd transit time
E XTF	0	45		Ë.	Ë.		Coef for bias dependence of TF
	0	V	Ξ.	Ξ.	Ξ.		Voltage for VBC dependence of TF
BITF	0	mA	Ē	Ē	Ē		High-current parameter for TF
E PTF	0		Ξ.	ñ.	Ē.		Excess phase param; must be degrees
BCC	9.12	pF	Ξ.	Ë.	Ē		CJ0 for BC junction
E VJC	0.4089	V	Ē	Ë.	Ē		BC built-in potential
ВМЈС	0.3508			Ë.			BC grading coefficient
	1		Ē	Ë.	Ē		Fraction of CBC to internal node
	0.1	us		Ë.			Rev transit time
	0.1	pF	Ē	Ë.			CJ0 for substrate capacitance
	0.75	V		Ë.			Built-in potential for substrate cap
E MJS	0.33	v	H	Ë.	H		
E XTB	0.33		H	H	Ë.		Substrate cap grading coeff Temperature scaling term for beta
E EG	1.11		H	Ë.	H		
			H	H	H		Energy gap at T=TNOM
	3						Temperature scaling term
BKF	1e-14		N		-	1	Flicker noise coefficient
AF	2						Flicker noise exponent
E FFE	1				-		Flicker noise frequency exponent
FC	0.5						Coefficient for forward-bias depletion
B NKF	0.5						Exponent for high-current Beta roll-off
E TNOM	27	DegC		<u> </u>			Nominal temperature (parameter extraction)
TEMP	27	DegC		<u> </u>			Simulation temperature
R KB	0		<u> </u>	<u> </u>	<u> </u>		Burst noise coefficient
B AB	1		<u> </u>	<u> </u>	<u> </u>		Burst noise exponent
E FB	1						Burst noise cutoff frequency

Figure F.1: New hybrid transistor model.

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DIM TEMP C FREQ HZ RES OH COND /OH IND H CAP F LNG M TIME SEC ANG DEG VOL V CUR A PWR DBM CKT GBJT 1 2 3 4 IS=3.0611e-014 NF=1.00124 BF=220 IKF=0.52 VAF=104 ISE=7.5e-015 NE=1.41 NR=1.005 BR=4 IKR=0.24 VAR=28 ISC=1.06525e-011 & NC=1.3728 RB=0.13 RE=0.22 RC=0.12 CJC=9.12e-012 & MJC=0.3508 VJC=0.4089 CJE=2.701e-011 TF=3.25e-010 & TR=1e-007 IRB=1e+015 MJE=0.33 MJS=0.33 VJE=0.75 & VJS=0.75 VTF=0 ID="2N2222A" DEF4P 2 1 3 4 "2N2222A" ! NOTE: This file was translated from a SPICE file. 1 ! SPICE orders the nodes of active devices as Drain Gate Source. ! The AWR convention is Gate Drain Source. The translator has reordered ! the nodes for active device elements (B, J, M and Q). The user should ! verify the node order for subcircuits representing active devices. ! Polynomial controlled sources have been decomposed to linear devices ! when possible. The user should verify the use of these devices. ! ZETEX 2N2222A Spice model Last revision 9/12/92 ! 1 (C) 1992 ZETEX PLC 1 ! The copyright in this model and the design embodied belong to Zetex PLC ("Zetex"). It is supplied free of charge by Zetex for 1 1 the purpose of research and design and may be used or copied intact (including this notice) for that purpose only. All other rights are reserved. The model is believed accurate but no ! 1 condition or warranty as to its merchantability or fitness for ! purpose is given and no liability in respect of any use is 1 1 accepted by Zetex PLC, its distributors or agents. 1 Figure F.2: Zetex SPICE model.

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                                     Chapter F. Transistor Simulation models
DIM
   TEMP
        C
   FREQ HZ
   RES OH
   COND
        /OH
    IND H
    CAP F
   LNG M
   TIME SEC
    ANG DEG
    VOL
        v
    CUR
        A
    PWR DBM
CKT
GBJT 1 2 3 4 IS=3.88184e-014 BF=929.846 NF=1.10496 VAF=16.5003 IKF=0.019539 &
    ISE=1.0168e-011 NE=1.94752 BR=48.4545 NR=1.07004 &
    VAR=40.538 IKR=0.19539 ISC=1.0168e-011 NC=4 RB=0.1 &
    IRB=0.1 RBM=0.1 RE=0.0001 RC=0.426673 XTB=0.1 &
    XTI=1 EG=1.05 CJE=2.23677e-011 VJE=0.582701 MJE=0.63466 &
    TF=4.06711e-010 XTF=3.92912 VTF=17712.6 ITF=0.4334 &
    CJC=2.23943e-011 VJC=0.576146 MJC=0.632796 XCJC=1 &
    FC=0.170253 CJS=0 VJS=0.75 MJS=0.5 TR=1e-007 &
    PTF=0 KF=0 AF=1 ID="Q2n2222a"
DEF4P 2 1 3 4 "Q2n2222a"
! NOTE: This file was translated from a SPICE file.
! SPICE orders the nodes of active devices as Drain Gate Source.
! The AWR convention is Gate Drain Source. The translator has reordered
1
 the nodes for active device elements (B, J, M and Q). The user should
! verify the node order for subcircuits representing active devices.
1
1
  Polynomial controlled sources have been decomposed to linear devices
! when possible. The user should verify the use of these devices.
1
1
      Model Generated by MODPEX
! Copyright(c) Symmetry Design Systems*
!
         All Rights Reserved
    UNPUBLISHED LICENSED SOFTWARE
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1
    Contains Proprietary Information *
      Which is The Property of
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1
      SYMMETRY OR ITS LICENSORS
! Commercial Use or Resale Restricted *
1
   by Symmetry License Agreement
 ******
!
! Model generated on Feb 28, 13
! MODEL FORMAT: PSpice
```

Figure F.3: Symmetry PSPICE model

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