AN RF FRONT-END SYSTEM COMPARISON OF SiGe HBT AND GaAs pHEMT : LIMITATIONS IN NON-LINEARITY AND BALANCE

By

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Statement of Originality

Except where acknowledged in the customary manner, the material presented in this thesis is, to the best of my knowledge, original and has not been submitted in whole or part for a degree in any university.

Sudipta Chakraborty 25. 7. 2017

To my parents

Acknowledgements

We all know that "time flies", and gradually the clock is ticking towards the end of the three years of my PhD tenure. The time has come to thank all the people who have helped me to reach this point.

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List of Publications

Articles

- S. Chakraborty, L. E. Milner, X. Zhu, L. T. Hall, O. Sevimli and M. C. Heimlich *A K-band Frequency Doubler with 35-dB Fundamental Rejection Based on Novel Transformer Balun in 0.13 μm SiGe Technology.* IEEE Electron Device Letters **37**, 1375-1378 (2016)

Conferences

- S. Chakraborty, L. E. Milner, L. T. Hall, X. Zhu, O. Sevimli and M. C. Heimlich *Characterisation of a Transformer Balun for a 7-15 GHz SiGe Frequency Doubler.* (Australian Microwave Symposium (AMS 2016), Adelaide, Australia)

- S. Chakraborty, L. E. Milner, L. T. Hall, Anthony E. Parker and M. C. Heimlich *A 30-60 GHz SiGe Transformer Balun with Offset Radii Coils for Low Amplitude and Phase Imbalance.* (International Microwave Symposium, (IMS 2017), (accepted))

- S. Chakraborty, Xi Zhu, Oya Sevimli and Michael Heimlich *A wideband Transformer-coupled Frequency Quadrupler Using an Asymmetrical Balun in 0.25 μm SiGe for Backhaul Communication.* (IEEE International Symposium on Circuits and Systems (ISCAS 2015), Lisbon, Portugal)

Others

- S. Chakraborty, B. Majumdar, M. Heimlich and K. P. Esselle *A Simple Reconfigurable BiCMOS Active Inductor and Its Implementation in A Phase-Shifter Unit Cell.* (2015 International Symposium on Antennas and Propagation (ISAP), Hobart, Tasmania, Australia)

- S. Chakraborty, B. Majumdar, M. Heimlich and K. P. Esselle *SiGe HBT Based Impedance Switch for On-Chip Antenna Reconfigurability.* (2015 Australian Symposium on Antennas, Sydney, New South Wales, Australia)

- B. Majumdar, D. Baer, S. Chakraborty, K. P. Esselle and M. Heimlich *A 3D Printed Dual-Ridged Horn Antenna.* (2016 International Conference on Electromagnetics in Advanced Applications (ICEAA / IEEE AWPC), Cairns, Queensland, Australia)

- B. Majumdar, D. Baer, S. Chakraborty, K. P. Esselle and M. Heimlich *Additive Manufacturing of a Dual-Ridged Horn Antenna.* Progress in Electromagnetics Research Letters **59**, 109-114 (2016)

- B. Majumdar, D. Baer, S. Chakraborty, K. P. Esselle and M. Heimlich *Advantages and limitations of 3D printing a dual-ridged horn antenna.* Microwave and Optical Technology Letters **58**, 2110-2117 (2016)

Abstract

For a successful system design of a wireless transmitter or receiver, it is important to investigate the overall linearity of a particular manufacturing process, where the limit of linearity can be viewed both as the onset of non-linearity above some threshold as well as loss of phase and amplitude balance. This dissertation presents a balanced frequency-doubler circuit as an archetype of a non-linear circuit that would allow the study of harmonics. The source of non-idealities in a frequency doubler is studied that would limit the overall linearity of a system design. In this context, a balun is used as an archetype of the passive structures that complements a frequency doubler when the linearity of a system is considered. For microwave and millimetre-wave circuit design, GaAs processing is well established but it involves high cost. SiGe processing is emerging in the microwave and millimetre-wave arena, promising reasonable performance at a lower cost and equipped with integrated digital logic capability. To compare the two process technologies, GaAs and SiGe, similar frequency-doubler circuits and passive baluns are implemented in both the processes using GaAs pHEMTs and SiGe HBTs. The design challenges, issues with layout and design flows developed for each of the processes are discussed. Analysis of harmonics in frequency doublers using GaAs pHEMTs and SiGe HBTs shows that pHEMTs are inherently more linear than HBTs. Large input power is needed to drive the frequency doubler using pHEMTs compared to SiGe HBTs. However, the area requirement of the GaAs frequency doubler is more than the SiGe counterpart. Measurement results demonstrate that high linearity (> 35 dB odd-harmonic suppression) and balance (< 0.15 dB amplitude imbalance and $< 2^o$

phase imbalance) is possible from both technologies over comparable bandwidths.

List of Abbreviations

AlGaAs	Aluminium Gallium Arsenide
AMS	Analogue and Mixed Signal
AWR	Applied Wave Research
BEOL	Back-end Offline
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BV_{CEO}	Collector emitter breakdown voltage
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibels
dBm	Decibels referred to 1 milliwatt
DRC	Design Rule Check
EM	Electro Magnetic
ESD	Electro-Static Discharge
f_{max}	Maximum frequency of oscillation
f_T	Transit frequency
GaAs	Gallium Arsenide

HBT Heterojunction Bipolar Transistor

HV−HBT High Voltage Heterojunction Bipolar Transistor

HS−HBT High Speed Heterojunction Bipolar Transistor

ITRS International Technology Roadmap for Semiconductors

LO Local Oscillator

LVS Layout Versus Schematic

MBE Molecular Beam Epitaxy

MIM Metal Insulator Metal

MMIC Monolithic Microwave Integrated Circuit

MWO Microwave Office

P−cells Parameterised cells

PDK Process Design Kit

pHEMT Pseudomorphic High Electron Mobility Transistor

PLL Phase Locked Loop

RF Radio Frequency

SiGe Silicon Germanium

SiN Silicon Nitride

SOLT Short Open Load Through

SPP Shape Pre-Processing rules

TFR Thin-film Resistor

TM1 Thick Metal 1

TM2 Thick Metal 2

UGW Unit Gate Width

VCO Voltage Controlled Oscillator

VLSI Very-Large-Scale Integration

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Introduction

Since the invention of bipolar junction transistors in 1947 by John Bardeen, Walter Brattain and William Shockley (Fig. 1.1), semiconductor electronics has evolved at a rapid pace. The device dimensions have been reduced, enabling integration of a large number of transistors on a single silicon chip, paving the way for silicon VLSI (very-large-scale integration). Besides silicon VLSI, RF electronics emerged as the other prominent field of electronics in the 1980s [1]. The introduction of mobile phones and the development of wireless communication systems created a large impact on human society. RF transistors, which have become steadily faster, form the backbone of modern communication systems. Fig. 1.2 shows the evolution of RF transistors over the years [1].

The first real mass market for RF semiconductors was created with the advent of

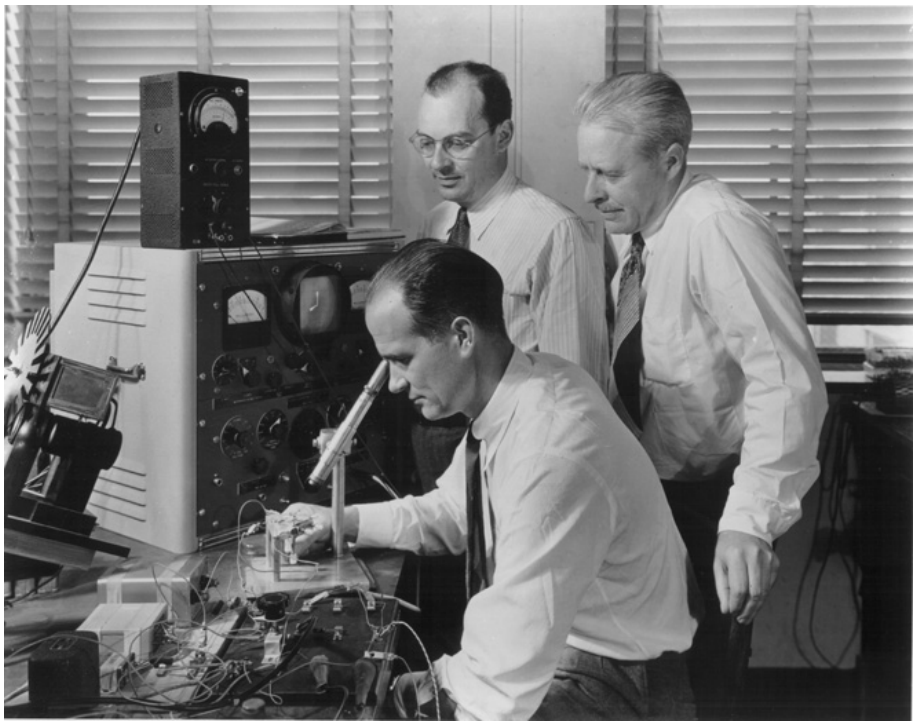


FIGURE 1.1: Inventors of transistors at Bell Laboratories 1947 [AT&T archive].

mobile phones. Since then the RF semiconductor industry has ridden a wave of evolution which has made it possible to realise today's transistors that can operate in the microwave and millimetre-wave and even the terahertz range [2]. The development of high-frequency transistors can be attributed, not only to transistors of smaller dimensions, but also to the exploration of a wide variety of semiconductor materials (Silicon (Si), Silicon Germanium (SiGe), Gallium Arsenide (GaAs), Indium Phosphide (InP) etc.) and different types of transistors (Bipolar junction transistors (BJTs), Heterojunction bipolar transistors (HBTs), Metal-oxide-semiconductor field-effect transistors (MOSFETs), Metal-semiconductor field-effect transistors (MESFETs), High-electron-mobility transistors (HEMTs) etc.).

1.1 Status of semiconductor market

GaAs technology has been paramount in providing high-frequency performance, with high reliability at a reasonable cost for high-volume applications. With the advent

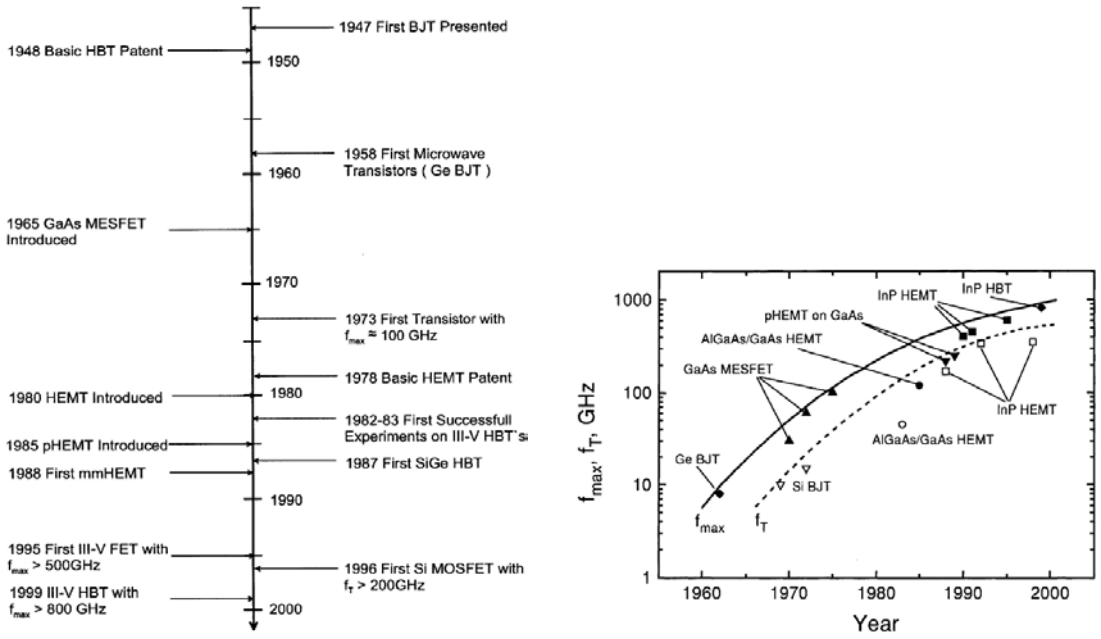


Figure 1.2: (a) History of development of RF transistors, (b) Plot of f_T and f_{max} of RF transistors over the years 1960 to 2000.

of the IoT (Internet of Things) and 5G systems, the semiconductor industry will be revolutionised. According to the latest Strategy Analytics forecast, more than 33 billion devices are expected to be connected to the Internet by 2020 [3].

The system complexity of communication systems is likely to continue to increase by orders of magnitude to provide increased user data rates and capacity. Due to these requirements, other technologies are in the process of capturing market share from GaAs. One such example is the mobile handset switch in which Silicon-on-Insulator (SoI) technology has replaced GaAs devices [3]. Silicon can provide high-volume digital, analogue and mixed-signal (AMS) integration, with low power and low cost. SiGe BiCMOS (Bipolar Complementary Metal Oxide Semiconductor) technologies equipped with high-speed HBTs and CMOS (Complementary Metal Oxide Semiconductor) with high integration capability will continue to grow in the field of microwave and millimetre-wave applications and pose a threat to at least some, if not all, GaAs-based applications.

1.2 GaAs and silicon technologies

The high-frequency performance of different devices is continually improving as advances in device technologies are made. It is also implied by the increase in cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) (details in Section 1.2.3) for different devices over the years. As the semiconductor industry offers various transistors in different materials with a variety of capabilities, the selection of a particular technology is made more difficult for the circuit designer. A complex system, like a typical transceiver for wireless communication system, consists of different building blocks such as amplifiers, mixers, oscillators, filters, switches, modulators and demodulators. A simplified block diagram of a wireless transceiver is shown in Fig. 1.3. Each of these building blocks has different requirements.

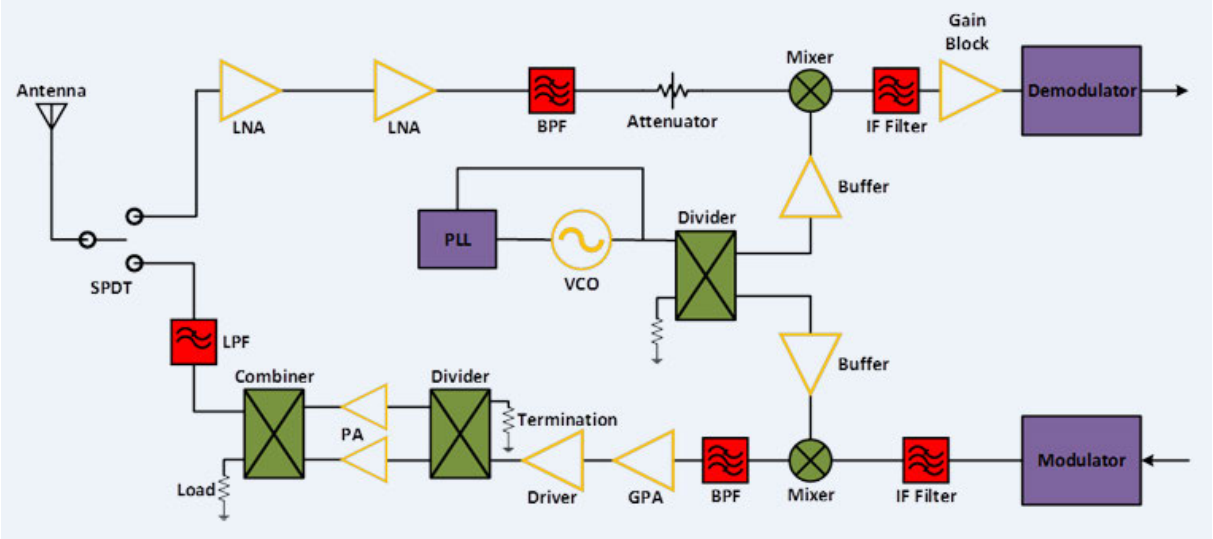


FIGURE 1.3: Simplified block diagram of a wireless communication transceiver.

In general for microwave and millimetre-wave designs, devices with higher f_T and f_{max} are necessary, but the choice of a particular device is not only limited to its higher f_T and f_{max}. For a specific application, many key parameters such as frequency of operation, linearity, current density, output power, supply voltage, gain, noise figure, power consumption play an important role. The level of integration supported by a particular process and the cost of manufacturing are also deciding factors for a

particular application.

A particular process is often selected based on the f_T and f_{max} of the devices, which decide the high-frequency performance of the circuit. In a complex system-level design such as a wireless transmitter or receiver, the overall linearity of the system is affected by the non-idealities from the active circuits. In other words, it is important to assess the overall linearity that could be achieved from a particular process. In this dissertation, it is proposed that the behaviour of a non-linear circuit can be studied and the non-idealities in a non-linear circuit can be investigated that limit the overall performance of a system.

Therefore, the status of the devices in different processes for microwave and millimetre-wave applications are reviewed.

1.2.1 Overview

The increasing demand for wireless communication systems has pushed research to higher frequencies, towards millimetre-wave applications. Traditional Monolithic Microwave Integrated Circuits (MMICs) using GaAs technology have been the stalwart of the microwave industry over the last three decades. Group III/V technologies, such as GaAs, have outstanding properties, both a low-loss (passive) substrate and a high-frequency (active) transistor technology. They offer high electron mobility and a high band gap, and fabrication of complex layer structures by epitaxial growth to support millimetre-wave circuits [4]. Due to the high band gap, the breakdown voltage is higher. But GaAs material is expensive and fragile, and the fabrication process is less repeatable. GaAs wafer breakage rates of as high as 18% were common previously, due to the brittleness of wafers [5]. Microcracks on the backside of the wafer and chips around the edges of the wafer caused a significant drop in the wafer strength. Micro-scratches caused unintentionally, and edge chips (caused due to collisions of wafers with metal cassettes and quartz boats, alignment pins on equipment or accidental handling errors) lead to wafer breakage, thereby reducing the yield [5]. Some improvements have been made recently by some companies [5] but they are still limited to a small wafer size.

On the other hand, silicon is known to be a robust material [4] that is widely

TABLE 1.1: Summary of key physical properties of silicon and GaAs

Property	**Si**	**GaAs**
Energy gap (eV)	1.12	1.424
Dielectric constant	11.9	13.1
Electric breakdown field (kV/cm)	300	400
Electron drift mobility ($cm^2/V-s$)	1500	8500
Intrinsic carrier concentration (cm^{-3})	1.45×10^{10}	1.79×10^6
Thermal conductivity (W/cm−K)	1.5	0.46

available and inexpensive. The thermal conductivity of silicon is three times as high as for GaAs, which is advantageous for power-dissipating devices [6]. The abundance of silicon and its inherent mechanical strength allow the growth of large defect-free wafers. This facilitates a tightly-controlled fabrication process compared to GaAs [7–9]. The silicon-based devices are also suitable for digital applications. Therefore, digital and analogue circuits can be integrated on the same silicon wafer, which facilitates a complete system solution.

But silicon-based RF and microwave integrated circuits are typically associated with a higher loss for passive designs and lower-frequency operation for active circuits. As the electron mobility in silicon is approximately one-fifth the electron mobility in GaAs [6], silicon-based devices are more limited in high-frequency operation. However, the speed of silicon-based devices can be improved by shrinking the size of the transistors, as this reduces the transit time of the electrons. This comes with a price, namely short-channel effects, as the devices are decreased in length. If the channel length of the device is decreased, it causes collisions among the carriers and reduces the velocity of the carriers, which gives rise to a saturation velocity. The lower electron mobility of silicon restricts the use of silicon-based devices for high-frequency applications. The less reliable and expensive group III-V processes, such as GaAs, became the natural choice of option for high-frequency high-performance applications. Therefore, there is a desire to improve the performance of silicon-based devices to achieve comparable performance to their GaAs counterparts, while maintaining the benefits of high yield and low cost of manufacturing. Some of the key physical properties of silicon and GaAs are listed in Table 1.1.

SiGe takes advantage of the silicon wafers while enabling the benefits of a heterojunction (details in Section 1.2.2). Recent advancements in SiGe processes have made it possible to design circuits at RF and microwave frequencies with relatively good performance, at a lower cost than with GaAs. Moreover, for millimetre-wave and sub-millimetre-wave applications, it is beneficial to integrate the passive and active circuits on the same substrate, to provide a System-on-chip solution which could be implemented in SiGe technology [10]. Also, digital and analogue circuits can be integrated on the same die, as they follow the same manufacturing process as silicon-based devices. The SiGe process has the potential to incorporate the benefits of silicon device technology, such as high yield and low fabrication cost, into the high-frequency world [10].

1.2.2 Development of heterostructures

Although the speed of transistors can be and has been improved by shrinking the device dimensions (gate length in FETs and base width in BJTs) for RF applications, implementation of heterostructures or "bandgap engineering" after 1980 pushed the limit of high-frequency operation [1]. The realisation of HBTs and HEMTs played a significant role in improving the high-frequency performance of high-speed devices.

A heterostructure consists of at least two different semiconductor materials with different bandgaps, grown epitaxially one on top of the other. The concept of the heterostructure is used in an HBT. The important part in the HBT is the emitter-base heterojunction. Typically, the bandgap of the emitter is larger than that of the base [1]. Due to the difference in the bandgap, the electrons travelling from the emitter to the base encounter a small energy barrier. In a SiGe HBT, germanium is selectively doped into the base of the silicon bipolar transistor. A graded germanium doping profile can be used in the base for bandgap engineering. This results in an accelerating field, thereby reducing the base transit time, which also helps to increase the transit frequency. The concept of an HBT is not new; it was conceived by Shockley in 1948 [11]. Later, in 1957, Kroemer formulated an HBT theory [12]. At that time the state of development of fabricating high-quality heterostructures posed a hindrance to realising

successful HBTs. Hence HBTs could not be fabricated until the 1980s, with the advent of molecular-beam epitaxy (MBE) [13].

The FET version of a heterostructure device is the HEMT. An HEMT can be constructed, for example, by exploiting an AlGaAs-GaAs heterostructure. As the bandgap energy for $Al_xGa_{1-x}As$ is larger than for GaAs, the energy level of the conduction band E_C of $Al_xGa_{1-x}As$ is higher than that of GaAs. Therefore the electrons flow from the E_C of $Al_xGa_{1-x}As$ to the E_C of GaAs by diffusion. These electrons are trapped at the heterointerface of AlGaAs-GaAs. A triangular potential well (quantum well) is formed on the undoped GaAs buffer layer. A two-dimensional electron-gas (2-DEG) sheet charge is developed on the undoped GaAs layer at the AlGaAs-GaAs interface, which creates a conducting channel for the HEMT devices. In the late 1970s at Bell Laboratories, intensive research was carried out to characterise a sequence of thin layers of GaAs and AlGaAs layers, called superlattices [1]. As this heterostructure showed higher mobility than bulk GaAs or AlGaAs, different research groups worked to utilise GaAs-AlGaAs heterostructures with enhanced mobilities, to develop faster FETs. The first device of this kind, known as an HEMT, was reported by Takashi Mimura from Fujitsu [14]. Later a pseudomorphic HEMT (pHEMT) on a GaAs substrate was developed using an AlGaAs/InGaAs/GaAs heterostructure [15].

1.2.3 Transit frequency and maximum frequency of oscillation

The high-frequency performance of transistors can be assessed by two important parameters which act as rough figures of merit for high-frequency circuit and system applications: cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) [7].

The frequency, f_T, at which the current gain drops to unity is called the cut-off frequency, making the device ineffective at higher frequencies than f_T [16]. f_T can be defined for BJTs and HBTs by the following equation [7, 17, 18]

$$f_T = \frac{1}{2\pi}\left[\frac{1}{g_m}\left(C_{EB} + C_{CB}\right) + \tau_B + \tau_C + \tau_E\right]^{-1} \tag{1.1}$$

where, g_m is the transconductance, C_{EB} and C_{CB} are the emitter-to-base and collector-to-base capacitances respectively, τ_B, τ_C and τ_E are the transit times in the base, collector and emitter respectively.

The maximum oscillation frequency f_{max} is the frequency at which the power gain of the transistor drops to unity. It can be defined for BJTs and HBTs by [7, 17, 18]

$$f_{max} = \sqrt{\frac{f_T}{8\pi \left(C_{CB} R_B\right)}} \tag{1.2}$$

Similar formulations for f_T and f_{max} can be derived for FET structures by appropriate substitution of drain, gate, source for collector, base and emitter respectively, as follows [19]:

$$f_T = \frac{1}{2\pi} \left[\frac{1}{g_m} \left(C_{gs} + C_{gd}\right) + C_{gd} \left(R_S + R_D\right) \right]^{-1} \tag{1.3}$$

$$f_{max} = \frac{1}{2} \frac{f_T}{\sqrt{2\pi f_T C_{gd} \left(R_g + R_S\right) + \frac{R_g + R_S}{r_o}}} \tag{1.4}$$

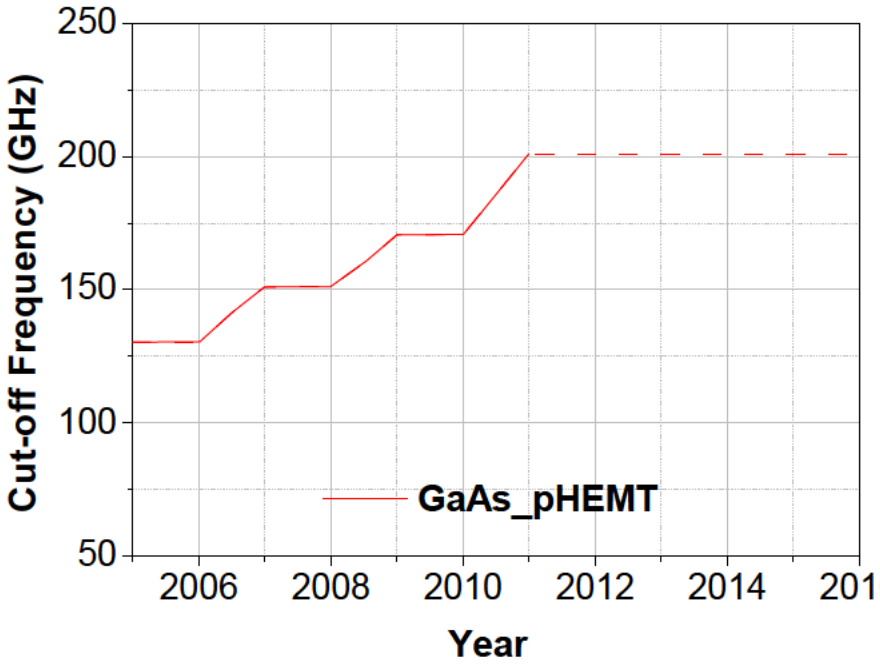
where, g_m is the transconductance, C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances respectively. R_S, R_D and R_g are the resistances in the source, drain and gate respectively.

1.2.4 Performance trend

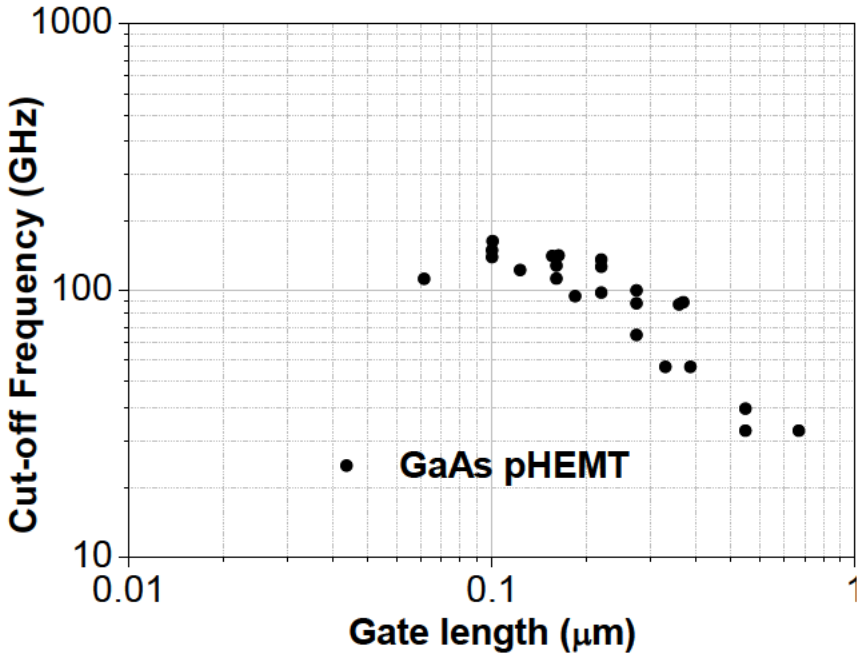
The performance trend of GaAs pHEMTs and SiGe HBTs over the years is discussed in this section.

GaAs pHEMT

The cut-off-frequency target for a GaAs pHEMT over time is plotted in Fig. 1.4(a) [20]. Significant increments in the cut-off frequency for a process occur in steps. For GaAs pHEMTs no significant improvement has been introduced in the last few years. For example in [21], a 0.1 μm GaAs pHEMT with more than 130 GHz f_T and 180 GHz



(a)



(b)

FIGURE 1.4: (a) ITRS f_T target for GaAs pHEMT. (b) Reported cut-off frequency (f_T) versus gate length for GaAs pHEMT.

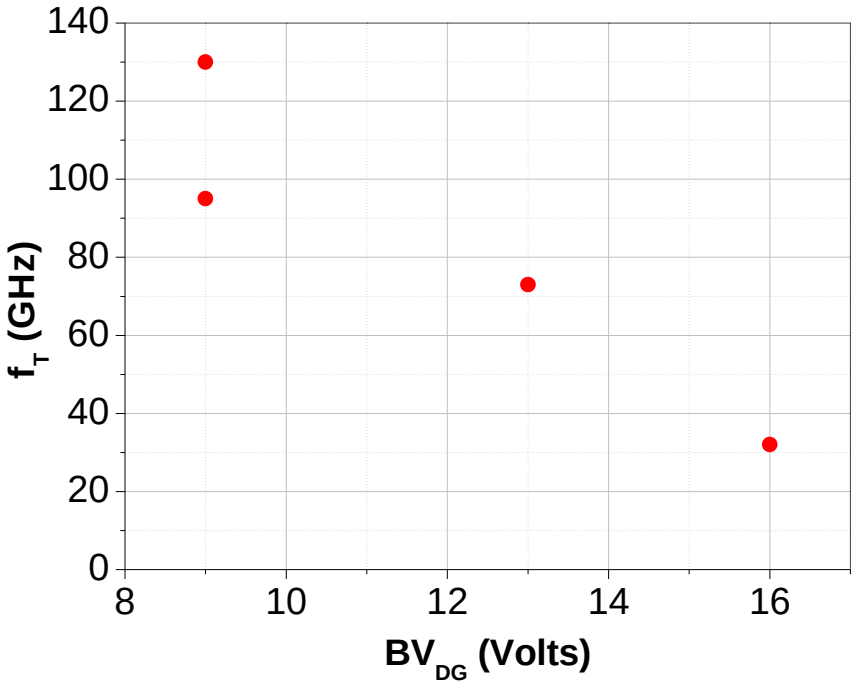


Figure 1.5: The plot of breakdown voltage vs f_T of GaAs pHEMTs available from WIN Semiconductors.

Table 1.2: Summary of pHEMT parameters from three different foundries

Parameter	**WIN Semi.** [25]	**Triquint** [26]	**Wavetek** [27]
Gate length (μm)	0.1	0.13	0.15
f_T (GHz)	130	110	100
f_{max} (GHz)	180	>200	120
Peak transconductance (Gm_{peak}) (mS/mm)	725	750	900
Maximum drain current (ID_{max}) (mA/mm)	760	530	500
Breakdown voltage (V)	9	9	14

f_{max} is used for W-band low-noise amplifier design. So the cut-off frequency is shown by a dotted line after 2011. To estimate the device dimensions for the projected f_T, Fig. 1.4(b) shows the plot of f_T versus the gate length of a GaAs pHEMT [20]. Generally, with the increase in the cut-off frequency the breakdown voltage of the transistors decreases. The plot of the breakdown voltage versus f_T for the GaAs pHEMT from WIN Semiconductors is depicted in Fig. 1.5 [22–25]. The key parameters of the GaAs pHEMTs offered from three foundries are listed in Table 1.2.

SiGe HBT

In early 2000, SiGe HBTs achieved a record f_T and f_{max} of 156 GHz and 160 GHz respectively [28]. Since then, the performance of SiGe HBTs has significantly improved over the last decade-plus. The International Technology Roadmap for Semiconductors (ITRS) f_T and f_{max} targets for SiGe HBTs as reported in [20] are shown in Fig. 1.6 and Fig. 1.7.

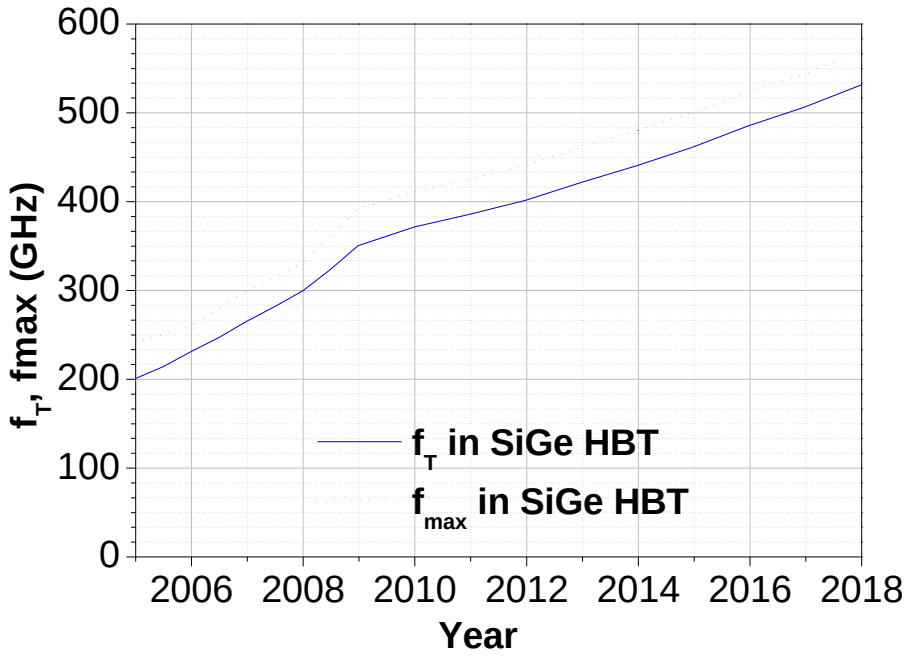


FIGURE 1.6: ITRS f_T and f_{max} targets for SiGe HBT.

Unlike III-V HBTs, one of the major problems with SiGe HBTs is the reduction of the breakdown voltage with an increase in cut-off frequency. The comparison of ITRS targets of f_T versus BV_{CEO} and experimental data for SiGe HBTs as presented in [20] are shown in Fig. 1.7.

The f_T and f_{max} of SiGe HBTs achieved in the European Dot Five project by different companies are listed in Table 1.3 [29]. The targeted f_{max} of 700 GHz is one of the main objectives in the European Dot Seven project, which is predicted to set a

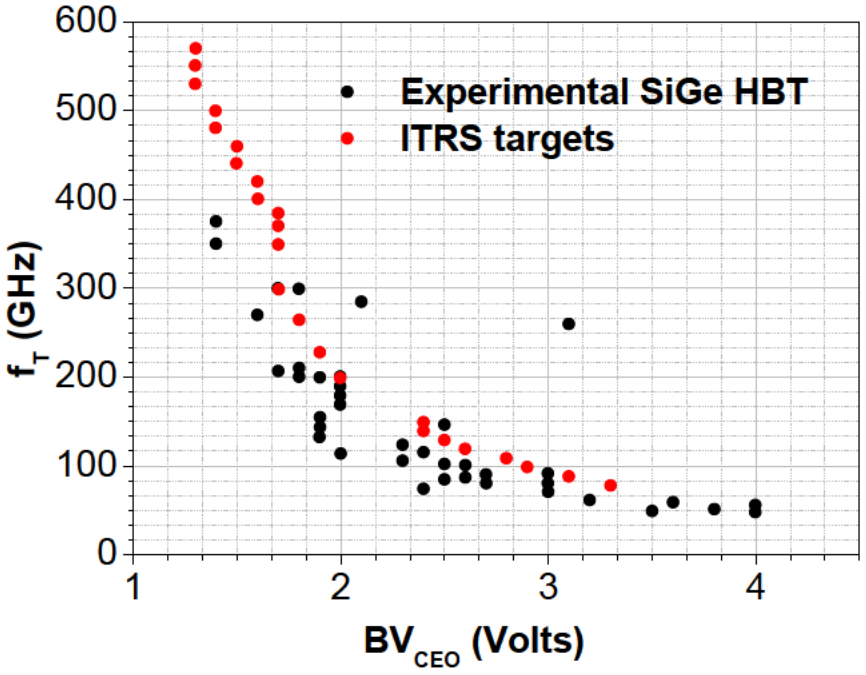


FIGURE 1.7: Reported cut-off frequency f_T as a function of the collector-emitter breakdown voltage BV_{CEO} and the ITRS targets for a SiGe HBT.

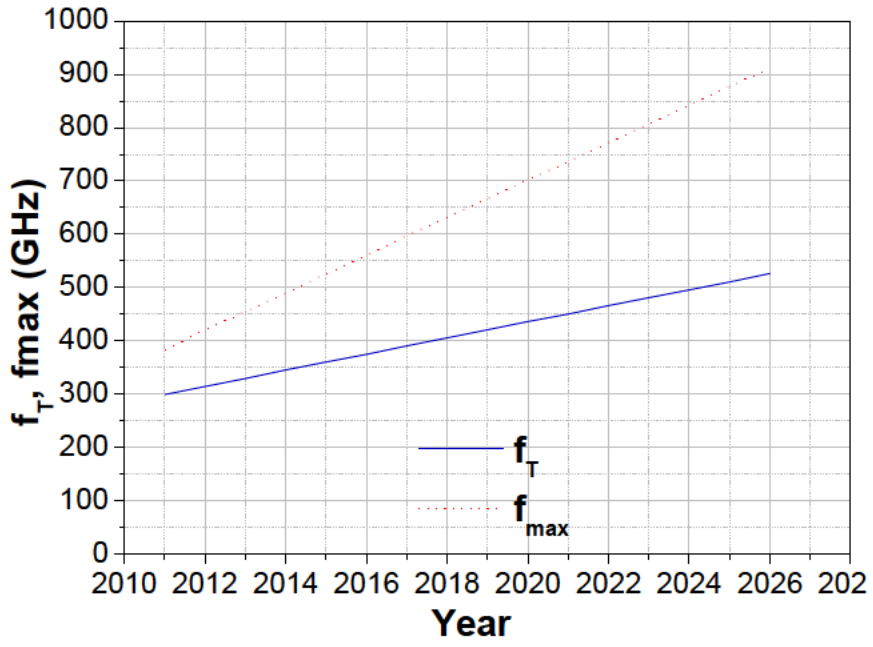


FIGURE 1.8: The f_T and f_{max} targets in the Dot Seven project for SiGe HBT.

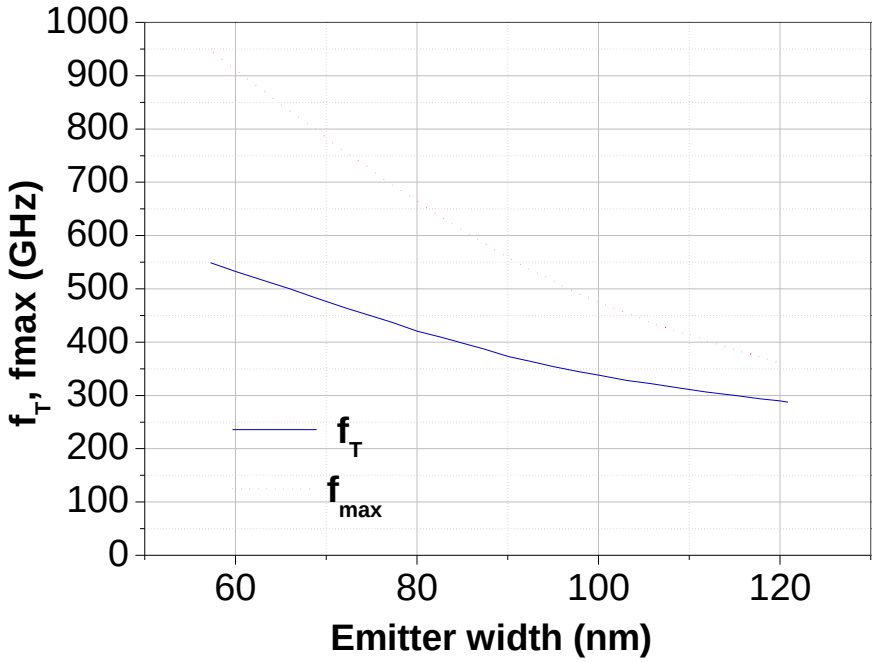


FIGURE 1.9: Estimated emitter width for projected f_T and f_{max} targets in the Dot Seven project for SiGe HBT.

TABLE 1.3: Summary of key physical properties of SiGe HBTs available from different companies in the European Dot Five project.

Parameter	**IHP**	**IMEC**	**ST**	**IFX**
Emitter width (nm)	120	75	100	130
f_T (GHz)	300	245	290	240
f_{max} (GHz)	500	460	430	380
BV_{CEO} (V)	1.6	1.7	1.5	1.5
t_{CML} (ps)	1.9	NA	1.9	2.4

new ITRS trend [29]. The projected f_T and f_{max} of SiGe HBTs in the European Dot Seven project are shown in Fig. 1.8 and the estimated emitter width corresponding to those f_T and f_{max} values is shown in Fig. 1.9 [29].

1.3 Aims

The aim of this dissertation is to compare the suitability of the two process technologies, SiGe HBTs and GaAs pHEMTs, for microwave and millimetre-wave designs. For

a circuit design at microwave and millimetre-wave frequencies such as a transceiver for a wireless communication system, the selection of the process technology is the most important decision. It is essential to put this aim of comparing the two process technologies in the context of a real-world functional system, to understand the performance that could be achieved and its related limitations, which would be relevant to IC designers. In the context of radio communication systems, Quadrature Amplitude Modulation (QAM) is used as the most desirable signal modulation technique. Higher order QAM systems have the capacity to carry more data in the same carrier signal which makes it the default choice of option but it has some limitations. A particular process technology influences the order of QAM system that could be realised. The two process technologies, SiGe HBTs and GaAs pHEMTs, can be compared along the lines of the limitation of higher order QAM system implementation which is described in Section 1.3.2.

1.3.1 Motivation for the performance comparison

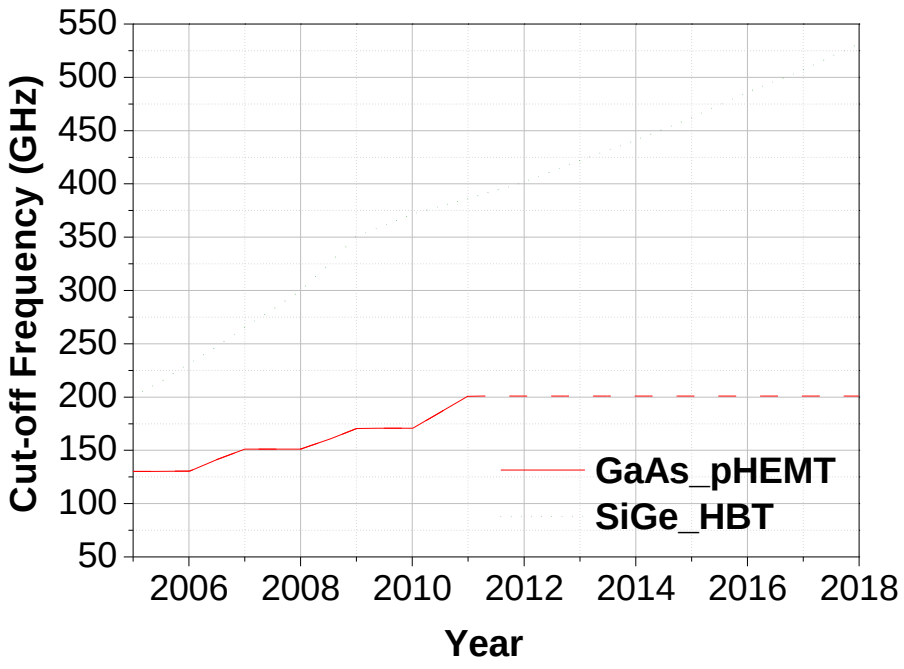


Figure 1.10: Comparison of cut-off frequencies of GaAs pHEMT and SiGe HBT up to 2018.

The comparison of the cut-off frequency of GaAs pHEMTs and SiGe HBTs, over the years, is shown in Fig. 1.10. Moreover, as can be seen from the graphs plotted in previous sections, GaAs pHEMTs and SiGe HBTs are constantly evolving. The key problem for the circuit designer is to select the appropriate technology based on the requirement of the circuit for microwave and millimetre-wave applications. The future technology roadmap suggests that these devices will be improved further over the years in terms of f_T and f_{max}.But the comparison of the two is not as simple as comparing f_T and f_{max}. It is quite important to estimate the "linearity" (to be defined and clarified below) that could be obtained in these technologies, in other words, the non-linearity of these technologies must be analysed.

Currently, silicon based technology is used if cost is the top priority of the designer while GaAs technology is used if the performance of the circuit is the main concern. But, if a circuit designer is given the task of designing a receiver or chip-set for a point-to-point radio, disregarding the area requirement, cost and production volume, it is important to figure out if SiGe technology can be superior to GaAs at the millimetre-wave frequency. One of the common question that is often asked in an industry perspective is, what is a good measure of what a technology can do or at which point a particular technology will fail in terms of performance. The key question in this context, is what level of QAM system can be supported by a particular technology. It is also aligned with our industry partner, MACOM (as a part of the ARC Linkage Project, LP130100734). This thesis topic was proposed by industry partner MACOM as part of this ARC Linkage Project and is directly derived from a question of profound industrial importance: at what point is the up-and-coming SiGe-based IC technology a viable replacement for the GaAs-based incumbent in MACOM's most advanced products. Fig. 1.10 would imply that SiGe should have replaced GaAs long ago, but, in fact, it has not because MACOM believes that it is not as "linear" as GaAs. Clearly, f_T and f_{max} alone do not determine the "best" technology.

1.3.2 QAM System

QAM is used for modulating data signals onto a carrier used for the radio communications; higher-order QAM systems mean more data for the same carrier bandwidth and so they are highly desirable. In a QAM system, the two carrier signals in phase quadrature (separated in phase by 90^o) are modulated and the resultant output signal consists of both amplitude and phase variations.

It offers several advantages over the other modulation techniques. For example, LTE through wireless systems including WiMAX, and Wi-Fi 802.11 use different forms of QAM, and the use of QAM is expected to increase in the field of radio communications systems.

QAM increases the efficiency of transmission in the radio communication systems by using both amplitude and phase variations but it is a complicated system. It is susceptible to noise as in a higher order QAM, the states are close together which require a low level noise to move the signal to a different decision point. Moreover, linearity must be maintained in a QAM as it contains an amplitude component.

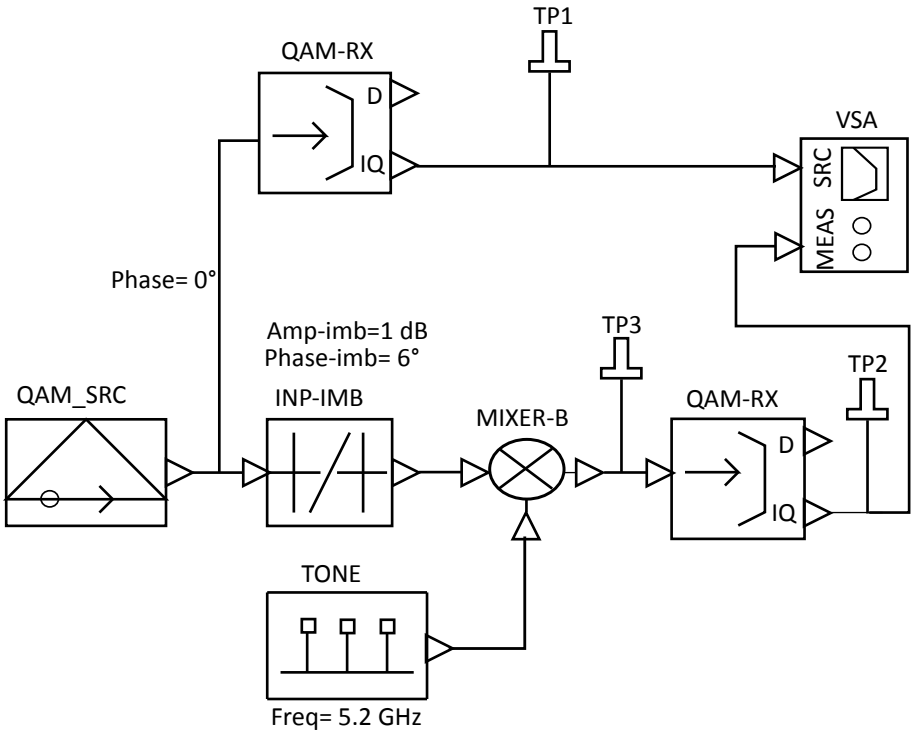


Figure 1.11: 16-QAM system set-up in AWR using the built-in System blocks.

Any analogue communication system is affected by in-phase to quadrature-phase (I-Q) imbalance which causes the signal to distort which particularly occurs in up-conversion and down-conversion. A 16-QAM system is set-up in AWR (Applied Wave Research) to demonstrate the effect of amplitude and phase imbalance in the system as shown in Fig. 1.11. Here, the input imbalance block (INP-IMBAL) creates an amplitude imbalance of 1 dB and a phase imbalance of 6^o. The constellation diagram shows that the output is skewed due to the amplitude and phase imbalance in the system as demonstrated in Fig. 1.12. The separation between blue and pink indicates a lack of linearity, in this case caused by phase/amplitude imbalance.

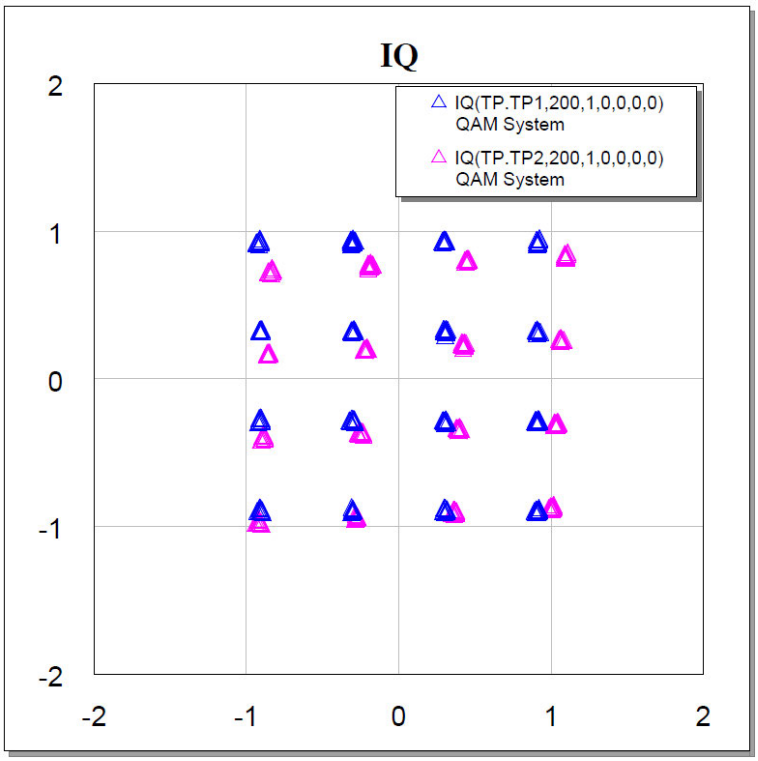


FIGURE 1.12: Constellation diagram for a 16-QAM system with (pink) and without (blue) amplitude and phase imbalance in the input signal.

Further, the effect of the harmonics on the QAM system can be demonstrated by adding the harmonics in the local oscillator signal as shown in Fig. 1.13. In this case, the fundamental signal is 5.2 GHz and the second and the third harmonic signals at 10.4 GHz and 15.6 GHz are added in the local oscillator. The resultant power spectrum

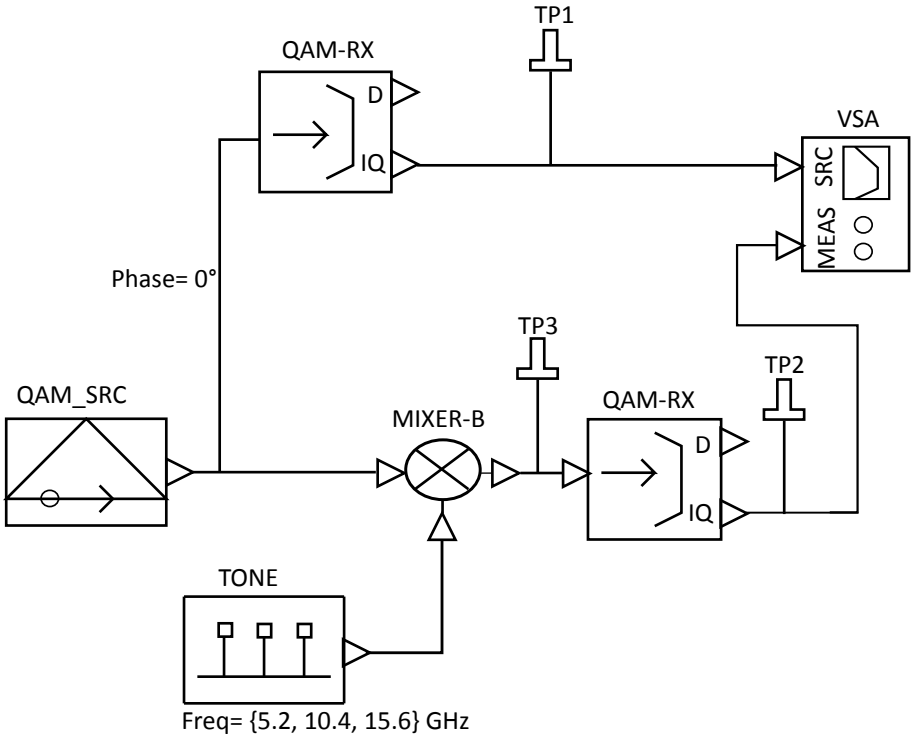


Figure 1.13: 16-QAM system set-up in AWR with harmonics in the local oscillator signal, using the built-in System blocks.

is shown in Fig. 1.14, which clearly shows that the signal is distorted.

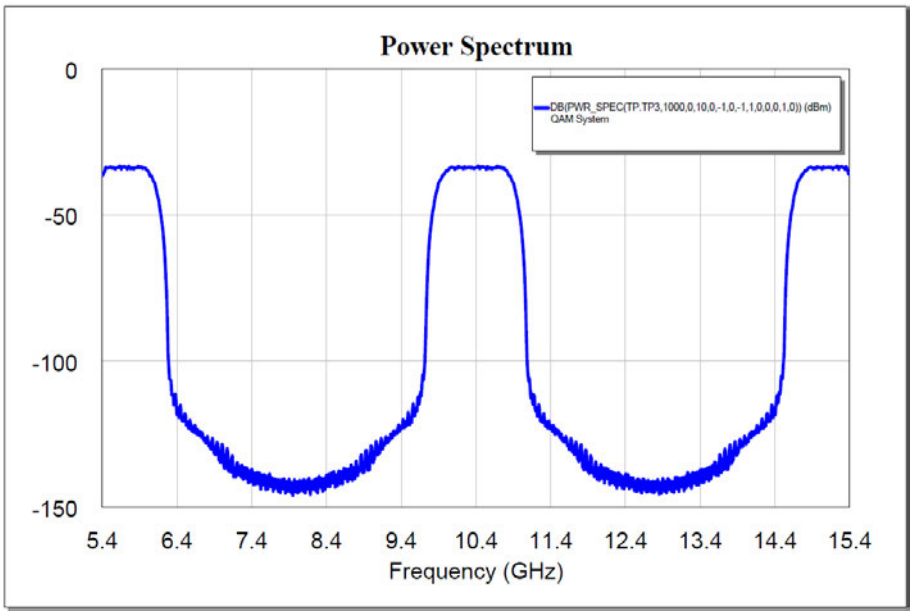


Figure 1.14: The power spectrum of the QAM system with harmonics (upto third order) in the local oscillator signal.

In a radio communication system, linearity is an important factor, which decides what level of QAM can be supported given the non-idealities (harmonic generation) in a particular technology. To answer this question, it is required to investigate systems that enable high harmonic rejection in active circuits and balance (amplitude and phase) in a passive circuit when used to drive a balanced active circuit.

1.3.3 Frequency multiplier as an archetype of non-linear circuit

Low-noise amplifiers can be designed to verify the suitability of the process. But the specifications for low-noise amplifiers are always over-estimated as they are typically designed for higher 1 dB compression points. The other way to look at this problem is to study the nonlinearity of a circuit. Oscillators are known for highly non-linear characteristics but it is difficult to monitor the behaviour of harmonics. The frequency multiplier is also a non-linear circuit, for which the harmonics can be studied. For the non-linear circuits, a frequency doubler can be used as the archetype. For microwave and millimetre-wave design, it is also essential to estimate the performance of the passive structures in the different processes. A passive balun is a suitable candidate as it deals with the balance of the differential signal, which could be significant for the performance of the next circuit block. Therefore a design of a frequency doubler and a passive balun implemented in two process technologies, IHP's 0.13 μm SiGe BiCMOS process (codenamed SG13S process) and WIN Semiconductor's 0.1 μm GaAs pHEMT process (codenamed PP10-10 process) are used to establish a methodology and to determine the linearity of each of these technologies.

1.3.4 Frequency bands of interest

With the growing demands of communication systems into remote areas, satellite technology is evolving rapidly. Although it is mainly used for radio communications, its applications are no longer so restricted. The available spectrum poses a major obstacle for satellite operators due to the increased congestion in the low-frequency bands.

Automatically there is a preference for the higher-frequency bands as they can provide high-bandwidth data throughput at lower cost, for example, Ka-band [30].

Similarly, wireless point-to-point links are growing and carry data by interconnecting cellular base stations or enterprise buildings [31]. According to [32], more than fifty percent of cellular base stations are interconnected by a wireless backhaul link, due to their low installation cost and high immunity to environmental effects. In order to cater to the demands of next-generation cellular networks, wireless point-to-point links will have to provide throughputs comparable to fibre-optic links. This is difficult to realise due to the limited available bandwidth in the microwave band [33]. Some opportunities have emerged with E-band, as multi-Gigabit per second (Gbps) wireless links could be developed [32, 34]. Apart from wireless communication systems, in the microwave and millimetre-wave range different applications are developing such as UWB imaging systems, anti-collision radar sensors [35, 36]. Due to the above-mentioned applications, a lot of research is carried out on K-Ka-band [37] and E-band transceivers [38–42].

As K-Ka band and E-band are identified as two important spectra for wireless communication systems, the frequency-multiplier circuits in the SG13S process and the PP10-10 process can be focused on one of these two frequency bands for the purpose of comparison. In this project, the designs are implemented in the K-Ka band, to consolidate the design flow and reliability of operation of circuits at a comparatively low frequency range. These designs can be explored further in the higher frequency range (E-band) to estimate the performance of the circuit at higher operating frequencies.

1.3.5 Objectives

A particular process technology cannot be selected based only on the f_T and f_{max} specifications. It is crucial to investigate the inherent linearity of the process, i.e. how non-linear is the device in that particular process.

As the research interest is shifted to higher and higher frequencies to cater to the ever-increasing demands of communication systems, the passive structures are integrated on-chip. Therefore, it is also important to estimate the performance of the passive components implemented in a particular process technology. The two process

technologies that are used for circuit design are IHP's 0.13 μm SiGe BiCMOS process (codenamed SG13S process) and 0.1 μm GaAs pHEMT process from WIN Semiconductors (codenamed PP10-10 process). Although SG13S is a BiCMOS process, only the HBTs are used for the circuit implementations. Therefore, SG13S SiGe HBTs are referred to henceforth in this dissertation wherever they are applicable. The aims of this project work are summarised in the following points:

Develop an analysis and understanding of:

1. Fundamental differences in the PP10-10 GaAs pHEMTs and the SG13S SiGe HBTs with respect to harmonic generation.

2. Non-linearity in the active circuits designed using SG13S SiGe HBTs and PP10-10 GaAs pHEMT devices. Establish the frequency doubler as an effective indicator of process linearity.

3. Effect of topology on the linear performance of a circuit.

4. Archetype passive structures (baluns) to serve a similar, but complementary, role to the frequency doubler when considering a process's linearity.

Implementation and testing of:

1. Implementation of frequency-doubler circuits in both the SG13S SiGe HBT and PP10-10 GaAs pHEMT processes.

2. Implementation of baluns in both the SG13S SiGe HBT and PP10-10 GaAs pHEMT processes.

3. Identify ways to minimise the non-ideality in frequency-doubler circuit and balun implementation.

4. Testing of the implemented circuits and analysis of the measured results. Help circuit designers to decide on the choice of process for their application.

1.4 Scope

The semiconductor industry offers a number of options to circuit designers in terms of the different devices available in different process technologies with a wide variety of capabilities. High performance and low cost are the two main driving factors for circuit designers. At microwave and millimetre-wave frequencies, GaAs has exercised its monopoly over the silicon-based technologies for higher performance (for example in terms of power) over the last few decades. But silicon is known for its device density and low-cost volume production. In a nutshell, a silicon-based process is chosen where cost is the supreme driver whereas GaAs is chosen for higher performance but involves high cost.

With the advances in silicon-based devices, the future of the silicon-based process looks promising. The key question for the circuit designer is to select the appropriate technology that will satisfy performance while balancing development cost versus production volume. This project work compares the inherent linearity of two process technologies: SiGe and GaAs. In order to compare the active circuits, a frequency-doubler circuit is considered as an archetype to study the harmonics. Analysis of the harmonics for a frequency doubler is demonstrated and helps to select the topology of the frequency doubler also. The accurate modelling of the transistors is out of the scope of this project work.

To compare the performance of the passive structures in the two processes, a passive balun design is explored. The cause of the imbalance in the differential signal is investigated due to its contribution to the non-linearity of balanced circuits. In both processes, novel methods are adopted to improve the balance compared to state-of-the-art designs. Simple coupled-line models of the baluns are analysed. The complete modelling of the balun that could predict the magnitude and the phase imbalance is out of the scope of this work. However, the parameters affecting the magnitude and phase imbalance are identified and verified by the simulation.

The design flows for the two processes SG13S and PP10-10 are described. The importance of the symmetry in layout for these designs is explained in detail. The

electromagnetic structures used for the estimation of the performances of the circuits are also shown. Finally, the results from a comparative study on the design in the SiGe and GaAs processes are summarised.

This thesis became of interest to DSTG Adelaide and MACOM Technology Solutions, North Sydney Design Centre. Leigh E. Milner from DSTG provided design consultation and PDK training. MACOM Technology Solutions, North Sydney Design Centre provided access to their laboratory facilities. Gerry McCoulloch, Melissa Rodriguez and Jim Harvey deserve special mention for guidance with measurement, tape-out and design review respectively.

1.5 Synopsis

The dissertation is divided over eight chapters. **Chapter 1** presents a general overview of the semiconductor market and the performance trends of SiGe HBTs and GaAs pHEMTs. It points out the necessity for a performance comparison of active and passive circuits in both processes. It also describes the aims and scope of the dissertation and outlines the thesis structure.

Chapter 2 presents the background and a literature review of the frequency-doubler architecture and the balun design. Initially, the performance of IHP's 0.13 μm SiGe HBT and WIN Semiconductor's 0.1 μm GaAs pHEMT are presented. Then the architecture types for the frequency doubler and balun are critically reviewed. Based on the literature review the differential topology for the frequency doubler along with a passive balun is selected.

In **Chapter 3** the analysis of the harmonics for a frequency doubler is presented. The theoretical concept of the inherent odd-harmonic cancellation for a frequency doubler with differential input is shown. The importance of balance in the differential signal for odd-harmonic rejection is investigated. The same analysis is applied to a SG13S SiGe HBT and a PP10-10 GaAs pHEMT. Accurate modelling of the transistors is out of the scope of this work. At first, the magnitude of the harmonics obtained from simulation using AWR are fitted with simple equations by introducing correction

coefficients on each of the terms (using MATLAB). These correction coefficients are then used for the rest of the analysis to provide a comparison between the calculated and simulated magnitudes of harmonics.

Chapter 4 focuses on balun design. First, the theoretical analyses for two different passive balun structures, the Marchand balun and the transformer balun, are discussed. The key differences between these two types of passive baluns are identified. Then the rest of the chapter discusses the design and implementation of the transformer balun in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process. The transformer balun in the SG13S SiGe HBT process is fabricated by IHP through Europractice while the balun in the PP10-10 GaAs pHEMT process is fabricated by WIN Semiconductors. A comparison of the simulated and measured results is shown and also the measurement results of the baluns implemented in the two processes are compared.

These balun designs are the work of Sudipta Chakraborty in consultation with Leigh E. Milner from DSTG, Adelaide. All measurements in Chapter 4 were performed by Sudipta Chakraborty. The transformer balun in SG13S SiGe HBT was measured at Macquarie University. Budhaditya Majumdar assisted with the measurement set-up. The transformer balun was also measured by Leigh E. Milner separately at DSTG to verify the measurement results. The transformer balun in the PP10-10 GaAs pHEMT process was measured at MACOM Technology Solutions, North Sydney Design Centre under the guidance of Gerry McCoulloch and Melissa Rodriguez.

Sections of this Chapter have been published as a conference paper:

- S. Chakraborty, L. E. Milner, L. T. Hall, X. Zhu, O. Sevimli and M. C. Heimlich, "Characterisation of a Transformer Balun for a 7-15 GHz SiGe Frequency Doubler", *Australian Microwave Symposium (AMS 2016)*, Adelaide, Australia.

The role of all other authors in this paper was supervisory. The results of the balun implemented in the PP10-10 GaAs pHEMT process are currently being considered for publication.

Chapter 5 presents the design and implementation of the frequency doubler in the SG13S SiGe HBT process. A systematic design flow is adopted to minimise the

time for the design in the SG13S SiGe HBT process. The use of P-cells (parameterised cells) made the layout efficient and also minimised the chances of error.

Sudipta Chakraborty designed the frequency-doubler circuit. Design consultation was provided by Leigh E. Milner from DSTG, Adelaide. The design was reviewed by Jim Harvey from MACOM Technology Solutions, North Sydney Design Centre. The frequency doubler is fabricated by IHP through Europractice. All measurements in Chapter 5 were performed by Sudipta Chakraborty at MACOM Technology Solutions, North Sydney Design Centre under the guidance of Gerry McCoulloch.

Sections of this Chapter and Chapter 4 have been published as an article:

- S. Chakraborty, L. E. Milner, X. Zhu, L. T. Hall, O. Sevimli and M. C. Heimlich, "A K-band Frequency Doubler with 35-dB Fundamental Rejection Based on Novel Transformer Balun in 0.13 μm SiGe Technology", *IEEE Electron Device Letters*. vol. 37, no. 11, pp. 1375-1378, Nov. 2016.

The role of all other authors in this article was supervisory.

In **Chapter 6** the design and implementation of the frequency doubler in the PP10-10 GaAs pHEMT process is discussed. The design flow adopted in the PP10-10 GaAs pHEMT process and a comparison of the simulated and the measured results are also presented.

Sudipta Chakraborty designed the frequency-doubler circuit. Design consultation was provided by Melissa Rodriguez from MACOM Technology Solutions. The frequency doubler is fabricated by WIN Semiconductors. All measurements in Chapter 6 were performed by Sudipta Chakraborty at MACOM Technology Solutions, North Sydney Design Centre under the guidance of Gerry McCoulloch and Melissa Rodriguez.

Chapter 7 outlines the comparison between the frequency-doubler circuits and the baluns implemented in the SG13S SiGe HBT and PP10-10 GaAs pHEMT processes in terms of circuit design and implementation challenges. Design parameters of the frequency-doubler circuits are reviewed with respect to the implemented designs. Simulation results of E-band baluns in both processes are also presented. Sections of this chapter have been submitted as a conference paper:

- S. Chakraborty, L. E. Milner, L. T. Hall, Anthony E. Parker and M. C. Heimlich, "A 30-60 GHz SiGe Transformer Balun with Offset Radii Coils for Low Amplitude and Phase Imbalance", *International Microwave Symposium, (IMS 2017)*, (submitted).

Finally, **Chapter 8** concludes the dissertation by summarising the major outcomes. Avenues for the future research work are briefly discussed.

2

Background

2.1 Introduction

As stated in Chapter 1, the aim of this dissertation is to study the inherent linearity that could be achieved from a particular process technology in the context of a real-world functional system (QAM), to understand the performance that could be achieved and its related limitations, which would be relevant to IC designers. For this purpose, a frequency-doubler circuit is considered as an archetype of the non-linear circuit whose non-idealities will limit the overall linearity of a system such as a wireless transmitter or receiver. Baluns are considered as an archetype for the passive circuits. The design and implementation of a frequency doubler and a balun in two processes, namely the 0.13 μm SiGe BiCMOS process from IHP (codenamed SG13S) and the 0.1 μm GaAs process from WIN Semiconductors (codenamed PP10-10), will be described in this

dissertation. Therefore, in this chapter, an overview of IHP's SG13S process and WIN Semiconductor's PP10-10 process are presented at the beginning. Then a literature review on the frequency-doubler design and the balun design is presented.

An overview of the two processes, the SG13S SiGe HBT and the PP10-10 GaAs pHEMT, is in the next section. Although SG13S is a BiCMOS process, it is referred to as the SG13S SiGe HBT process because only the HBTs are used for the circuit implementation.

2.2 SG13S SiGe HBT process

Modern wireless communication systems with a data rate of greater than 1 Gbit/s require process technologies with high-speed transistors and high-density logic [43]. This paved the way for BiCMOS technologies which integrate high-speed SiGe Heterojunction Bipolar transistors (HBTs) in advanced RF CMOS platforms, catering to the demands of millimetre-wave communication systems operating above 100 GHz and optical communication systems with data rates of above 100 Gb/s. [43]. In the last decade, different companies have developed their advanced HBTs in 0.13 μm CMOS technology [43–47]. With the improved performance of the transistors from one technology node to the other, the SiGe BiCMOS process is increasingly used for applications such as millimetre-wave sensing and imaging, high-data-rate wireline and wireless communications and automotive radars [2].

Available HBTs

IHP's 0.13 μm SiGe BiCMOS process supports two types of HBTs: high speed (HS-HBT) and high voltage (HV-HBT) [48]. f_{max} and f_T for devices with an emitter length of 2 μm are 300 GHz and 250 GHz respectively, with a BV_{CEO} of 1.7 V for HS-HBTs. A minimum noise figure below 1 dB is measured up to 26 GHz, which is quite competitive with the noise figures reported for state-of-the-art GaAs pHEMTs. f_T and f_{max} for HV-HBT devices are 50 GHz and 130 GHz respectively for a 1.5 V collector-to-emitter voltage. A BV_{CEO} of 3.7 V is obtained due to lower collector doping of the HV-HBT. The different parameter values of HS and HV HBTs are listed in Table 2.1.

Table 2.1: Summary of HBT parameters of IHP SG13S process

Parameter	HS-HBT	HV-HBT
β at V_{BE}=0.7 V	900	800
peak f_T (GHz) at V_{CE}=1.5 V	240	50
peak f_{max} (GHz) at V_{CE}=1.5 V	330	130
BV_{EBO} at 1 μA (V)	1.6	1.6
BV_{CEO} at 1 μA (V)	1.7	3.7
BV_{CBO} at 1 μA (V)	5	14
A_E (μm ^{2})	0.17×0.53	0.23×1.05

Electrical characteristics

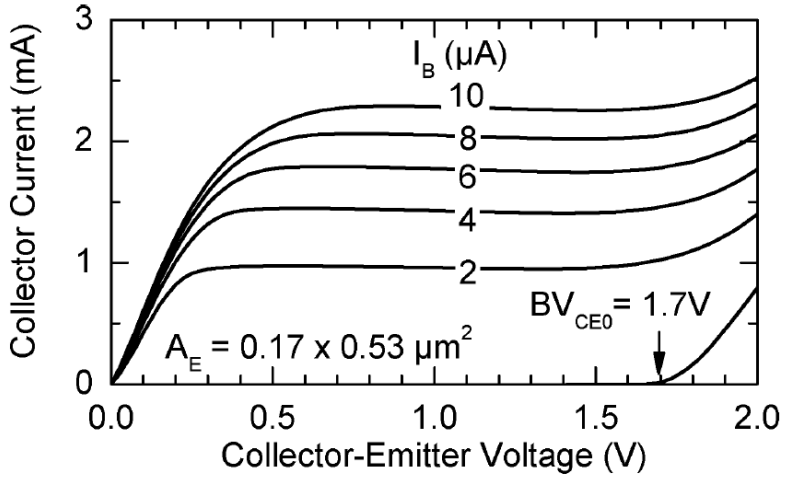


Figure 2.1: Output characteristics of HS-HBT.

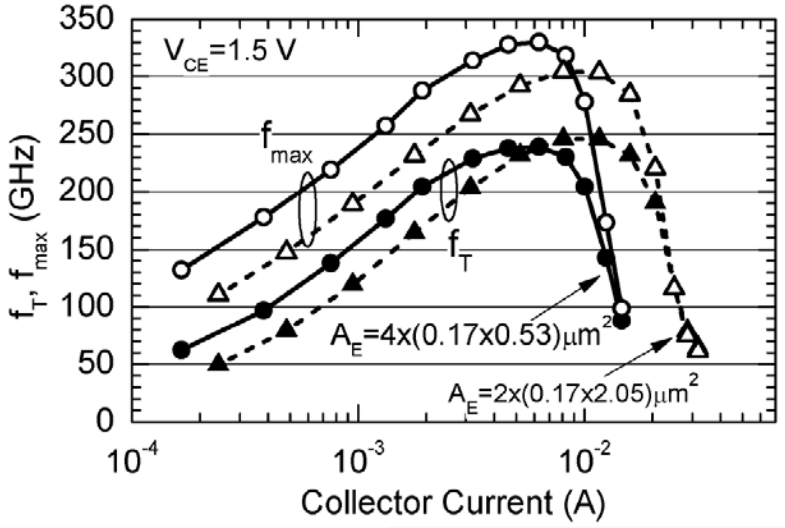


Figure 2.2: f_T and f_{max} of the HS-HBT.

For the high-frequency circuit implementation (frequency doubler) HS-HBTs are suitable for their high f_T and f_{max}. Fig. 2.1 depicts the output characteristics of an HS-HBT with an emitter area of $0.17 \times 0.53\ \mu m^2$. Fig. 2.2 illustrates the f_T and f_{max} of the HS-HBT versus the collector current [48].

Stack-up of metal layers

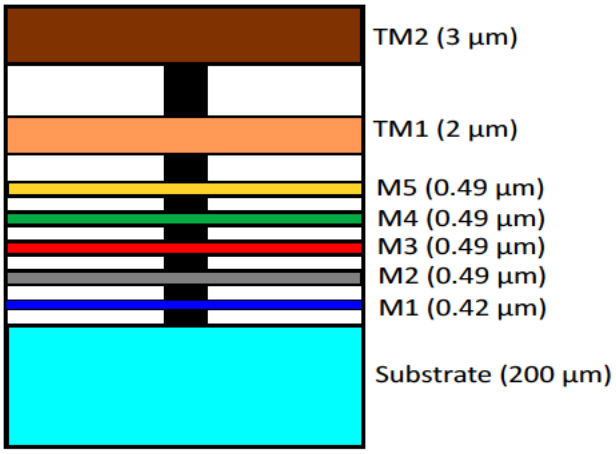


FIGURE 2.3: Detailed cross-sectional view of the metal layers available in the SG13S SiGe HBT process.

The SG13S process offers a stack-up of five different thin metal layers (M1 to M5) and two thick metal layers (TM1 and TM2). A detailed cross-sectional view of the metal layers available in the SG13S process is shown in Fig. 2.3. This is a planarised process; a particular metal layer is at the same height throughout the layout. Cross-over connections can be easily implemented in this process due to the availability of seven metal layers. In the SG13S process, the substrate is 200 μm thick. The transistors and the resistors are embedded in the substrate beneath the metal layers. The MIM capacitor lies between M5 (bottom plate) and TM1 (top plate). More information on the process specifications is provided in Appendix B.

2.3 PP10-10 GaAs pHEMT process

High-performance, reliable process technologies are required for emerging applications in the E and W bands such as point-to-point radio and active-scanning security systems [49]. WIN Semiconductors has developed 2 mil and 4 mil thick substrates for high-performance 0.1 μm GaAs pHEMTs that are targeted towards applications in 3G / 4G backhaul communication and radars for airport surveillance [25]. The electron-beam lithography technique is used for the gate formation. As demonstrated in [25], in this process, codenamed PP10-10, a typical gate width of 0.1 μm at the bottom and 0.5 μm at the top is fabricated within the drain-to-source spacing of 2 μm. This results in a very low gate resistance of the channel, critical for high-frequency operation.

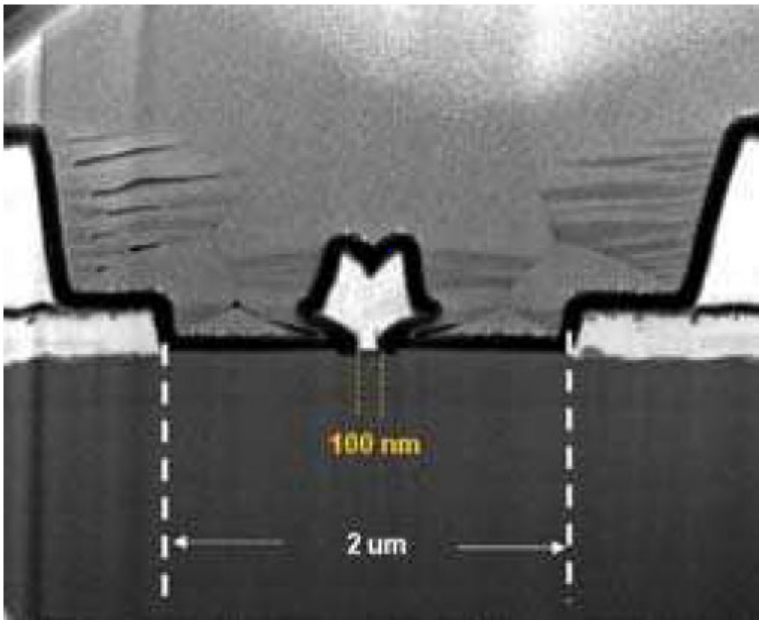


Figure 2.4: The cross-section of a 0.1 μm GaAs PP10-10 pHEMT device.

The cross-section of the 0.1 μm GaAs pHEMT in the PP10-10 process is shown in Fig. 2.4 [25]. The transistor's pinch-off voltage is -0.95 V. A maximum drain current of 760 mA/mm is achieved at a maximum transconductance of 725 mS/mm by applying a drain-source voltage of 0.5 V. The drain-source breakdown of the transistor is at about 9 V. The key parameter values for the 0.1 μm GaAs pHEMT in the PP10-10 process

TABLE 2.2: Summary of pHEMT parameters of WIN Semiconductor's PP10-10 process

Parameter	Units	Value
f_T	GHz	130
f_{max}	GHz	180
Peak transconductance (Gm_{peak})	mS/mm	725
Maximum drain current (I_{Dmax})	mA/mm	760
Pinch-off voltage	V	-0.95
Breakdown voltage (V_{DG})	V	9

are listed in Table 2.2 [25].

Electrical characteristics

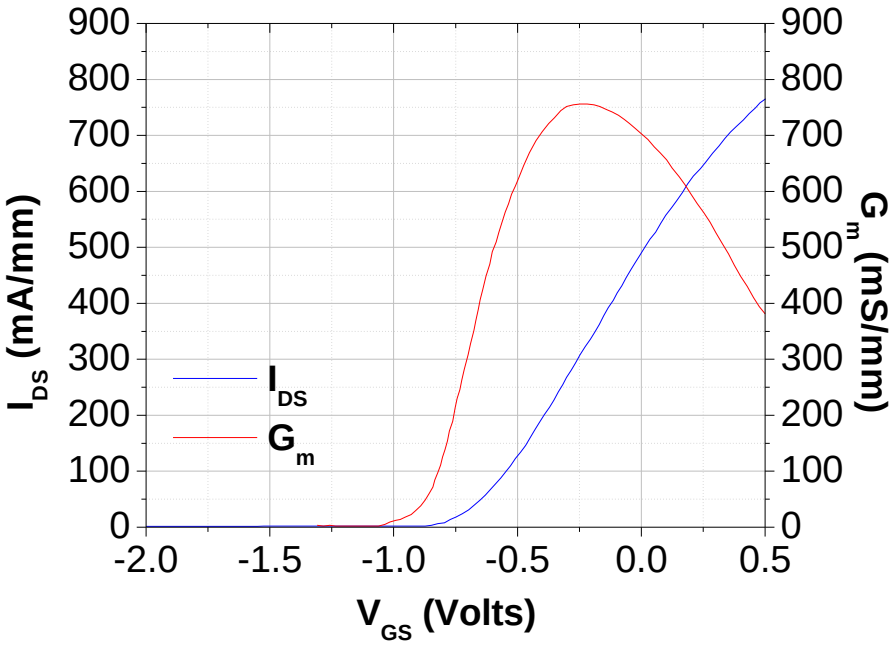


FIGURE 2.5: Plot for transconductance and drain current of a 2 × 50 μm transistor in the PP10-10 GaAs pHEMT process.

The DC behaviour plot for I_{DS} vs V_{GS} and g_m vs V_{GS} are shown in Fig. 2.5 for a 2-finger, 50-μm-gate transistor. I_{DS} vs V_{DS} curves are shown in Fig. 2.6, and Fig. 2.7 shows the maximum stable gain [25].

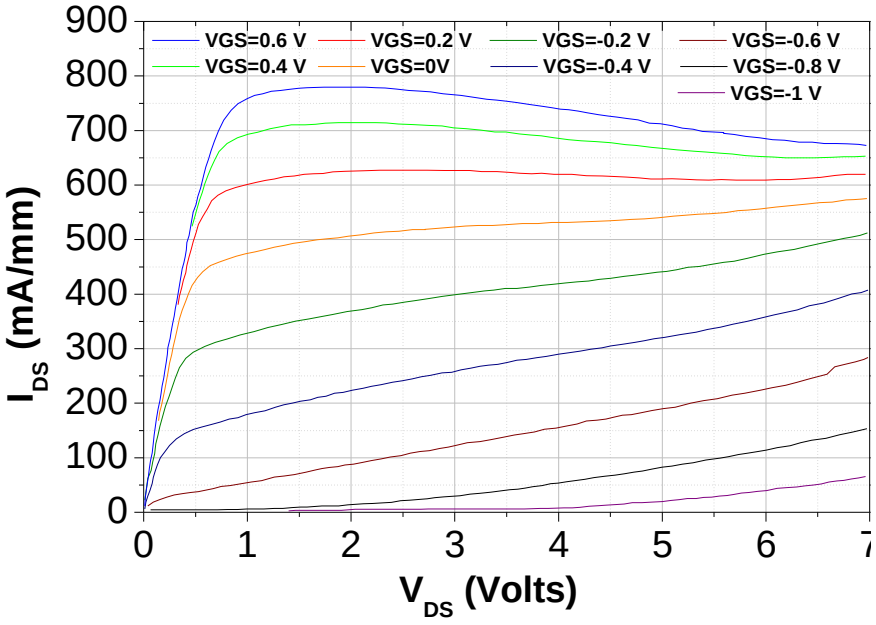


FIGURE 2.6: IV characteristics of a 2 × 50 μm transistor in PP10-10 GaAs pHEMT process.

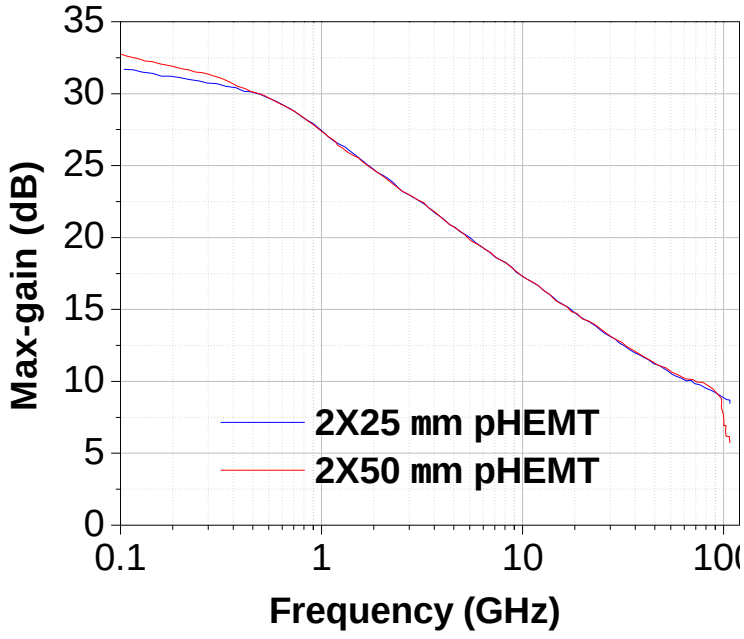


FIGURE 2.7: Maximum gain performance of 2 × 25 μm and 2 × 50 μm transistors in PP10-10 GaAs pHEMT process.

Stack-up of metal layers

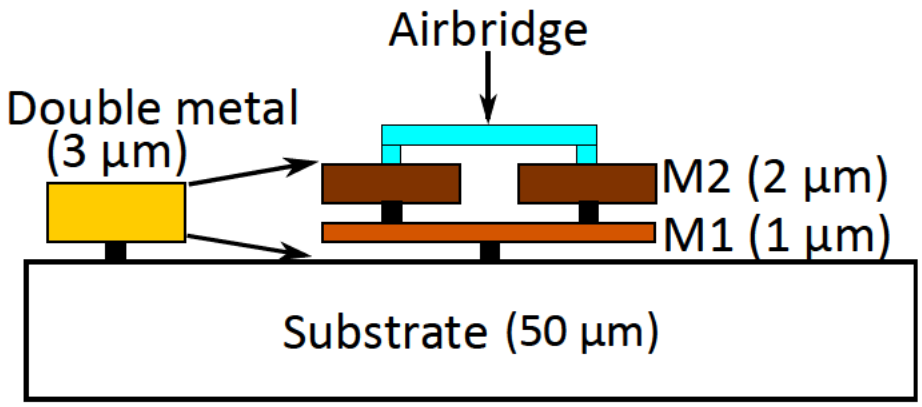


FIGURE 2.8: Metal stack-up available in the PP10-10 GaAs pHEMT process.

The PP10-10 GaAs pHEMT process offers a stack-up of only two metal layers, metal 1 (M1) and metal 2 (M2). The thicknesses of M1 and M2 are 1 μm and 2 μm respectively. The current density for the M1 layer is 4 mA/μm and for the M2 layer is 6 mA/μm. A double metal layer or combined M1 and M2 (3 μm thickness) connected by via is also allowed for the layout. The double metal layer provides increased current-handling capability. The current density in the double metal layer is 10 mA/μm. A cross-sectional view of the metal layers available in the PP10-10 process is shown in Fig. 2.8. As the PP10-10 GaAs pHEMT process is not planarised, the metal lines are not at the same level throughout the layout. Cross-over connections cannot be implemented easily in this process. Usually, airbridges are used to connect two sections of M2 lines to provide a jump over the M1 lines in order to implement a cross-over connection.

In the PP10-10 GaAs pHEMT process, the substrate is 50 μm thick. An epitaxial structure is grown on top of the GaAs wafer to form the pHEMT and the passive elements. Thin-film resistors (TFR) are grown on the substrate. Capacitors are made with M1 (bottom plate) and M2 (top plate) with silicon nitride (SiN) as an insulator in between. More information on the process specifications is provided in Appendix B.

2.4 Frequency doublers

Frequency multipliers are non-linear circuits that multiply the low frequency of the input signal by a predetermined (integer) factor to generate a high-frequency signal at the output. Frequency multipliers with high conversion gain and high efficiency over a large bandwidth are desirable for transceivers. The non-linearity of the semiconductor device is exploited to generate harmonics. The desired harmonic is allowed to pass to the output, which thereby translates the low-frequency input signal to a high-frequency output. Several techniques can be adopted to realise the frequency multiplier. Frequency doublers (×2), triplers (×3), quadruplers (×4) are reported in the existing literature. To design a higher-order frequency multiplier in one step, large input power is required to drive the device into the highly non-linear region. The conversion loss of the device increases with the multiplication factor [50–53]. Moreover, high-order filters are required with these single-stage large-multiplication-factor frequency multipliers to suppress the undesired harmonics, which lead to a small bandwidth. Therefore, for

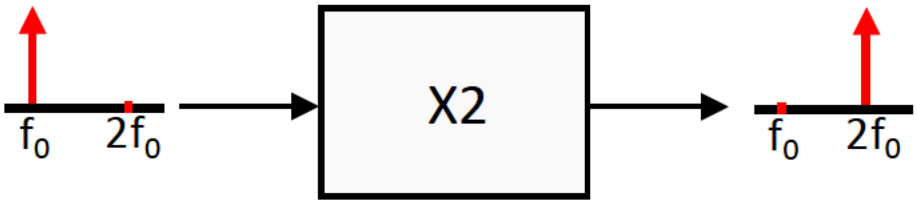


Figure 2.9: Block diagram of a frequency doubler.

higher-order frequency multiplication, it is desirable to cascade several low-order frequency multipliers rather than implement a higher-order multiplier at one step. This increases the conversion efficiency and bandwidth of the system. For example, for a power-of-two multiplication factor, several frequency doublers are cascaded, which can provide high odd-harmonic suppression. This also reduces the requirement for sharp harmonic filters, which occupy a large area and limit the bandwidth [54]. Hence, a frequency doubler is considered as an archetype of a non-linear circuit in this work. The basic block diagram of a frequency doubler is shown in Fig. 2.9.

Frequency doublers can be classified into two categories, depending on the type of

semiconductor devices used: active or passive. In passive frequency doublers, diodes are used as the nonlinear device, unlike active frequency doublers, where transistors are used. Frequency doublers can be implemented in several ways using diodes or transistors.

2.4.1 Single diode

Diode frequency multipliers are implemented using a Schottky-barrier diode or varactor. Frequency multipliers using a Schottky-barrier diode utilise the nonlinear I-V characteristics of the diode to generate harmonics. For a frequency doubler, parallel LC resonators are used at the input and the output, short-circuiting the unwanted harmonics at the input and allowing the second harmonic at the output. The sizes of the inductors and capacitors are selected to optimise the source and load impedances of the diode [55]. At microwave frequencies, microstrip lines are used. For a frequency doubler, a $\lambda/4$ transmission line at f_0 is short-circuited through a stub at the input of the Schottky diode, which creates a short circuit at $2f_0$ ($\lambda/2$) and prevents the second harmonic from travelling back from the output to the input. A $\lambda/4$ transmission line at f_0, an open-ended stub, is used at the output and short-circuits any f_0 signal at the output. These $\lambda/4$ transmission lines at f_0 (or $\lambda/2$ lines at $2f_0$) increase the chip size and reduce the doubler bandwidth [56]. A single diode multiplier can be used for low-cost applications and they are also easy to bias.

2.4.2 Balanced diodes

A pair of diodes is also used for implementing frequency multipliers. Balanced frequency multipliers provide a higher output power than single-diode multipliers. Anti-parallel diodes provide even-harmonic suppression and can be used as an odd-order frequency multiplier. An output filter is required to suppress the fundamental signal at the output.

Bridge rectifier circuits can be used to realise resistive frequency doublers. In a balanced bridge multiplier, a train of half-sinusoidal pulses of current is formed. These

doublers inherently reject all the odd harmonics. Hence additional filtering is not required for the fundamental and third harmonic. This type of resistive frequency doubler using a quad diode can provide good bandwidth and fundamental rejection [57, 58] but they have a high conversion loss due to their large series resistance. The sizes of the diodes can be increased to improve the performance, but this also increases the parasitic capacitance, limiting the frequency range of operation [56].

Varactor multipliers have a higher efficiency and higher output power than resistive multipliers, but they have a small bandwidth [59] and are susceptible to any small changes in the circuit parameters. Step-recovery diodes have a higher efficiency than varactor diodes for implementing higher-order frequency multipliers, but the output frequency is limited. Overall these diode-based multipliers need a large input power to drive the diodes into the non-linear region of operation. They suffer from a conversion loss. It might be difficult to integrate these Schottky-diode-based multipliers with other blocks like oscillators and amplifiers [60]. In any diode-based multiplier, isolation between the input and output is a problem [61].

2.4.3 Transistor-based

The non-linearity of transistors is used in these frequency doublers. They can provide a conversion gain even for input signals with low power levels, unlike diode-based frequency multipliers. Typically, in FETs, the square-law characteristics, and in HBTs the exponential relation between the collector current and input voltage, are exploited to generate the harmonics. Research on frequency multipliers implemented using FETs [62, 63], HEMTs [64–67], HBTs [68–74] is reported in the existing literature. Several topologies are commonly used such as single-ended, balanced, injection-locked and Gilbert cell.

Single-ended

A single-ended signal is sent to the input of the multiplier [50, 75]. This topology has the advantage of not using a balun at the input, which saves area. The DC power

consumption of the single-ended topology is less than its differential counterparts, but filters are needed at the input and output to match the fundamental signal at the input and the second harmonic at the output, respectively, for a frequency doubler. The odd-harmonic suppression at the output of these doublers depends on the sharpness of the bandpass filters. This makes this topology inefficient for broadband designs, where the undesired harmonics fall into the desired band of harmonics and cannot be effectively removed by filtering.

Gilbert cell

In some applications, it is required to generate a differential signal at the output of a frequency multiplier. Gilbert-cell mixers can be used as frequency doublers with differential output, by injecting the same signal into the RF and LO ports. According to the analysis presented in [76], the output signal is not truly differential. [71, 77] suggest that an amplitude balance can be obtained at the output if the RF and LO signals appear in phase quadrature, for which long transmission lines are needed [68, 78].

Research in [76] demonstrates that if the RF and LO signals are in phase, then the RF input to the Gilbert-cell mixer can be switched to the output to produce a second-harmonic differential signal. But common-mode feedthrough from the LO port will be added to the output to create an unbalance in the differential output signal. [76] further suggests that it is impossible to realise both amplitude and phase balance simultaneously, at the differential output signal of a Gilbert-cell mixer, by tuning the phase between the RF and LO signals. A special transformer is designed to overcome this problem. However, it will occupy a large area. Moreover, it requires a large DC power consumption and, as the transistors are biased in the Class-A region, the output power is low [56].

Balanced

A differential signal is sent to the input of the doubler [84–86]. Theoretically, if the input signals are combined to a single-ended output, then it can inherently suppress the odd harmonics, and additional filters are not necessary for suppression of undesired odd

harmonics. Therefore, the balanced topology is suitable for broadband applications, and this topology is adopted for the frequency doubler implementation in this work. However, the magnitude of the odd-harmonic suppression depends on the symmetry of layout, match between the transistors and the quality of the differential signals [87]. Hence the design of the balun is crucial, as any imbalance in the differential signals will affect the capability of undesired-harmonic suppression by the balanced frequency doubler.

2.5 Design parameters of a frequency doubler

Frequency doublers are often used as unit cells in a chain of frequency multipliers. Broadband frequency doublers with high conversion gain and efficiency are used with low-frequency stable VCOs to provide a cost-effective solution. The different design parameters for a frequency doubler can be explained by a design pentagon as demonstrated in Fig. 2.10. A tradeoff exists between some of these parameters. For example, it is difficult to achieve a large bandwidth and good conversion gain simultaneously, or large harmonic rejection over a broad band. Therefore these parameters can be used to assess the performance of a frequency doubler such as harmonic rejection, bandwidth, conversion gain/loss, power dissipation, area.

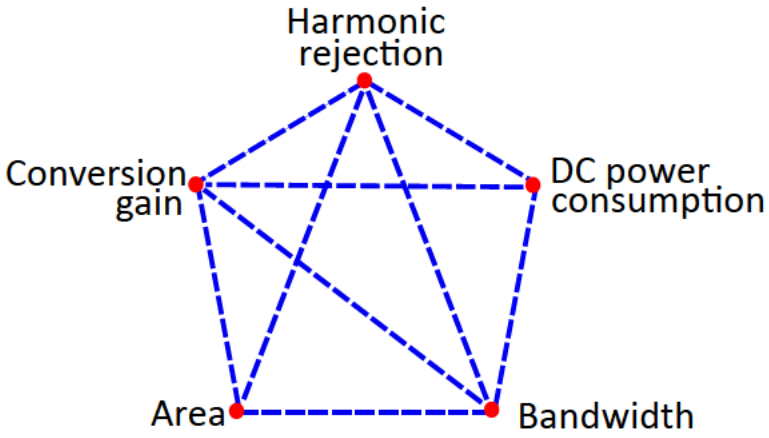


Figure 2.10: Tradeoff between the design parameters of a frequency doubler.

2.5.1 Conversion gain

A frequency multiplier is used with a VCO in a transceiver. The output of the VCO is connected to the input of the frequency multiplier. A frequency multiplier, cascaded with a VCO, drives a mixer, the next building block in the transceiver chain. The output power of the VCO might not be enough to provide adequate LO (local oscillator) power to the mixer at the high-frequency range. If an amplifier is used with a VCO, then the DC power consumption is increased. Hence, it is desirable to have a reasonable power of the wanted harmonic at the output of the frequency multiplier. For a frequency doubler, the conversion gain is used as one of the performance parameters and can be formulated as the ratio of the power of the second harmonic at the output to the power of the fundamental at the input

$$Conversion\ Gain\ (dB) = 10 \times \log_{10} \frac{P_o(2f_0)}{P_i(f_0)} \tag{2.1}$$

Generally, the magnitudes of the higher-order harmonics increase with an increase in the input power level. To get a suitable conversion gain the transistors should be biased optimally and also the input and output matching networks must be designed appropriately. It is also a difficult task to achieve good conversion gain over a large bandwidth. With an increase in the input power, the conversion gain could be improved but the harmonic rejection might be compromised.

2.5.2 Bandwidth

Microwave frequency bands such as K-band (18-26.5 GHz) and Ka-band (26.5-40 GHz) are widely used for backhaul communication. Recently, E-band (60-90 GHz) is gaining prominence for backhaul communication to avoid spectrum congestion at the lower frequency bands. Therefore, it is important for the operation bandwidth of a frequency doubler to cover these frequency bands. In other words, the operation bandwidth of the frequency doubler should be large enough to cover K-Ka band or E-band of the frequency spectrum. The 3-dB operation bandwidth is quoted as a percentage. It can

be expressed as

$$Bandwidth\ (\%) = \frac{f_{high} - f_{low}}{f_{midband}} \times 100 \tag{2.2}$$

It is more difficult to achieve a large bandwidth at higher frequency than at lower frequency. One of the reasons is the effect of the parasitic capacitance and series inductances which arise with small lengths of interconnect. Several design tradeoffs are encountered to obtain large bandwidth. In some design architectures, a large current is allowed to flow through the last stage of the design to shift the poles at the high frequency, which in turn increases the bandwidth.

2.5.3 Power consumption

The DC power consumption is an important design consideration, specially for systems which use a battery. Therefore it is desirable to keep the DC power consumption reasonably low. The total power consumption by the balun and the frequency doubler must be taken into account. It is advantageous, in terms of DC power consumption, to use a passive balun with a frequency doubler, as a passive balun does not consume any DC power. Based on the DC power consumption, a figure of merit can be formulated as

$$FOM\ (power) = 10 \times \log_{10} \frac{P_o(2f_0)}{P_{DC}} \tag{2.3}$$

2.5.4 Area

As the manufacturing cost increases with increase in area, it is desirable to make the circuit compact. Passive structures in general occupy a large area. Frequency doublers with an active balun or a single-ended input are better in terms of area, but they require a filter, which occupies a large area, to provide adequate harmonic suppression. At high frequency, as the wavelength reduces, the area occupied by passive baluns become comparable with their active counterparts. Apart from the topology of the circuit, the process itself influences the layout structure which affects the occupied area. The layouts of the circuits are different in a silicon-based process and in a GaAs-based process. For example, a silicon-based process offers a stack-up of different metal layers,

which allows a stacked layout. The layout in a GaAs-based process is spread out all over compared to the SiGe process and occupies a large area.

2.5.5 Harmonic rejection

In an active frequency multiplier involving transistors, the non-linearity of the transistors is exploited to generate the harmonics. The desired harmonic is sent to the output while the undesired harmonics are suppressed by a filter. Ideally, this filter returns all the energy found in the undesirable harmonics back into the doubler so that it can use this energy to possibly create more of the desired harmonic. The energy dissipated in a filter is just wasted energy.

The desired output power of a frequency doubler is the power at the second-harmonic frequency. In reality, undesired harmonics are also present at the output. Specifically, the fundamental and the third harmonics interfere with the second harmonic as they are close to the second-harmonic frequency and have strong output power. If these unwanted harmonics pass into the next building block in a transceiver chain, then the performance of the transceiver is greatly degraded [107]. These unwanted harmonics interfere with the desired signal resulting in undesired effects such as desensitisation, cross-modulation and inter-modulation [108]. Typically, for a frequency doubler, harmonic suppression of greater than 20 dBc is targeted. The harmonic rejection is one of the most important performance parameters for a frequency multiplier. For a frequency doubler, the harmonic rejection can be quantified by

$$Harmonic\ rejection\ (dB) = 10 \times \log_{10} \frac{P_o(2f_0)}{P_o(nf_0)} \tag{2.4}$$

where, n = 1,3,4,5.....

Among the odd harmonics present at the output of a frequency-doubler circuit, the fundamental signal is large in magnitude (as the magnitudes of the harmonics degrades with the order of the harmonics). To improve the fundamental rejection, it is better to reduce the fundamental leakage at the output of the doubler rather than just trying to increase the magnitude of the second harmonic by tuning the bias voltage of the

device.

Tradeoffs exist between good odd-harmonic suppression and other performance parameters of the frequency doubler. For example, it is challenging to achieve good odd-harmonic suppression over a large bandwidth. Higher-order harmonics can be suppressed if the input power level of the signal is low, but the conversion gain will be degraded. An addition of a filter at the output of the doubler to improve the odd-harmonic rejection will occupy a large area.

2.6 Balun

Baluns are often used in microwave and millimetre-wave circuits with balanced frequency multipliers. For these differential circuits unbalanced-to-balanced signal converters are necessary, and on-chip baluns are used for this purpose. A balun is a three-port device comprised of an "unbalanced" port and two "balanced" (differential) ports. Ideally, the differential signals generated at the output of the balun are equal in magnitude and 180^o out of phase across all frequencies, but there is always an amplitude and phase imbalance in reality. Therefore, amplitude and phase imbalance are used as a performance metric for the balun. Baluns can be classified into two major types: active and passive baluns.

A simple active balun can be designed using a single transistor in which the input is fed to the base, and the output is taken from the emitter and collector [88]. To minimise the imbalance, the impedances as seen from the collector and emitter should be equal. Fig. 2.11 [89] shows the schematic of a single-transistor active balun, with matched inductances at the collector and emitter [88]. This topology is simple, but it has a large imbalance in the differential signals.

To overcome this problem, [90, 91] use an active balun which consists of a common-emitter stage followed by a differential limiting cascode-amplifier stage. This helps to limit the output power and minimises common-mode leakage from the input at high frequency. It provides better common-mode rejection, which in turn improves the

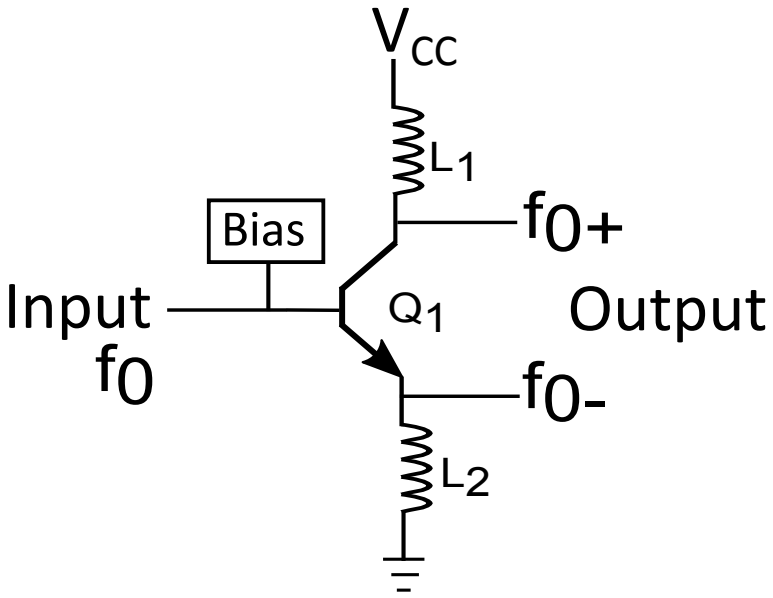


FIGURE 2.11: Active balun using a single transistor.

balance of the differential signal. But these active baluns use inductors for input and output matching, which increases the overall area. Further, [92] reported an active balun which consists of a common-emitter stage followed by two stages of differential cascade amplifiers for better common-mode rejection. It also uses a resistive load to minimise the area. But this design is complicated, as it requires maintaining of a bias for ten transistors, and has a high power consumption.

The common-emitter based differential pair can be used as a balun [93]. The single-ended signal is fed to the base of one transistor while the base of the other transistor is connected to AC ground by a capacitor. The output is taken from the two collectors as in Fig. 2.12 [89]. At high frequencies, the Miller effect comes into the picture and the gain deteriorates [89]. Moreover, the linearity is poor but could be improved by inductive degeneration. This topology suffers from a high phase imbalance and poor CMRR at high frequencies [89]. The performance of the differential-pair balun could be improved by adding an amplifier at the output [89].

[94] shows an active balun design using pHEMTs. The input signal is sent through two paths, with a common-source transistor stage in one path and a common-gate transistor stage in the other. The differential signal is generated at the output, as the

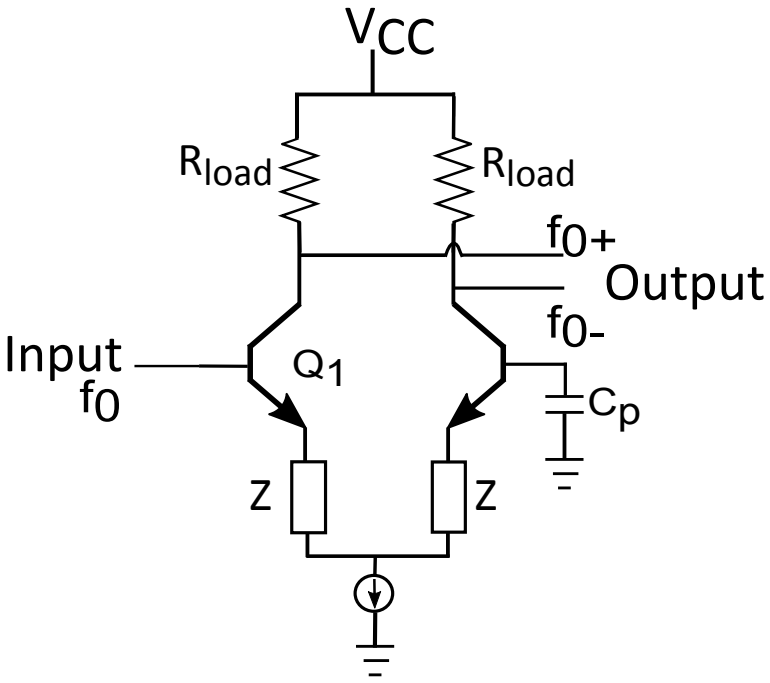


Figure 2.12: Active balun using a modified differential-pair configuration.

phase of the input signal is changed by 180^o by the common-source stage while the common-gate stage does not change the phase of the signal. Phase imbalance could be a problem for this topology over a broad band [65]. Different matching circuits are used at the output of the common-source and common-gate stages to improve the phase imbalance [65].

In Monolithic Microwave Integrated Circuit (MMIC) design, different types of passive baluns using a Lange coupler, Marchand balun [95, 96], rat-race coupler [97, 98], transformer balun [99, 100], and passive-element balun using LC networks are reported [101]. Passive baluns implemented using planar waveguides and microstrip transmission lines are reported in [102–106]. Passive baluns using LCR networks are suitable for their high integration capability [89] and impedance transformation [101]. But these baluns have a small bandwidth, as the LC networks can be tuned over only a narrow band. The accuracy of the passive-element baluns depends on the design of the inductors and capacitors. The sizes of the inductors are large at lower frequencies, and the high Q-factor requirement may not be achieved in practice.

Among these passive baluns, the planar Marchand balun is commonly used in

MMIC designs for its wideband operation [96]. Marchand proposed the conventional Marchand balun structure in 1944 [95]. It consists of two quarter-wavelength coupled line sections with an open circuit at the other end of the input port line. As the size of the balun is proportional to the wavelength, it occupies a large area at low frequencies, which makes it unsuitable for low-frequency applications. These baluns are mostly used with the GaAs process. A transformer can be converted into a balun by grounding one terminal of the primary, and a differential signal is generated at the two terminals of the secondary. Transformer baluns can provide an impedance transformation by varying the number of turns [102, 106]. Unlike the Marchand baluns, transformer baluns are not dependent on wavelength. Therefore these baluns are more compact than Marchand baluns, making them more suitable for low-frequency operation.

For integrated-circuit application, an active balun is an attractive solution for an unbalanced-to-balanced signal conversion, because of its smaller size. Active baluns have the capacity to provide gain, but they may distort the signal and consume DC power. Passive baluns, on the other hand, do not consume DC power, provide good linearity and are bi-directional. But they introduce an insertion loss and occupy a large area. As the main aim of this work is to study the non-linearity in a particular process, therefore passive baluns are chosen for the balanced frequency doublers, as the passive baluns do not distort the generated differential signals. Implementation of a passive balun with minimum non-idealities and compact size will be the design challenge. It is also important to find if passive baluns are suitable for both the SG13S SiGe HBT process (without an underneath ground plane) and the PP10-10 GaAs pHEMT process (with an underneath ground plane).

2.7 Summary

In this chapter an overview of the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process is presented. The plots for the electrical characteristics and the important parameter values are listed for a SiGe HBT in the SG13S process and a pHEMT in the PP10-10 GaAs process. From the process overview, it is found that both of these

processes can be utilised for high-frequency circuit design. Hence implementation of frequency-doubler circuits using the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process will be described in this work.

From the literature review of the frequency doubler, it is found that the balanced topology can inherently cancel the odd harmonics and is suitable for wide-band applications. Therefore, the balanced topology will be adopted for the frequency-doubler implementation. An analysis of the harmonics for a balanced frequency doubler will be presented in the next chapter.

Among the different types of balun reported in the literature, the passive balun is chosen to provide a differential signal to the balanced frequency doubler. Marchand baluns are often used for microwave and millimetre-wave circuits, but the transformer balun has some merits over the Marchand balun. The analysis for the transformer balun and the Marchand balun will be studied in the Chapter 4. It will be followed by the implementation of the passive balun in both the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process.

3

Analysis of harmonic generation in frequency doubler

3.1 Introduction

The frequency multiplier is an important building block in microwave and millimetre-wave transceiver design for wireless communication systems. At this high frequency, it is difficult to design voltage-controlled oscillators (VCO) with good phase noise, wide tuning range and flat output power. To mitigate this problem, frequency multipliers (for example frequency doublers) are used with a low-frequency fundamental signal source to relax the design constraints of the VCO. In frequency multipliers, non-linearity of the transistors biased at a suitable operating point is utilised to generate the harmonics in the output current. One of the key performance parameters of the

frequency doubler is the odd-harmonic suppression.

For a frequency doubler with a large bandwidth, undesired harmonics may fall into the desired band, thereby rendering the filters unusable for this application. Differential-input frequency doublers are more suitable for wideband operation as they have the ability to inherently cancel the odd harmonics when optimally designed and operated. In practical circuits, odd harmonics are present at the output of the balanced frequency doubler. The odd-harmonic rejection of a balanced frequency doubler is mainly dependent on the match between the transistors, the symmetry of the layout and the balance of the differential signals.

The balance of the differential signals is a critical parameter. Non-ideality in the input differential signals affects the odd-harmonic suppression which in turn will affect the linearity of an overall system such as a wireless transmitter or a receiver. The importance of the amplitude and phase balance of input differential signals with respect to a balanced frequency doubler is studied in this chapter. In this work, frequency doublers are implemented in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process. Therefore, the non-linear behaviour which generates the harmonics in a SiGe HBT and a GaAs pHEMT with respect to a frequency doubler is studied. Simple equations are derived to demonstrate the effect of amplitude and phase imbalance on the odd-harmonic suppression.

3.2 Harmonic generation in a SG13S SiGe HBT

The harmonics generated in a SG13S SiGe HBT is studied at the beginning. Then the analysis is extended further for a balanced frequency doubler.

3.2.1 Simple bipolar transistor model

To study the harmonics, a simple bipolar transistor model is considered. If the transistor is biased with base-emitter voltage V_{BE} and supply voltage V_{CC}, a quiescent collector current I_C and a base current I_B will flow through the transistor. A small-signal voltage v_{be}, applied at the base, will cause a small variation in the base current i_b

and the collector current i_c. The total collector current i_C, can be represented as [109]-

$$i_C = I_C + i_c \tag{3.1}$$

For a bipolar transistor, the collector current i_C is exponentially related to the base emitter voltage v_{BE}. The total collector current i_C, can be expressed as

$$i_C = I_S \exp(\frac{V_{BE} + v_{be}}{\eta V_T}) \tag{3.2a}$$

where I_S is the reverse saturation current, η is the ideality factor, V_T is the thermal voltage. But the DC collector current is

$$I_C = I_S \exp(\frac{V_{BE}}{\eta V_T}) \tag{3.2b}$$

Therefore the total instantaneous collector current is expressed as

$$i_C = I_C \exp(\frac{v_{BE}}{\eta V_T}) \tag{3.2c}$$

Theoretically, the harmonics can be calculated by assuming a small-signal voltage $v_{be} < V_T$ and expanding i_C by the Taylor series.

$$i_C = I_C \left[1 + \left(\frac{v_{be}}{\eta V_T}\right) + \frac{1}{2!}\left(\frac{v_{be}}{\eta V_T}\right)^2 + \frac{1}{3!}\left(\frac{v_{be}}{\eta V_T}\right)^3 + \frac{1}{4!}\left(\frac{v_{be}}{\eta V_T}\right)^4 + ...\right] \tag{3.3}$$

Considering the sinusoidal signal excitation to be $v_i = V_m \cos \omega_o t$ where V_m is the small-signal amplitude, and assuming R_B, R_E, R_C as negligible, v_{be} is equal to the applied external signal excitation v_i. Therefore the above equation can be expanded

by Taylor series as:

$$i_C = I_C \left[1 + \left(\frac{V_m \cos\omega_o t}{\eta V_T}\right) + \frac{1}{2!}\left(\frac{V_m \cos\omega_o t}{\eta V_T}\right)^2 + \frac{1}{3!}\left(\frac{V_m \cos\omega_o t}{\eta V_T}\right)^3 + \frac{1}{4!}\left(\frac{V_m \cos\omega_o t}{\eta V_T}\right)^4 + ...\right] \tag{3.4a}$$

$$i_C = I_C \left[\left(1 + \frac{V_m^2}{4\eta^2 V_T^2} + \frac{3V_m^4}{192\eta^4 V_T^4}\right) + \left(\frac{V_m}{\eta V_T} + \frac{3V_m^3}{24\eta^3 V_T^3}\right)\cos(\omega_o t) + \left(\frac{V_m^2}{4\eta^2 V_T^2} + \frac{4V_m^4}{192\eta^4 V_T^4}\right) \cos(2\omega_o t) + \left(\frac{V_m^3}{24\eta^3 V_T^3}\right)\cos(3\omega_o t) + \left(\frac{V_m^4}{192\eta^4 V_T^4}\right)\cos(4\omega_o t) + ...\right] \tag{3.4b}$$

3.2.2 Foundry HBT model

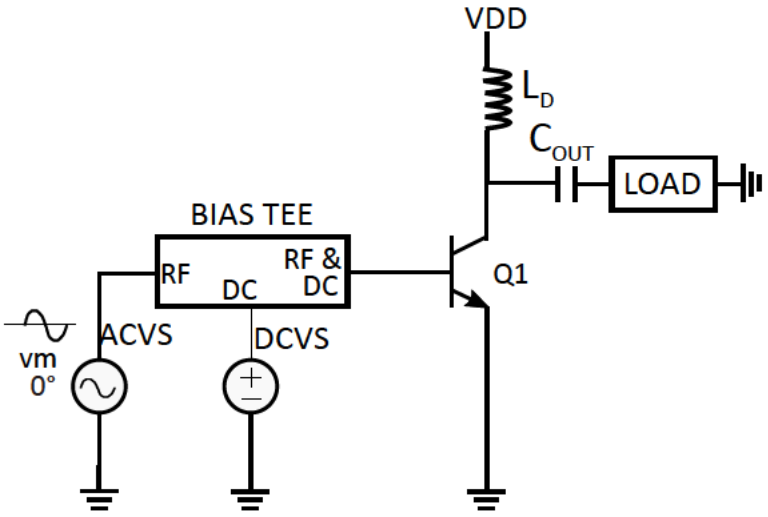


FIGURE 3.1: Test bench for simulating the harmonics in collector current of a SG13S SiGe HBT.

To study the harmonics of a SG13S SiGe HBT, a single transistor Q_1 is considered in AWR. The transistor is biased close to the saturation region, with V_{BE} at 0.82 V (selected from bias sweep) and supply voltage V_{CC} at 1.7 V (maximum BV_{CEO}). The quiescent collector current I_C (1.65 mA) and the base current I_B flow through the transistor. An alternating current (AC) voltage signal v_{be} is also applied through the bias tee. This causes a small variation in the base current i_b and the collector current i_c. The harmonics in the collector current are simulated by using a probe at the collector.

AWR Analog Office is used to simulate the equation 3.4 by using a SG13S SiGe HBT from the SG13S library. The schematic is shown in Fig. 3.1.

The magnitude of the harmonics calculated in MATLAB using equation 3.4, do not match the AWR simulation results for a SG13S SiGe HBT. A SiGe HBT is developed by selective incorporation of germanium into the base of a silicon bipolar transistor with the help of bandgap engineering [110–112]. This bandgap grading in a SiGe HBT results in an accelerating drift field which facilitates the minority carrier transport through the base of the transistor. Therefore, f_T for the HBTs is improved. Also, the base grading profile in SiGe HBTs improves transistor parameters such as forward current gain (β) and transconductance (g_m) compared to silicon BJTs [113]. As the model of the HBTs is complicated, some research has been carried out in the recent past [114–117]. Some special features in HBTs, like the Kirk effect and temperature effects, are also captured by the models. By using device engineering different parameter values for the transistors are extracted for these models. As the focus of this work is not on the device engineering, accurate modelling of the transistors is out of the scope of this work. Also the applied external signal excitation signal v_{in} is not equal to v_{be} as the internal resistances of the HBT (R_B, R_C, R_E) cannot be neglected.

Therefore, equations in 3.4 need to be modified. For the purpose of the analysis of harmonics in a SG13S SiGe HBT, the magnitudes of the harmonics derived in equation 3.4 are multiplied by some constants ($k_1 - k_4$). These constants are derived by curve fitting in MATLAB with reference to AWR simulation results. For a particular bias of the transistor, these parameter values are then kept fixed for the rest of the analysis.

The modified expressions of the harmonics for a SG13S SiGe HBT are:

$$i_C(\omega_0) = I_C \left[\frac{k_1 V_m}{V_T} + \frac{3(k_3 V_m)^3}{24 V_T^3} \right] \delta(\omega - \omega_o) \tag{3.5a}$$

$$i_C(2\omega_0) = I_C \left[\frac{(k_2 V_m)^2}{4 V_T^2} + \frac{4(k_4 V_m)^4}{192 V_T^4} \right] \delta(\omega - 2\omega_o) \tag{3.5b}$$

$$i_C(3\omega_0) = I_C \left[\frac{(k_3 V_m)^3}{24 V_T^3} \right] \delta(\omega - 3\omega_o) \tag{3.5c}$$

$$i_C(4\omega_0) = I_C \left[\frac{(k_4 V_m)^4}{192 V_T^4} \right] \delta(\omega - 4\omega_o) \tag{3.5d}$$

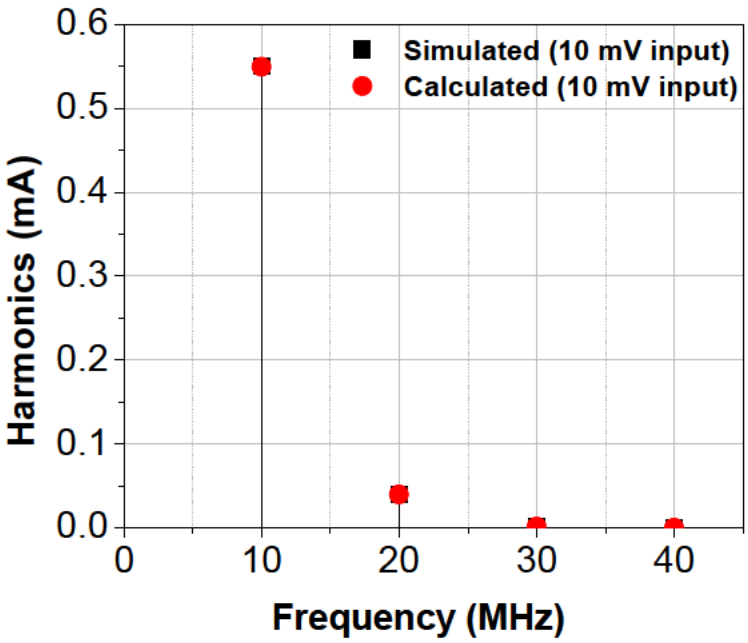


FIGURE 3.2: Comparison of the simulated (black line) and calculated (red dot) magnitudes of harmonics in the collector current of a SG13S SiGe HBT, for a 10 MHz input.

A comparison of the calculated magnitude (in MATLAB) and the simulated magnitude (in AWR) of the harmonics in the collector current for v_{in} of 10 mV at 10 MHz is shown in Fig. 3.2. As seen from the Fig. 3.2, the collector current at 10 MHz is 0.55 mA; the second harmonic at 20 MHz is 0.04 mA, for a 10 mV input signal. The simulated and the calculated values correspond well with each other.

3.2.3 Balanced doubler

This understanding of harmonics in a single SG13S SiGe HBT can now be leveraged into a doubler with two HBTs. In reality, it is difficult to generate an ideal differential signal. Therefore, analysis of frequency doubler for ideal and non-ideal cases are studied.

Ideal case

Two identical SG13S SiGe HBTs (Q_1 and Q_2) are connected in a push-push configuration with the same DC bias. Differential signals are applied at the base of the transistors, the collectors are tied together to provide a single-ended output and the emitters are connected to ground. This doubler configuration is shown in Fig. 3.3.

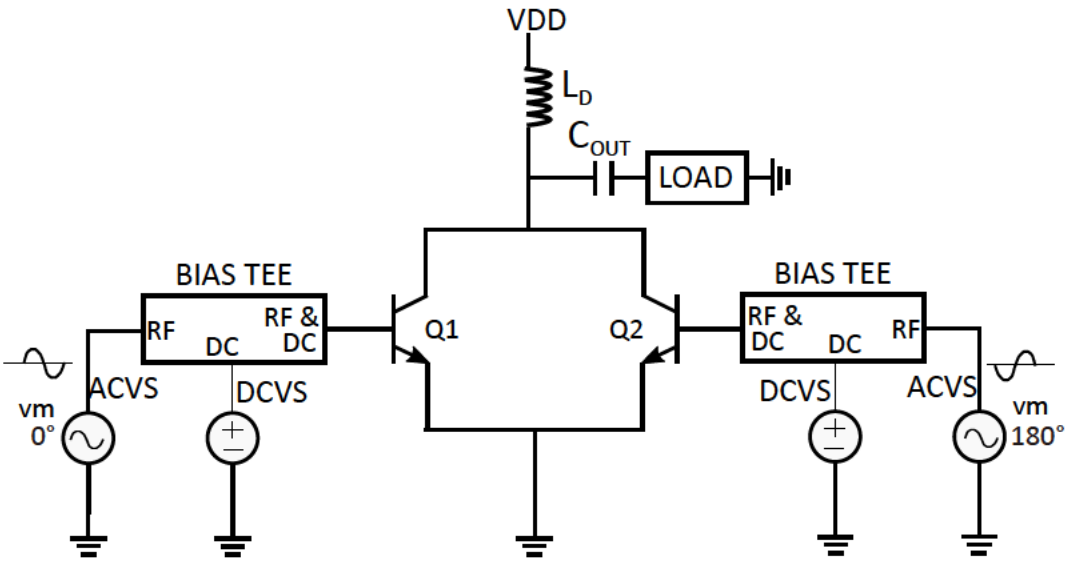


Figure 3.3: Test bench for simulating the harmonics in collector current of an ideal push-push doubler.

If the differential signals applied at the bases of the transistors are v_{be1} and v_{be2}, then the collector currents through the two transistors (bipolar transistor model) are

expressed as:

$$i_{C1} = I_S \exp(\frac{V_{BE} + v_{be1}}{\eta V_T}) \tag{3.6a}$$

$$i_{C2} = I_S \exp(\frac{V_{BE} + v_{be2}}{\eta V_T}) \tag{3.6b}$$

For an ideal case, the amplitude of differential signals are same and are 180^o out of phase with each other. If the applied differential signals are assumed to be equal to the base-emitter voltages for simplicity, then $v_{be1} = v_{in1} = V_m \cos \omega_0 t$ and $v_{be2} = v_{in2} = V_m \cos(\omega_0 t + 180^o)$. By applying the Taylor series expansion, these collector currents (bipolar transistor model) are expanded as:

$$i_{C1}(t) = I_C \left[1 + \left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right) + \frac{1}{2!}\left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right)^2 + \frac{1}{3!}\left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right)^3 + \frac{1}{4!}\left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right)^4 + ...\right] \tag{3.7a}$$

$$i_{C2}(t) = I_C \left[1 - \left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right) + \frac{1}{2!}\left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right)^2 - \frac{1}{3!}\left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right)^3 + \frac{1}{4!}\left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right)^4 + ...\right] \tag{3.7b}$$

Therefore, if the two collectors are shorted, then the odd harmonics ideally cancel each other and the total collector current (bipolar transistor model) at the output can be expressed as:

$$i_{CT}(t) = i_{C1} + i_{C2} \tag{3.8a}$$

$$i_{CT}(t) = 2I_C \left[1 + \frac{1}{2!}\left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right)^2 + \frac{1}{4!}\left(\frac{V_m \cos \omega_0 t}{\eta V_T}\right)^4 + ...\right] \tag{3.8b}$$

By Fourier transform the magnitudes of the second and the fourth harmonics are

expressed as (considering the positive half of the frequency spectrum)-

$$i_{CT}(2\omega_0) = 2I_C \left[\frac{V_m^2}{4\eta^2 V_T^2} + \frac{4V_m^4}{192\eta^4 V_T^4}\right] \delta(\omega - 2\omega_o) \tag{3.9a}$$

$$i_{CT}(4\omega_0) = 2I_C \left[\frac{V_m^4}{192\eta^4 V_T^4}\right] \delta(\omega - 4\omega_o) \tag{3.9b}$$

The DC term is neglected as it will be suppressed by the output capacitor C_{out}. For the SG13S SiGe HBTs, these equations are modified as discussed in the previous section -

$$i_{CT}(2\omega_0) = 2I_C \left[\frac{(k_2 V_m)^2}{4V_T^2} + \frac{4(k_4 V_m)^4}{192V_T^4}\right] \delta(\omega - 2\omega_o) \tag{3.10a}$$

$$i_{CT}(4\omega_0) = 2I_C \left[\frac{(k_4 V_m)^4}{192V_T^4}\right] \delta(\omega - 4\omega_o) \tag{3.10b}$$

Comparisons of the simulated and calculated magnitudes of the harmonics in the collector current for a 10 mV excitation signal is depicted in Fig. 3.4. As seen from

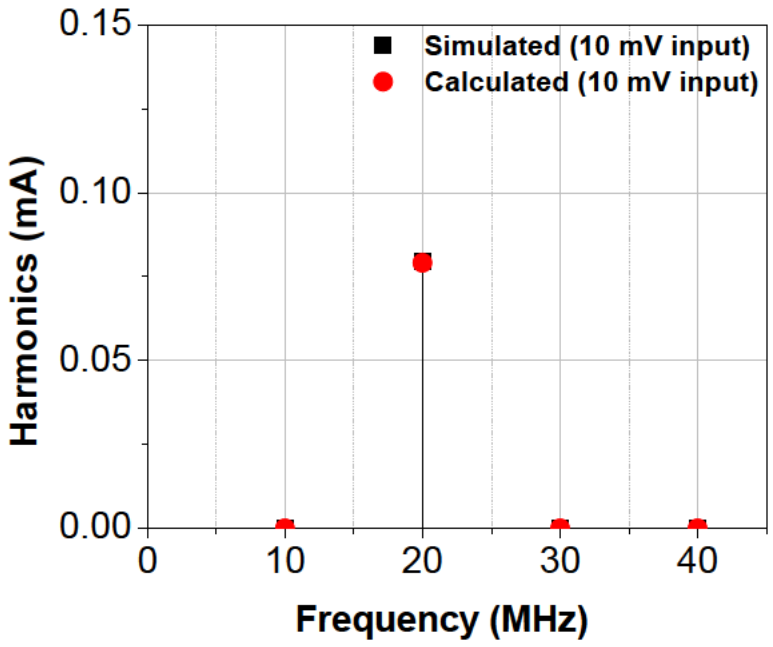


FIGURE 3.4: Comparison of the simulated (black line) and calculated (red dot) magnitudes of harmonics in collector current for the push-push configuration, at 10 MHz input.

Fig. 3.4, the second harmonic at 20 MHz is 0.08 mA for a 10 mV input signal at 10

MHz, which is double the magnitude of the second harmonic in the collector current of a single HBT as shown in Fig. 3.2.

Equation 3.10 suggests that this push-push configuration with an ideal differential input can be used as a frequency doubler with the inherent capability of odd-harmonic suppression. For a wide-band doubler, for instance the approximate octave at 7-15 GHz input, the intended output of the doubler is 14-30 GHz. But the fundamental signal at 15 GHz and the third harmonics of 7 GHz (i.e. 21 GHz) to 10 GHz (i.e. 30 GHz) fall within the desirable frequency band. It is difficult to design such a broad-band frequency doubler with good odd-harmonic suppression. As seen from equation 3.10, if the push-push configuration is used as a frequency doubler, it can eliminate the requirement of a high-order filter at the output, providing a broadband solution.

However, the differential signal excitation provided at the input of the two transistors is very crucial. In reality, it is almost impossible to generate the differential signals with perfect magnitude and phase balance. Hence it is important to study the effect of magnitude and phase mismatch in the differential signals on the collector-current harmonics.

Magnitude imbalance

For an ideal differential signal, the magnitudes of both the signals are equal and they are 180^o out of phase. Considering that a Δv magnitude difference exists between the two signals, then the two input signals can be expressed as $v_{in1} = (V_m \pm \Delta v)\cos\omega_0 t$ and $v_{in2} = V_m \cos(\omega_0 t + 180^o)$.

By applying the Taylor series expansion, the collector currents in the SG13S SiGe

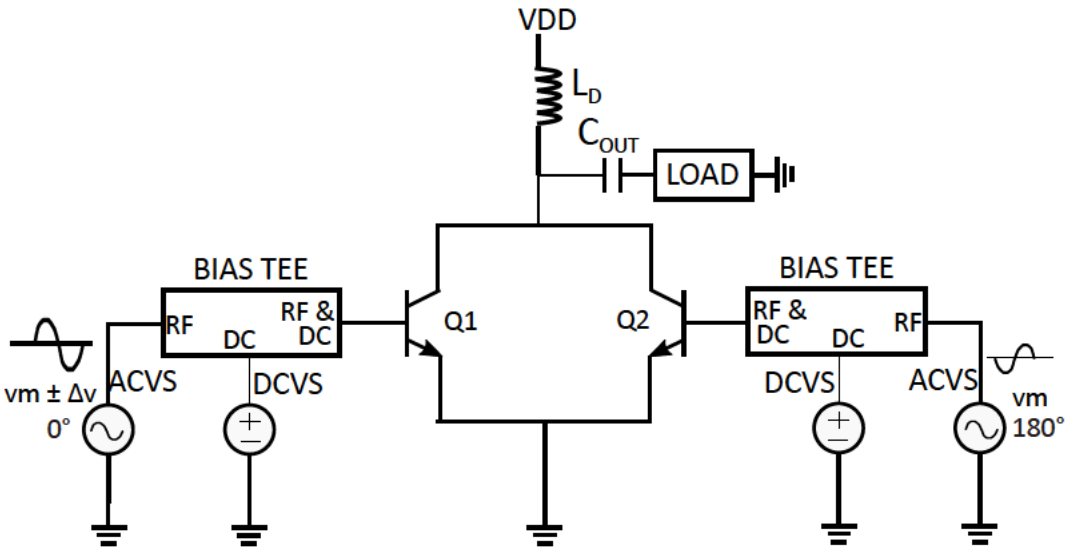


FIGURE 3.5: Test bench for simulating the harmonics in the collector current of a push-push doubler with magnitude imbalance in the input differential signals.

HBTs, Q_1 and Q_2 as shown in Fig. 3.5, are given as:

$$i_{C1}(t) = I_C \left[1 + \left(\frac{k_1 (V_m \pm \Delta v)\cos\omega_0 t}{V_T}\right) + \frac{1}{2!}\left(\frac{k_2 (V_m \pm \Delta v)\cos\omega_0 t}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{k_3 (V_m \pm \Delta v)\cos\omega_0 t}{V_T}\right)^3 + \frac{1}{4!}\left(\frac{k_4 (V_m \pm \Delta v)\cos\omega_0 t}{V_T}\right)^4 + ...\right] \tag{3.11a}$$

$$i_{C2}(t) = I_C \left[1 - \left(\frac{k_1 V_m \cos\omega_0 t}{V_T}\right) + \frac{1}{2!}\left(\frac{k_2 V_m \cos\omega_0 t}{V_T}\right)^2 - \frac{1}{3!}\left(\frac{k_3 V_m \cos\omega_0 t}{V_T}\right)^3 + \frac{1}{4!}\left(\frac{k_4 V_m \cos\omega_0 t}{V_T}\right)^4 + ...\right] \tag{3.11b}$$

where $k_1 - k_4$ are the constant values obtained from the curve-fitting as in equation 3.5. For a frequency-doubler configuration, as the collectors will be connected together, the total collector current will be given as

$$i_{CT} = i_{C1} + i_{C2} \tag{3.12}$$

As seen from equation 3.11, the odd harmonics are not cancelled completely at the output of the frequency doubler. By taking the Fourier transform, the magnitudes of

the harmonics are given as (considering the positive half of the frequency spectrum):

$$i_{CT}(\omega_0) = \left[\frac{k_1\left(V_m \pm \Delta v\right)}{V_T} + \frac{3k_3^3\left(V_m \pm \Delta v\right)^3}{24V_T^3} - \frac{k_1 V_m}{V_T} - \frac{3k_3^3 V_m^3}{24V_T^3}\right]\delta(\omega - \omega_o) \quad (3.13a)$$

$$i_{CT}(2\omega_0) = \left[\frac{k_2^2\left(V_m \pm \Delta v\right)^2}{4V_T^2} + \frac{4k_4^4\left(V_m \pm \Delta v\right)^4}{192V_T^4} + \frac{k_2^2 V_m^2}{4V_T^2} + \frac{4k_4^4 V_m^4}{192V_T^4}\right]\delta(\omega - 2\omega_o) \quad (3.13b)$$

$$i_{CT}(3\omega_0) = \left[\frac{k_3^3\left(V_m \pm \Delta v\right)^3}{24V_T^3} - \frac{k_3^3 V_m^3}{24V_T^3}\right]\delta(\omega - 3\omega_o) \quad (3.13c)$$

$$i_{CT}(4\omega_0) = \left[\frac{k_4^4\left(V_m + \Delta v\right)^4}{192V_T^4} + \frac{k_4^4 V_m^4}{192V_T^4}\right]\delta(\omega - 4\omega_o) \quad (3.13d)$$

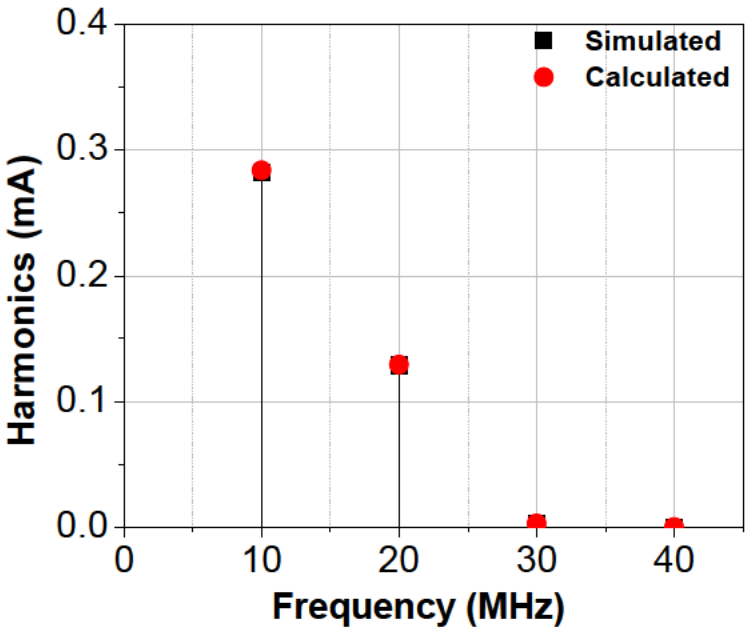


FIGURE 3.6: Comparison of the simulated (black line) and calculated (red dot) magnitudes of harmonics in collector current for magnitude mismatch of 5 mV, with 10 MHz input signal.

For 15 mV input signal at transistor Q_1 and 10 mV signal at transistor Q_2 and assuming the phase difference is 180^o, a comparison of the simulated and the calculated magnitudes of the harmonics is shown in Fig. 3.6. As seen from the plotted results, the odd harmonics are not cancelled at the output of the frequency doubler due to the magnitude imbalance in the input signals. Most importantly, the magnitude of the

collector current at the fundamental frequency is even higher than the second-harmonic component for this amplitude imbalance.

Phase imbalance

To study the effect of phase imbalance on the harmonics at the output of the frequency doubler, the input differential signals are considered to be of the same magnitude with a phase difference of ϕ. The input differential signals can be expressed as $v_{in1} = (V_m)\cos(\omega_0 t)$ and $v_{in2} = V_m \cos(\omega_0 t + 180^o \pm \phi)$ as shown in Fig. 3.7.

By applying the Taylor series expansion, the collector currents in the SG13S SiGe HBTs, Q_1 and Q_2, are given as:

$$i_{C1}(t) = I_C \left[1 + \left(\frac{k_1 V_m \cos\omega_0 t}{V_T}\right) + \frac{1}{2!}\left(\frac{k_2 V_m \cos\omega_0 t}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{k_3 V_m \cos\omega_0 t}{V_T}\right)^3 + \frac{1}{4!}\left(\frac{k_4 V_m \cos\omega_0 t}{V_T}\right)^4 + ...\right] \tag{3.14a}$$

$$i_{C2}(t) = I_C \left[1 + \left(\frac{k_1 V_m \cos(\omega_0 t + 180^o \pm \phi)}{V_T}\right) + \frac{1}{2!}\left(\frac{k_2 V_m \cos(\omega_0 t + 180^o \pm \phi)}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{k_3 V_m \cos(\omega_0 t + 180^o \pm \phi)}{V_T}\right)^3 + \frac{1}{4!}\left(\frac{k_4 V_m \cos(\omega_0 t + 180^o \pm \phi)}{V_T}\right)^4 + ...\right] \tag{3.14b}$$

The magnitudes of the harmonics at the output of the doubler can be expressed by the following equations (considering the positive half of the frequency spectrum).

$$i_{CT}(\omega_0) = I_C \left[\frac{k_1 V_m}{V_T} + \frac{3k_3^3 V_m^3}{24 V_T^3}\right] \left(\delta(\omega - \omega_0)\right)\left(1 - e^{\pm j\phi}\right) \tag{3.15a}$$

$$i_{CT}(2\omega_0) = I_C \left[\frac{k_2^2 V_m^2}{4 V_T^2} + \frac{4k_4^4 V_m^4}{192 V_T^4}\right] \left(\delta(\omega - 2\omega_0)\right)\left(1 + e^{\pm 2j\phi}\right) \tag{3.15b}$$

$$i_{CT}(3\omega_0) = I_C \left[\frac{k_3^3 V_m^3}{24 V_T^3}\right] \left(\delta(\omega - 3\omega_0)\right)\left(1 - e^{\pm 3j\phi}\right) \tag{3.15c}$$

$$i_{CT}(4\omega_0) = I_C \left[\frac{k_4^4 V_m^4}{192 V_T^4}\right] \left(\delta(\omega - 4\omega_0)\right)\left(1 + e^{\pm 4j\phi}\right) \tag{3.15d}$$

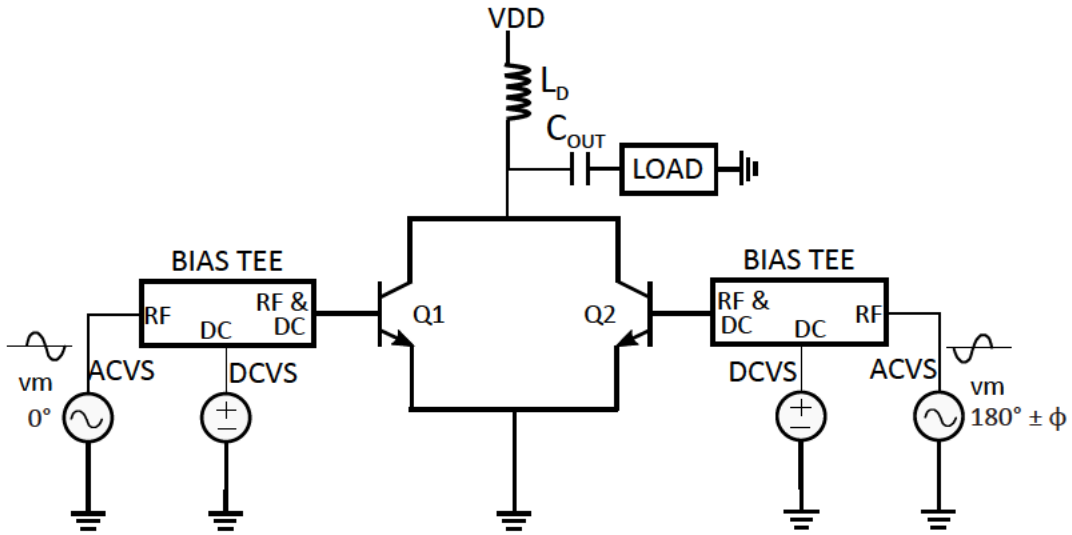


FIGURE 3.7: Test bench for simulating the harmonics in the collector current of a push-push doubler with a phase imbalance in the input differential signals.

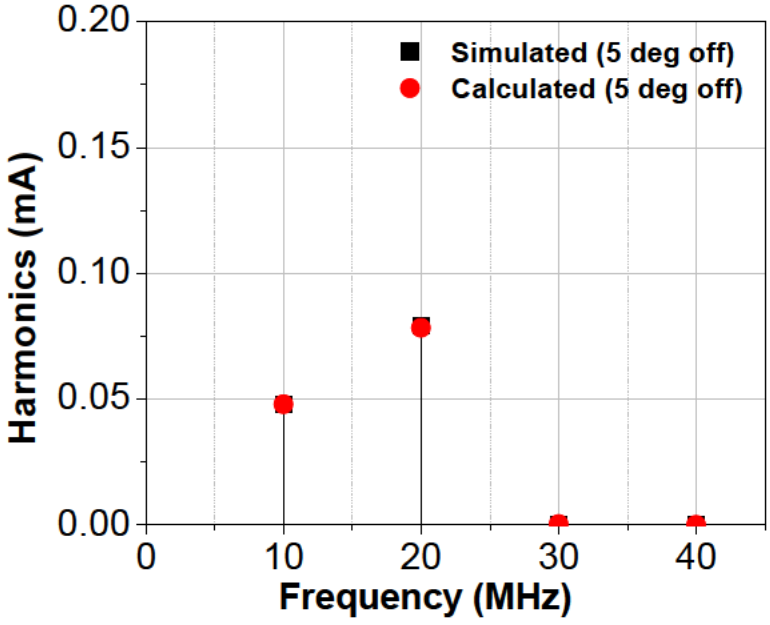


FIGURE 3.8: Comparison between the simulated (black line)and the calculated (red dot) magnitudes of the harmonics in the collector current of a push-push doubler with a phase imbalance of 5^o in the input differential signals, at 10 MHz input.

Comparisons between the simulated and calculated values for a 10 mV input and 5^o offset in the differential signals are plotted in Fig. 3.8. This result shows the effect of the phase imbalance on the output of the doubler. The odd harmonics are not

nullified completely at the output of the doubler. The magnitude of the fundamental component is close to that of the second-harmonic component.

Magnitude and Phase imbalance

In reality, all practical differential signals will have some magnitude imbalance and phase imbalance. For a push-push frequency doubler, these imbalances in the input differential signals will affect the harmonics at the output. Assuming a magnitude difference of Δv and a phase difference ϕ between the differential signals, the magnitudes of the harmonics at the output of the frequency doubler can be calculated. The input differential signals can be expressed as $v_{in1} = (V_m \pm \Delta v)\cos(\omega_0 t)$ and $v_{in2} = V_m \cos(\omega_0 t + 180^o \pm \phi)$ as shown in Fig. 3.9. The collector currents of the SG13S SiGe HBTs, Q_1 and Q_2, are given as:

$$i_{C1}(t) = I_C \left[1 + \left(\frac{k_1 (V_m \pm \Delta v)\cos\omega_0 t}{V_T}\right) + \frac{1}{2!}\left(\frac{k_2 (V_m \pm \Delta v)\cos\omega_0 t}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{k_3 (V_m \pm \Delta v)\cos\omega_0 t}{V_T}\right)^3 + \frac{1}{4!}\left(\frac{k_4 (V_m \pm \Delta v)\cos\omega_0 t}{V_T}\right)^4 + ...\right] \tag{3.16a}$$

$$i_{C2}(t) = I_C \left[1 + \left(\frac{k_1 V_m \cos(\omega_0 t + 180^o \pm \phi)}{V_T}\right) + \frac{1}{2!}\left(\frac{k_2 V_m \cos(\omega_0 t + 180^o \pm \phi)}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{k_3 V_m \cos(\omega_0 t + 180^o \pm \phi)}{V_T}\right)^3 + \frac{1}{4!}\left(\frac{k_4 V_m \cos(\omega_0 t + 180^o \pm \phi)}{V_T}\right)^4 + ...\right] \tag{3.16b}$$

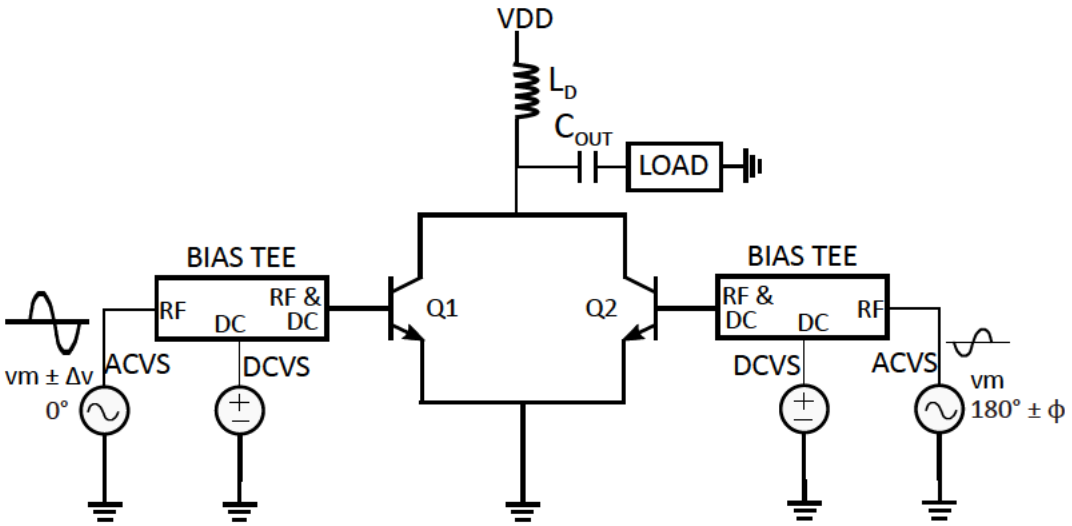


FIGURE 3.9: Test bench for simulating the harmonics in the collector current of a push-push doubler with both magnitude and phase imbalance in the input differential signals.

Therefore, the total collector current at the output can be expressed as -

$$
\begin{aligned}
i_{CT}(t) = I_C \Bigg[& \left(2 + \frac{k_2^2 \left(V_m \pm \Delta v\right)^2}{4V_T^2} + \frac{k_2^2 V_m^2}{4V_T^2} + \frac{3k_4^4 \left(V_m \pm \Delta v\right)^4}{192V_T^4} + \frac{3k_4^4 V_m^4}{192V_T^4}\right) \\
& + \left(\frac{k_1 \left(V_m \pm \Delta v\right)}{V_T} + \frac{3k_3^3 \left(V_m \pm \Delta v\right)^3}{24V_T^3}\right) \cos \omega_0 t \\
& - \left(\frac{k_1 V_m}{V_T} + \frac{3k_3^3 V_m^3}{24V_T^3}\right) \cos\left(\omega_0 t \pm \phi\right) \\
& + \left(\frac{k_2^2 \left(V_m \pm \Delta v\right)^2}{4V_T^2} + \frac{4k_4^4 \left(V_m \pm \Delta v\right)^4}{192V_T^4}\right) \cos 2\omega_0 t \\
& + \left(\frac{k_2^2 V_m^2}{4V_T^2} + \frac{4k_4^4 V_m^4}{192V_T^4}\right) \cos\left(2\omega_0 t \pm 2\phi\right) \\
& + \left(\frac{k_3^3 \left(V_m \pm \Delta v\right)^3}{24V_T^3}\right) \cos 3\omega_0 t - \left(\frac{k_3^3 V_m^3}{24V_T^3}\right) \cos\left(3\omega_0 t \pm 3\phi\right) \\
& + \left(\frac{k_4^4 \left(V_m \pm \Delta v\right)^4}{192V_T^4}\right) \cos 4\omega_0 t + \left(\frac{k_4^4 V_m^4}{192V_T^4}\right) \cos\left(4\omega_0 t \pm 4\phi\right) \Bigg]
\end{aligned}
\tag{3.17a}
$$

Therefore, by applying the Fourier Transform, the total collector current can be expressed in the frequency domain by the following set of equations.

$$i_{CT}(\omega_0) = I_C \left[\left(\frac{k_1 (V_m \pm \Delta v)}{V_T} + \frac{3k_3^3 (V_m \pm \Delta v)^3}{24V_T^3} \right) \delta(\omega - \omega_o) - \left(\frac{k_1 V_m}{V_T} + \frac{3k_3^3 V_m^3}{24V_T^3} \right) \delta(\omega - \omega_o) e^{\pm j\phi} \right] \tag{3.18a}$$

$$i_{CT}(2\omega_0) = I_C \left[\left(\frac{k_2^2 (V_m \pm \Delta v)^2}{4V_T^2} + \frac{4k_4^4 (V_m \pm \Delta v)^4}{192V_T^4} \right) \delta(\omega - 2\omega_0) + \left(\frac{k_2^2 V_m^2}{4V_T^2} + \frac{4k_4^4 V_m^4}{192V_T^4} \right) \delta(\omega - 2\omega_0) e^{\pm 2j\phi} \right] \tag{3.18b}$$

$$i_{CT}(3\omega_0) = I_C \left[\left(\frac{k_3^3 (V_m \pm \Delta v)^3}{24V_T^3} \right) \delta(\omega - 3\omega_0) - \left(\frac{k_3^3 V_m^3}{24V_T^3} \right) \delta(\omega - 3\omega_0) e^{\pm 3j\phi} \right] \tag{3.18c}$$

$$i_{CT}(4\omega_0) = I_C \left[\left(\frac{k_4^4 (V_m \pm \Delta v)^4}{192V_T^4} \right) \delta(\omega - 4\omega_0) + \left(\frac{k_4^4 V_m^4}{192V_T^4} \right) \delta(\omega - 4\omega_0) e^{\pm 4j\phi} \right] \tag{3.18d}$$

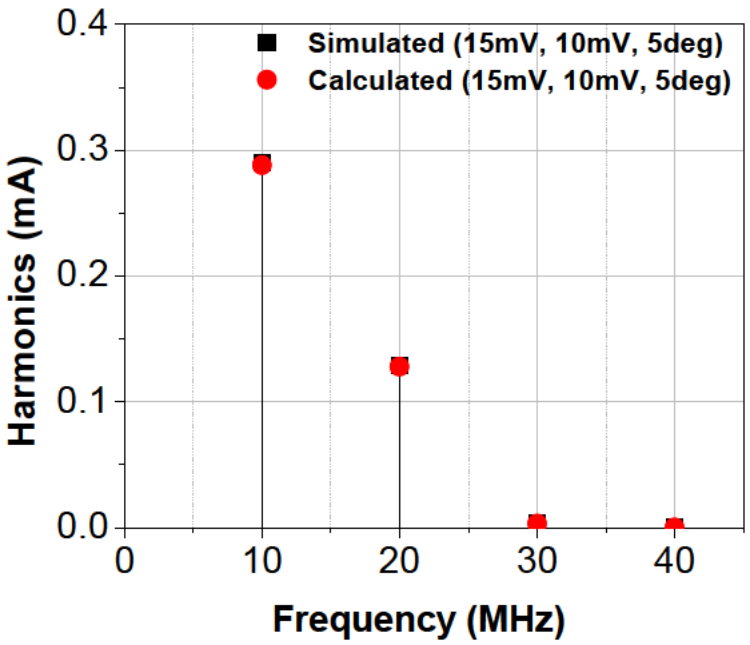


FIGURE 3.10: Comparison of the simulated (black line) and calculated (red dot) magnitudes of the harmonics in the collector current of a push-push doubler with a magnitude imbalance of 5 mV (15 mV, 10 mV) and a phase imbalance of 5^o, in the input differential signals at 10 MHz input.

The comparison between the simulated and measured results for a 5 mV offset in magnitude (15 mV, 10 mV) and 5^o offset in phase is shown in Fig. 3.10. The result clearly shows that odd harmonics exist at the output of the doubler due to the magnitude and phase imbalance in the differential signal. The magnitude of the fundamental component is even dominant over the second-harmonic current. Therefore, the intended frequency doubling is not obtained due to the magnitude and phase imbalance of the differential signals.

3.3 Harmonic generation in PP10-10 GaAs pHEMTs

The harmonics generated in a PP10-10 GaAs pHEMT is studied at the beginning. Then the analysis is extended further for a balanced frequency doubler using PP10-10 GaAs pHEMTs.

3.3.1 Simple FET model

To study the harmonics, a simple FET model is considered at first. If the transistor is biased with gate-source voltage V_{GS} and supply voltage V_{DD}, a quiescent drain current I_D will flow through the transistor. A small signal voltage v_{gs}, applied at the gate, will cause a small variation in the drain current i_d. The quiescent drain current I_D [19] and the small-signal drain current i_d [118], can be represented as:

$$I_D = I_{Dsat}\left[1 - \frac{V_G}{V_{GT}}\right]^P \tag{3.19a}$$

where I_{Dsat} is the saturation drain current, V_G is the gate bias voltage, V_{GT} is the threshold voltage.

$$i_d = g_1 v_g + g_2 v_g^2 + g_3 v_g^3 + ... \tag{3.19b}$$

and g_1, g_2, g_3 are the derivates of transconductances, v_g is the small-signal gate voltage, and

$$g_1 = \frac{dI_D}{dV_G} = -\frac{P}{V_{GT}} I_{Dsat} \left[1 - \frac{V_G}{V_{GT}}\right]^{P-1} \tag{3.19c}$$

$$g_2 = \frac{1}{2}\frac{d^2 I_D}{dV_G^2} = \frac{1}{2}\frac{P(P-1)}{V_{GT}^2} I_{Dsat} \left[1 - \frac{V_G}{V_{GT}}\right]^{P-2} \tag{3.19d}$$

$$g_3 = \frac{1}{6}\frac{d^3 I_D}{dV_G^3} = -\frac{1}{6}\frac{P(P-1)(P-2)}{V_{GT}^3} I_{Dsat} \left[1 - \frac{V_G}{V_{GT}}\right]^{P-3} \tag{3.19e}$$

Theoretically, the harmonics can be calculated by assuming a small-signal voltage $v_g < V_T$ and expanding by power coefficients. Considering the sinusoidal signal excitation to be $v_g = V_m \cos \omega_0 t$ where V_m is the small signal amplitude, the small signal drain current can be expressed as-

$$i_d = g_1 \left(V_m \cos \omega_0 t\right) + g_2 \left(V_m \cos \omega_0 t\right)^2 + g_3 \left(V_m \cos \omega_0 t\right)^3 + ... \tag{3.20a}$$

$$i_d = \frac{g_2 V_m^2}{2} + \left(g_1 V_m + \frac{3 g_3 V_m^3}{4}\right) \cos \omega_0 t + \left(\frac{g_2 V_m^2}{2}\right) \cos\left(2\omega_0 t\right) + \left(\frac{g_3 V_m^3}{4}\right) \cos\left(3\omega_0 t\right) + ... \tag{3.20b}$$

The harmonics in the drain current are simulated in AWR.

3.3.2 Foundry GaAs pHEMT model

For the purpose of comparison of the harmonics in the collector current of a SG13S SiGe HBT and the harmonics in the drain current of a PP10-10 GaAs pHEMT, the gate bias voltage, the load and the multiplication factor of the pHEMT are set in such a way that the same DC bias current flows through it as for the SG13S SiGe HBT and the same voltage gain is obtained in both cases.

At first, a single PP10-10 GaAs pHEMT (2-finger with 25 μm gate length) is considered. If the transistor is biased with gate-source voltage V_{GS} and supply voltage V_{DD}, a quiescent drain current I_D will flow through the transistor. A small signal

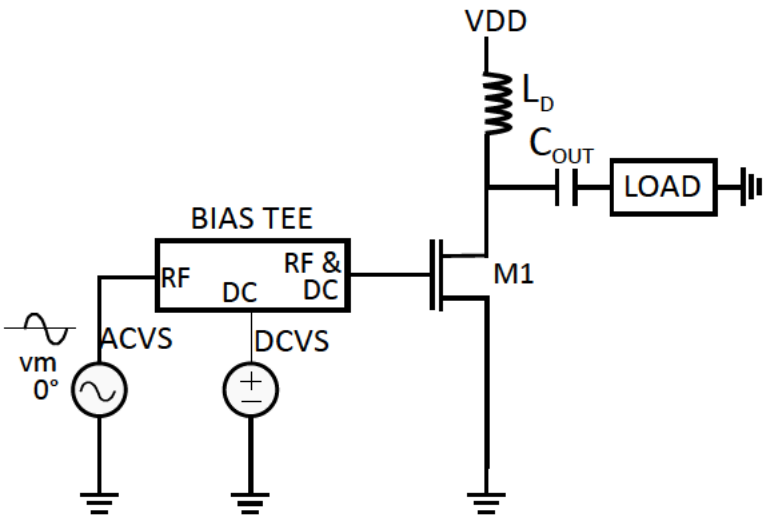


FIGURE 3.11: Test bench for simulating the harmonics in the drain current of a PP10-10 GaAs pHEMT.

voltage v_{gs}, applied at the gate, will cause a small variation in the drain current i_d. The quiescent drain current I_D and the small-signal drain current i_d, do not match with the equations shown in the previous section.

The model of a PP10-10 GaAs pHEMT is very complicated. Different models of pHEMTs can be found in the literature. Accurate modelling of pHEMTs is out of the scope of this work. Therefore, following the same analysis as for the SG13S SiGe HBT, the values of the derivatives of transconductances g_1, g_2, g_3, for a PP10-10 GaAs pHEMT are derived by curve fitting from AWR simulation results and the calculated drain current equations (using MATLAB). For a particular bias of the transistor, these parameter values are then kept fixed for the rest of the analysis.

To study the harmonics of a pHEMT, a single transistor from the PP10-10 library is considered in AWR. The testbench is shown in Fig. 3.11. The transistor is biased at V_{GS} = -0.65 V (selected to match the current condition of a single SG13S SiGe HBT for comparison purpose) and supply voltage V_{DD} = 4 V (limited by BV_{DS}). The quiescent drain current I_D = 1.65 mA flows through the transistor. A small signal voltage v_{gs} is applied through the bias tee. This causes a small variation in the drain current i_d. The harmonics in the drain current are simulated by using a probe at the drain. The

modified equation of the drain current is expressed as

$$i_d = \frac{g_2 V_m^2}{2} + \left(g_1 V_m + \frac{3 g_3 V_m^3}{4}\right) \cos \omega_0 t + \left(\frac{g_2 V_m^2}{2}\right) \cos\left(2\omega_0 t\right) + \left(\frac{g_3 V_m^3}{4}\right) \cos\left(3\omega_0 t\right) + ... \tag{3.21a}$$

where, g_1, g_2, g_3 are the derivatives of transconductances for a PP10-10 GaAs pHEMT, derived using correction factors.

The comparison of the simulated and the calculated values (using MATLAB) of the magnitude of the harmonics in the drain current, for v_{gs} of 10 mV at 10 MHz, is shown in Fig. 3.12.

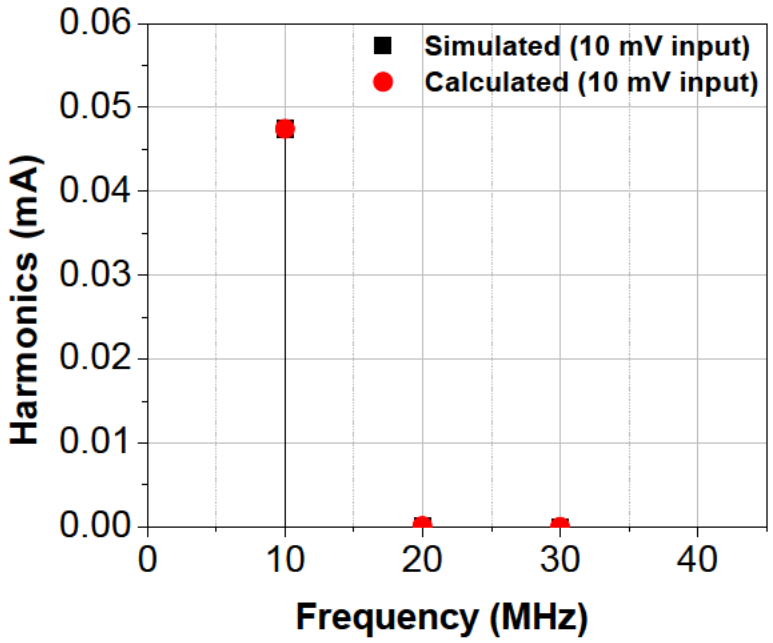


FIGURE 3.12: Comparison of the simulated (black line) and calculated (red dot) magnitudes of harmonics in the drain current of a pHEMT in PP10-10 process, for a 10 MHz input signal.

The magnitudes of the fundamental component is 0.047 mA; and of the second harmonic is 0.085 μA, for a 10 mV input signal. Comparing equations 3.5 and 3.20, it can be seen that the harmonics in a PP10-10 GaAs pHEMT are significantly lower

than those of a SG13S SiGe HBT at the same frequency, for the same bias currents (I_C and I_D) and the same voltage gain. This bias condition is therefore not appropriate for the PP10-10 GaAs pHEMT to generate the harmonics, but is selected for the purpose of comparison of the harmonics in a SG13S SiGe HBT and a PP10-10 GaAs pHEMT under the same conditions.

3.3.3 Balanced doubler

This understanding of harmonics in a single PP10-10 GaAs pHEMT can now be leveraged into a doubler with two pHEMTs. In reality, it is difficult to generate an ideal differential signal. Therefore, analysis of frequency doubler for ideal and non-ideal cases are studied.

Ideal case

A frequency doubler is designed using the PP10-10 GaAs pHEMTs. Following the same approach as for the push-push doubler using the SG13S SiGe HBTs, two identical PP10-10 GaAs pHEMTs (M_1 and M_2) are connected in a push-push configuration. The same DC bias is applied to both transistors. An ideal differential signal is applied at the gate of the transistors, the drains are tied together to provide a single-ended output and the sources are connected to ground. This doubler configuration using pHEMTs is shown in Fig. 3.13.

For an ideal case, the amplitude of differential signals are same and are 180^o out of phase with each other. If the applied differential signals at the gates of the transistors are v_{gs1} and v_{gs2}, then $v_{gs1} = V_m \cos\omega_0 t$ and $v_{gs2} = V_m \cos(\omega_0 t + 180^o)$. The drain currents through the two transistors are expressed as:

$$i_{d1}(t) = g_1 \left(V_m \cos\omega_0 t\right) + g_2 \left(V_m \cos\omega_0 t\right)^2 + g_3 \left(V_m \cos\omega_0 t\right)^3 + ... \tag{3.22a}$$

$$i_{d2}(t) = g_1 V_m \cos\left(\omega_0 t + 180^o\right) + g_2 V_m^2 \cos^2\left(\omega_0 t + 180^o\right) + g_3 V_m^3 \cos^3\left(\omega_0 t + 180^o\right) + ... \tag{3.22b}$$

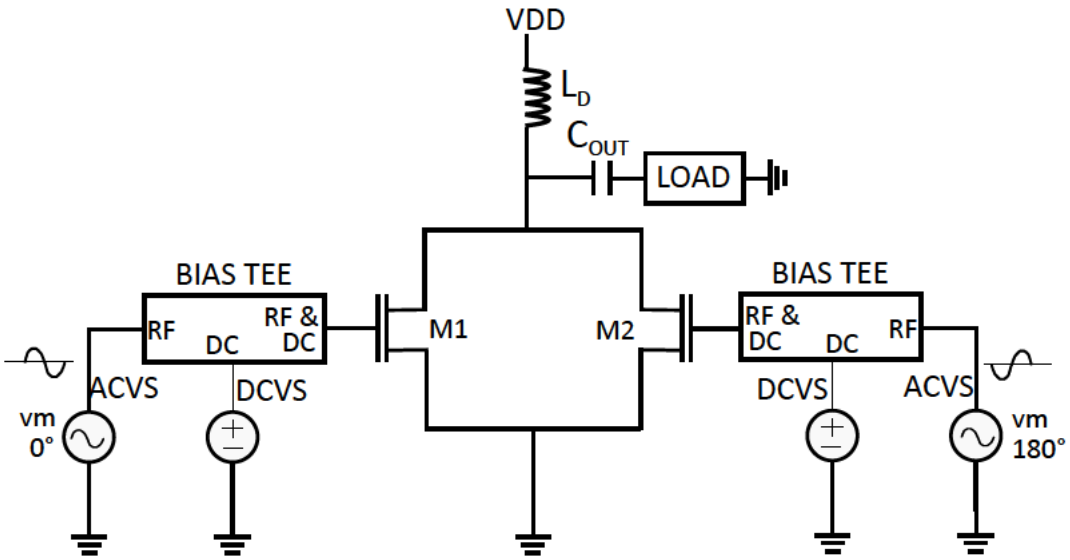


FIGURE 3.13: Test bench for simulating the harmonics in the drain current of a push-push doubler using pHEMTs in PP10-10 process.

Therefore, $i_{d2}(\mathrm{t})$ can be written as

$$i_{d2}(t) = -g_1 V_m \cos(\omega_0 t) + g_2 V_m^2 \cos(\omega_0 t)^2 - g_3 V_m^3 \cos(\omega_0 t)^3 + \ldots \tag{3.22c}$$

and therefore, by adding $i_{d1}(\mathrm{t})$ and $i_{d2}(\mathrm{t})$, the total drain current $i_{dT}(\mathrm{t})$ is

$$i_{dT}(t) = i_{d1} + i_{d2} \tag{3.22d}$$

$$i_{dT}(t) = 2\left[\frac{g_2 V_m^2}{2} + \frac{g_2 V_m^2}{2}(\cos 2\omega_0 t) + \ldots\right] \tag{3.22e}$$

Theoretically, the total drain current will contain only the even harmonics if a perfect differential signal is applied to the transistors in the push-push configuration. Therefore, this topology can be utilised for a wideband frequency doubler using pHEMTs, as the odd harmonics are cancelled inherently. This concept is also verified from the AWR simulation. Comparisons between the calculated and measured magnitudes of the harmonics are shown in Fig. 3.14.

The magnitude of the second harmonic is 0.17 μA for a 10 mV input signal.

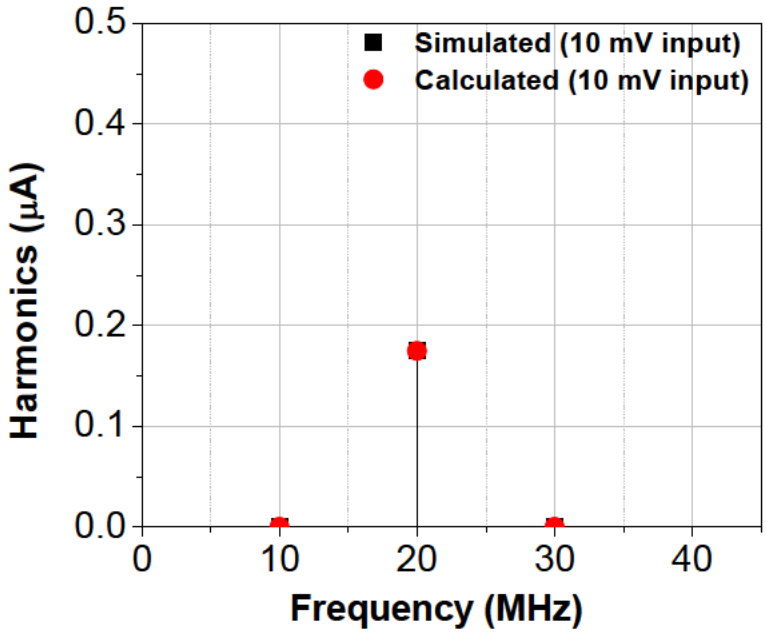


FIGURE 3.14: Comparison of the simulated (black line) and calculated (red dot) magnitudes of the harmonics in the drain current of the push-push doubler implemented using PP10-10 GaAs pHEMTs, for 10 MHz input differential signals.

Magnitude imbalance

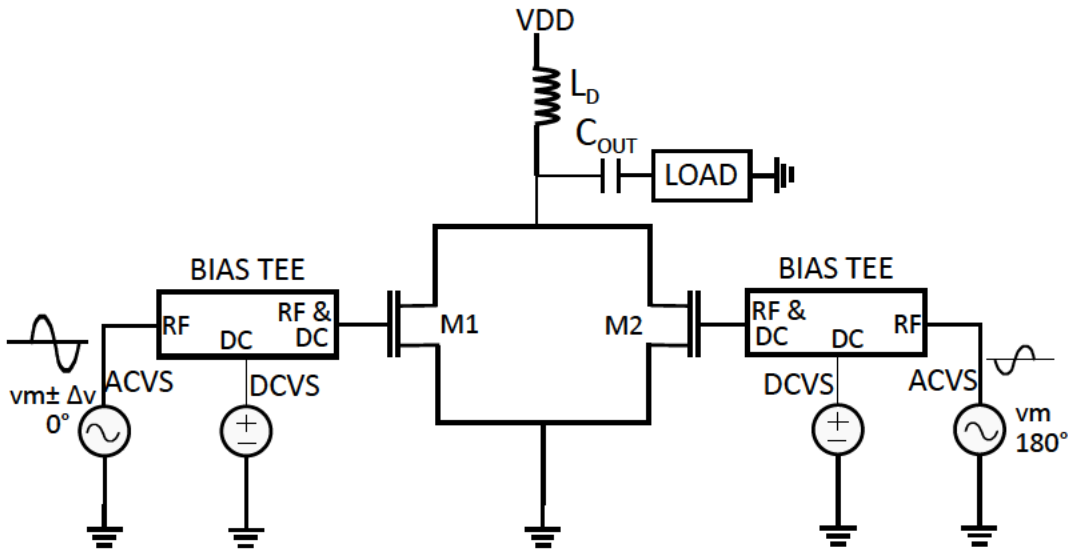


FIGURE 3.15: Test bench for simulating the harmonics in drain current of the push-push doubler with magnitude imbalance in the input differential signal.

As discussed previously, it is difficult to realise an ideal differential signal in practice. The effect of a magnitude imbalance on the current harmonics can be studied by following the same analysis as for the SG13S SiGe HBT. Assuming magnitude difference Δv exists between the input differential signals, these two input signals can be expressed as $v_{gs1} = (V_m + \Delta v)\cos\omega_0 t$ and $v_{gs2} = V_m \cos(\omega_0 t + 180^o)$. The testbench for the AWR simulation is shown in Fig. 3.15.

The drain currents in PP10-10 GaAs pHEMTs can be expressed as:

$$i_{d1}(t) = g_1\left[(V_m \pm \Delta v)\cos\omega_0 t\right] + g_2\left[(V_m \pm \Delta v)\cos\omega_0 t\right]^2 + g_3\left[(V_m \pm \Delta v)\cos\omega_0 t\right]^3 + ... \tag{3.23a}$$

$$i_{d2}(t) = -g_1 V_m \cos(\omega_0 t) + g_2 V_m^2 \cos^2(\omega_0 t) - g_3 V_m^3 \cos^3(\omega_0 t) + ... \tag{3.23b}$$

Therefore, by adding i_{d1}(t) and i_{d2}(t), the total drain current i_{dT}(t)can be written as

$$\begin{aligned} i_{dT}(t) = \Bigg[& \left(\frac{g_2 V_m^2}{2} + \frac{g_2(V_m \pm \Delta v)^2}{2}\right) \\ & + \left(g_1(V_m \pm \Delta v) + \frac{3g_3(V_m \pm \Delta v)^3}{4} - g_1 V_m - \frac{3g_3 V_m^3}{4}\right) cos\omega_0 t \\ & + \left(\frac{g_2(V_m \pm \Delta v)^2}{2} - \frac{g_2 V_m^2}{2}\right) cos2\omega_0 t + \left(\frac{g_3(V_m \pm \Delta v)^3}{4} - \frac{g_3 V_m^3}{4}\right) cos3\omega_0 t + ... \Bigg] \end{aligned} \tag{3.23c}$$

Comparisons between the calculated and the measured magnitudes of the harmonics are shown in Fig. 3.16. This result shows that the odd harmonics are dominant at the output of the doubler. The magnitude of the fundamental component is 25 μA while the magnitude of the second harmonic is 0.54 μA only.

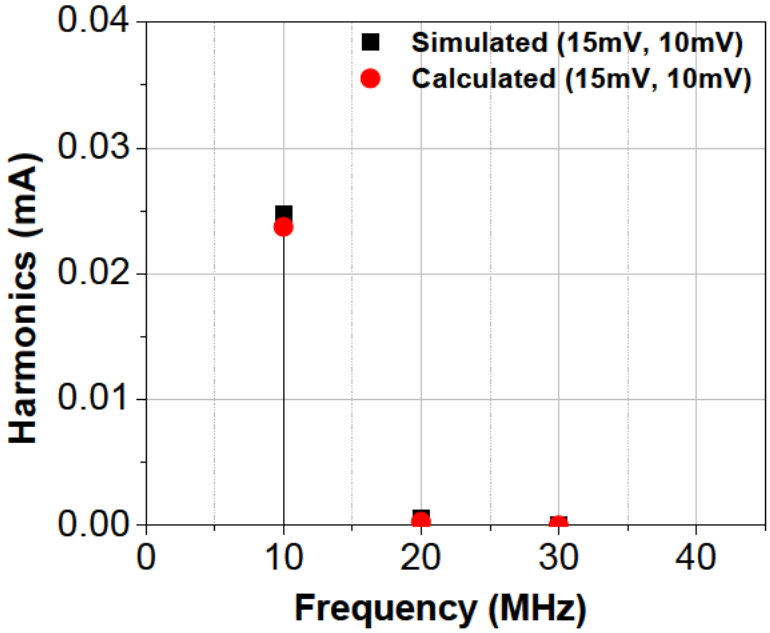


FIGURE 3.16: Comparison of the simulated (black line) and calculated (red dot) magnitudes of harmonics in drain current of the doubler with a magnitude mismatch of 5 mV in the input differential signals, at 10 MHz.

Phase imbalance

To study the effect of the phase imbalance on the harmonics at the output of the frequency doubler, the input differential signals are assumed to be of the same magnitude, but with phase difference ϕ. The input differential signal is expressed as $v_{gs1} = (V_m)\cos(\omega_0 t)$ and $v_{gs2} = V_m \cos(\omega_0 t + 180^o \pm \phi)$. The drain current equations in PP10-10 GaAs pHEMTs are shown below:

$$i_{d1}(t) = g_1 (V_m \cos\omega_0 t) + g_2 (V_m \cos\omega_0 t)^2 + g_3 (V_m \cos\omega_0 t)^3 + ... \tag{3.24a}$$

$$i_{d2}(t) = [g_1 [V_m \cos(\omega_0 t + 180^o \pm \phi)] + g_2 [V_m \cos(\omega_0 t + 180^o \pm \phi)]^2 + g_3 [V_m \cos(\omega_0 t + 180^o \pm \phi)]^3 + ...] \tag{3.24b}$$

Therefore, $i_{d2}(\mathrm{t})$ can be rearranged as

$$i_{d2}(t) = -g_1\left[V_m\cos\left(\omega_0 t \pm \phi\right)\right] + g_2\left[V_m\cos\left(\omega_0 t \pm \phi\right)\right]^2 - g_3\left[V_m\cos\left(\omega_0 t \pm \phi\right)\right]^3 + ... \tag{3.24c}$$

and by adding $i_{d1}(\mathrm{t})$ and $i_{d2}(\mathrm{t})$, the total drain current $i_{dT}(\mathrm{t})$can be written as

$$\begin{aligned} i_{dT}(t) = \Bigg[& 2\frac{g_2 V_m^2}{2} + \left(g_1 V_m + \frac{3g_3 V_m^3}{4}\right)\left(\cos\omega_0 t - \cos\left(\omega_0 t \pm \phi\right)\right) \\ & + \left(\frac{g_2 V_m^2}{2}\right)\left(\cos 2\omega_0 t + \cos\left(2\omega_0 t \pm 2\phi\right)\right) \\ & + \left(\frac{g_3 V_m^3}{4}\right)\left(\cos 3\omega_0 t - \cos\left(3\omega_0 t \pm 3\phi\right)\right)\Bigg] \end{aligned} \tag{3.24d}$$

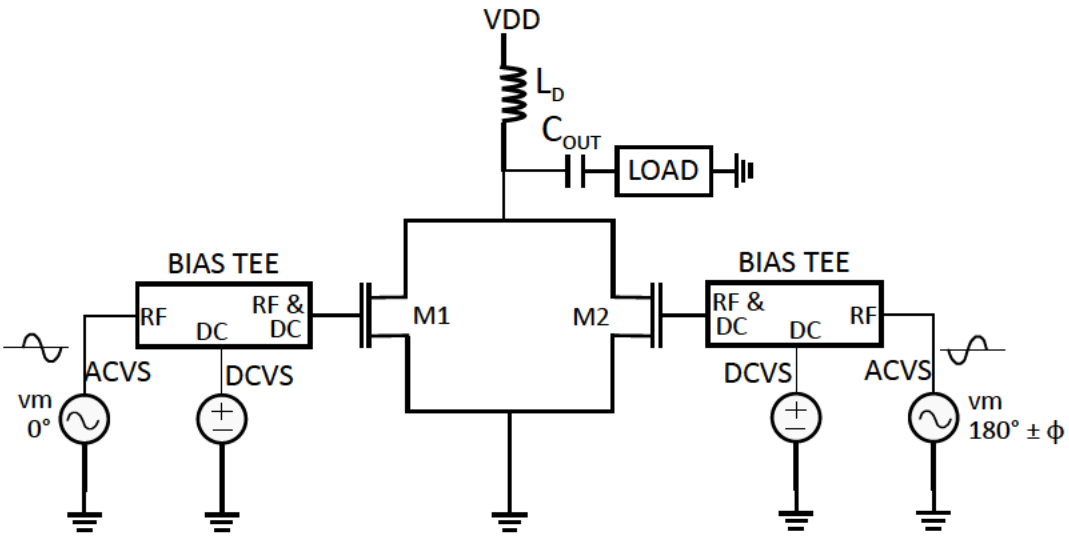


Figure 3.17: Test bench for simulating the harmonics in the drain current of the push-push doubler with phase imbalance in the input differential signals.

The testbench for this simulation is shown in Fig. 3.17. Comparisons between the calculated and measured magnitudes of the harmonics are shown in Fig. 3.18. It can be seen from the plotted result that the magnitude for the fundamental component is higher than for the second-harmonic component at the output of the doubler.

It is interesting to note that the fundamental component is stronger than the second harmonic for the pHEMT for a phase difference of 5^o. But for the HBT, although the

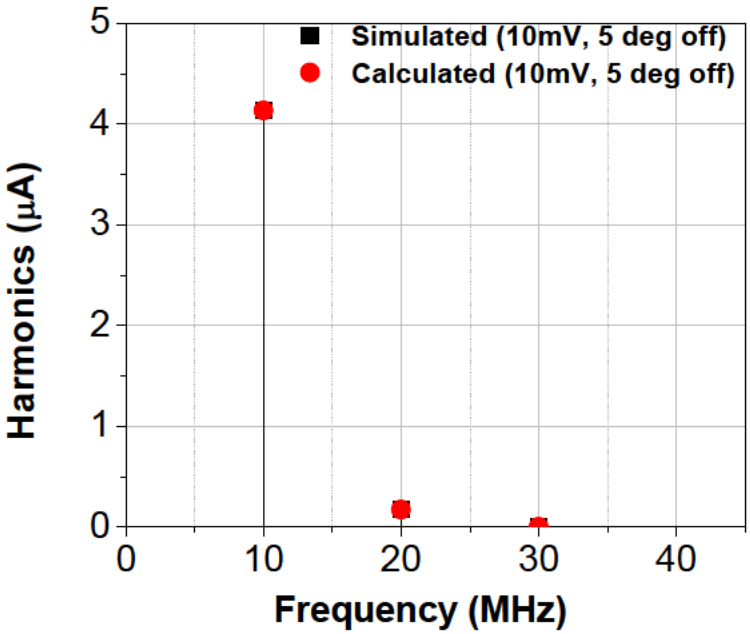


FIGURE 3.18: Comparison between the simulated (black line) and the calculated (red dot) magnitudes of the harmonics in the drain current of the push-push doubler with a phase imbalance of 5^o in the input differential signals, at 10 MHz.

fundamental component was not cancelled at the output for 5^o phase difference, it was lower than the second-harmonic magnitude. The bias drain current for the pHEMT was set to be equal to that of the collector current of the HBT, for the purpose of comparison. In reality, this bias condition is not suitable for the pHEMT doubler.

Magnitude and Phase imbalance

To model a practical differential signal available in real life, both magnitude and phase imbalances must be considered. For a differential-input frequency doubler these imbalances in the input differential signals will affect the harmonics at the output. Assuming a magnitude difference Δv and a phase difference ϕ between the input signals, the magnitudes of the harmonics at the output of the frequency doubler can be calculated. The input differential signals can be expressed as $v_{gs1} = (V_m \pm \Delta v)\cos(\omega_o t)$ and $v_{gs2} = V_m \cos(\omega_o t + 180^o \pm \phi)$ as shown in Fig. 3.19. The drain currents of the

transistors M_1 and M_2, are given as:

$$i_{d1}(t) = g_1\left[(V_m \pm \Delta v)\cos\omega_0 t\right] + g_2\left[(V_m \pm \Delta v)\cos\omega_0 t\right]^2 + g_3\left[(V_m \pm \Delta v)\cos\omega_0 t\right]^3 + ... \tag{3.25a}$$

$$i_{d2}(t) = \left[g_1\left[V_m\cos\left(\omega_0 t + 180^o \pm \phi\right)\right] + g_2\left[V_m\cos\left(\omega_0 t + 180^o \pm \phi\right)\right]^2 + g_3\left[V_m\cos\left(\omega_0 t + 180^o \pm \phi\right)\right]^3 + ...\right] \tag{3.25b}$$

Therefore, by adding i_{d1}(t) and i_{d2}(t), the total drain current i_{dT}(t)can be written as

$$\begin{aligned} i_{dT}(t) = \Bigg[& \left(\frac{g_2\left(V_m \pm \Delta v\right)^2}{2} + \frac{g_2 V_m^2}{2}\right) \\ & + \left(g_1\left(V_m \pm \Delta v\right) + \frac{3g_3\left(V_m \pm \Delta v\right)^3}{4}\right)\cos\omega_0 t - \left(g_1 V_m + \frac{3g_3 V_m^3}{4}\right)\cos\left(\omega_0 t \pm \phi\right) \\ & + \left(\frac{g_2\left(V_m \pm \Delta v\right)^2}{2}\right)\cos\left(2\omega_0 t\right) + \left(\frac{g_2 V_m^2}{2}\right)\cos\left(2\omega_0 t \pm 2\phi\right) \\ & + \left(\frac{g_3\left(V_m \pm \Delta v\right)^3}{4}\right)\cos 3\omega_0 t - \left(\frac{g_3 V_m^3}{4}\right)\cos\left(3\omega_0 t \pm 3\phi\right)\Bigg] \end{aligned} \tag{3.25c}$$

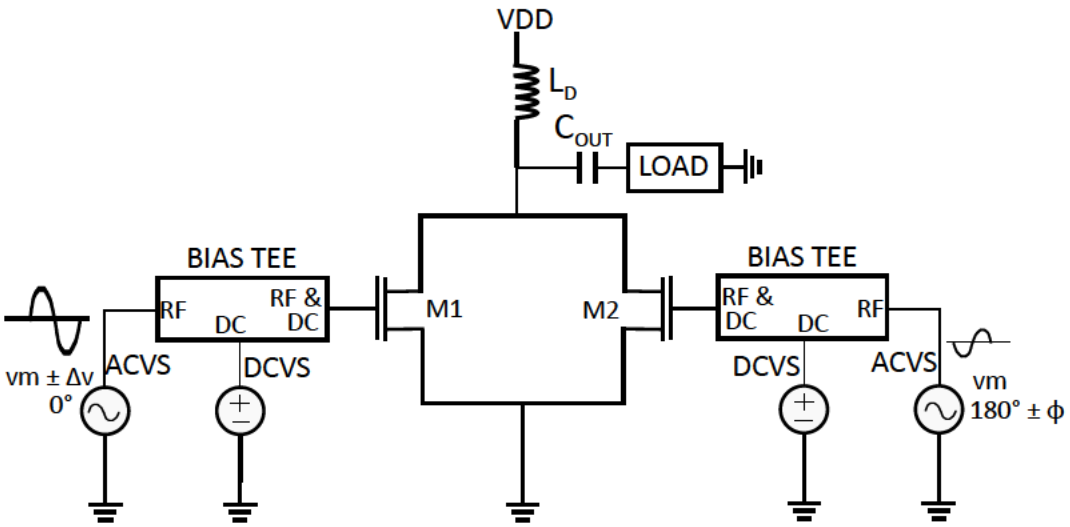


FIGURE 3.19: Test bench for simulating the harmonics in the drain current of the push-push doubler with both magnitude and phase imbalance in the input differential signals.

The testbench for this simulation is shown in Fig. 3.19. Comparisons between the

calculated and measured magnitudes of the harmonics are shown in Fig. 3.20. It can be seen from the plotted results that the odd harmonics remain at the output of the doubler.

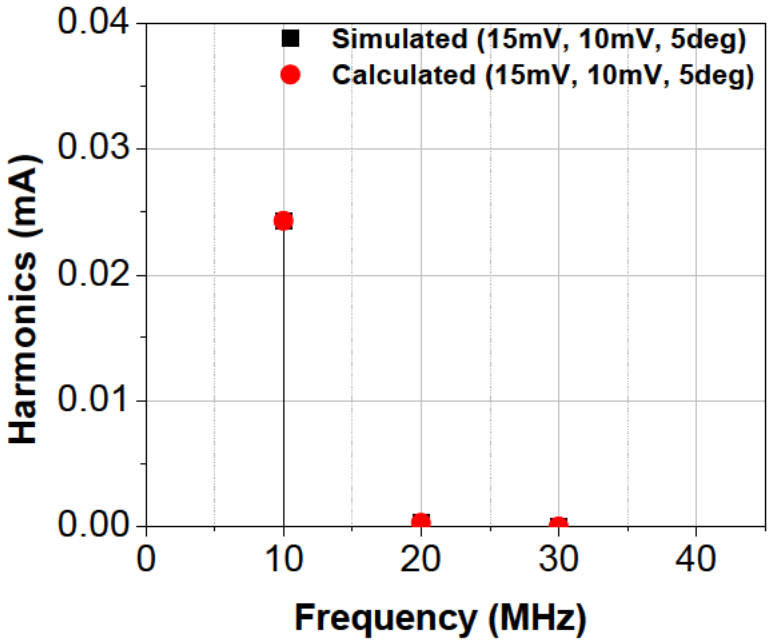


FIGURE 3.20: Comparison of the simulated and calculated harmonics in the drain current of a push-push doubler with a magnitude imbalance of 5 mV (15 mV, 10 mV) and phase imbalance of 5^o, in the input differential signals, at 10 MHz.

The simulated results match well with the calculated harmonics in the collector current for the SG13S SiGe HBT and the drain current for the PP10-10 GaAs pHEMT. From these simple equations, it can be inferred that the imbalance in the differential signals can be detrimental for the odd-harmonic rejection in a frequency doubler with differential inputs. The next chapter will focus on the design of the passive balun in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process to generate the differential signals with good balance.

3.4 Summary

In a system design such as a wireless transmitter or receiver, the overall linearity of the system is affected by the non-idealities from the active devices. To understand this aspect, a balanced frequency doubler circuit is considered as an archetype of a non-linear circuit. In this chapter, the harmonics for frequency doublers implemented using SG13S SiGe HBTs and PP10-10 GaAs pHEMTs are studied. For the purpose of comparison of the harmonics in the collector current of a SG13S SiGe HBT and the harmonics in the drain current of a PP10-10 GaAs pHEMT, the gate bias voltage, the load and the multiplication factor of the pHEMT are set in such a way that the same DC bias current flows through it as for the SG13S SiGe HBT and the same voltage gain is obtained in both cases. Under this condition, it is found that the harmonics are stronger in the HBT than in the pHEMT. This is because the current in an HBT is exponentially related to the input voltage whereas in a pHEMT the current is related to the input voltage by the power series. Other parameters such as the power of the input signal will affect the harmonic generation.

Theoretically for a balanced frequency doubler topology, if the transistors are matched, all the odd harmonics are rejected at the output of the doubler. But it has been found that for a balanced architecture, the odd-harmonic rejection is sensitive to the balance in the differential signals for both the SG13S SiGe HBT and the PP10-10 GaAs pHEMT process. Any imbalance in the input differential signals will affect the ability of the balanced doubler to reject the odd harmonics at the output.

Therefore, for a balanced frequency doubler, the effect of the imbalance in the differential signals on the harmonics at the output of the doubler is analysed in this chapter. It is inferred from the analysis that the balance in the differential signals is critical for the odd-harmonic rejection of the balanced frequency doubler, although theoretically the topology itself can reject all the odd harmonics at the output. This makes the balun design important in both the processes, which is the topic of discussion in the next chapter.

4

Balun design and implementation

4.1 Introduction

Frequency doublers are often used as a unit cell in a chain of frequency multipliers. The previous chapter discussed the frequency doubler in an analytical study for both the PP10-10 GaAs pHEMT process and the SG13S SiGe HBT process. Balanced frequency doublers are preferred due to their inherent capability of rejecting odd harmonics without any bandpass filter. However, in reality the odd-harmonic rejection capability of a balanced frequency doubler depends on the symmetry of the layout, the match between the transistors and most importantly on the amplitude and phase imbalance of the differential signals. Therefore, the design of the balun is a critical factor to achieve good odd-harmonic suppression for a frequency doubler. For the performance requirement of a frequency doubler, the objective is to design a compact balun with good

amplitude and phase balance over a broad band. As stated in Chapter 2, a passive balun is selected for the balanced frequency-doubler design. From the literature review in Chapter 2, Marchand balun and transformer balun are identified as the potential balun structures. At first the two types of baluns are briefly analysed and the choice is made. This chapter deals with the analysis, design and implementation of a passive balun in both the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process.

4.2 Design considerations

Baluns can be broadly classified into two main types: Passive and Active (as discussed in Section 2.6). Active baluns can provide a conversion gain and occupy a small area. Passive baluns are known to occupy a large space but they are linear, unlike active baluns. The comparisons between active and passive baluns are summarised in Table 4.1.

TABLE 4.1: Summary of key physical properties of an active and a passive balun.

Parameter	**Active balun**	**Passive balun**
Linearity requirement	Required	NA
Balance performance	Moderate	Good
Bandwidth	Narrow	Moderate to large
Conversion gain/loss	Gain	Loss
DC power consumption	Required	NA
Area	Moderate	Large
Directionality	Unidirectional	Bi-directional

The different design parameters for a balun can be explained by Fig. 4.1. Sometimes a tradeoff exists between some of these parameters. For example it is difficult to achieve good amplitude and phase balance over a wide band. Therefore, these parameters can also be used to assess the performance of a balun such as imbalance (amplitude and phase), bandwidth, area, DC power consumption, conversion gain/loss.

Ideally, for a balun the two signals at the output port should be equal in magnitude and 180^o out of phase at all frequencies. In reality, the magnitudes of the differential signals are different which is quantified as an amplitude or magnitude imbalance.

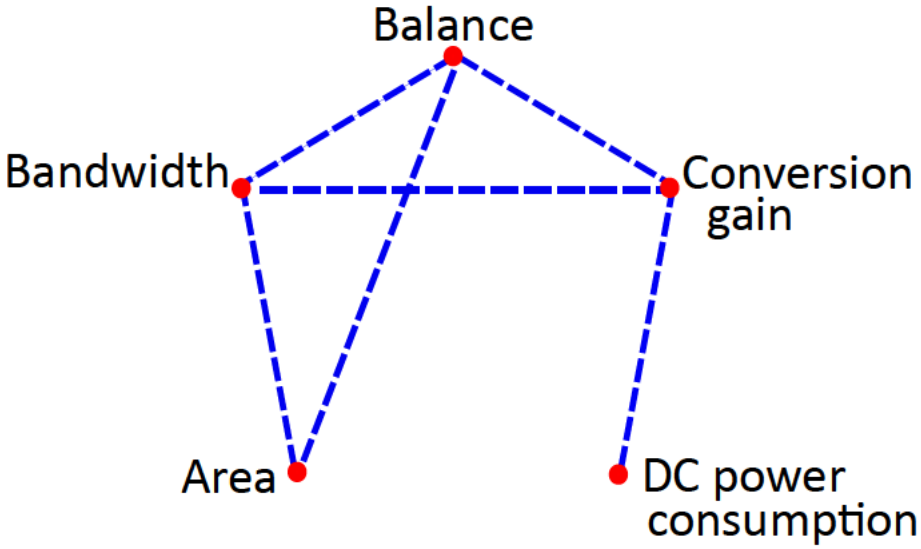


FIGURE 4.1: Tradeoff between the different key parameters of a balun.

Similarly the phase difference varies from the ideal 180^o value and is represented by phase imbalance. The amplitude and the phase imbalances can be represented by the following equations:

$$\text{Amplitude Imbalance, } \Delta v = 20 \times \log_{10} \frac{S_{31}}{S_{21}} \tag{4.1a}$$

$$\text{Phase Imbalance, } \phi = \angle S_{21} - \angle S_{31} - 180^o \tag{4.1b}$$

where S_{21} and S_{31} are the transmission S-parameters from the unbalanced port to the balanced ports of the balun.

As the linearity and good balance of the balun are of primary concern for balanced frequency-doubler design, passive balun design is selected.

4.3 Passive baluns

As stated in Chapter 2, among the passive baluns the planar Marchand balun is commonly used in MMIC designs for its wideband operation [96]. As the size of the balun is proportional to the wavelength, it occupies a large area at low frequencies, which makes it unsuitable for low-frequency applications. On the other hand, transformer baluns are not dependent on wavelength [119]. Therefore these baluns are more compact than

Marchand baluns, making them more suitable for low-frequency operation.

Transformers have been widely used in RF electronic circuits for a wide variety of applications such as impedance matching for maximum power transfer, voltage and current step-up or step-down, isolation of DC between circuits [120]. These transformers can be utilised for balun design. In the recent past, much research work was dedicated to integrating an on-chip transformer in silicon technologies. The design of a microstrip directional coupler by Shibata [121] was a step forward to realise on-chip transformers. Later, several investigations on monolithic transformers were reported by Podell (in GaAs IC technology) [122, 123], Frlan [124], Boulouard and Le Rouzic [125] as summarised in [99]. More recently research on monolithic transformer baluns was reported in [99, 100, 126, 127].

A comparison of the Marchand and transformer balun analysis is presented in the next section, to investigate the suitability of using one of the baluns for frequency-doubler design.

4.3.1 Analysis of Marchand balun

The block diagram of a typical Marchand balun is shown in Fig. 4.2.

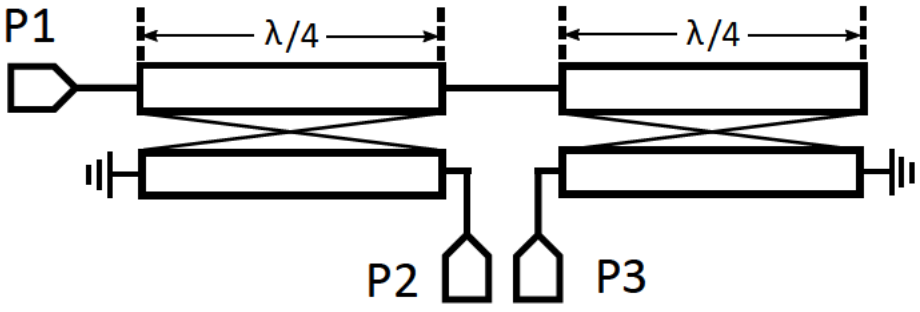


FIGURE 4.2: Marchand balun configuration with two identical coupled lines.

If the termination impedances of the asymmetric two-conductor coupled lines are considered to be equal to the characteristic impedances of the individual uncoupled lines, the propagation constants of the even and odd modes can be assumed to be equal [128]. Based on this assumption, [128] showed that the four-port S-parameters

of the asymmetrical two-conductor coupled lines, with electrical length of θ, is given by -

$$[\mathrm{S}]_{\mathrm{coupler}} = \begin{pmatrix} 0 & x/z & y/z & 0 \\ x/z & 0 & 0 & y/z \\ y/z & 0 & 0 & x/z \\ 0 & y/z & x/z & 0 \end{pmatrix} \tag{4.2}$$

where $x = \sqrt{1-k^2}$, $y = jk\sin\theta$, $z = \sqrt{1-k^2}\cos\theta + j\sin\theta$ and k is the coupling coefficient.

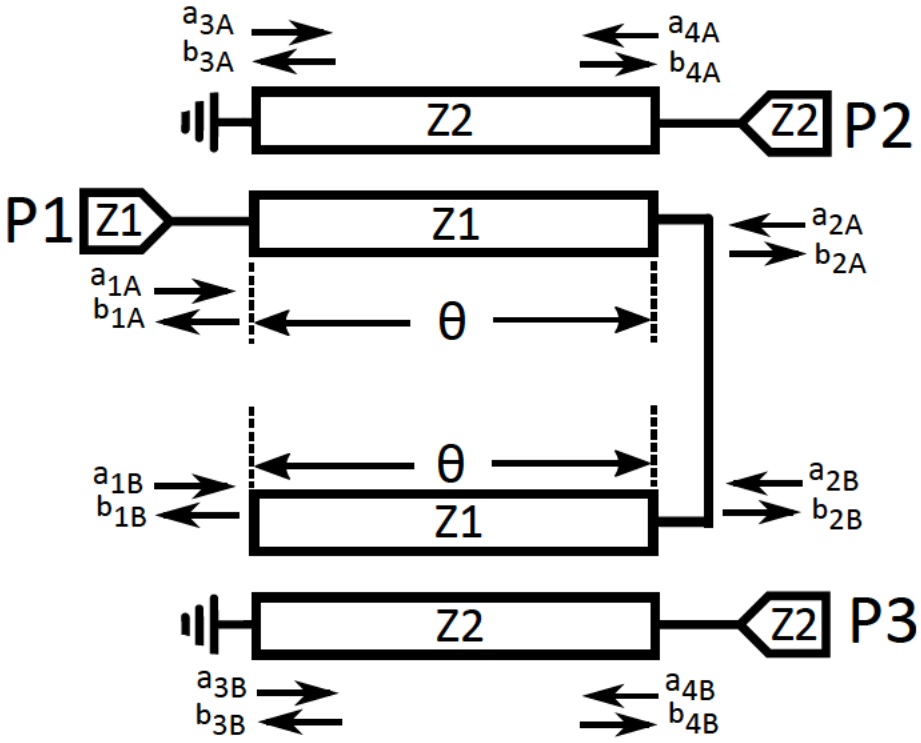


FIGURE 4.3: Block diagram of Marchand balun with two identical coupled lines.

Considering two coupled-line sections as shown in Fig. 4.3, the S-matrix for a three-port Marchand balun can be derived as follows (also mentioned in [129])-

$$[S]_{Marchandbalun} = \begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix} \tag{4.3}$$

$$S_{11} = \frac{x^4 - y^4 - y^2z^2}{z^2(y^2 + z^2)}$$

$$S_{12} = S_{21} = \frac{x^3y - xy^3 - xyz^2}{z^2(y^2 + z^2)}$$

$$S_{13} = S_{31} = \frac{-x^3y + xy^3 + xyz^2}{z^2(y^2 + z^2)}$$

$$S_{23} = S_{32} = \frac{-x^2y^2 + y^4 + y^2z^2}{z^2(y^2 + z^2)}$$

$$S_{22} = S_{33} = \frac{-x^2z^2}{z^2(y^2 + z^2)}$$

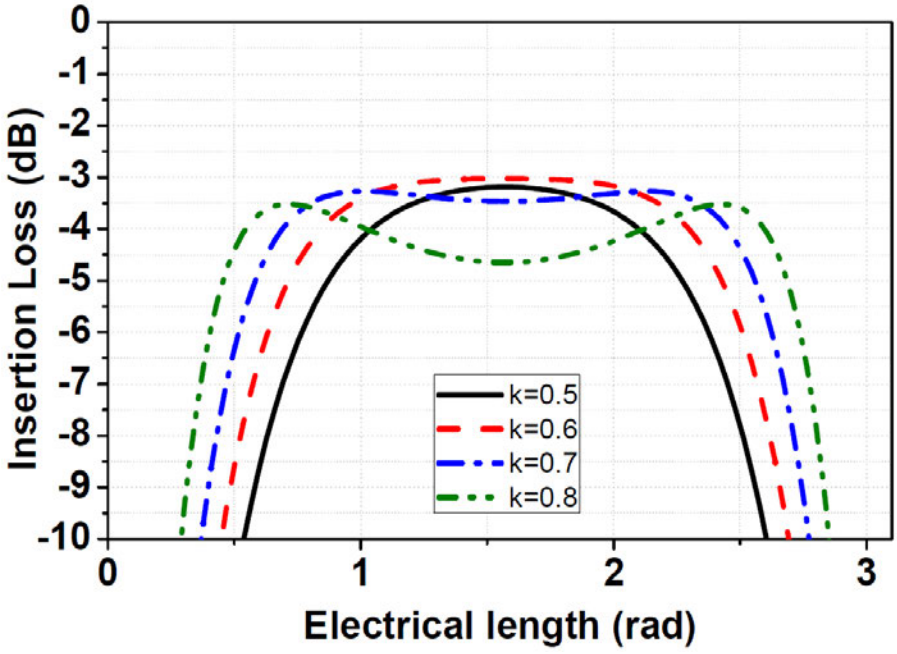


FIGURE 4.4: Insertion loss of Marchand balun with respect to electrical length for varying coupling coefficient.

From the S_{21} and the S_{31} equations, it is found that there are no amplitude and phase imbalances for any values of k and θ. However, the relation between the bandwidth and the coupling coefficient k can be studied from these equations as in [129]. It is found that the bandwidth of the Marchand balun increases with increasing k values but the insertion loss increases at the frequency f_o corresponding to electrical length $\lambda/2$ as in Fig. 4.4. There exists a tradeoff between the bandwidth and insertion loss

for different coupling coefficients.

4.3.2 Analysis of transformer balun

A typical transformer balun configuration is shown in Fig. 4.5. Following similar anal-

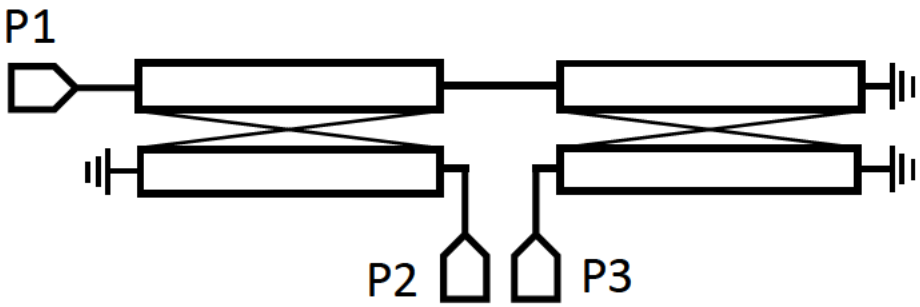


FIGURE 4.5: Transformer balun configuration with two identical coupled line.

ysis to the Marchand balun, the S-parameters are derived for a transformer balun. The block diagram for the transformer balun using two identical coupled lines is shown in Fig. 4.6. The S-matrix for the transformer balun is derived as follows-

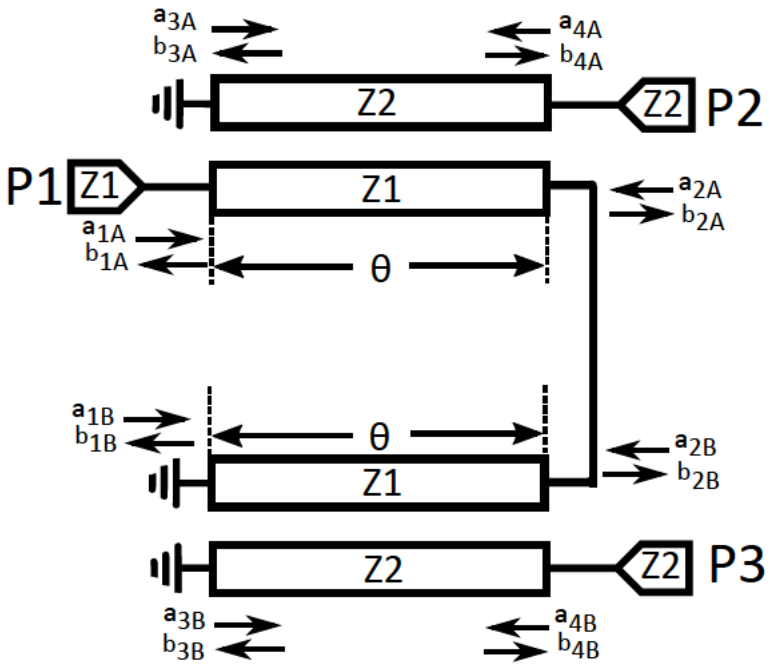


FIGURE 4.6: Block diagram of transformer balun with two identical coupled lines.

$$S_{11} = \frac{y^4 - x^4 - y^2z^2}{z^2(z^2 - y^2)}$$

$$S_{12} = S_{21} = \frac{-x^3y + xy^3 - xyz^2}{z^2(z^2 - y^2)}$$

$$S_{13} = S_{31} = \frac{x^3y - xy^3 + xyz^2}{z^2(z^2 - y^2)}$$

$$S_{23} = S_{32} = \frac{x^2y^2 - y^4 + y^2z^2}{z^2(z^2 - y^2)}$$

$$S_{22} = S_{33} = \frac{-x^2z^2}{z^2(z^2 - y^2)}$$

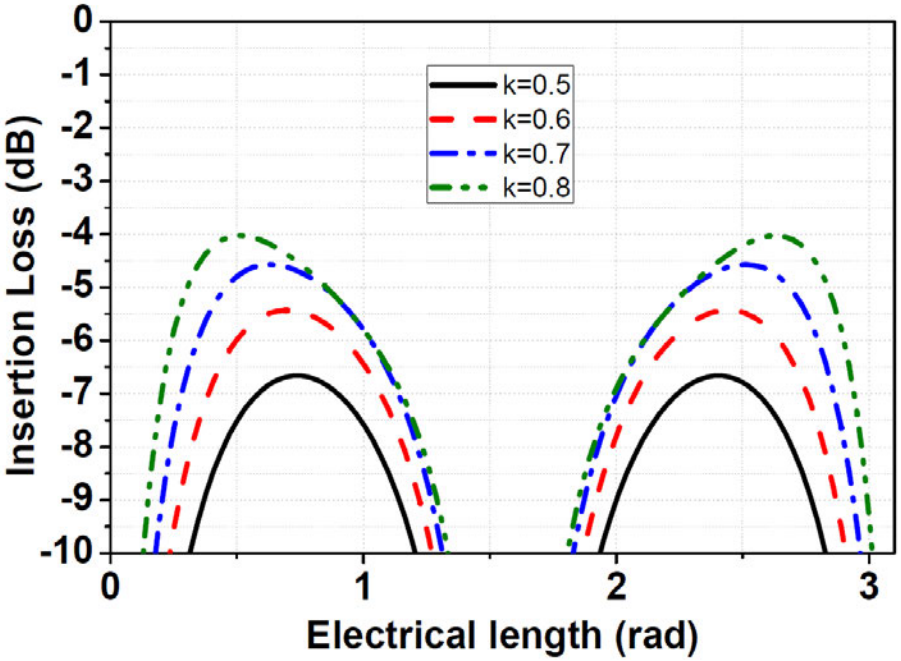


FIGURE 4.7: Insertion loss of transformer balun with respect to electrical length for varying coupling coefficient.

S_{21} and S_{31} for the transformer balun are given by the derived equations. These equations also demonstrate that the magnitude and the phase imbalances are zero for all values of k and θ for a transformer balun as found in the Marchand balun analysis. The relation between the bandwidth and the coupling coefficient k is seen in Fig. 4.7. From the coupled-line model, it is found that the insertion loss of the transformer

balun is higher than for the Marchand balun. It is interesting to note that, unlike the Marchand balun, the insertion loss of a transformer balun decreases with increasing coupling coefficient. Also, for the same length of coupled line, the bandwidth of a transformer balun is less than for a Marchand balun. But it can be inferred that the length of the transformer balun can be much smaller than for the Marchand balun for a particular operational frequency.

4.3.3 Balun selection

The theoretical analysis for the Marchand balun and the transformer balun can be verified from the coupled-line models of the baluns in AWR. Two coupled-line models of the same length (950 μm) are configured as a transformer balun and a Marchand balun and are simulated in AWR. For both the baluns, if the even-mode and the odd-mode dielectric constants are equal then there are no amplitude and phase imbalances for any length of the coupled lines. The amplitude imbalance is 0 dB and phase imbalance is 180^o, indicating that the differential signal is perfect. This is illustrated in Fig. 4.8 and Fig. 4.9.

For the same length of the coupled-line structures and the same even- and odd-mode dielectric constants, the bandwidth for the Marchand balun is greater than for the transformer balun. This is depicted in Fig. 4.10. But, from the S_{21} plot, it can be observed that the transformer balun does not need to be as long as the Marchand balun. Moreover, the transformer balun can be implemented for any frequency range by changing the length of the coupled line, whereas for a Marchand balun design in a low frequency range, the length becomes unrealistically long.

In reality, the propagation constants for the even and the odd modes will be different, and a magnitude and phase imbalance will exist over the frequency range. This can be explained from electromagnetic simulations of baluns using Axiem, the EM simulator tool within AWR Analog Office. The even- and odd-mode dielectric constants

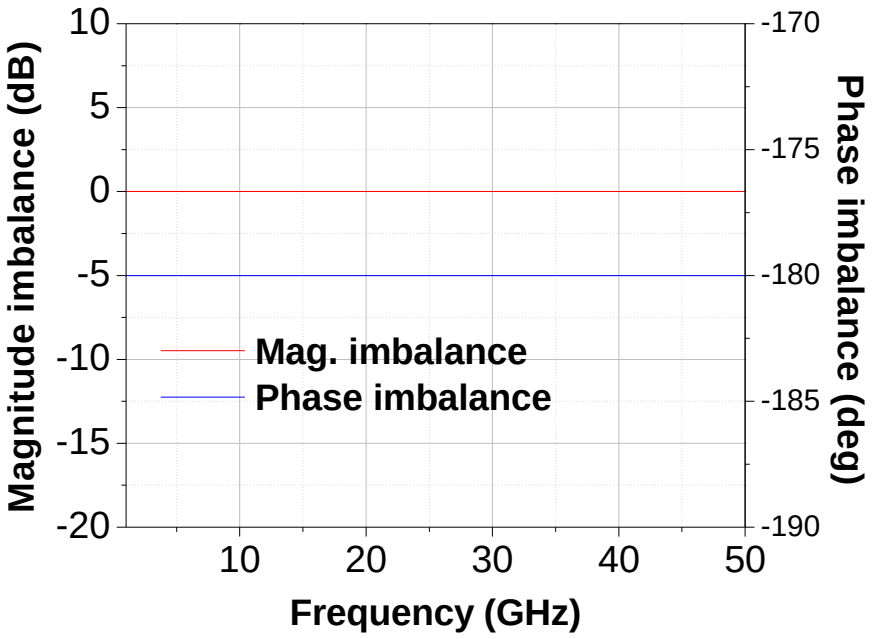


FIGURE 4.8: Amplitude and phase imbalance of a typical coupled-line Marchand balun simulated in AWR.

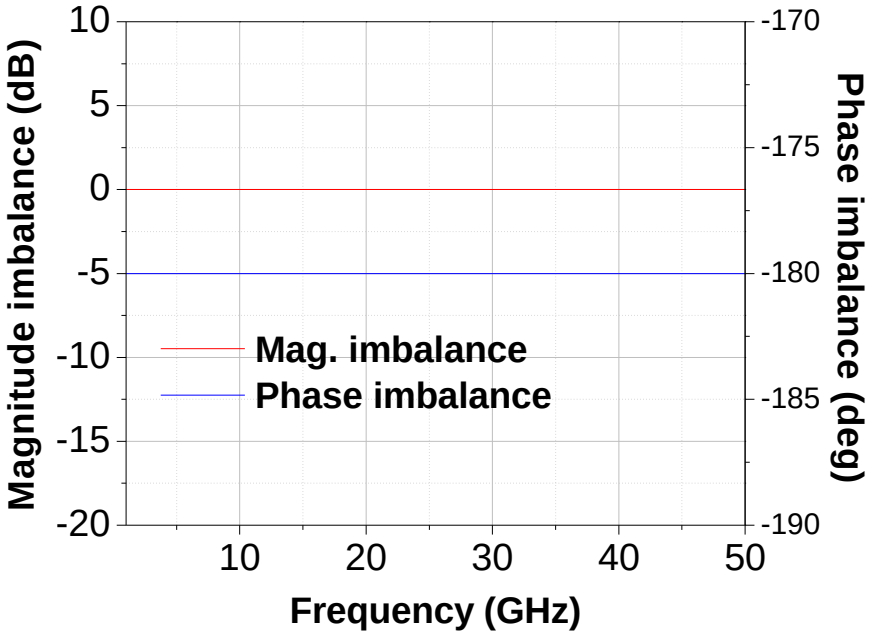


FIGURE 4.9: Amplitude and phase imbalance of a typical coupled-line transformer balun simulated in AWR.

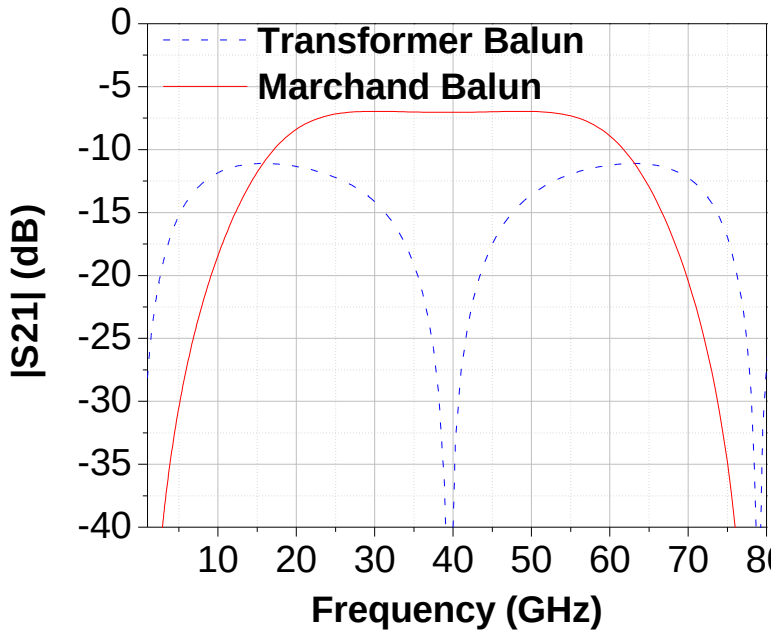
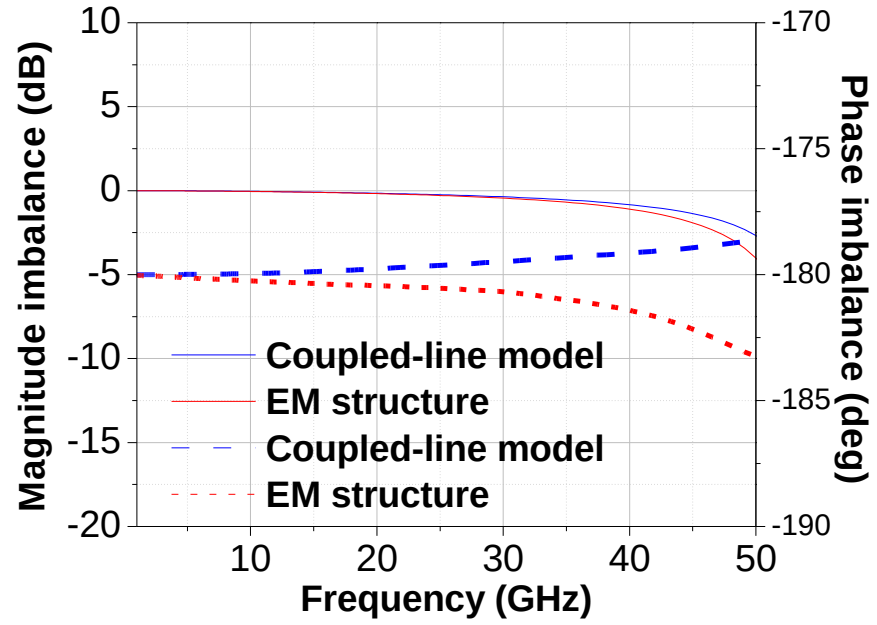


Figure 4.10: Bandwidth of a typical coupled-line Marchand balun and a transformer balun simulated in AWR.

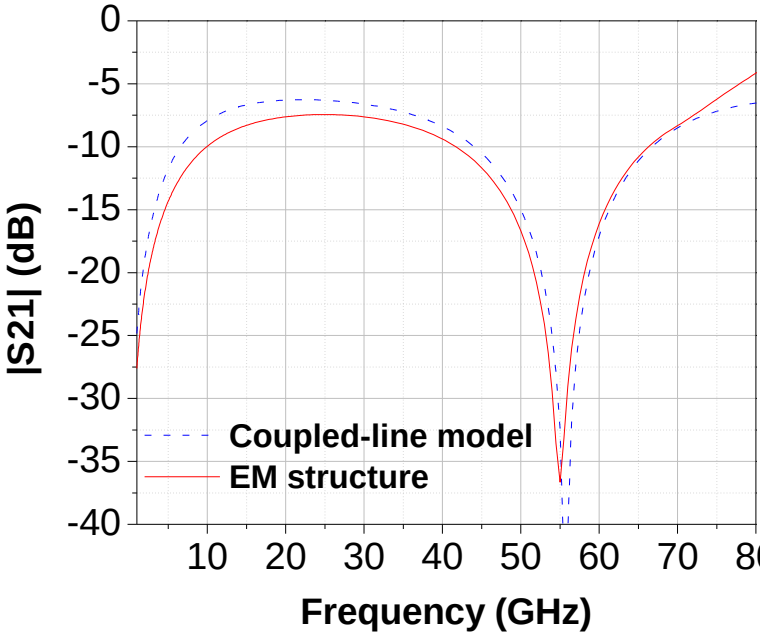
of the baluns configured using coupled-line models are tuned to fit the electromagnetic simulation results of the baluns in Axiem. The comparative results (from the coupled-line model and EM structure) for the transformer balun and Marchand balun are shown in Figs 4.11 and 4.12. The source of imbalances in a transformer balun is discussed in Section 4.4.

As seen from the graphs, the maximum magnitude imbalance of the transformer balun and the Marchand balun are 1.5 dB and 3 dB respectively over 1 to 45 GHz. The maximum phase imbalance is 2^o and 4^o over 5 GHz to 45 GHz for the transformer balun and the Marchand balun respectively.

Although the bandwidth of the transformer balun is found to be not as large as that of the Marchand balun, its magnitude and phase balances are better, as seen from the coupled-line model. As the balance of the differential signal is crucial for the harmonic rejection of a frequency-doubler design, the transformer balun can be a better candidate than the Marchand balun for this purpose. Therefore, a transformer balun is selected for the balanced frequency doubler design. Transformer balun designs

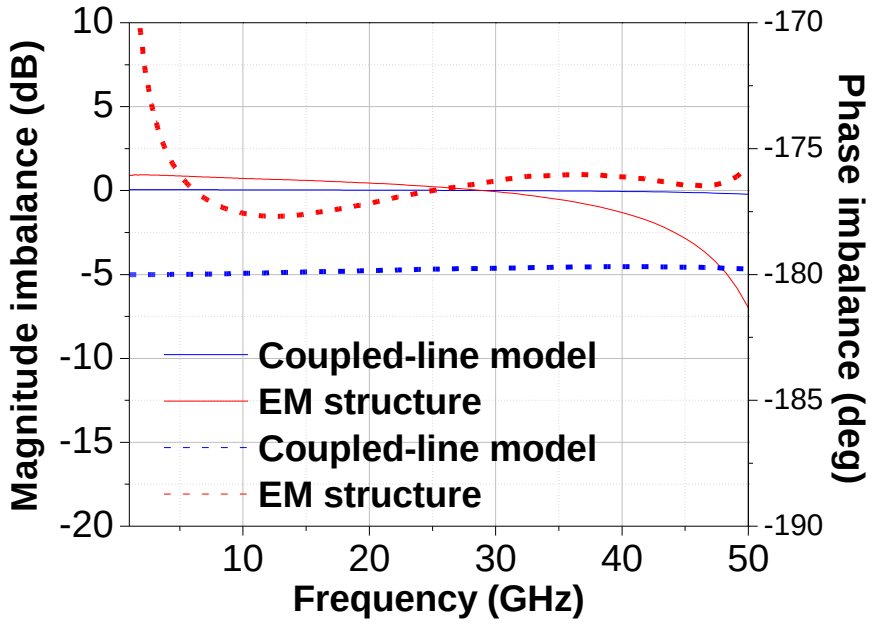


(a)

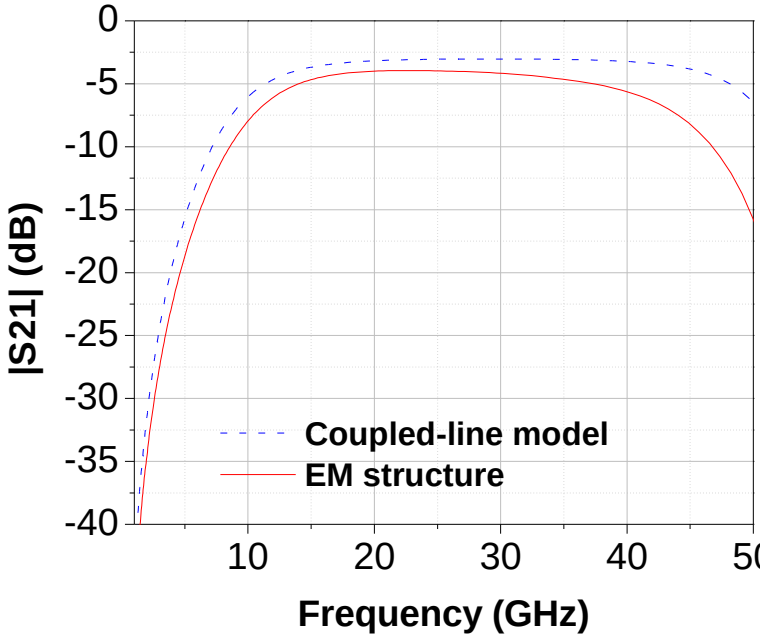


(b)

FIGURE 4.11: Comparison of coupled-line model and EM simulation of a transformer balun. (a) Magnitude imbalance and Phase imbalance (b) Insertion loss and bandwidth.



(a)



(b)

Figure 4.12: Comparison of coupled-line model and EM simulation of a Marchand balun. (a) Magnitude imbalance and Phase imbalance (b) Bandwidth.

in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process are presented in the following sections.

4.4 Operating principle of transformer balun

A block diagram of a transformer balun is shown in Fig. 4.13. The single-ended signal enters through one end of the primary and the differential signal is obtained at the output ports of the secondary. In the primary coil, the input signal enters at port 1 and the other end of the primary is connected to ground. In the secondary, ports 2 and 3 are connected to ground at the centre tap of the secondary through two separate coils. Unlike the Marchand balun, the length of the transformer balun is not dependent on the wavelength.

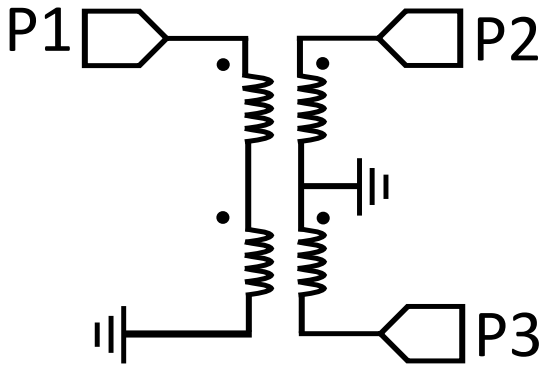


FIGURE 4.13: Block diagram of Transformer balun.

The primary and the secondary coils are magnetically coupled through the coupled inductors distributed around the coils. A current in the primary coil induces a response in the secondary coil that acts to resist the total change in the magnetic field. In a transformer balun, the excitation signal at the input of the primary couples to the secondary and generates a differential signal at ports 2 and 3. In practice, the parasitic capacitance between the coils degrades the balance. Although the two sections of the secondary coil have the same length, the excitation signal at the primary couples more strongly with one section of the secondary than with the other, as one end of the primary coil is grounded. This causes an imbalance in the differential signal and

degrades the common-mode rejection. The ground at the centre tap plays a vital role to short circuit the imbalanced signal at the secondary.

Apart from the inherent imbalance, magnetic flux leakage, parasitic capacitive coupling and resistive loss in metal lines also degrade the performance of on-chip transformer baluns [99]. To mitigate these problems the size of the spirals could be reduced and the width of the metal lines could be increased, but this affects the insertion loss and the size respectively [130].

Transformer balun designs in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process are implemented in this work (presented in Section 4.5-4.6) which leverage the analysis.

4.5 Transformer balun implementation in SG13S process

As mentioned in Chapter 1, the design of a K-Ka band frequency doubler will be shown. The design of a transformer balun implemented in the SG13S SiGe HBT process, to be used with a 14 to 30 GHz frequency doubler is presented here. The operating principle of the balun is illustrated in Fig. 4.14. As seen from Fig. 4.14, a differential pair is used for the doubler design. The cause of the imbalance in the differential signal generated by the transformer balun is explained in this section and a novel solution is proposed.

4.5.1 Design details

The parasitic capacitance between the coils (in red in Fig. 4.14) degrades the balance of the signal. Fig. 4.14 illustrates that the AC voltage couples more strongly to the upper half of the secondary, which is the source of the imbalance. The centre tap on the secondary coil is grounded to short circuit the asymmetrically coupled voltage signal, for reducing the imbalance. The effect of grounding the centre tap is illustrated in Fig. 4.15, using the Axiem. Without a grounded centre tap the magnitude and the phase imbalance are 0.8 dB and 6^o at 20 GHz. With a centre-tap ground, the

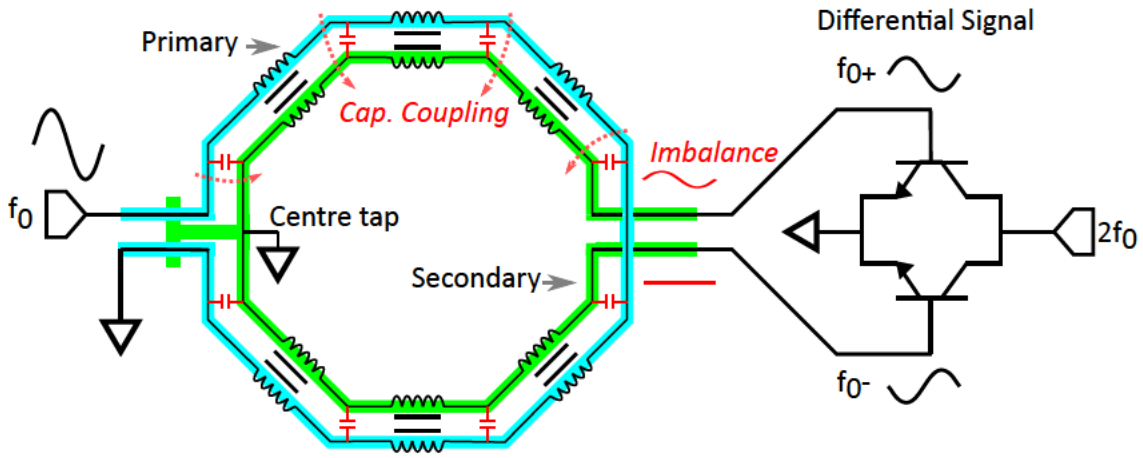


FIGURE 4.14: Schematic representation of Transformer balun with doubler.

magnitude and phase imbalance are reduced to 0.12 dB and 1^o at 20 GHz.

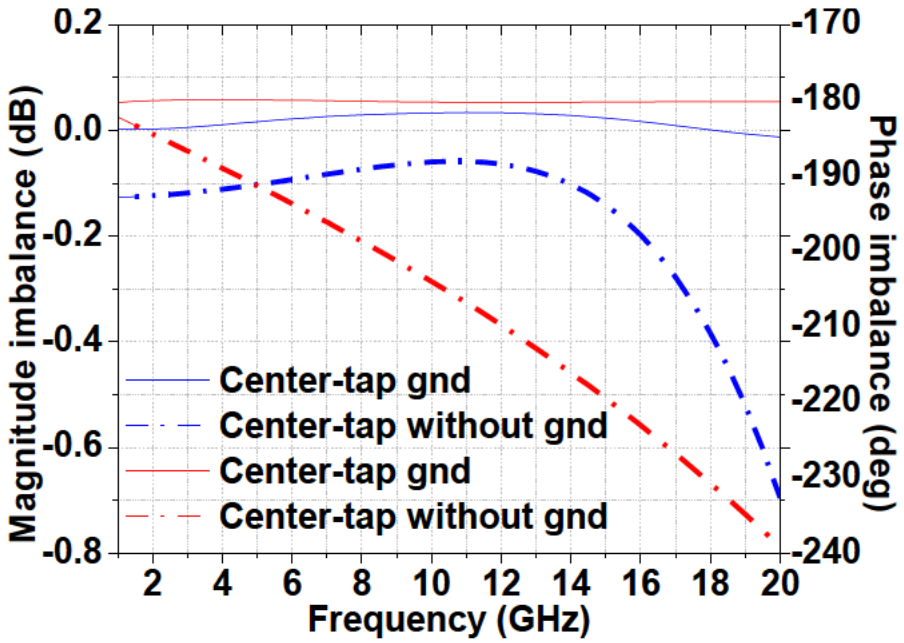
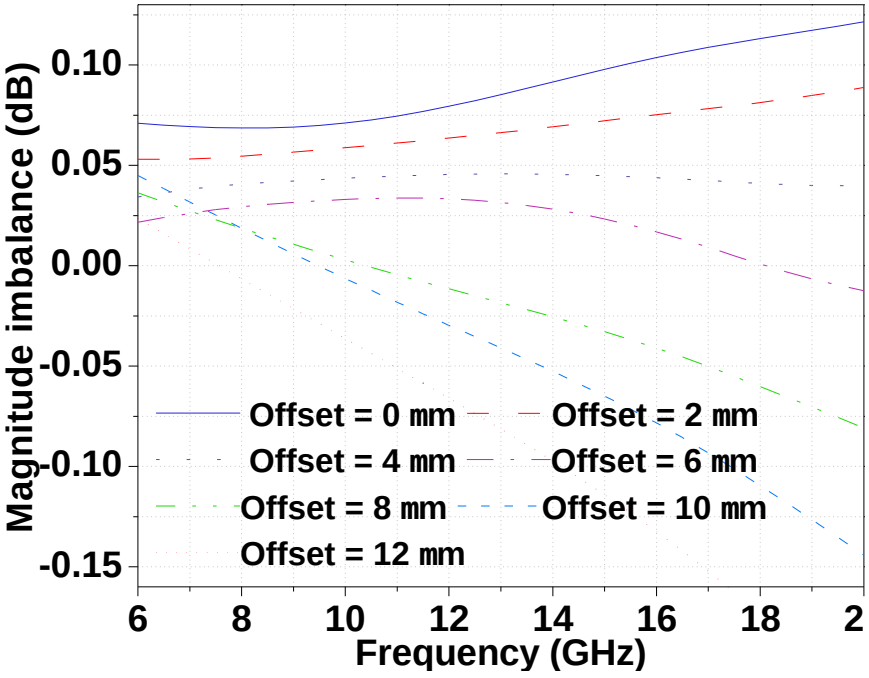
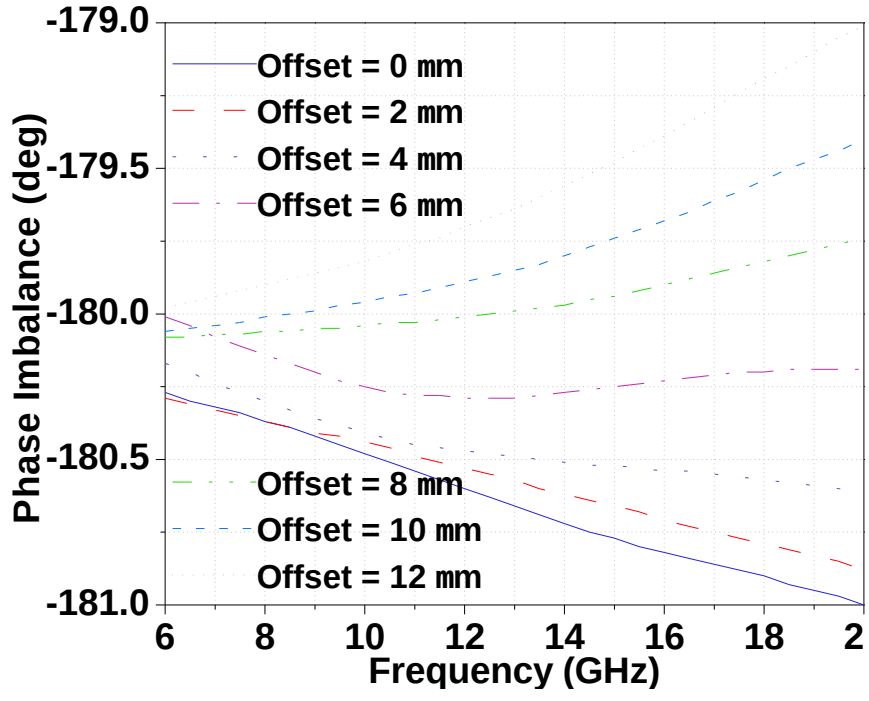


FIGURE 4.15: Magnitude imbalance (blue) and phase imbalance (red) with (solid) and without (dotted) centre-tap ground on secondary for 6 μm offset between the coil radii.

In this work, offsetting the radii of the primary and secondary coils is incorporated to attempt to improve the balance of the signal. Fig. 4.16 shows the amplitude and the phase imbalance for varying offsets; 0 μm corresponding to broadside coupling. For an offset of 0 μm, the maximum amplitude and phase imbalance is 0.12 dB and 1^o



(a)



(b)

Figure 4.16: Effect of varying offset between primary and secondary coil radii. (a) Simulated magnitude imbalance and (b) simulated phase imbalance.

between 1 and 20 GHz. An offset of 6 μm was chosen which improves the performance to an amplitude and phase imbalance of 0.03 dB and 0.25^o over the same frequency band.

But offsetting the radii of the coils reduces the magnetic and capacitive coupling between the primary and secondary coils, thus increasing the insertion loss of the balun. To understand this tradeoff the Gmax (maximum gain) of the balun is plotted in Fig. 4.17 which indicates the insertion loss under ideally matched conditions. The insertion loss is 1.5 dB for broadside coupling (0 μm offset) and 1.78 dB for the proposed 6 μm offset.

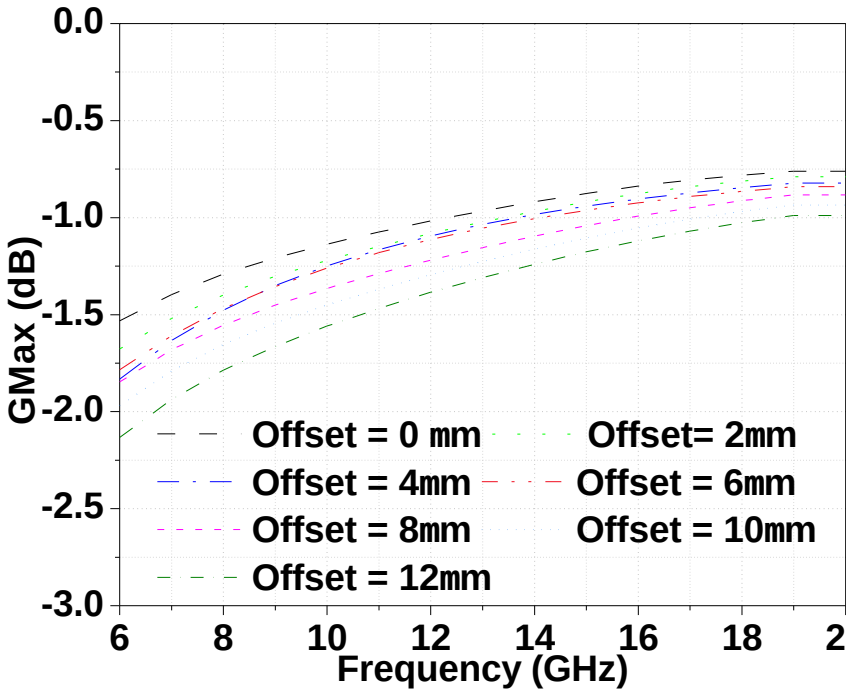


FIGURE 4.17: Plot of Gmax for the transformer balun for varying radius offset.

The coupling coefficient is reduced from 0.69 for broadside coupling to 0.61 for the proposed 6 μm offset and 0.49 for a 12 μm offset as demonstrated in Fig. 4.18.

For the frequency-doubler application, the additional loss at the input is deemed an acceptable tradeoff to enable high odd-order harmonic cancellation in the doubler, leading to improved spectral purity.

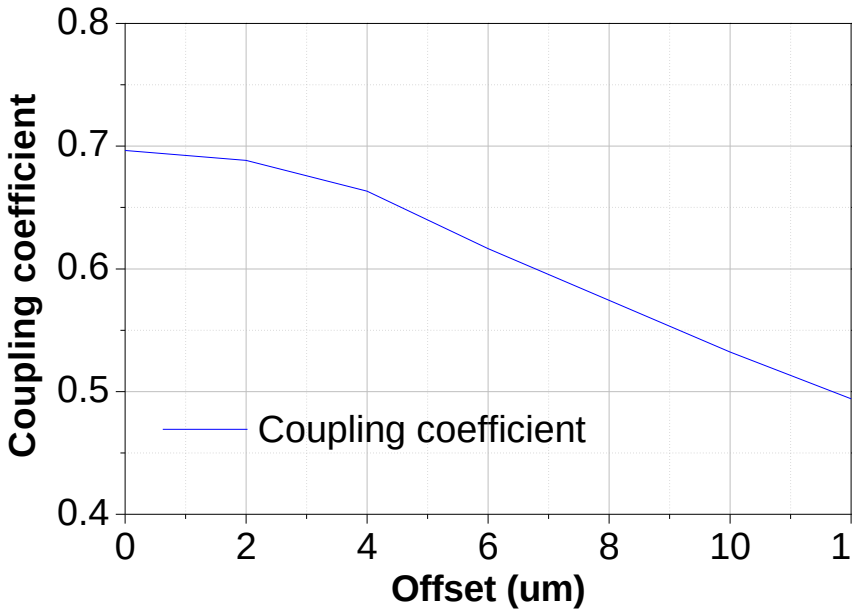


Figure 4.18: plot of coupling coefficient with respect to varying radius offset.

4.5.2 Layout and fabrication

The SG13S SiGe HBT process back end of line (BEOL) has five thin metal layers, a metal-insulator-metal (MIM) capacitor and two thick metals (discussed in Section 2.2). In the balun considered here, the primary and secondary coils are implemented in the top two metals, TM2 (3 μm thick) and TM1 (2 μm thick), as depicted in the cross-sectional view of Fig. 4.19. This minimises metal losses, increases DC current handling capacity and reduces coupling to the lossy substrate. A ground ring surrounding the balun is used to aid electromagnetic simulation by providing a ground reference for the excitation ports.

Unlike the PP10-10 GaAs pHEMT process, there is no continuous backside ground plane. A ground ring surrounding the balun is used to provide RF shielding from the neighbouring metals, to aid electromagnetic simulation by providing a ground reference for the excitation ports. This ground ring consists of a stack-up of all the metal layers from TM2 to M1 up to the substrate, connected by vias between the metal layers.

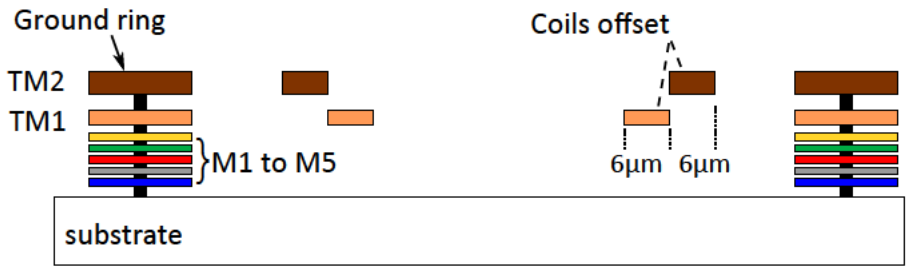


FIGURE 4.19: Cross-sectional view of the metal stack-up of SG13S SiGe HBT process showing offset radius coils in the balun.

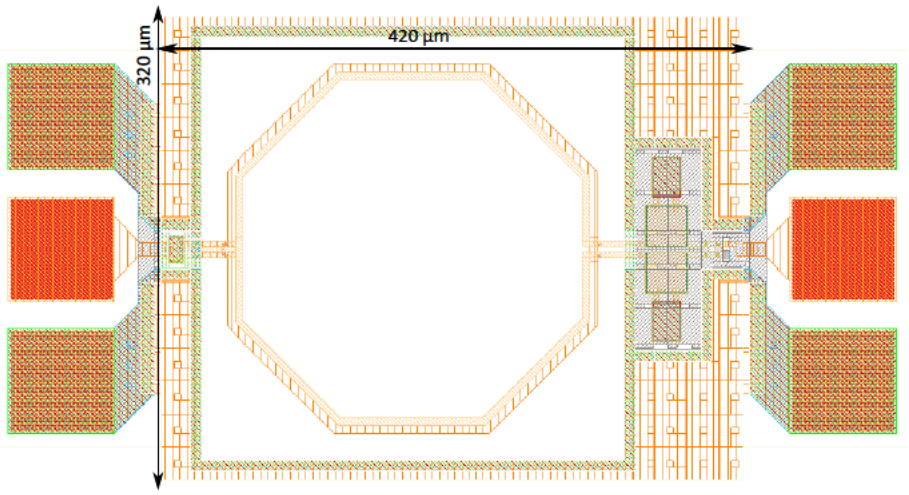
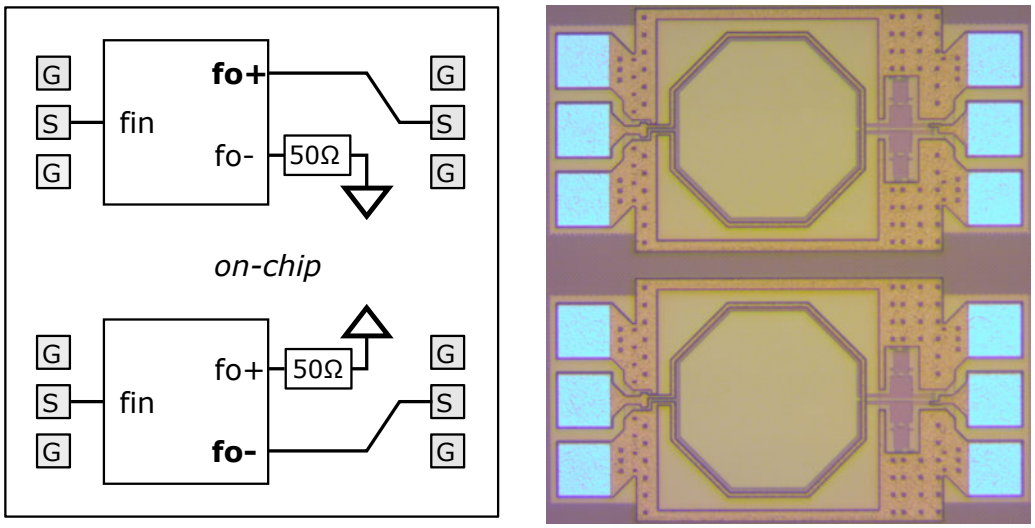


FIGURE 4.20: Layout of the designed transformer balun.

The balun is octagonal in shape to make it compact and to reduce the corner effects of a square structure. The structure of the designed balun is shown in Fig. 4.20. The radius of the primary coil is 134 μm while the radius of the secondary coil is 128 μm to maintain an offset of 6 μm. The width of both the primary and secondary coils is 6 μm. A ground plane (using any of the metal layers) is not created under the transformer balun to increase the quality factor. Matching capacitors are used at the input and the output of the balun. Symmetry is maintained throughout the layout of the balun. As the capacitors are placed in the RF path, they are also enclosed by the ground ring to protect from interference from the surrounding metal structures.

A differential measurement can be used for a balun as it is a three-port structure. But the set up and calibration of a differential measurement is not straightforward. Sometimes, back-to-back balun structures are used to test the design. But this only

allows 2-port S-parameter measurements. Our objective is to measure the amplitude and phase imbalance of the differential signal. Therefore, in order to quantitatively assess the balun design and to ascertain its suitability for the frequency doubler, two-port characterisation structures are used as depicted in Fig. 4.21.



(a) (b)

Figure 4.21: (a) Diagram showing the position of on-chip resistors to facilitate two port measurements. (b) Die photo of transformer balun characterisation structures.

These characterisation structures are identical to each other except for on-chip 50 Ω resistors at the output, that are placed on opposite sides. These structures facilitate the usual two-port measurements. Two-port S-parameter files are measured and compared to determine the magnitude and the phase imbalance.

4.5.3 Test and measurement results

The balun is measured using an Anritsu Vector Star MS4642B, vector network analyser and a Summit 9000 on-wafer probing station. Off-chip calibration was used for the measurement. Fig. 4.22 and Fig. 4.23 show the measured amplitude and phase imbalance of the balun respectively. Five dice were measured to investigate the process variation. The amplitude and the phase imbalance are approximately less than 0.38 dB and 1.4^o across all five dice from 1 to 20 GHz. The mean trace has an imbalance

of 0.13 dB and 0.4^o across 7 to 15 GHz.

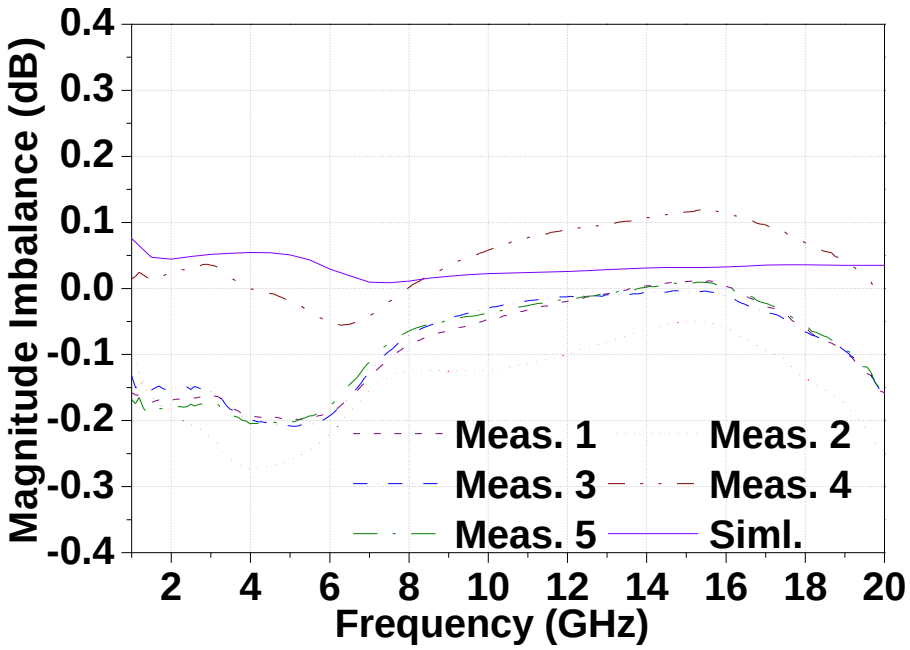


FIGURE 4.22: Measured (dotted lines) and simulated (solid lines) magnitude imbalance across five dice.

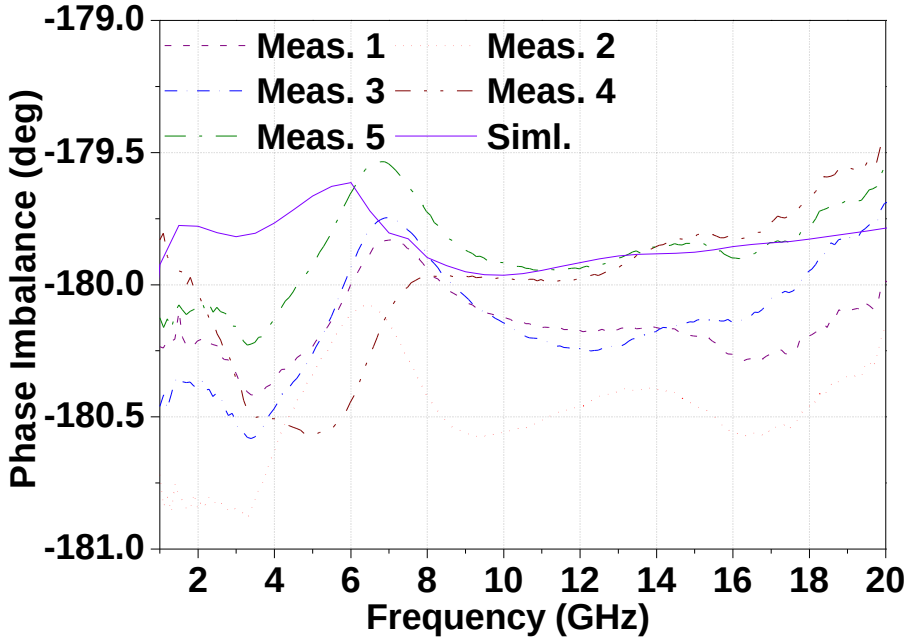


FIGURE 4.23: Measured (dotted lines) and simulated (solid lines) phase imbalance across five dice.

Table 4.2: Performance summary of the designed transformer balun and comparisons with other state-of-the-art designs

Parameters	[131]	[132]	[133]	[134]	**This work**
Amp. imb. [dB]	0.5	0.2	1.5	1	< 0.13
Ph. imb. [deg]	5	2.7	7	<3	$< 0.4^o$
Ins. Loss [dB]	2.5	1.9	<4.7	2	<3
BW [%]	66	40	105	60	73
Area [mm^2]	-	0.036	0.11	-	0.029
Tech. [μm]	0.2 SiGe	0.18 SiGe BiCMOS	0.18 SiGe BiCMOS	GaAs	0.13 SiGe BiCMOS

The comparison between the performance of the designed transformer balun and the state-of-the-art designs is presented in Table 4.2.

4.6 Transformer balun implementation in PP10-10 process

The design of a transformer balun implemented in the PP10-10 GaAs pHEMT process, for an 11 to 20 GHz frequency doubler is presented here. The topology, design and performance of the transformer balun that could be implemented in the GaAs process is described.

4.6.1 Design details

The performance of the transformer balun depends on the structure and the layout. The structure of the transformer balun in turn is dependent on the process technology. Two types of orientation are common for the transformers: planar and stacked. In this respect, process technology plays a significant role. The silicon-based processes, such as CMOS and SiGe, offer a stack-up of different metal layers for the implementation of the passive structures, whereas in the PP10-10 GaAs pHEMT process there is only

two metal layers (details in Section 2.3). Moreover, in this process, M2 cannot be used as a stand-alone layer, it is usually enclosed by the M1 layer except the air-bridge. Therefore, the silicon-based processes can support both stacked and planar orientations of the transformer baluns, but only planar transformers are supported by the GaAs process. As the PP10-10 GaAs pHEMT process only supports passive structures with planar orientation, the layout occupies more area. On the other hand, the passive structures in silicon-based processes can be more compact as they offer multiple metal layers to implement stacked structures.

A planar transformer balun is implemented in the PP10-10 GaAs pHEMT process. In the broadside coupled design, the primary and the secondary coils are stacked together. This leads to a higher coupling coefficient due to capacitive coupling between the coils in addition to the magnetic coupling. In the edge-coupled design, as the metal lines for the primary and secondary lie side by side, the coupling is less. The metal lines for implementing the primary and the secondary coils must be placed at a minimum separation to increase the coupling. The minimum spacing between the metal lines is limited by the design rules. The selection of the metal layer and the metal width are also critical for the balun design. Increasing the metal width of the primary and the secondary coils leads to a larger area and higher parasitic capacitance. To minimise the metal losses, a thick metal layer could be used.

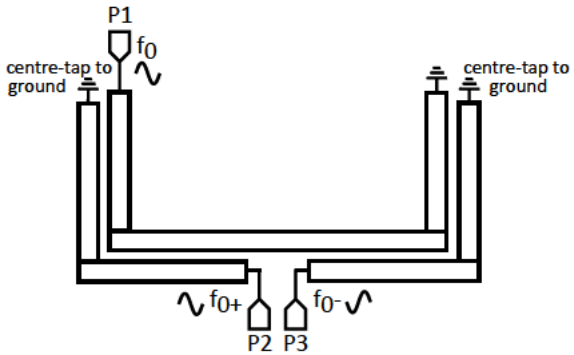


FIGURE 4.24: Layout of the proposed balun.

Typically, in MMIC design, spiral transformers are used to reduce the area. But the small inner diameter of the spiral limits the insertion loss and the amplitude balance

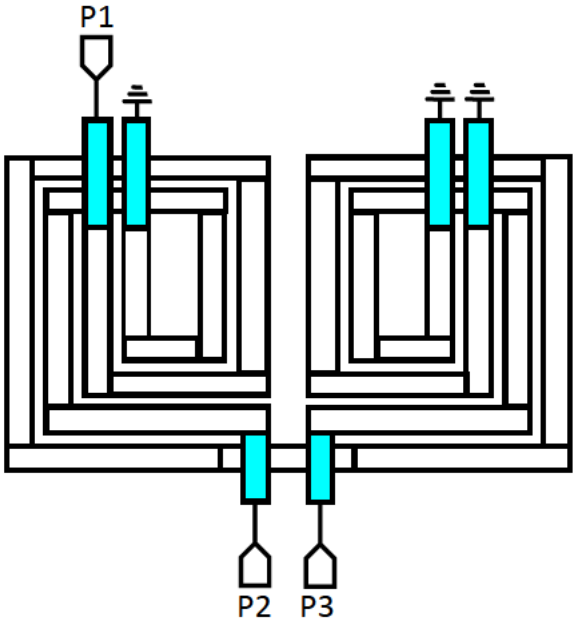


FIGURE 4.25: Layout of the conventional spiral balun.

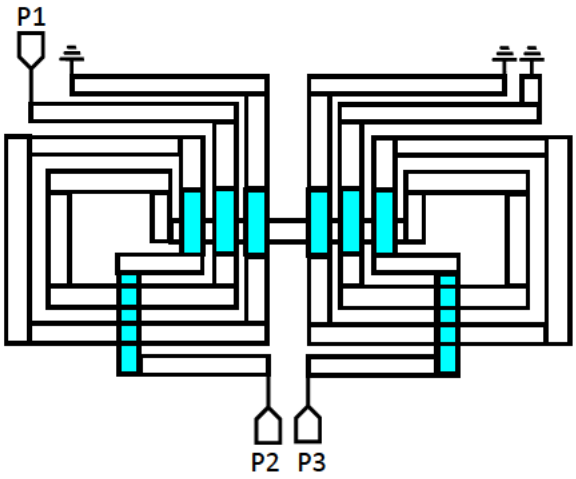


FIGURE 4.26: Layout of the conventional spiral balun.

as demonstrated in [135]. To study this tradeoff between the smaller inner diameter of the transformer balun and the insertion loss, three different structures for the planar transformer balun (over the same frequency range) are simulated: two transformer baluns with inter-wound primary and secondary coils, and a "U" shaped transformer balun. The schematics for these baluns are shown in Fig. 4.24, Fig. 4.25, Fig. 4.26.

The maximum-gain plots of these structures show that the "U" shaped transformer

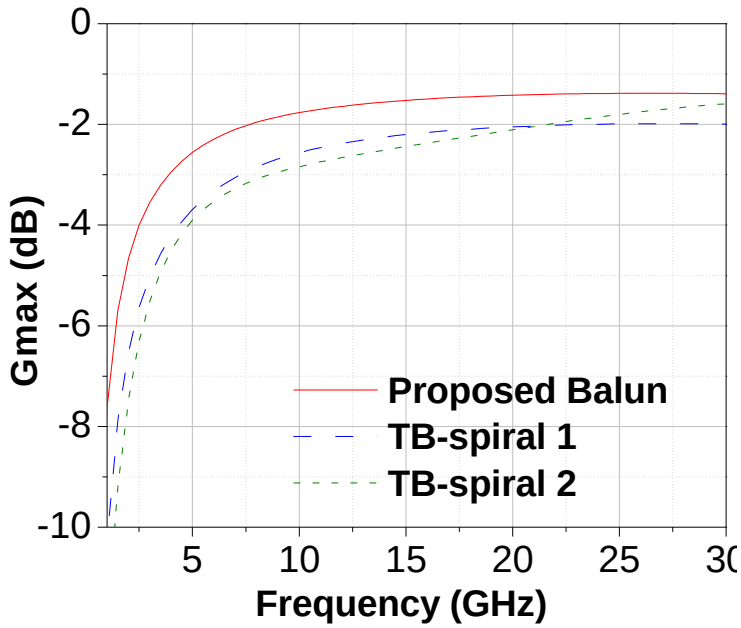


FIGURE 4.27: Plot of Gmax for the "U-shaped" and the other two spiral transformer baluns.

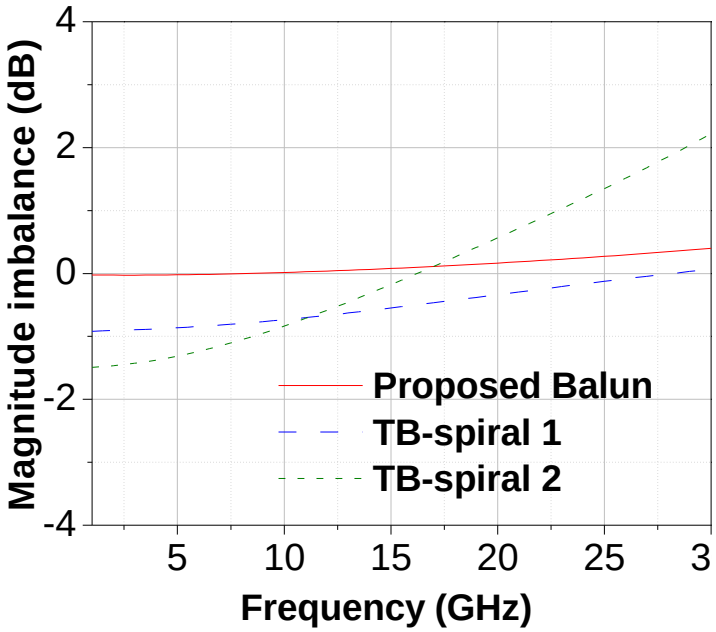


FIGURE 4.28: Plot of Amplitude imbalance for the "U-shaped" and the other two spiral transformer baluns.

balun with a larger inner dimension has the lowest insertion loss among these three structures as shown in Fig. 4.27. The amplitude balance and the phase balance are also better for the "U" shaped transformer balun than for the spiral configurations as demonstrated in Fig. 4.28 and Fig. 4.29. Hence, the "U" shaped structure is adopted for our work.

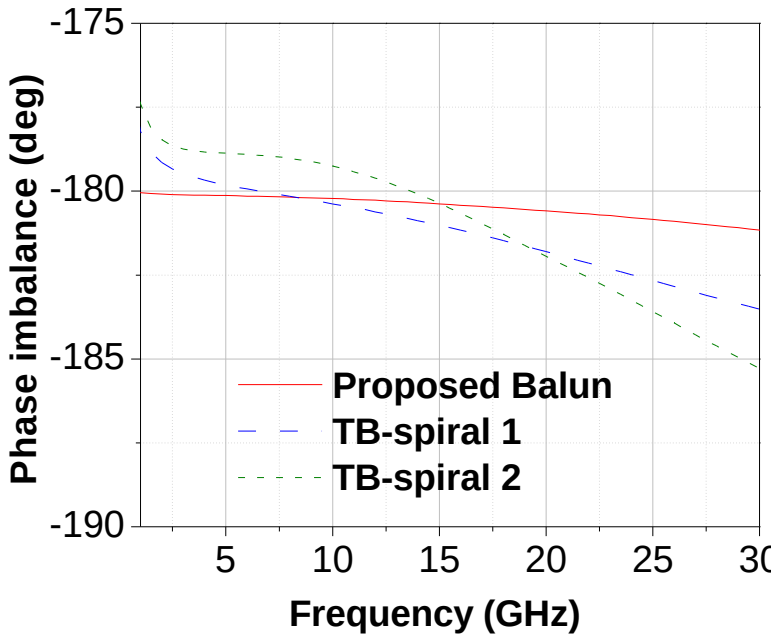


Figure 4.29: Plot of Phase imbalance for the "U-shaped" and the other two spiral transformer baluns.

4.6.2 Layout and fabrication

To minimise the metal losses, both the primary and the secondary coils are implemented in thick metal (with a total thickness of 3 μm), i.e. a combination of metal 1 (M1, 1 μm thickness) and metal 2 (M2, 2 μm thickness). The separation between the primary and the secondary coils is maintained at the minimum spacing of 5 μm, as per the design rule limitation. The cross-section of the transformer balun is shown in Fig. 4.30. The coupling coefficient for different spacings between the primary and secondary coils is shown in Fig. 4.31. As wider metal layers add parasitic coupling to the ground at the

bottom, a minimum metal width of 7 μm for the thick metal is used.

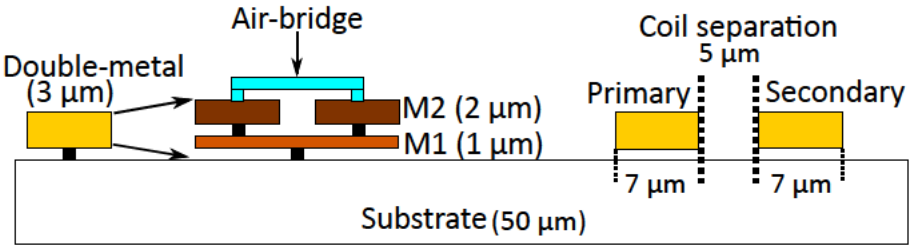


FIGURE 4.30: PP10-10 GaAs pHEMT process cross-section.

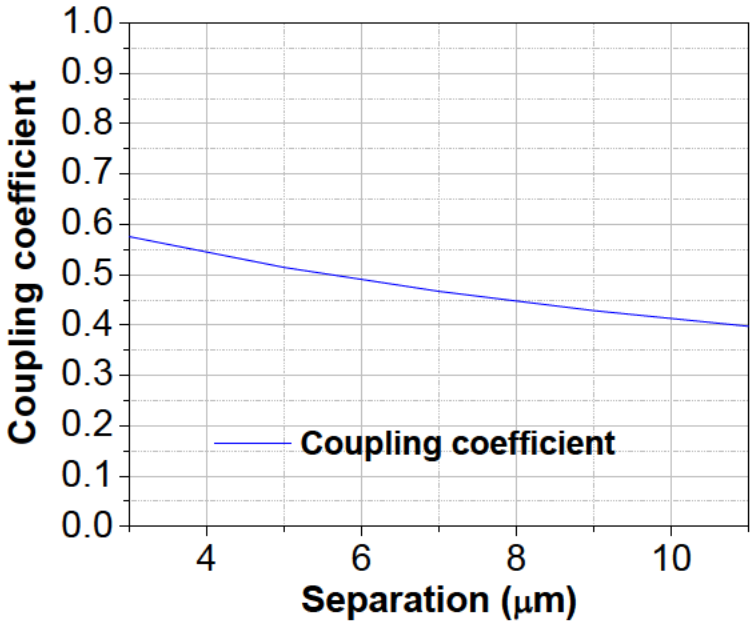
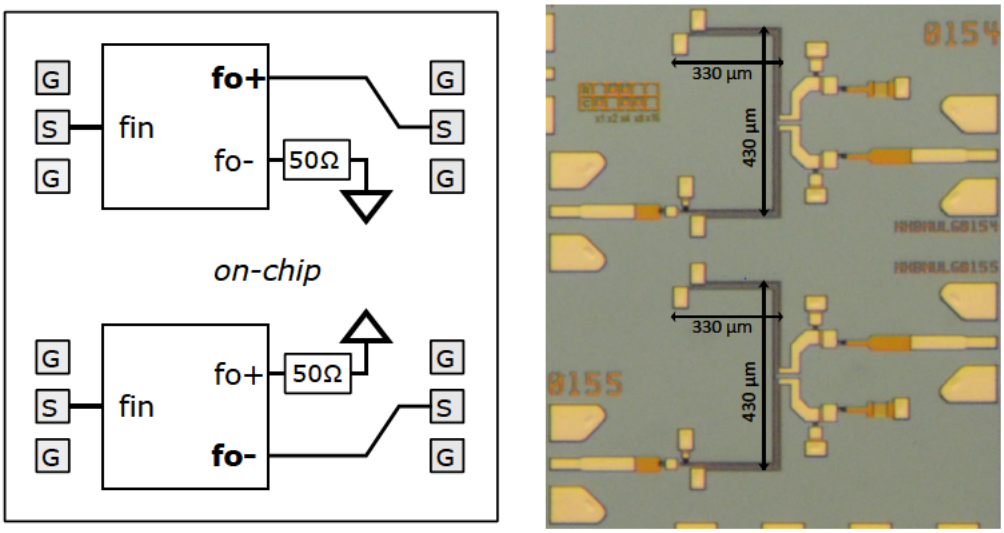


FIGURE 4.31: Coupling coefficient for different spacing between the primary and the secondary coils.

The secondary coil is placed on the outer side of the primary coil as shown in Fig. 4.24. The layout of this transformer balun is symmetrical and avoids any cross-over of the metal lines. Usually, for the spiral balun topologies reported in the literature [136], there are multiple cross-overs of the metal lines making the structure much more complicated, and also they are not absolutely symmetrical. The centre tap is connected to ground at two points instead of connecting through a single via. The size

and the position of the via to ground the centre tap affects the phase imbalance of the balun.

Although the amplitude and phase imbalance of the balun could meet the specifications of the state-of-the-art designs, the input and output matching are poor. While the Marchand balun could be easily matched to a 50 Ω termination, the transformer balun shows poor matching with the 50 Ω port. The input and output matching for the transformer balun could be improved by the addition of a suitable matching network. Matching networks involving inductors are not suitable for this purpose, as they occupy a large area and affect the amplitude and the phase imbalance of the balun. Capacitors are used for matching in this design. A combination of series and shunt capacitors is used to design the matching network at the single-ended input and the differential output. This improves the matching at the input and the output without affecting the balance of the balun.



(a) (b)

FIGURE 4.32: (a) Diagram showing the position of on-chip resistors to facilitate two-port measurements. (b) Die photo of transformer balun characterisation structures.

As discussed in the previous section (Section 4.5.2), similar two-port characterisation structures are used for the balun in the PP10-10 GaAs pHEMT process to quantitatively assess the balun design and to ascertain its suitability for the frequency

doubler as illustrated in Fig. 4.32.

These characterisation structures are identical except for the on-chip 50 Ω resistors at the output, that are placed on opposite sides. These structures facilitate the usual two-port measurement. From the two-port S-parameter measurements, the amplitude and the phase imbalance of the balun are determined.

4.6.3 Test and measurement results

The designed transformer balun has been fabricated in the PP10-10 GaAs pHEMT process. The balun core is only 430 μm × 330 μm. The transformer balun is measured using a Keysight PXA Signal Analyzer, N9030A. On-chip SOLT calibration was used. As mentioned earlier, the two-port measurement was carried out on the two instances of the transformer balun with the 50 Ω on-chip termination at one of the output ports of the balun.

The fractional bandwidth is approximately 60%. The measured S_{21} for both the test structures is -4.3 dB at the mid band. 3 dB of the power loss is due to the power splitting. Therefore, the actual insertion loss of the balun is only 1.3 dB. Fig. 4.33 and Fig. 4.34 show the measured amplitude and the phase imbalance respectively obtained from the two-port measurements. Five dice were measured to investigate the process variation. The amplitude imbalance is less than 0.2 dB over 1 to 25 GHz. The mean trace shows a measured phase imbalance of less than 2^o over 10 to 20 GHz. The variation between the simulated and the measured phase imbalance can be attributed to inaccurate calibration.

Table 4.3 summarises the performance of the designed balun as compared to other state-of-the-art designs in the GaAs process. Not only the performance for the transformer baluns, but the performance for the state-of-the-art Marchand baluns in the GaAs process, are also included to provide a wide perspective of the results achieved for our design compared to the results reported in the literature so far.

* TB = Transformer Balun

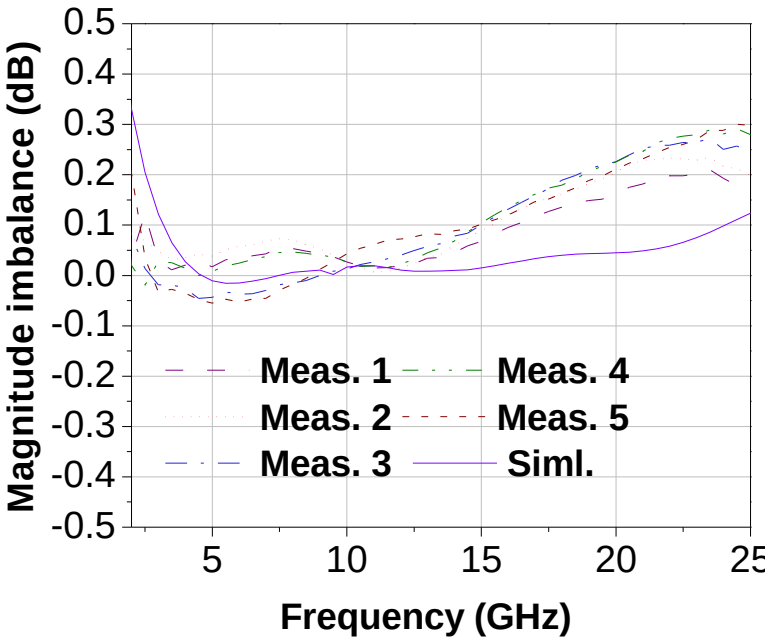


Figure 4.33: Measured (dotted lines) and simulated (solid line) amplitude imbalance of the transformer balun across five dice.

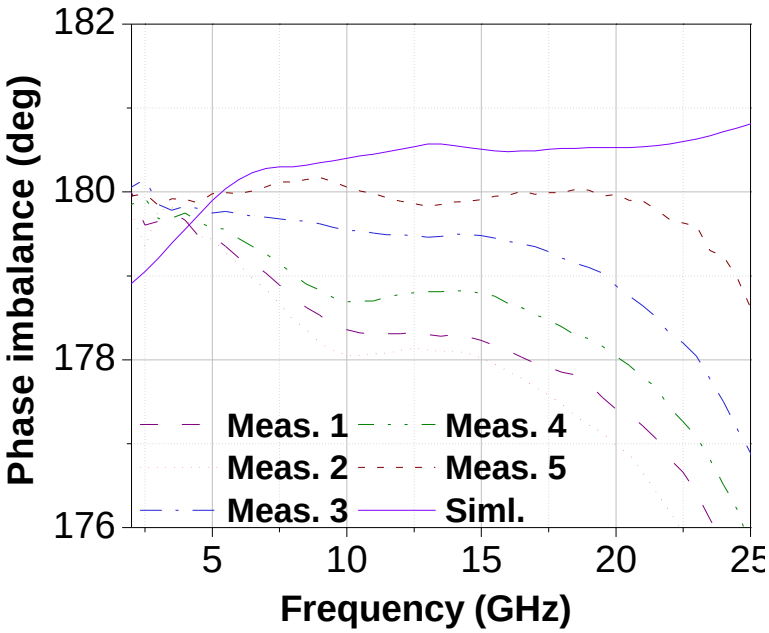


Figure 4.34: Measured (dotted lines) and simulated (solid line) phase imbalance of the transformer balun across five dice.

TABLE 4.3: Performance summary of the balun in PP10-10 compared to the other state-of-the art designs.

Ref.	**Amplitude Imbalance (dB)**	**Phase Imbalance (deg)**	**Bandwidth (GHz)**	S_{21} **(dB)**	**Tech.**	**Type of balun**
[135]	$\pm$ 1.5 (1-25 GHz)	$< 10^o$ (5-25 GHz)	-	-4.5	0.15 μm GaAs	TB*
[135]	-1 to 10 (5-10 GHz)	$< 10^o$ (5-15 GHz)	-	-5	0.15 μm GaAs	TB*
[137]	< 1 (14-28 GHz)	$\pm$ 10^o (14-28 GHz)	66.6 (check)	-4	GaAs	Spiral MB*
[138]	2 (25-58 GHz)	172^o-192^o (20-55 GHz)	20-60	-8 to -10	0.15 μm GaAs	Double spiral dual TB*
[139]	$\pm$ 0.5 (24-40 GHz)	172^o-182^o (24-40 GHz)	30-44 (S_{11} bw)	-5	GaAs	Uniplanar MMIC balun
[140]	1 (8-20 GHz)	$< 6^o$ (8-20 GHz)	8-20	-7.5 to -4	0.5 μm GaAs	MB*
[136]	$\pm$ 1.5 (4-24 GHz)	$< 10^o$ (2-22 GHz)	6-18	-5	GaAs	Transformer type MB*
[134]	0.5 to -1 (1-22 GHz)	$< 3^o$ (2-22 GHz)	2-22	-4 to -5	BCB GaAs MMIC	MB*
This work	< 0.2 (1-25 GHz)	$< 2^o$ (1-20 GHz)	10-18	-4.3	0.1 μm GaAs	TB*

* MB = Marchand Balun

4.7 Evaluation and comparison

In this chapter, the analyses of a transformer balun and a Marchand balun are first presented. For the two types of balun using the coupled-line model of the same length, it is found that the magnitude imbalance and the phase imbalance of the Marchand balun are greater than the transformer balun, although the bandwidth is larger for the Marchand balun. As a result, the focus of this work was on the transformer balun as it would have less impact on the linearity of the system level performance.

Table 4.4: Comparison of the performance of the baluns implemented in the PP10-10 GaAS pHEMT and the SG13S SiGe HBT process.

Parameter	SG13S SiGe HBT	PP10-10 GaAs pHEMT
Amp. imb. [dB]	< 0.13	< 0.2
Ph. imb. [deg]	0.4^o	$< 1.5^o$
Ins. Loss [dB]	<3	< 1.5
Freq. range [GHz]	7-15	10-18
Area [mm^2]	0.029	0.14
Topology	Broadside coupled	Edge coupled

For a frequency-doubler design, because the balance of the differential signal is critical for odd-harmonic suppression, the transformer balun is selected over the Marchand balun. The design and implementation of the transformer balun in the two processes, SG13S SiGe HBT and PP10-10 GaAs pHEMT, are demonstrated. The topology of the balun is dependent on the process technology. It is found that only edge-coupled design can be implemented using the PP10-10 GaAs pHEMT process due to the nature of the metal stack-up whereas both broadside-coupled and edge-coupled baluns can be implemented in the SG13S SiGe HBT process. Broadside coupling is used for the transformer balun implemented in the SG13S SiGe HBT process and edge coupling is used for the PP10-10 GaAs pHEMT balun.

Differential measurement is not used for the balun as the set up of calibration is not straightforward. Back-to-back balun structures can be used, but it only allows two port S-parameter measurement. Therefore, two-port characterisation structures with 50 Ω on-chip terminations are used for the measurement of amplitude and phase imbalances in the balun. Good agreement is found between the simulation and the measured results. The comparison of the measurement results of the baluns implemented in the two processes is presented in Table 4.4. From the measurement results, it can be said that it is possible to achieve similar performances for the baluns in both the processes.

5

K-band frequency doubler implemented in SG13S process

5.1 Introduction

In microwave and millimetre-wave receiver systems, spectrally pure high-frequency signal sources are required. At this high frequency, it is difficult to design a voltage-controlled oscillator with good phase noise, wide tuning range and flat output power. To mitigate this problem, frequency multipliers are used with a low-frequency fundamental signal source which relax the design constraints of a VCO. Frequency multipliers are non-linear circuits which translate a low-frequency signal to a higher frequency. Frequency multipliers with large multiplication factors degrade the phase noise of the signal and have low conversion gain. To design a frequency multiplier with a large

multiplication factor in one step, high-power input signals are required to drive the device into highly non-linear regions. Instead, several frequency doublers are cascaded to generate a higher-order frequency multiplier. Therefore, broadband frequency doublers with high conversion gain and efficiency are required with low-frequency stable VCOs to provide a cost-effective solution.

A frequency doubler circuit is considered as an archetype for non-linear circuits which allows the study of harmonics. As stated in the previous chapters, a frequency-doubler circuit is implemented in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes, to study the linearity that could be achieved in both processes. This chapter focuses on the design and implementation of a frequency doubler in the K-band range in the SG13S SiGe HBT process. The important design considerations, design flow, issues of the layout to achieve low imbalance, details of the biasing are discussed. The aim of the frequency doubler design is to achieve large odd-harmonic suppression over a large bandwidth.

5.2 Specification

The design specification of a frequency doubler depends on the targeted application. Based on a literature review of the different performance parameters of state-of-the-art frequency doublers, the design specification for the frequency doubler is summarised in Table 5.1. The input frequency range for the K-band doubler is from 7 to 15 GHz and the output frequency range is between 14 and 30 GHz, which covers a significant part of the K-band. More than 30 dB odd-harmonic rejection is targeted, such that the overall linearity of a system such as a wireless transmitter or receiver could be maintained. It is desirable to achieve conversion gain for the frequency doubler to be able to drive the next block (usually a mixer) in a system. A supply voltage of 1.7 V is selected for the push-push doubler as the maximum BV_{CEO} for a single HS-HBT in the SG13S process is 1.7 V.

Table 5.1: Design specification for the frequency doubler.

Parameter	Specification
Harmonic rejection (dB)	30
Bandwidth (GHz)	14 to 30
Conversion Gain (dB)	> 0
Supply voltage (V)	1.7
DC power consumption (mW)	< 20

5.3 Design

The details of the implementation of the design, design flow and the P-cells for the layout are discussed in this section.

5.3.1 Implementation

The main design objective of a frequency doubler is to achieve large odd-harmonic suppression over a broad band. Frequency doublers can be broadly classified into two types: active and passive. From the literature review discussed in Chapter 2, it is evident that passive frequency multipliers can provide a large bandwidth but they suffer from conversion loss. Particularly a frequency doubler consists of an input balun, a pair of anti-parallel diodes, and an output balun to combine the two 180^o out-of-phase second-harmonic signals [141–143]. They usually need high input power, occupy a large area, and suffer from conversion loss. The active frequency doublers utilise the non-linearity of the transistors, have the capacity to provide conversion gain and occupy a small area [84–86].

As discussed in Chapter 3, a balanced frequency doubler can cancel the odd harmonics inherently. For the implementation of a K-band frequency doubler, a balanced topology is selected to take advantage of this inherent odd-harmonic cancelling property. A passive balun is used for generating the differential signals as it is more linear than an active balun, but the passive balun suffers from its conversion loss. Hence, an active frequency-doubler topology is used with a passive transformer balun to attempt to get the best of both when it comes to the overall linearity of a system.

The transformer balun design over 7-15 GHz as discussed in section 4.5 is used

with the K-band frequency doubler. A balanced frequency doubler is designed using a simple push-push configuration (analysis of harmonics shown in Chapter 3). The schematic diagram of the frequency doubler is depicted in Fig. 5.1.

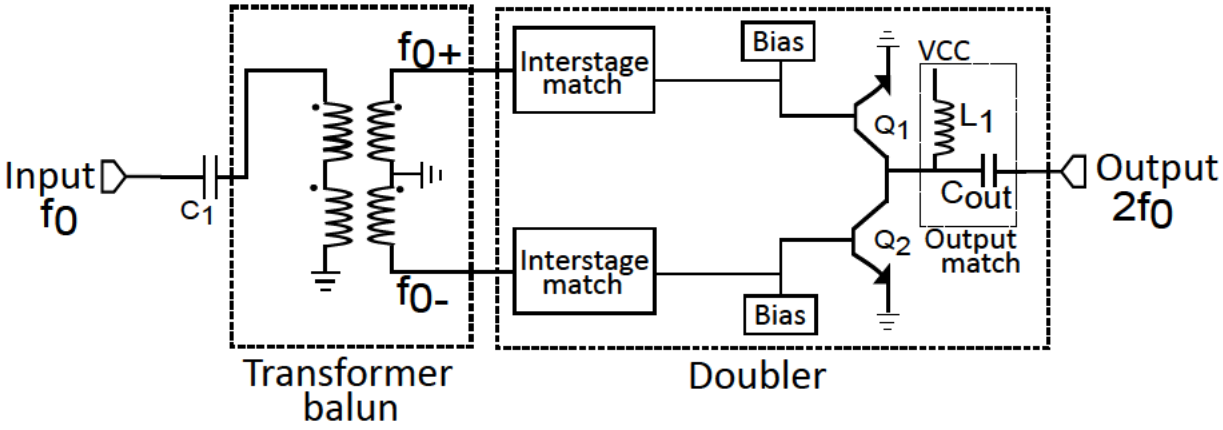


FIGURE 5.1: Schematic of the designed frequency doubler.

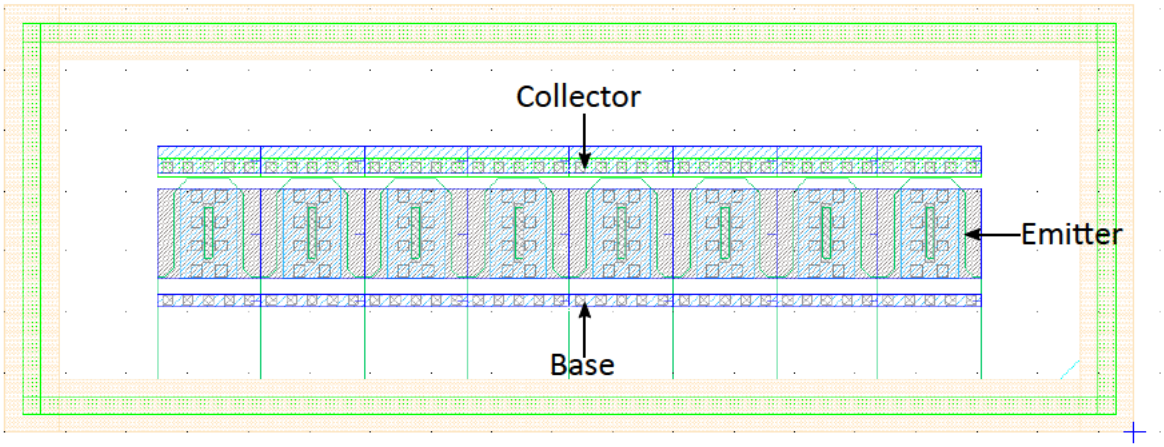


FIGURE 5.2: Layout of a single transistor as used in the frequency-doubler core.

For the K-band frequency doubler, the input frequency range is selected to be from 7 to 15 GHz, for which the output is from 14 to 30 GHz. The doubler core consists of two identical SG13S SiGe HBTs (referred as Q_1 and Q_2 henceforth) in the common-emitter configuration. Each SG13S SiGe HBT consists of 8×0.84 μm emitters, where 0.84 μm is the emitter length and 8 stands for the multiplicity of emitters. The maximum collector current for each of Q_1 and Q_2 at f_T is 16 mA (2 mA $\times$ N_x) for V_{CE} of 1.2 V (details in

Appendix B). The layout of a single transistor is shown in Fig. 5.2. The emitters of Q_1 and Q_2 are connected to ground. The collectors are shorted together and connected to the supply voltage through an inductive load (L_1) as shown in Fig. 5.1. The output is taken from the collector. DC bias is provided at the base of the transistors, as shown in Fig. 5.3. Transistors Q_3 and Q_4 are used for setting the biasing current in the doubler core by the current-mirroring technique. In order to study the effect of the bias voltage at the base of Q_1 and Q_2 on the harmonics at the doubler output, the bias is not shared. Two separate bias lines are provided for the two transistors in order to have a control on the base bias.

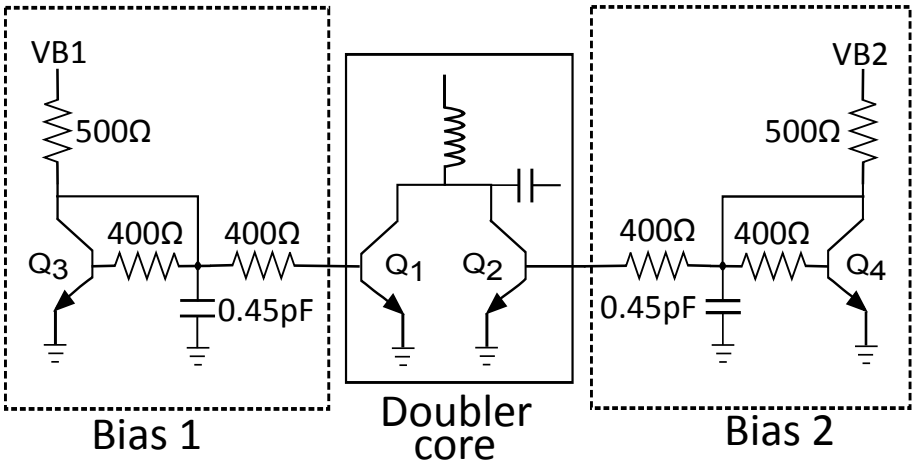


Figure 5.3: Biasing circuit of the frequency doubler.

There is an impedance mismatch between the differential outputs of the transformer balun (100 Ω) and the high-impedance input at the base of Q_1 and Q_2. As the input impedance looking into the base of each of Q_1 and Q_2 is in the order of kΩ, increasing the number of turns of the transformer balun does not help in impedance matching. An impedance matching network is needed between the differential output of the transformer balun and the input at the bases of Q_1 and Q_2. Series-parallel capacitors ($C_2 - C_7$) along with resistors ($R_1 - R_2$) are used for impedance matching. The series capacitors ($C_6 - C_7$) also help in DC blocking. The matching circuit is depicted in Fig. 5.4. Although there is some signal loss due to the grounded resistors, this interstage matching circuit helps in matching over a wide band.

A series capacitor (C_1) is used at the input of the transformer balun to provide impedance matching with the input 50 Ω termination as shown in Fig. 5.1.

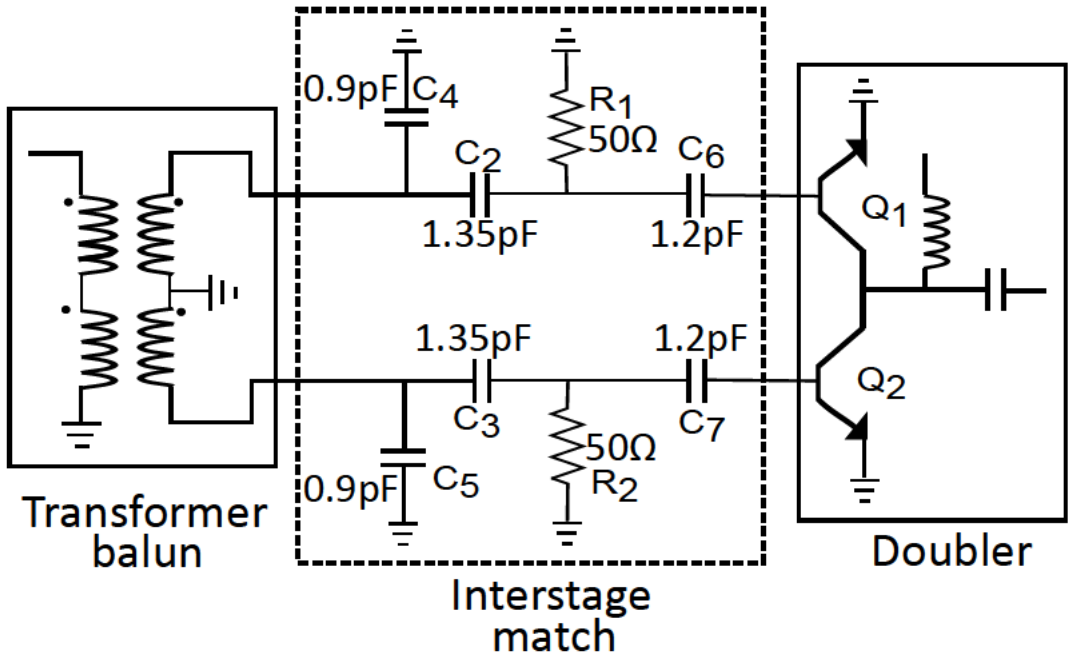


FIGURE 5.4: Interstage matching circuit of the frequency-doubler.

The inductor L_1 and capacitor C_{out} at the common-collector terminal, as shown in Fig. 5.1, helps in matching. The inductance and capacitance values are tuned to select the desired second-harmonic frequency band. As the primary objective of this work is to study the harmonics, an additional matching network is not used at the output because the matching network also provides some filtering effect.

As mentioned previously, the primary design objective of the frequency doubler was to achieve large odd-harmonic rejection over a wide band, so a balanced doubler topology was selected. Not only are identical transistors Q_1 and Q_2 needed for the doubler design, but it is also important to maintain a symmetrical layout. The challenges in the layout of the doubler and the effect on the odd-harmonic rejection will be discussed in the following sections.

The input frequency range of the doubler is between 7 GHz and 15 GHz while the output is from 14 GHz to 30 GHz. The higher end of the fundamental frequency (14 to 15 GHz) at the input and the third harmonic at the lower end (21 to 30 GHz) fall

within the desired frequency range of the doubler at the output (14 to 30 GHz). For such a broad-band doubler design, filters cannot provide an effective solution as the fundamental and the third harmonics sometimes fall into the desired frequency band. To achieve a wideband frequency response for the doubler, the "staggered tuning" technique is adopted.

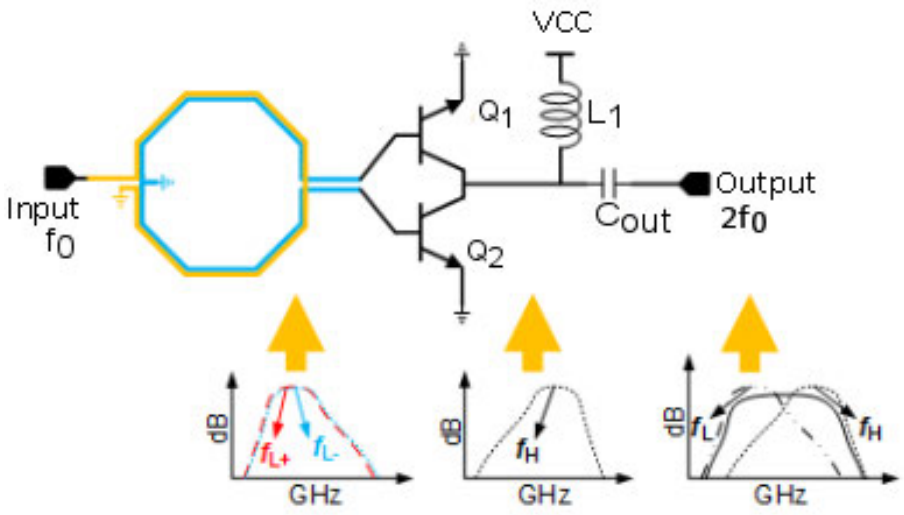


Figure 5.5: Simplified schematic of the proposed staggered tuning frequency doubler.

The idea of "stagger tuning" is illustrated in Fig. 5.5. The output of the transformer balun is matched over 7 to 9 GHz while the inductor L_1 at the output of the frequency doubler is matched over 14 to 15 GHz. The transformer balun and the frequency doubler are optimised together to provide a flat second-harmonic response. These designs can be sensitive to process variation which would be a limiting factor in the successful use of staggered tuning.

As illustrated in Fig. 5.5, there is a design tradeoff between the output power and gain flatness of the designed frequency doubler. Based on the different design specifications, the inductance value of L_1 can be selected. In Fig. 5.6, the simulated output power of the designed frequency doubler is plotted as a function of input frequency with varied load inductance. As demonstrated, the overall bandwidth of the frequency doubler can be significantly affected by the selection of load inductance. Therefore, the bandwidth of the balun needs to be optimised together with the frequency doubler

for a flat second harmonic at the output of the doubler.

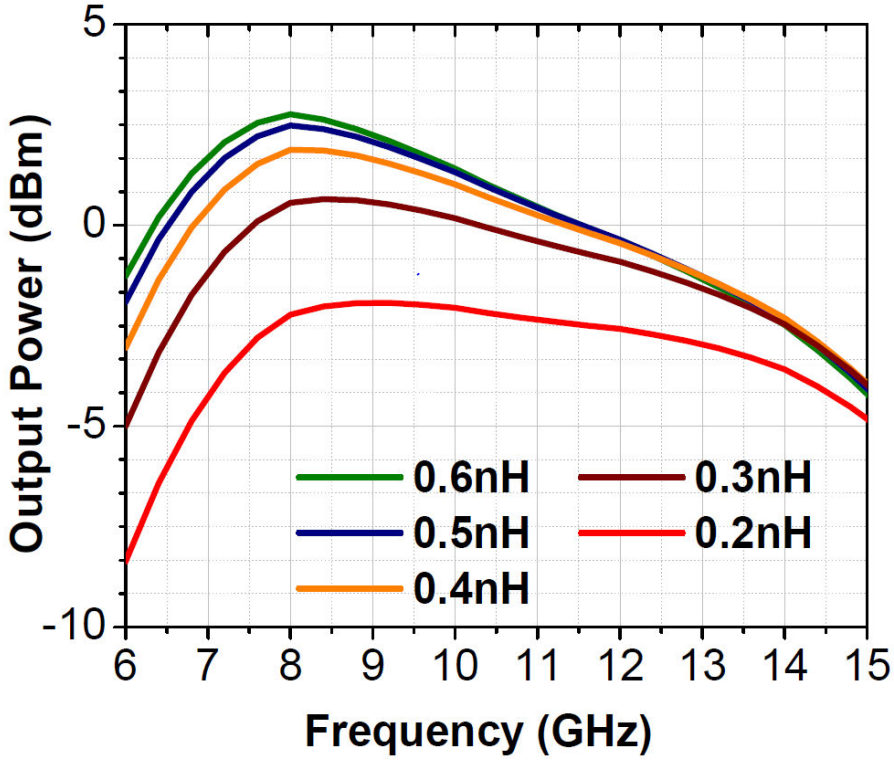


FIGURE 5.6: Simulated output power of the frequency doubler in terms of second harmonic as a function of input frequency with swept inductance value of L_1.

5.3.2 Design flow

Design flow is an important principle which involves a number of steps to do efficient design. It is very important to work out a strategy to implement the design, starting from the schematic to generation of the GDSII for tape-out. About 70% of the design cycle time is spent in floorplan, layout and post-extraction simulation. A proper design flow leverages the efficient design process, minimising the overall design time.

To start with the design of the frequency doubler the schematic is first simulated in AWR. The schematic is designed using the closed-form models of the circuit elements from the IHP SG13S library. The transformer balun is used as a parameterised-cell (P-cell) component. P-cells have the flexibility of changing some parameters. For example, for the transformer balun different parameters, such as the radius of the primary and

secondary coils, the metal width of the coils, the position of the centre-tap of the secondary, are parameterised. The frequency doubler is simulated together with the transformer balun and the interstage matching network. Depending on the simulation results some values of the circuit elements and the parameters of the P-cell are tuned to meet the specifications.

In the next step, the whole schematic is divided into sub-blocks. Each of these sub-blocks constituting the RF part of the frequency doubler is replaced by its layout one by one. Layout Versus Schematic (LVS) and Design Rule Check (DRC) are verified using ICED as each of the sub-blocks is added. Once the layout of all the sub-blocks is constructed, the EM structures are created, drawn in Axiem.

The EM structures of the sub-blocks are drawn in the same way as their layout. In the circuit schematic, all the sub-blocks lying in the RF path are replaced by the EM structure, one by one. The EM simulation involves some iterations. Once a sub-block in the circuit schematic is replaced by its corresponding EM structure, the whole circuit is simulated. The EM structures are modified so as not to change the simulation results. Optimisation is also performed at this stage. Gradually all the sub-blocks with closed-form elements in the schematic are replaced by their EM structures. Then the EM simulation result for the frequency doubler with the transformer balun is considered as the reference simulation result.

To get an accurate estimation of the performance of the frequency doubler, the whole circuit should be simulated as one single EM block. EM simulation is very time-consuming and this becomes a constraint for designers managing a large design. To mitigate this problem, the entire circuit is divided into sub-blocks, even though this is not 100 % accurate, but it helps in faster simulations. The whole circuit should be divided into sub-blocks such that the overall simulation result will not be affected to a large extent. With a 64-bit operating system, 16 GB RAM, Intel i7 processor, the EM simulation for the frequency doubler would take more than an hour to finish. To further increase the simulation speed, Shape Preprocessing (SPP) rules are written for the EM structures. SPP rules provide simplification of the geometry drawn in the EM structure. For example, instead of simulating each of the actual metal layers the corresponding

EM layers are used for EM simulations. All the passive structures including the metal layers, vias, MIMcaps, resistors (Rsil, Rppd, Rhigh) that are available in the SG13S SiGe HBT process can be processed by the SPP rules.

After the RF part of the entire frequency doubler circuit is constructed in layout and the EM simulation is carried out, the biasing circuits are laid out. In the circuit simulation, these biasing blocks are also replaced with EM structures. However, it has been found that the biasing circuits do not affect the simulation results as the RF parts are shielded by the ground ring (discussed in Section 5.4). Then the DC and RF pads are attached in the layout. LVS and DRC are checked for this entire circuit including the DC and RF pads. Finally, the GDS II file is generated for tape-out.

5.3.3 Verification of layout cells

As mentioned in Section 2.2, the SG13S SiGe HBT process offers a stack-up of five different thin metal layers (M1 to M5) and two thick metal layers (TM1 and TM2). Due to the availability of seven metal layers, there is more option for the routing in this process but the layout becomes a complicated task.

To make the layout of the frequency doubler faster and more efficient in the SG13S SiGe HBT process, a separate library is developed with some P-cells such as transmission lines, Tee junctions, and corners etc. These P-cell blocks are often used in the layout. They have the flexibility to change the metal layers and to change the length and width in order to fit into the appropriate space. Thus the dimensions and the metal layers of the P-cells are automatically modified and do not need manual drawing.

Another important P-cell included in the layout library is the ground ring. All the structures in the RF path are surrounded by the ground ring to provide shielding from any interference from the surrounding metal structures. The ground ring consists of a stack-up of all the seven metal layers up to the substrate. Unlike the GaAs process, as there is no solid ground underneath the substrate, a continuous metal layer is drawn below the transmission lines and connected to the ground ring. This metal layer creates a ground plane beneath the transmission line. This is demonstrated in Fig. 5.7 in which

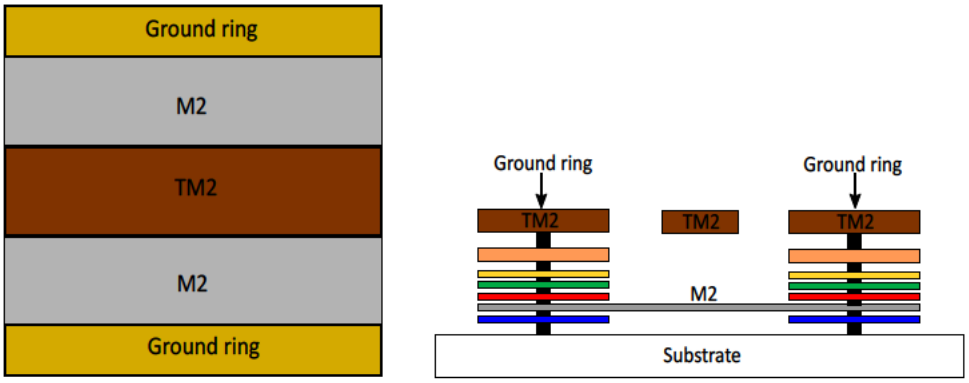


FIGURE 5.7: Diagram of a transmission line (a) P-cell (b) cross-sectional view.

the transmission line is implemented in TM2 and the ground plane in M2.

This approach of using the P-cells makes the layout faster and easier as the use of some of these common P-cells saves time for repeated manual drawing. It also reduces the chance of making DRC errors in a large layout, as the P-cells are already verified by DRC checker. These P-cells (originally developed at DSTG), are at first tested as individual units, debugged (if needed) and improved for different applications. Then these P-cells are used in the layout of the frequency doubler.

5.4 Final circuit layout

The layout of the frequency doubler is accomplished at few levels of hierarchy. The whole frequency doubler design along with the transformer balun is divided into few sub-blocks.

- At first the layout of the sub-blocks lying on the RF path of the doubler are finished.
- In the next level, the interconnections between all the sub-blocks are established.
- Then the bias lines are implemented.
- Finally at the top level, the GSG pads, the DC pads, ESD protection diodes are added and the layout is finalised.

- LVS and DRC are checked at every step to avoid errors.

Some layout rules are developed at the very beginning. These conventions are then followed throughout the layout. For instance, all the interconnections between the sub-blocks on the RF path are implemented in TM1 and TM2, as these metal layers can handle more current than the thin metal layers and also the parasitic capacitance to the substrate is less.

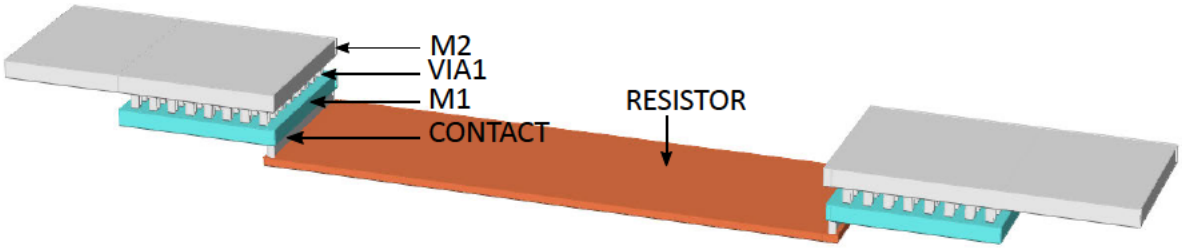


FIGURE 5.8: Connection of a resistor in M2 layer.

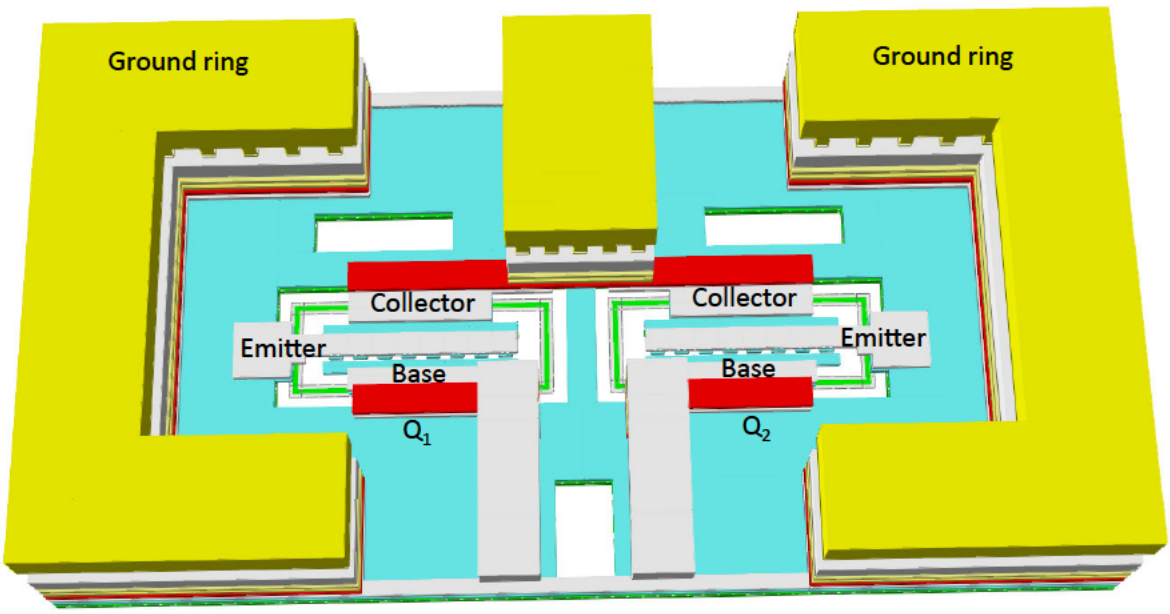
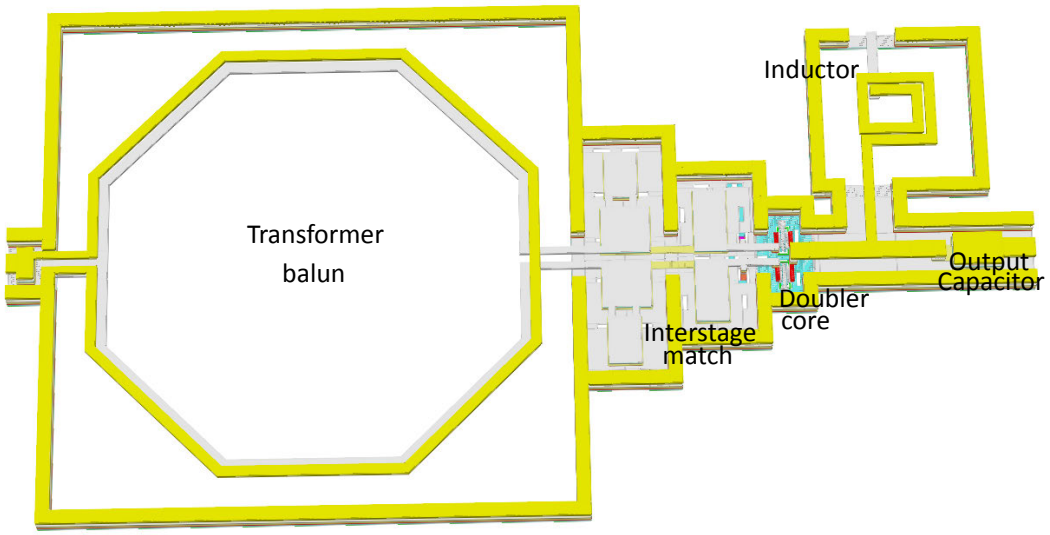


FIGURE 5.9: Layout of the doubler core.

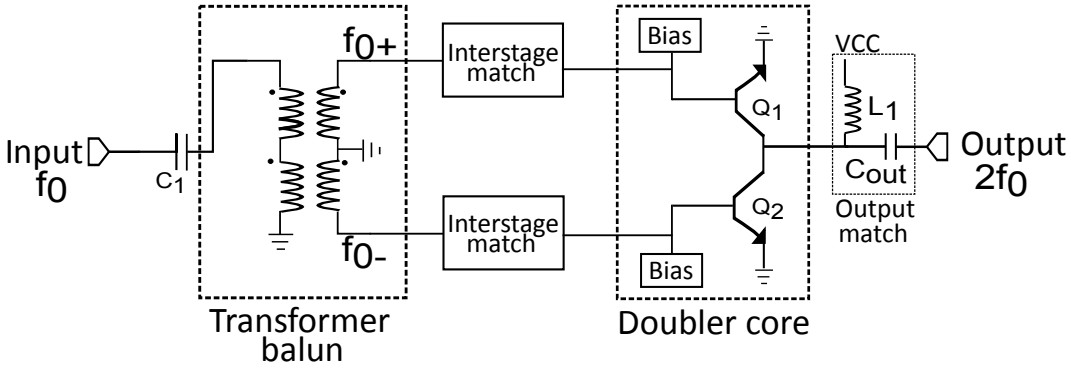
The connections with the resistors and the transistors are difficult to deal with. The metal layers need to be cut out at the location of the resistors and transistors

as they are situated beneath the metal layers. For the resistors, interconnections are established using M1 or M2 by using vias all the way down to their contacts. One such resistor connectivity is shown in Fig. 5.8. Typically for an HBT in the SG13S SiGe HBT process, the emitter connection is implemented in M1 while the base and the collector terminals are implemented in M2. The doubler core is shown in Fig. 5.9, which depicts that the layout of this sub-block is symmetric.

Passive structures such as inductors are drawn in the TM2 or TM1 layers. They are also surrounded by the ground ring to protect them from external interference.



(a)



(b)

Figure 5.10: The frequency doubler design (a) layout of the RF chain, (b) schematic diagram.

As the metal layers are pre-decided for some of the connections, it saves time for the layout. A bottom-up approach is followed for the overall layout of the frequency doubler. Symmetry of layout is maintained throughout, as it has been found critical for the balance in the differential signal in the two signal paths. The layout of the RF chain for the frequency doubler and the corresponding schematic diagram of the frequency doubler circuit is shown in Fig. 5.10(a) and Fig. 5.10(b) respectively. The details of the biasing line and the pads are not shown for simplicity.

As shown in Fig. 5.10(a), symmetry is maintained throughout the layout along a horizontal line through the transformer balun, interstage matching circuit, doubler core. The inductor is shifted upward to make a connection with the DC pad, symmetry could not be maintained at this stage which is a layout constraint.

In the SG13S SiGe HBT process, the whole chip is filled up with metal density filler to satisfy the design rule. This adds extra complication to the layout and could be detrimental to the tape-out success. Specific no-filler metal layers must be added in the specific regions of the layout such as RF path to avoid unwanted short circuit connections.

5.5 Harmonic rejection simulation and measurement

The comparison of the simulated and the measured results are presented in this section. Off-chip SOLT calibration is used for the measurement. For the measurement of the doubler, a Keysight E8257D signal generator suitable for 50 GHz measurement is used to provide the input signal and the harmonics were measured using a Keysight PXA Signal Analyzer, N9030A, (3 Hz-50 GHz).

5.5.1 Frequency sweep

For the purpose of simulation, the frequency-doubler circuit with the transformer balun is divided into a few sub-blocks. Each of these sub-blocks is replaced by their corresponding EM structure. The supply voltage (VCC) of 1.7 V is used, as the maximum BV_{CEO} is 1.7 V as per the foundry limit. Two separate bias lines VB_1 and VB_2 are

used to control the bias of the two transistors used in the doubler core. This test bench is shown in Fig. 5.11.

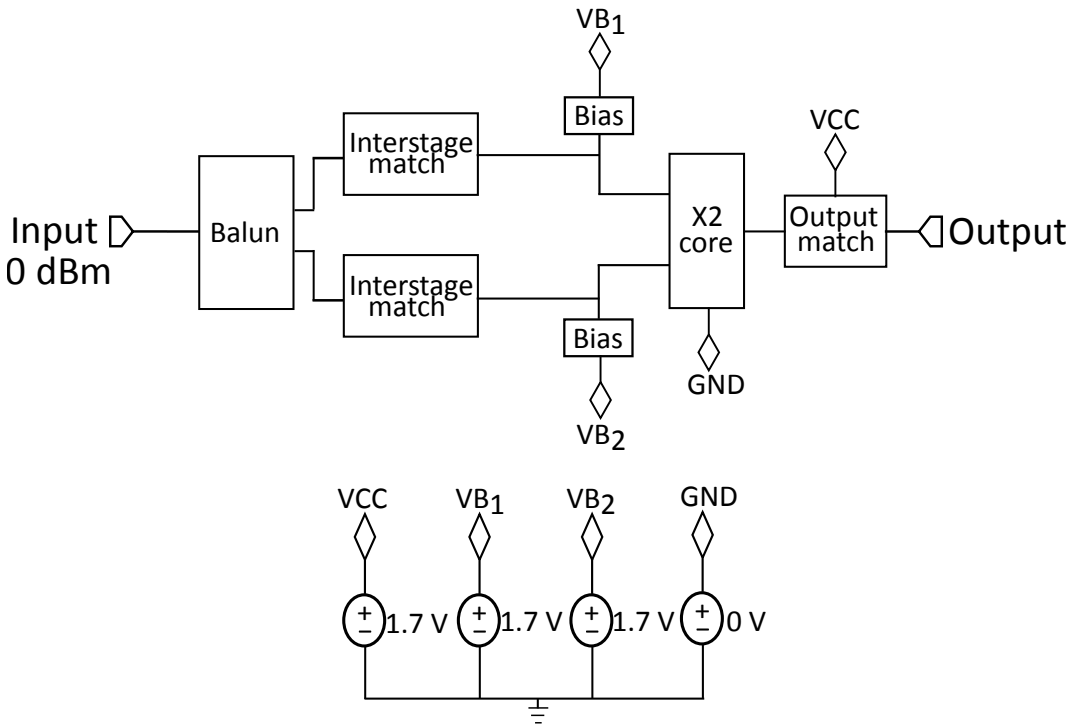


Figure 5.11: Test-bench for simulating the harmonics with 0 dBm input.

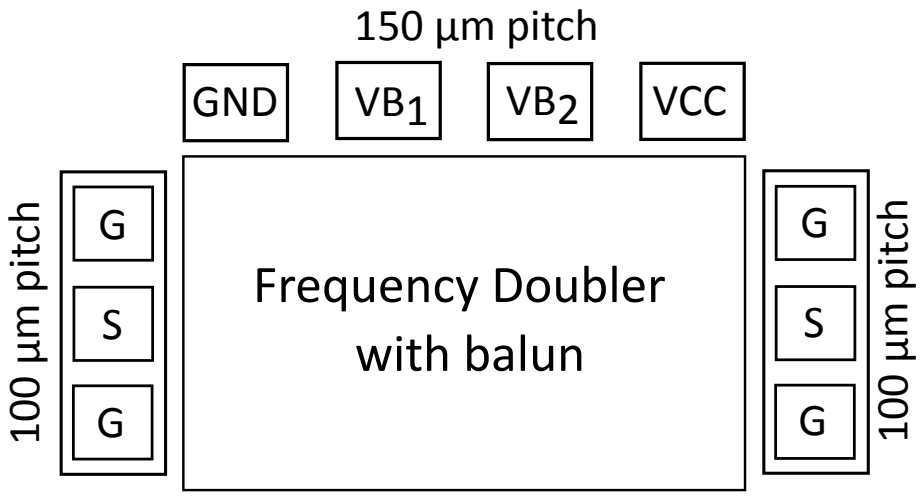


Figure 5.12: Pin configuration for measurement of the frequency doubler.

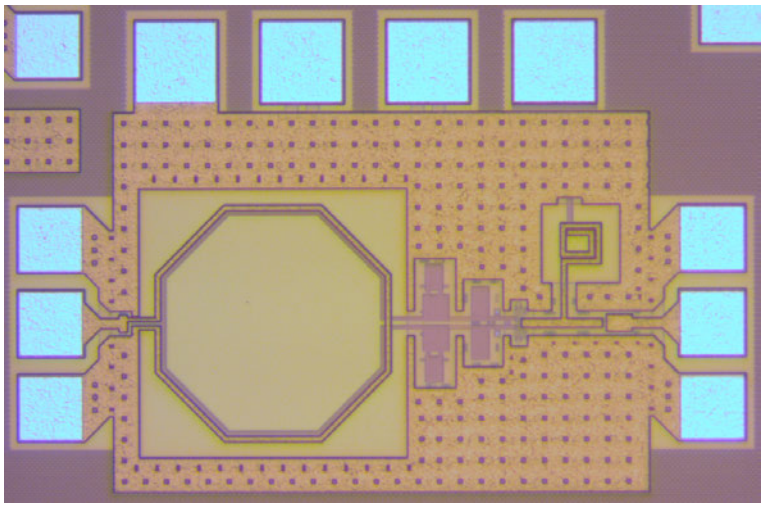


FIGURE 5.13: The die-photo of the frequency doubler.

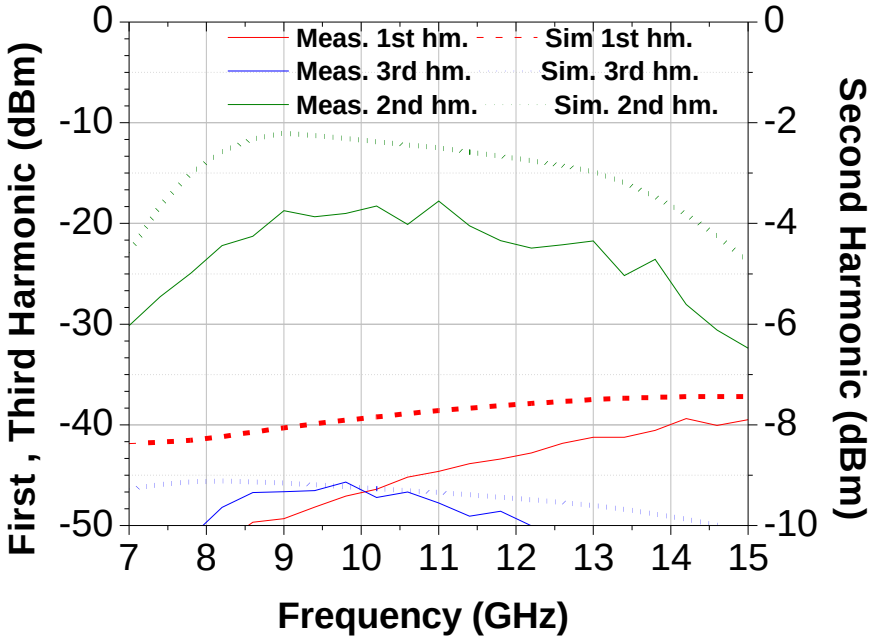


FIGURE 5.14: Output power of harmonics as a function of input frequency, measured (solid) and simulated (dotted), fundamental (red lines), second harmonic (green lines) and third harmonic (blue lines).

The pin configuration of the frequency doubler with the transformer balun is shown in Fig. 5.12. For the measurements, the required DC voltages are provided through a DC probe in the GPPP configuration. A pair of GSG probes (suitable for measurements up to 67 GHz, from GGB Industries) is used to provide the input signal to the frequency

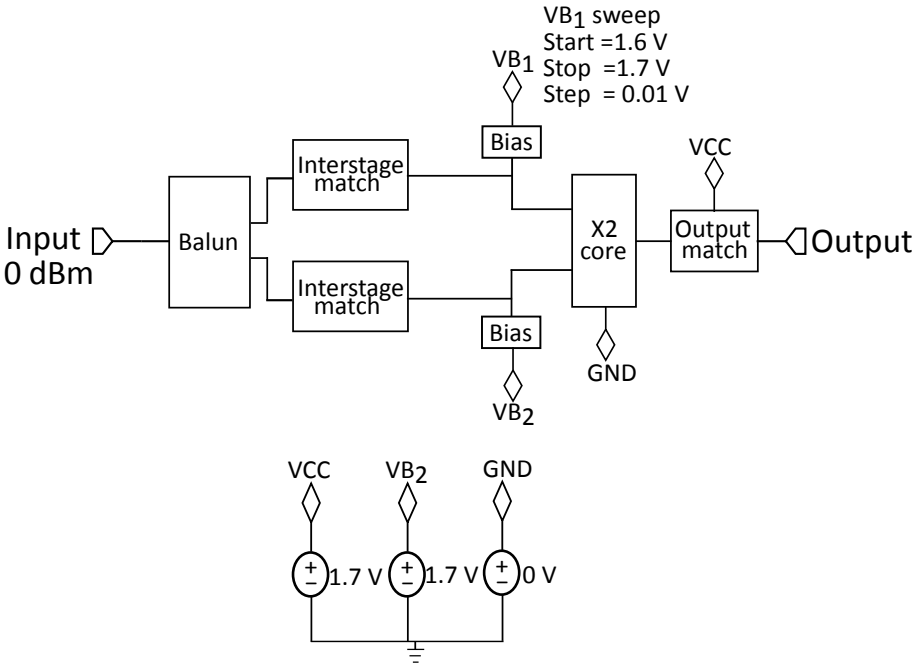
doubler and to measure the output signal. The die-photo of the frequency doubler with the transformer balun is shown in Fig. 5.13.

The simulation results suggest at least 35 dB odd-harmonic suppression across the frequency band from 7 to 15 GHz for 0 dBm input. The total power consumption of the frequency doubler at 11 GHz for 0 dBm input is 23.5 mW from a 1.7 V supply voltage. The comparison between the simulation and measurement results is depicted in Fig. 5.14. As seen from Fig. 5.14, the measured fundamental rejection is better than 35 dB and the third-harmonic rejection is better than 40 dB across the band.

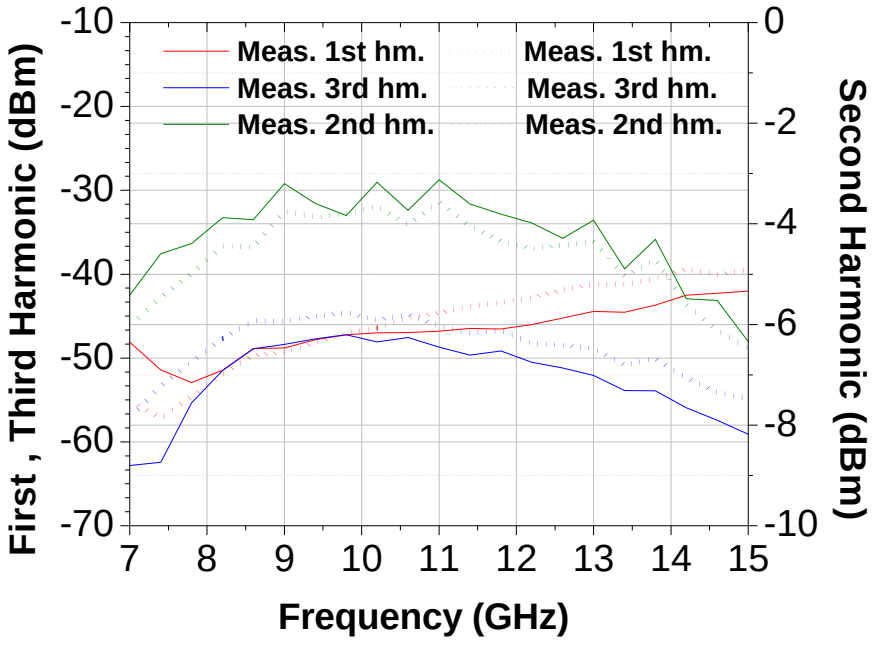
5.5.2 Bias offset

Two separate bias lines VB_1 and VB_2 are used to provide the DC bias at the base of the two transistors, Q_1 and Q_2, of the doubler core. Practically it is not possible to maintain absolute 100% symmetry in the layout. For instance, all the DC pads are aligned on the same side. Therefore, one of the bias lines is routed further than the other line. This creates a difference between the base bias voltages of the two transistors Q_1 and Q_2, which affects the odd harmonics at the output of the frequency doubler. To mitigate these effects, the base-bias voltage of one transistor is tuned such that a null point can be found where the two transistors would generate the same harmonics in the collector current. It causes better cancellation of the odd harmonics.

This concept has been tested in simulation and also verified in measurement. The simulated result corresponding to 1.68 V and 1.70 V at the two bias lines (VB_1 and VB_2) helped in increased odd-harmonic rejection. The simulation test-bench for the bias sweep is shown in Fig. 5.15(a). The comparison of the measured results for equal bias and different bias is shown in Fig. 5.15(b). As symmetry in the layout was enforced, only a slight improvement in the odd-harmonic rejection could be achieved by tuning the bias voltage. The fundamental and the third-harmonic rejection are improved by approximately 1 to 2 dB across the band, as shown in the measured results in Fig. 5.15(b).

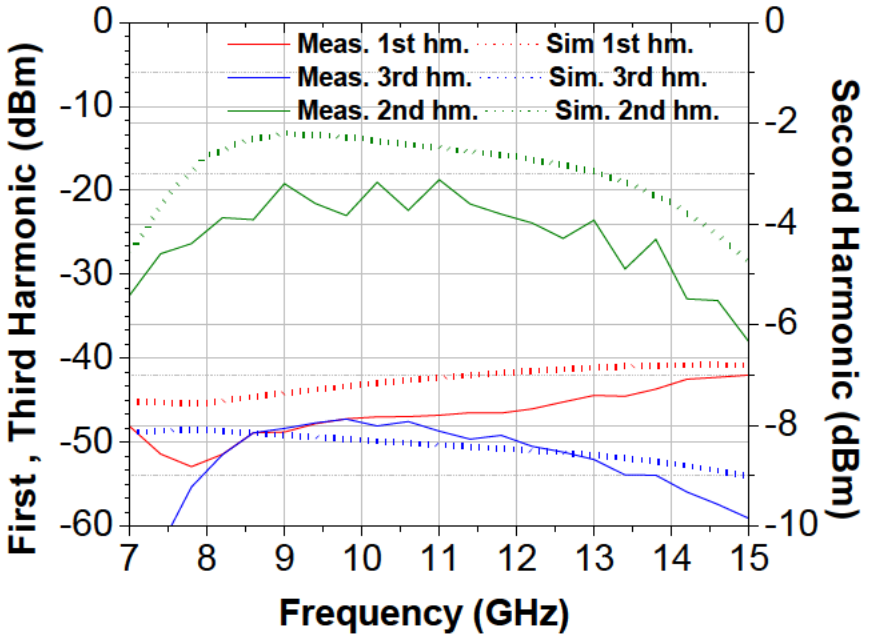


(a)

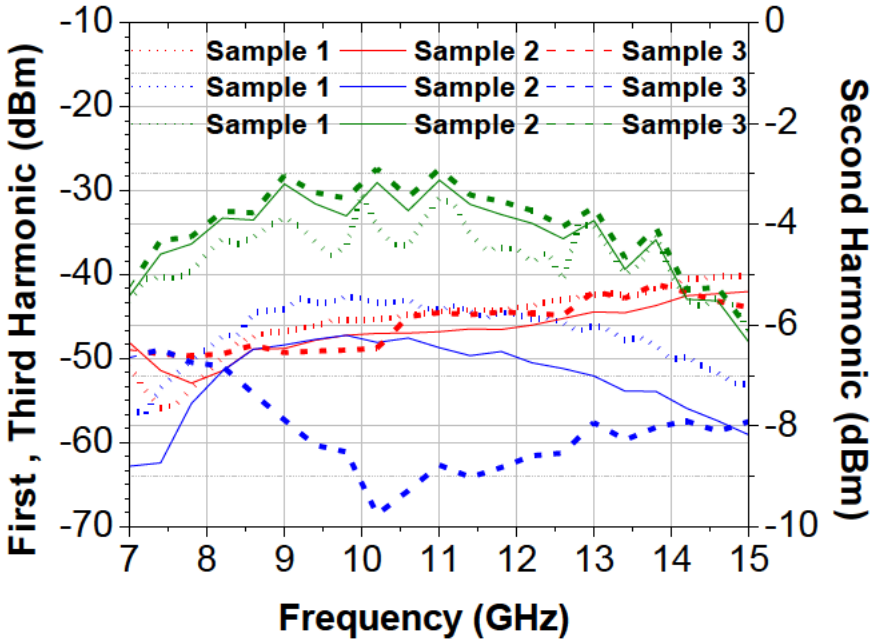


(b)

FIGURE 5.15: (a) Test-bench for simulating the harmonics with bias sweep, (b) Comparison of the measured results for the harmonics with equal and different bias, equal bias 1.7 V on each line (dotted), unequal bias 1.68V-1.70 V (solid). Fundamental (red lines), second harmonic (green lines) and third harmonic (blue lines).



(a)



(b)

FIGURE 5.16: Output power of harmonics as a function of input frequency with unequal bias, 1.68 V and 1.70 V: (a) comparison of measured (solid) and simulated (dotted) results, (b) measured results for three samples.

A comparison of the measured and simulated results with unequal bias 1.68 V (at VB_1) and 1.70 V (at VB_2)is illustrated in Fig. 5.16(a). To investigate the effect of process variation on the odd-harmonic rejection, three samples were measured as demonstrated in Fig. 5.16(b), under the unequal bias conditions. The mean trace shows a fundamental rejection of approximately 38 dB and a third-harmonic rejection of 45 dB across the band. The measured second harmonic power of -3.8 dBm is measured at the mid band for 0 dBm input. Although the desired target of more than 30 dB odd-harmonic rejection is achieved, the second harmonic power is low. This is mainly because of the output matching circuit which could be improved.

5.5.3 Input power sweep

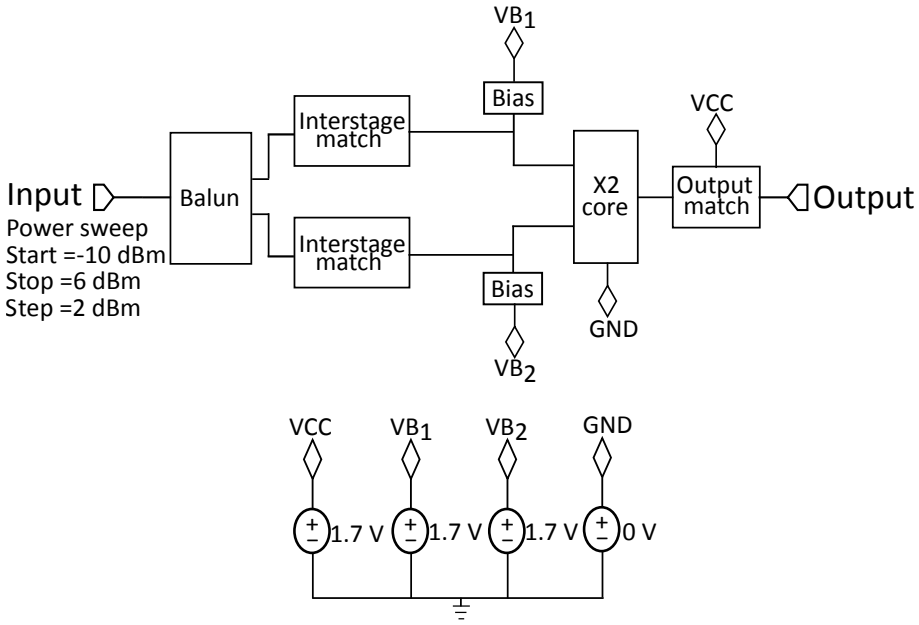
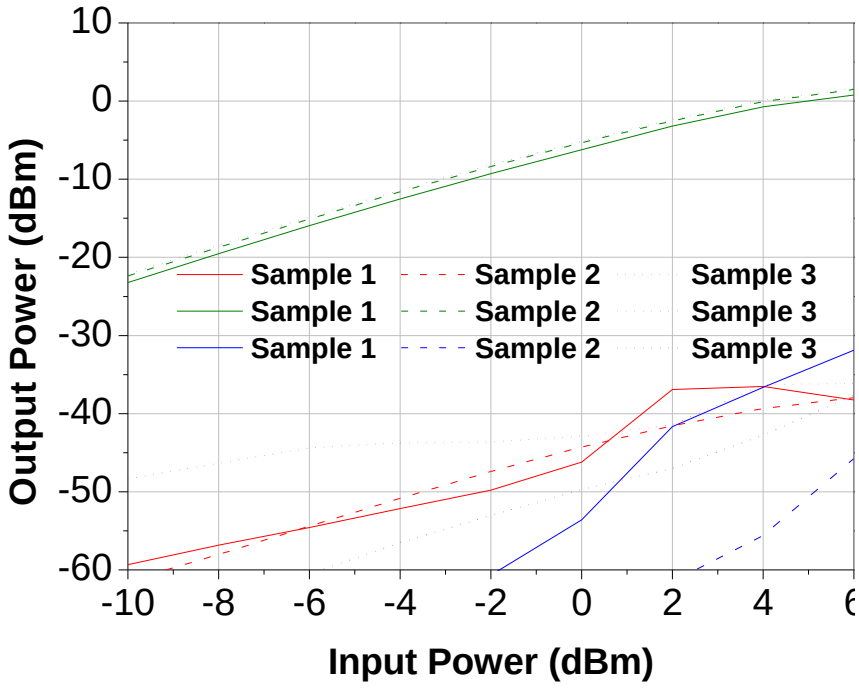
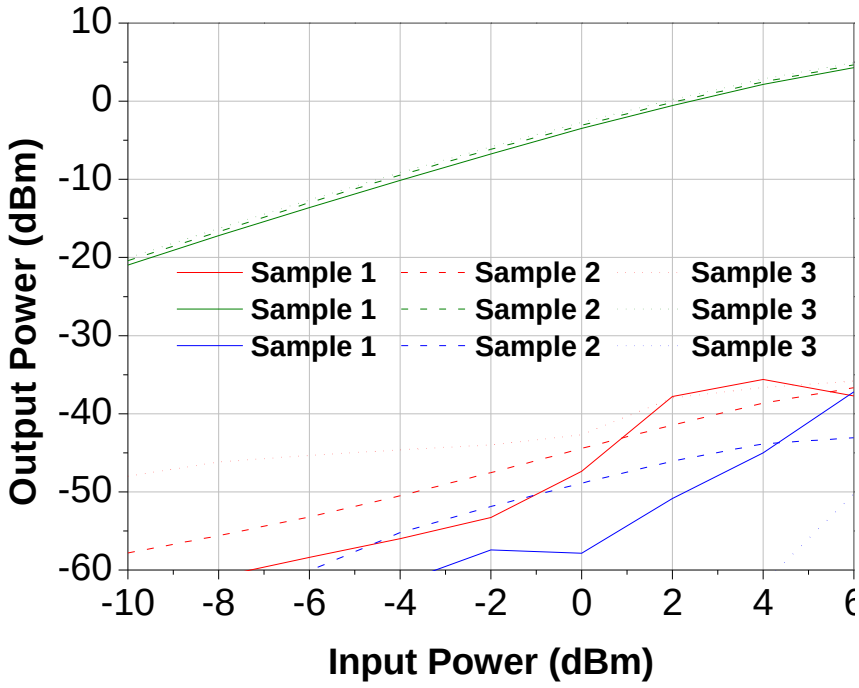


FIGURE 5.17: Test-bench for simulating the harmonics with input power sweep.

The magnitudes of the harmonics at the output of the frequency doubler not only depend on the balance of the differential signal, they are also dependent on the input power. For high input power, the level of the harmonics rises with a slope greater than that of the fundamental signal. In order to estimate the performance of the frequency multiplier, the input power is swept. The simulation test-bench is depicted in Fig. 5.17.



(a)



(b)

Figure 5.18: Output power of harmonics as a function of input power: (a) measured results of three samples for 7 GHz input, (b) measured results of three samples for 11 GHz input. Fundamental (red lines), second harmonic (green lines) and third harmonic (blue lines).

For the frequency doubler with 7 to 15 GHz input, the harmonics for 7 GHz, 11 GHz and 15 GHz input for an input power sweep from -10 dBm to 6 dBm are measured. The measurement results of three samples for each of these frequencies are shown in Fig. 5.18, Fig. 5.19.

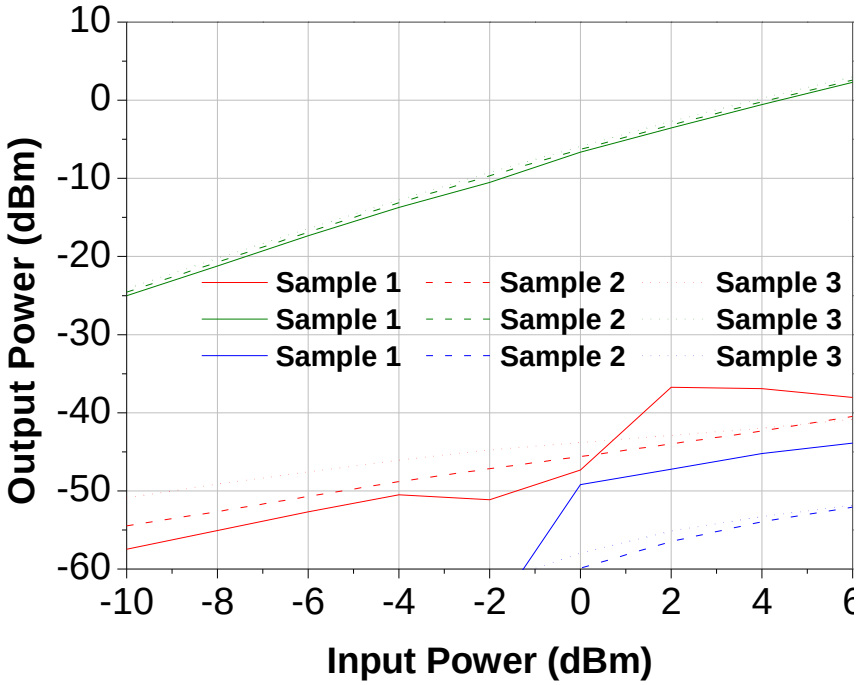


FIGURE 5.19: Measured results of output power of harmonics as a function of input power across three samples for 15 GHz input. Fundamental (red lines), second harmonic (green lines) and third harmonic (blue lines).

As seen from the measurement results in Fig. 5.18 and Fig. 5.19, the fundamental rejection is better than 35 dB and third-harmonic rejection is better than 40 dB for an input power sweep of -10 dBm to 6 dBm. This testifies that the designed frequency doubler has reasonable odd-harmonic rejection over a broad band. From the measurement results in Fig. 5.18 and Fig. 5.19, it can also be observed that for low input power level like -10 dBm, the second harmonic power at the output of the doubler is quite low. Gradually, with the increase in the input power, the level of second harmonic increases which is consistent with the theory.

The performance of the designed frequency doubler and a comparison with other

Table 5.2: Performance summary of the designed frequency doubler and comparisons with other state-of-the-art designs

Parameters	[144]	[85]	[54]	**This work**
Fund. rejection [dB]	14	26	27	38
f_{-3dB}[%]	43	41	50	73
DC pow. [mW]	66	22	37	12.75
V_{DD} [V]	2	2	2.7	1.7
Area [mm^2]	0.56	0.34	0.34	0.24
Tech. [nm]	180	130	130	130

state-of-the-art designs are summarised in Table 5.2.

5.6 Discussion and conclusion

The frequency-doubler design implemented in the SG13S SiGe HBT process is presented in this chapter. First, the design of a K-band balanced doubler (using the push-push topology) with 7-15 GHz input and 14-30 GHz output is shown. The transformer balun with excellent balance shown in Section 4.5 is used with the K-band balanced frequency doubler. The design flow used for the frequency-doubler design in the SG13S SiGe HBT process is discussed. A stagger tuning technique between the transformer balun and the doubler is adopted for a flat second-harmonic response over a wide band. Symmetry in the layout is found to be crucial in achieving good odd-harmonic rejection over a broad band. Asymmetry in the layout may lead to different bias voltages at the transistors in the doubler core. It has been found that the bias voltage of the two transistors can be tuned to overcome the effect of asymmetry in the layout. A fundamental rejection of at least 38 dB and more than 40 dB third-harmonic rejection is measured across the output band. This indicates that the balance in the differential signals is indeed critical for the odd-harmonic rejection at the output of the frequency doubler. Also, good agreement between the simulated and the measured results justifies the design flow. In the next chapter, a frequency-doubler design in the PP10-10 GaAs pHEMT process will be presented.

6

K-Ka band frequency doubler implemented in PP10-10 process

6.1 Introduction

In the MMIC design, GaAs process has been widely used over last few decades. In a millimetre-wave transceiver system, a frequency doubler circuit is an important building block which is used with a low-frequency and spectrally pure VCO. A frequency-doubler circuit is considered as an archetype for non-linear circuits, which allows the study of harmonics as discussed in Chapter 5, where a frequency-doubler design in the SG13S SiGe HBT process is discussed. This chapter focuses on the design and implementation of a frequency doubler in the PP10-10 GaAs pHEMT process. The frequency doubler is designed using 0.1 μm pHEMTs in the K-Ka band range. For the

purpose of comparison of the frequency doublers in the two processes, the SG13S SiGe HBT and the PP10-10 GaAs pHEMT, an overlapping input frequency band is chosen. The input frequency range of the doubler in the PP10-10 GaAs pHEMT process is from 11 to 20 GHz while the output is from 22 to 40 GHz. The important design considerations, design flow, and critical issues with the layout are described.

6.2 Specification

The design specification of the frequency doubler depends on the application. For the purpose of comparison with the frequency doubler implemented in the SG13S SiGe HBT process, a K-Ka band frequency range is targeted. Based on a literature review, the intended design specification for the frequency doubler using pHEMTs for this work is summarised in Table 6.1. More than 30 dB odd-harmonic rejection is targeted similarly to the frequency doubler in the SG13S SiGe HBT process. It is also desirable to achieve conversion gain to be able to drive the next block in a system design. A supply voltage of 4 V is selected for the push-push doubler as the maximum BV_{DS} for a single pHEMT in the PP10-10 GaAs pHEMT process is 4 V.

Table 6.1: Design specification for the K-Ka band PP10-10 frequency doubler.

Parameter	**Specification**
Harmonic rejection (dBc)	30
Bandwidth (GHz)	20 to 40
Conversion Gain (dB)	> 0
Supply voltage (V)	4
DC power consumption (mW)	< 100

6.3 Design

The details of the implementation of the design and the design flow is discussed in this section.

6.3.1 Implementation

In wireless communication systems, frequency multipliers are often used with low-frequency local oscillators to relax the design constraints of VCOs. One of the main objectives of a frequency doubler is to achieve large odd-harmonic suppression over a broad band. Designs of both passive and active frequency multipliers in MMIC are found in the literature. The design of varactor-based monolithic doublers has been reported in [145]. Active frequency doublers based on transistors are favoured for better conversion gain. Single-ended MMIC frequency doublers using pHEMTs are reported in [146–148], while [65, 67, 69, 149] show balanced frequency doublers. Based on the literature review it is evident that the balanced topology can be used for good odd-harmonic rejection without the need of an additional filter.

An analysis for the balanced frequency doubler using PP10-10 GaAs pHEMTs is shown in Section 3.3. Theoretically, if an ideal differential signal is fed to a pair of identical field effect transistors, the odd harmonics are cancelled inherently at the combined drain. Based on that analysis, a balanced topology is adopted for the frequency-doubler design in the PP10-10 GaAs pHEMT process, implemented using two pHEMTs in the push-push configuration. An active balun using transistors can provide conversion gain but transistors introduce non-linearity into the response. As the main objective of studying the frequency doubler is to analyse the harmonics, so an active balun is not used with it (similar to the frequency doubler in the SG13S SiGe HBT process). A passive balun is selected for generating the differential signal due to its having better linearity than an active balun. The U-shaped transformer balun implemented in the PP10-10 GaAs pHEMT process, as presented in Section 4.6, is used along with the balanced frequency doubler. Hence an active frequency-doubler topology is used with a passive transformer balun to attempt to get the best of both when it comes to the overall system linearity. The schematic diagram of the frequency doubler is depicted in Fig. 6.1.

For the K-Ka band frequency doubler, the input frequency range is selected from

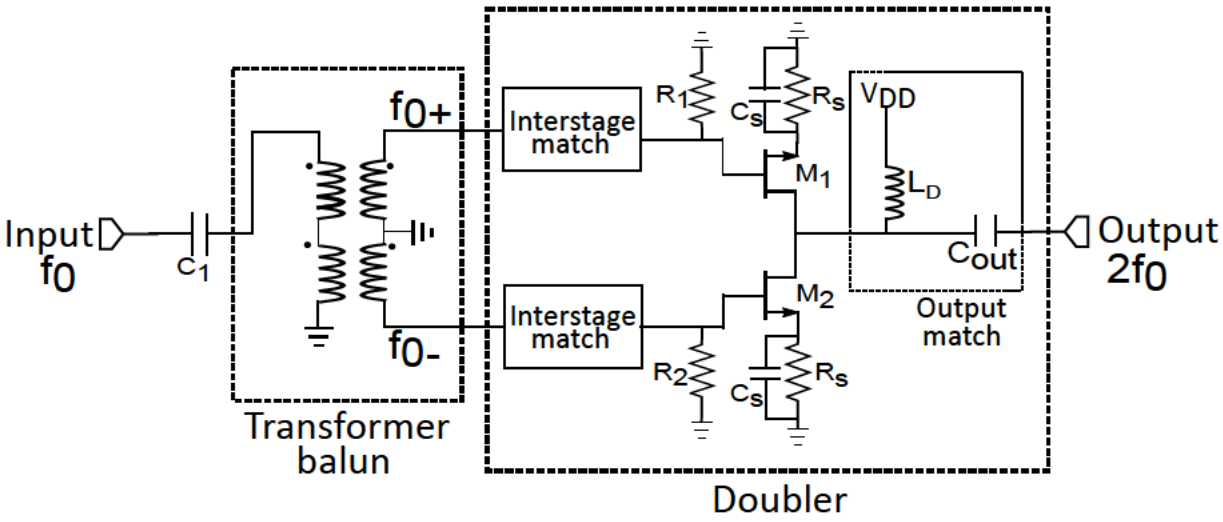


FIGURE 6.1: Schematic of the designed frequency doubler.

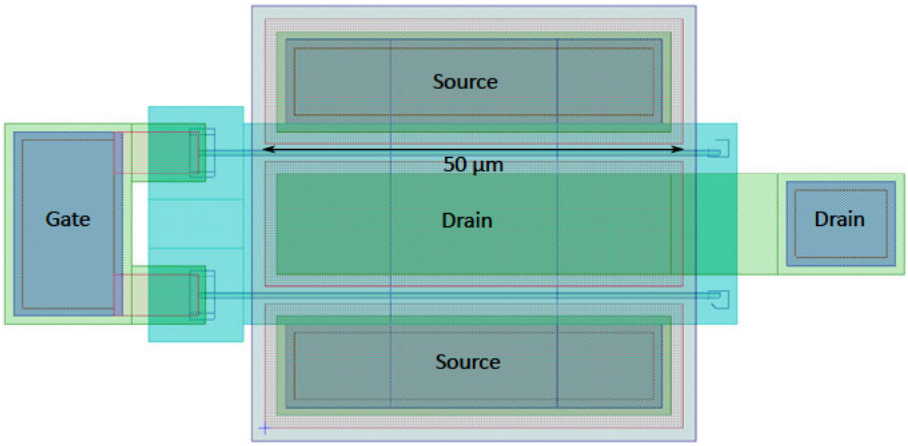


FIGURE 6.2: Layout of a single transistor used in the frequency doubler.

11 to 20 GHz for which the output is from 22 to 40 GHz. The U-shaped transformer balun (shown in Section 4.6) with 10 to 20 GHz input is used to drive the frequency doubler.

The doubler core consists of two identical PP10-10 GaAs pHEMTs (referred as M_1 and M_2 henceforth) in the common-source configuration. Each pHEMT consists of 2 fingers with a 50 μm unit gate width (UGW). The layout of one such single PP10-10 GaAs pHEMT is shown in Fig. 6.2. The drains of the transistors are connected together to cancel the odd harmonics, as suggested in the doubler analysis (Section 3.3). The common drain node is connected to the power supply through an inductor (L_D) as shown in Fig. 6.1. The output is taken from the common drain node.

This is a self-biasing circuit. The biasing part of the doubler circuit is highlighted in Fig. 6.3. The sources of M_1 and M_2 are connected to ground through source degeneration resistor R_s and bypass capacitor C_s. The gates are connected to ground through the resistors $R_1 - R_2$. V_{GS} is around -0.85 V (selected from bias sweep) and V_{DS} is around 3.4 V. The supply voltage of 4 V is used as the maximum BV_{DS} for a PP10-10 GaAs pHEMT is 4 V.

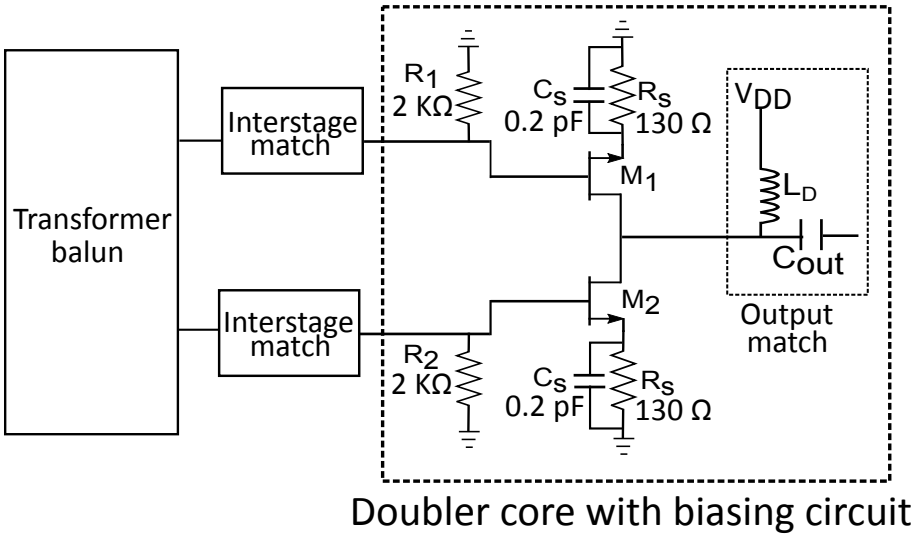


Figure 6.3: Layout of the two transistors of the frequency doubler.

A series capacitor C_1 is used at the input of the transformer balun. There is an impedance mismatch between the differential output of the transformer balun (100 Ω) and the high-impedance input at the gate of M_1 and M_2. An impedance matching network is needed between the differential output of the transformer balun and the input at the gates of M_1 and M_2. A similar interstage matching circuit to the frequency doubler in the SG13S SiGe HBT process is used here. Series-parallel capacitors ($C_2 - C_7$) along with resistors ($R_1 - R_2$) are used for impedance matching. The series capacitors ($C_6 - C_7$) also provide DC blocking. The matching circuit is depicted in Fig. 6.4. The whole doubler circuit is simulated together with the balun for a flat second-harmonic output.

At the common drain of the transistors, an inductor L_D is used to connect to the

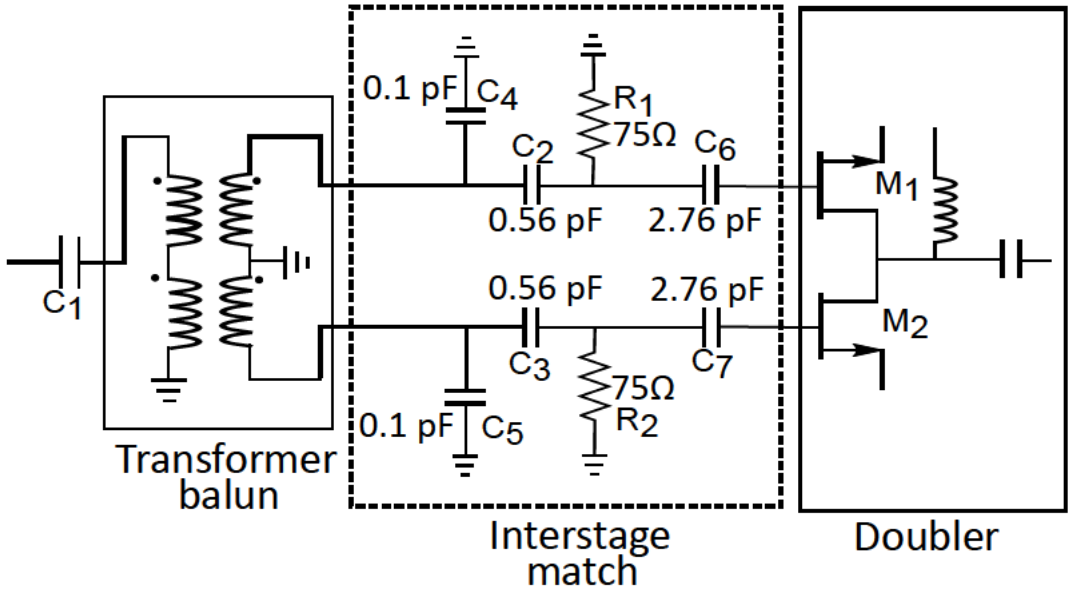


FIGURE 6.4: Schematic of the matching circuit between the transformer balun and the frequency doubler (biasing resistor at the gate is omitted in the figure for simplicity).

power supply. A series inductor and a capacitor C_{out} are connected between the drain and the output. These inductors and capacitors help in determining the frequency band and also improve the matching at the output port. Additional filtering is not used at the output in order to study the harmonic rejection from the doubler itself.

As mentioned in the design specification, one of the primary design objectives of the frequency doubler is to achieve large odd-harmonic rejection over a broad band. The input frequency range of the doubler is between 11 GHz and 20 GHz while the output is from 22 GHz to 40 GHz. A portion of the third harmonic frequency range (33 to 40 GHz) fall within the desired frequency range of the doubler output (22 to 40 GHz). For this wide-band doubler design filtering is not suitable for rejection of the third harmonics. So a balanced topology is found to be an effective solution for the wide-band doubler. To ensure good odd-harmonic rejection, the match between the two transistors M_1 and M_2 is essential and also it depends on the symmetry in the layout. To achieve a flat second harmonic response over a broad band, the doubler should be optimised together with the transformer balun and the interstage matching circuit.

6.3.2 Design flow

The design flow for a circuit design in a particular process is an important principle which involves a number of steps. As discussed in Chapter 5, it is essential to chalk out a design flow at the beginning of the circuit design. A well-planned design flow allows a circuit designer to work methodically and to achieve a successful design in an efficient manner with fewer iterations.

The design flow followed for the GaAs design is different from the one followed for the SiGe designs. The design of the frequency doubler is started with the schematic simulation. To test the circuit, initially lumped components from the AWR library are used to build the circuit schematic. The pHEMTs are taken from the PP10-10 library. The transistors used for the frequency doubler design do not use the foundry models, but ones developed at MACOM Technology Solutions, North Sydney design centre, which provide better accuracy of the simulation results.

If the desired specifications are met using the lumped components from the AWR library, then they are replaced with the closed-form models from the PP10-10 GaAs pHEMT process library. The inductors can be adopted from the PP10-10 library or can be customised by the designer. The inductors used for the frequency-doubler design are drawn as EM structures in Axiem. In the PP10-10 GaAs pHEMT process, as a continuous ground plane is present at the bottom of the substrate, all the interconnecting metal lines are modelled as microstrip lines. In this step of the circuit design (using closed-form models), the interconnecting metal lines are also added to the schematic as microstrip lines, keeping in mind the layout of the design. Ground connections are also replaced with their corresponding closed-form models. The circuit element values are tuned to meet the desired specifications. The circuit schematic of the frequency doubler using the closed-form elements is illustrated in Fig. 6.5.

In the next step, the transistors are replaced with their EM structures. Basically, the layout of the transistors available from the foundry is copied into Axiem. The detailed layers used in the transistor layouts are not included in Axiem, to reduce the complexity of the EM simulation, but the basic geometry of the transistors is preserved. Symmetry

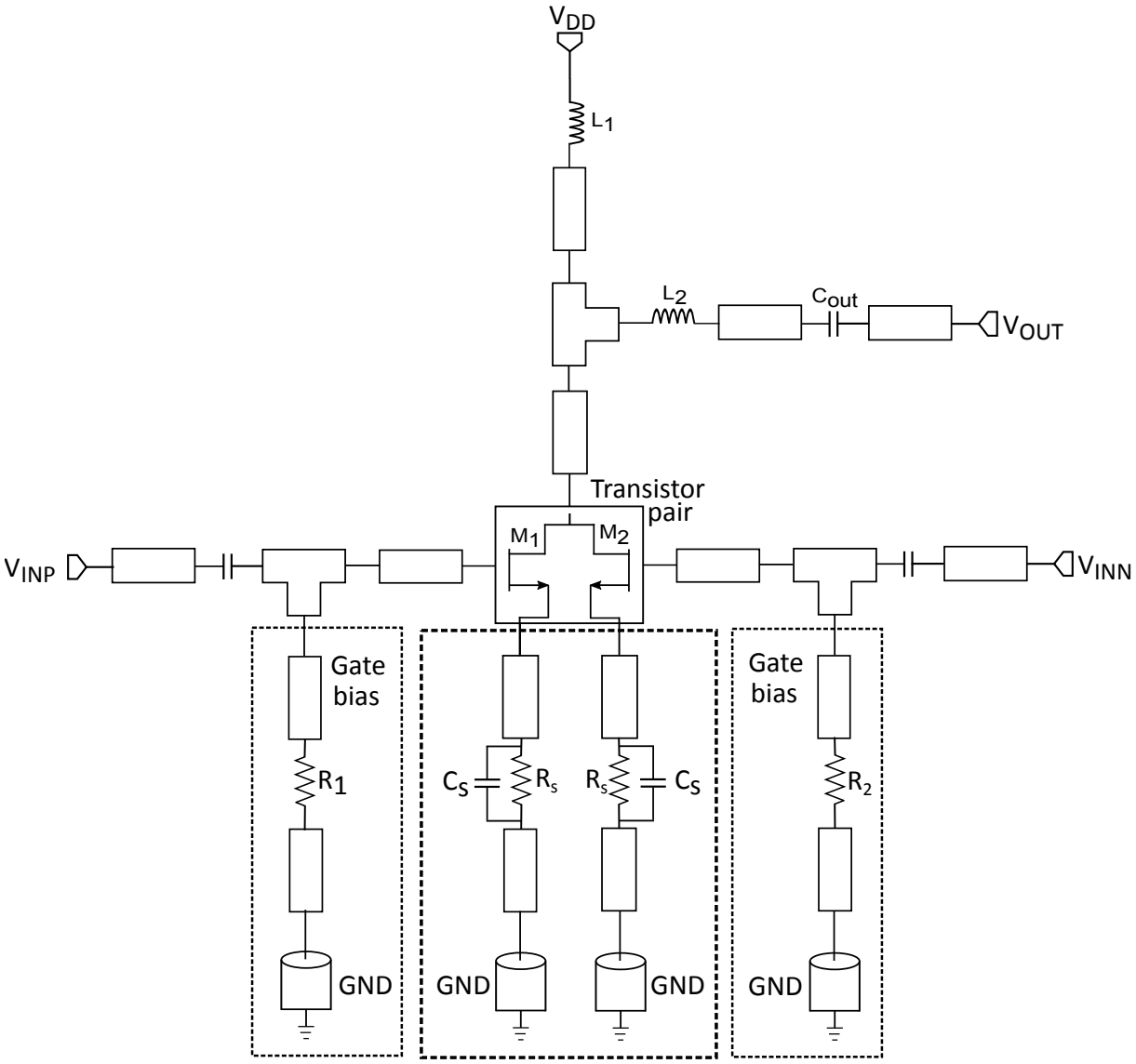


Figure 6.5: Schematic of the frequency doubler using the closed-form elements.

is maintained in the layout of the transistors. The transistors used for the doubler core are placed close to each other to avoid the interconnecting metal lines. The frequency doubler with closed-form models (for the resistors, capacitors, microstrip lines and ground) together with the inductors and transistors as EM structures are simulated. Depending on the simulation results, some of the circuit elements are tuned to meet the specifications. Once the simulation results are optimised, then the closed-form elements are gradually replaced with their EM structures.

The whole circuit is incorporated into one single EM block. For the MMIC design it

is better to simulate the entire circuit as one EM block, to capture the electromagnetic effects, rather than divide the whole circuit into a number of sub-blocks. As guard rings are not available, sufficient spaces are provided between the circuit elements to minimise the interference from the surrounding metal lines. Due to the large size of the EM structure, the EM simulation is time-consuming. At this step, some of the components need to be retuned to meet the design specifications. Optimisation at this step is quite time-consuming and requires proper planning to set up the simulations.

At the final step, the layout of the circuit is generated. Essentially the entire structure is copied from the single EM block to the layout cell library. All the detailed metal layers, airbridge, span layers are drawn. The LVS and the DRC are checked on this layout. In a nutshell, this design methodology is followed for the implementation of the PP10-10 GaAs pHEMT frequency doubler design.

6.4 Final circuit layout

As mentioned in Section 2.3, the PP10-10 GaAs pHEMT process offers a stack-up of only two metal layers (M1 and M2). It is difficult to implement the cross-over connections in this process compared to SiGe due to the availability of only two metal layers. The layout of the frequency doubler in the PP10-10 GaAs pHEMT process is less compact than for the SiGe design due to the nature of the metal layer stack-up available in the PP10-10 GaAs pHEMT process.

The layout of the frequency doubler is accomplished in few steps which are summarised below:

- At first the layout of the whole frequency doubler design used in Axiem for EM simulation is copied into the schematic layout.
- All the simplified EM layers used for Axiem simulation are mapped into proper metal layers as per the design rule. For example, all the double metal layers are mapped to M1, M2 and via2 (between M2 and M1) in the layout.
- Next the RF and the DC pads are connected and the layout is finalised.

- DRC is checked using WIN's web DRC tool.

All the interconnections in the frequency doubler are drawn as microstrip lines. As the dimensions of these microstrip lines are wavelength dependent, the overall layout in the PP10-10 GaAs pHEMT process occupies a larger area. As ground rings are not available in this process to provide shielding to the circuit elements in the RF path, the circuit components cannot be placed closely. To avoid any interference from the surrounding structures, sufficient space is provided between the interconnecting metal lines in the layout of the frequency doubler.

Some layout conventions are followed from the beginning to be consistent throughout the layout. For example, all the interconnecting microstrip lines are implemented either in double metal or in M1. This is because the double metal layer can handle more current than M1 or M2 and the resistance is less due to its thickness. To minimise corner effects, 90^o bends in the interconnecting metals are avoided. The capacitors are realised using M1 and M2 layers. Therefore, the interconnections associated with the capacitors are drawn using M1 to connect to the bottom plate while the top plate is connected to the double metal using the airbridge. Resistor terminals are implemented in double metal or in M1.

In the balanced topology, the transistors are placed close to each other to avoid the interconnecting metal lines. For the frequency-doubler core, the layout of the two transistors M_1 and M_2 is shown in Fig. 6.6. The sources of the two transistors are combined to minimise the metal interconnection. There are two separate gates for M_1 and M_2. The drains of the two transistors are tied together and a common drain connection is taken out from the two transistors.

A limited cross-over of the metal layers can be achieved in the PP10-10 GaAs pHEMT process due to the availability of only two metal layers. This can be illustrated with an example of an inductor layout, as shown in Fig. 6.7. The inductor is implemented using double metal lines. One terminal of the inductor is connected to ground while the other terminal is connected to a part of the circuit. An intersection of the metal lines is encountered at one of the terminals of the inductor, in this case at

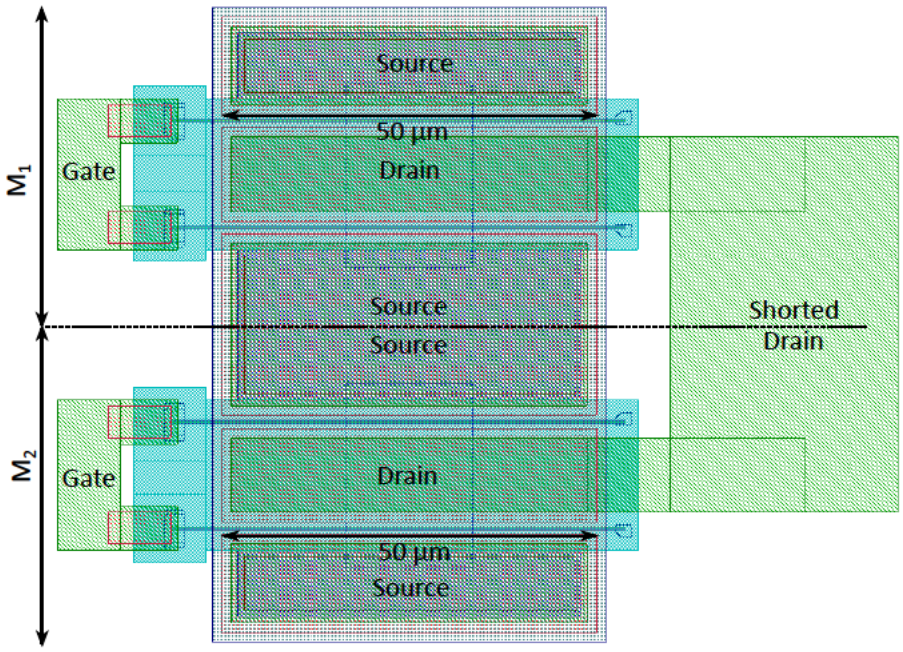


FIGURE 6.6: Layout of the two transistors of the frequency-doubler core.

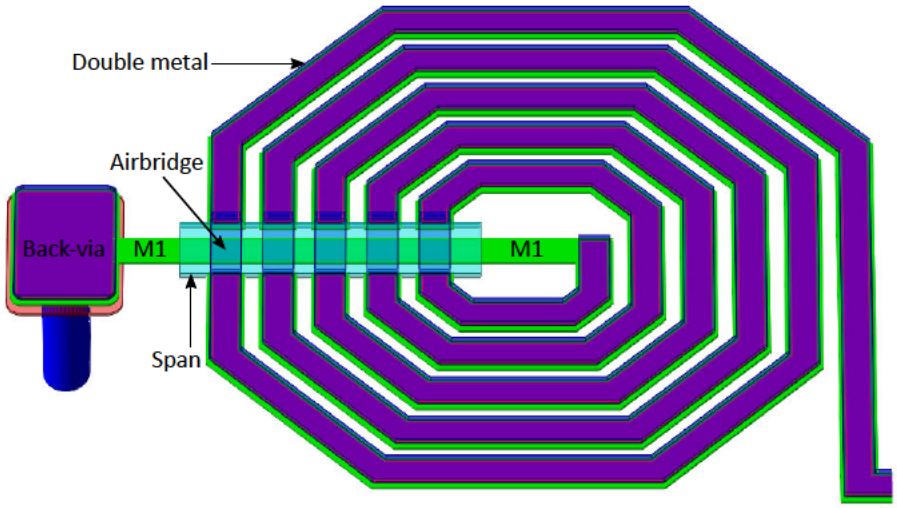


FIGURE 6.7: Diagram showing the cross-over implementation in the PP10-10 GaAs pHEMT process using an airbridge.

the terminal connected to ground. The airbridge is used to implement the cross-over, joining two M2 layers, while the M1 layer can be used for interconnection beneath the airbridge. Due to the design rule limitation for the airbridge and the span layers it is challenging to implement the cross-overs in the millimetre-wave designs where the

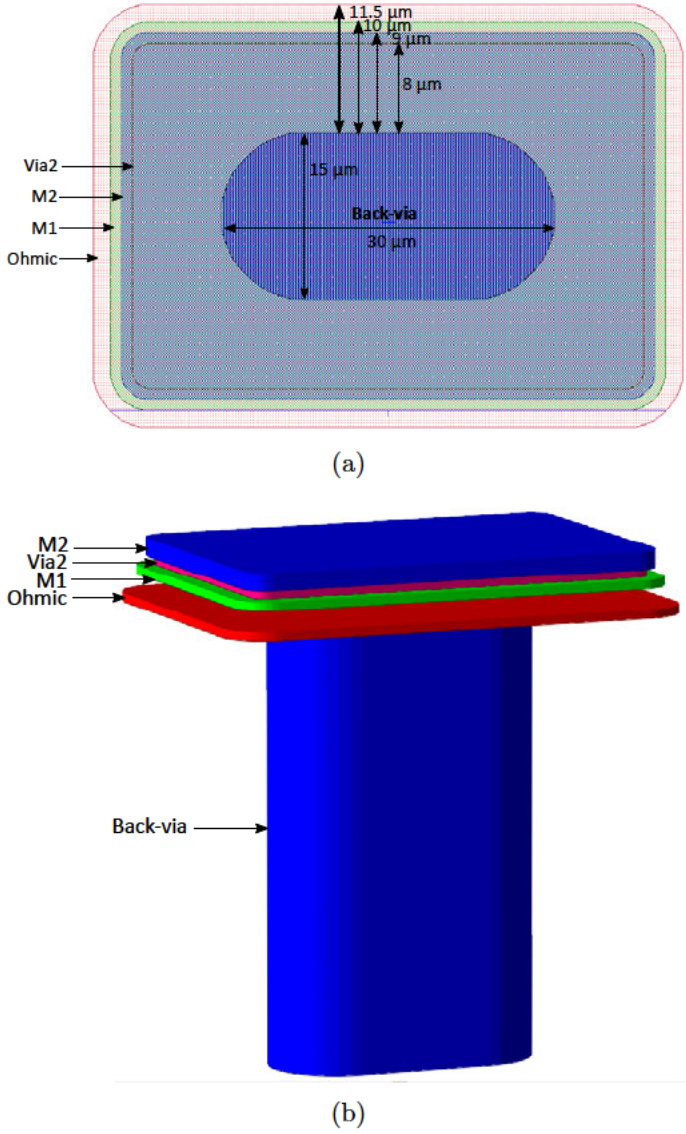


FIGURE 6.8: The layout of a back-via for ground connection: (a) 2D view (b) 3D view.

dimensions of the interconnecting metal lines become smaller.

Unlike the SiGe process, it is not required to spread the ground connections over the entire layout in the PP10-10 GaAs pHEMT process, due to the availability of the ground plane underneath. The ground connections are provided by back-vias to the ground plane. A typical back-via connection (2D view and 3D view) is shown in Fig. 6.8. There is a design-rule limitation for the size of the back-via. Also it cannot be used as a standalone layer. According to the foundry design rule, the back-via must be enclosed by M2, M1, via2 (between M2 and M1) and the ohmic layer. The minimum dimensions for the different metal-layer enclosures of the back-via are

shown in Fig. 6.8. Particularly for the high frequency design such as millimetre-wave applications, the dimension of this back-via poses a challenge for the layout where the circuit elements are smaller in size and are relatively closely spaced.

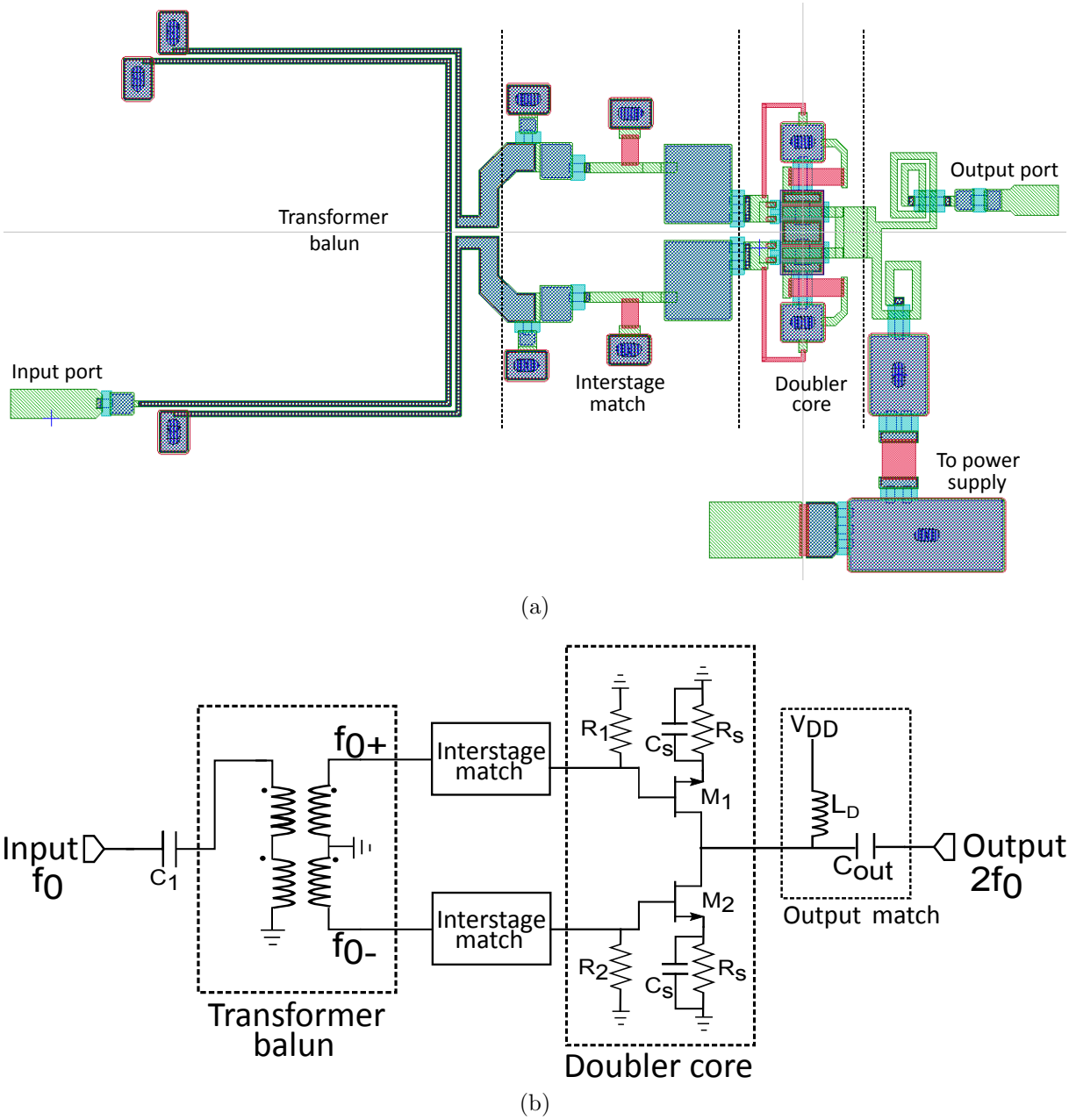


Figure 6.9: The frequency doubler design (a) layout with the transformer balun, (b) schematic diagram.

Symmetry is maintained throughout the layout. The overall layout and the corresponding circuit schematic of the frequency doubler with the transformer balun are

shown in Fig. 6.9(a) and Fig. 6.9(b). As this is a self-biased circuit, separate bias lines are not required to be connected to the bias pads. However, as the frequency-doubler circuit has a single-ended input and single-ended output, symmetry could not be maintained at the input and output port connections. This is a practical problem for circuit implementation.

6.5 Harmonic rejection simulation and measurement

The comparison of the simulated and the measured results are presented in this section. Off-chip SOLT calibration is used for the measurement. For the measurement of the doubler, a Keysight E8257D signal generator suitable for 50 GHz measurement is used to provide the input signal and the harmonics were measured using a Keysight PXA Signal Analyzer, N9030A, (3 Hz-50 GHz).

6.5.1 Frequency sweep

For the purpose of simulation, the frequency-doubler circuit along with the transformer balun is designed as one single EM structure to better capture the electromagnetic effects. As the frequency-doubler circuit is self-biased, only a supply voltage of 4 V is provided. The test bench for simulating the output power of the harmonics is illustrated in Fig. 6.10.

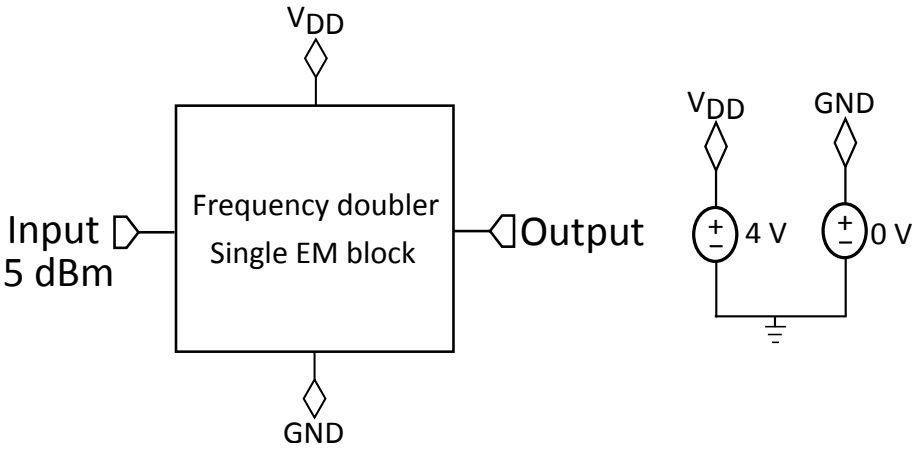


Figure 6.10: Test-bench for simulation of the harmonics.

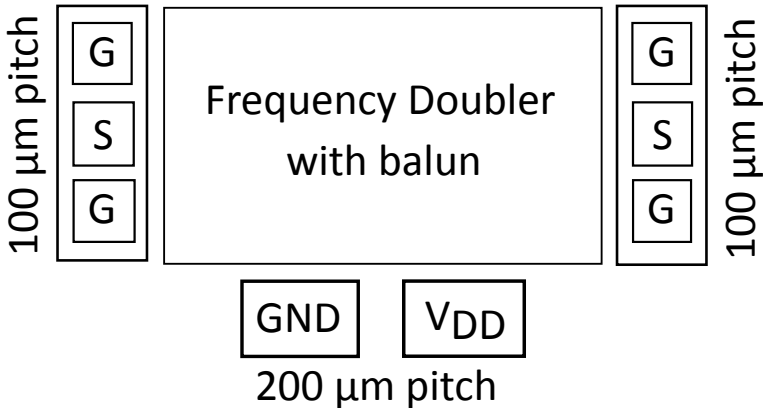


Figure 6.11: Diagram showing the pin configuration of the frequency doubler with the transformer balun.

The pin configuration of the frequency doubler with the transformer balun is shown in Fig. 6.11. The input frequency range is swept from 11 to 20 GHz, with 5 dBm input power. According to the simulation results of the harmonics, more than 30 dB harmonic suppression can be achieved over most of the band (from 12 to 20 GHz).

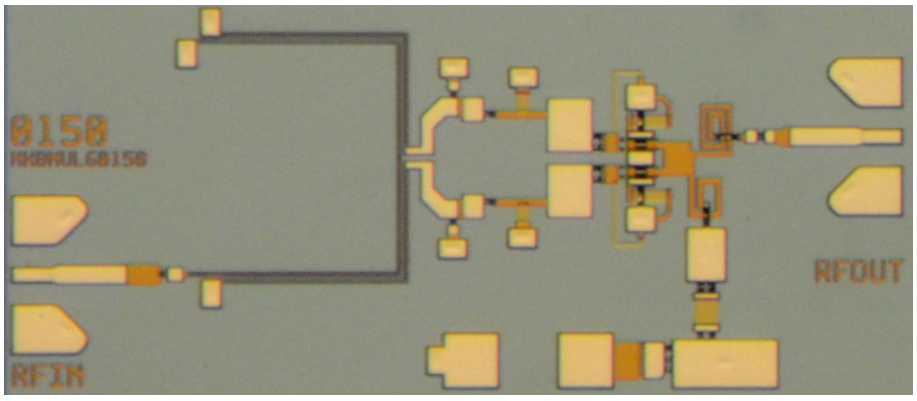
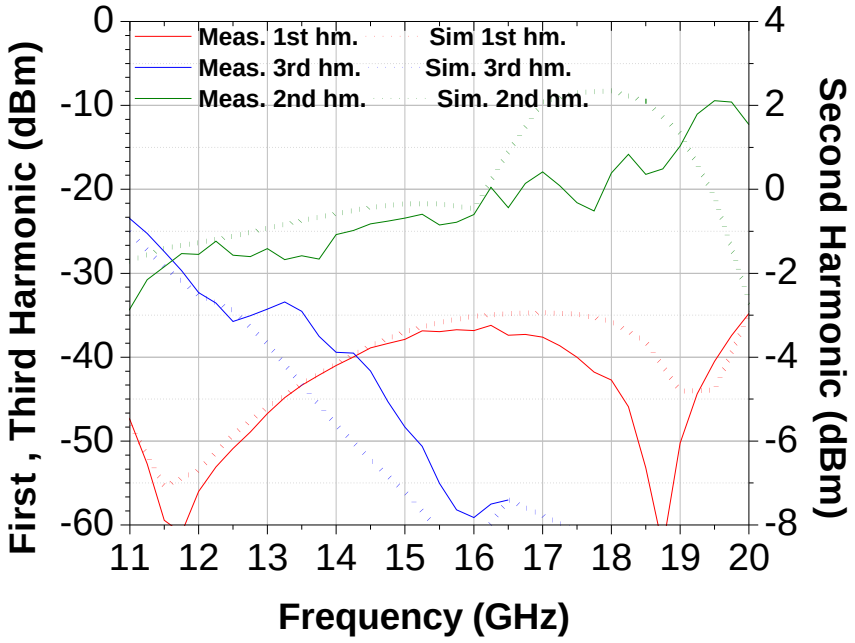
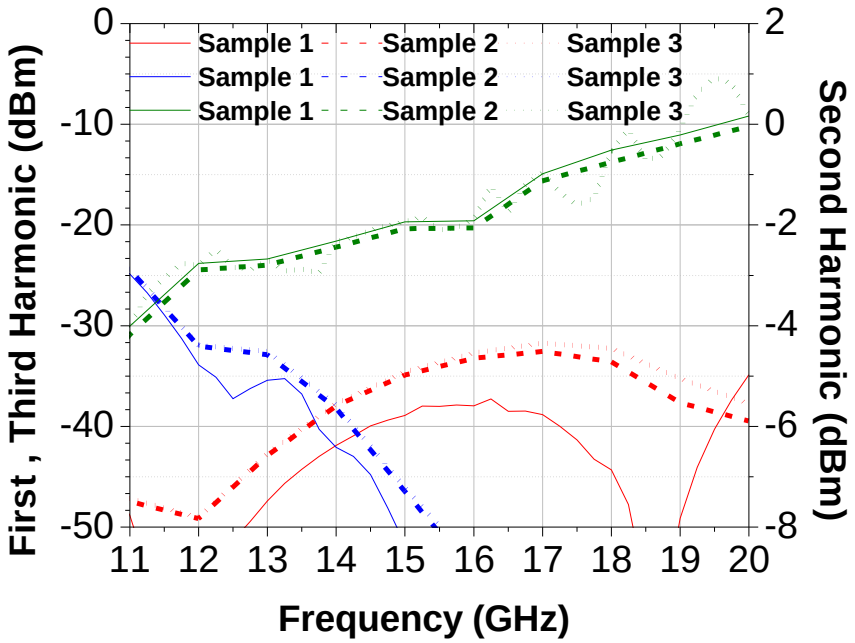


Figure 6.12: Die-photo of the frequency doubler with the transformer balun.

The die photo of the frequency doubler with the transformer balun is shown in Fig. 6.12. For the measurements, a supply voltage of 4 V is provided through the DC probe in the GP configuration. The frequency of the input signal is varied from 11 to 20 GHz. A pair of GSG probes (suitable for measurements up to 67 GHz, from GGB Industries) is used to provide the input signal to the frequency doubler and to measure the output signal. The comparison of the simulation and measurement results of the



(a)



(b)

Figure 6.13: Output power of harmonics as a function of input frequency (a) for 5 dBm input, measured (solid), simulated (dotted), (b) for 4 dBm input, measured results for three dice.

harmonics for 5 dBm input power is presented in Fig. 6.13(a). As seen from the graph, more than 35 dB fundamental suppression is measured across 11 to 20 GHz. The measured third-harmonic suppression is better than 30 dB across most of the band. The total power consumption of the frequency doubler at 15 GHz for 5 dBm input power is 45 mW from a 4 V supply.

To investigate the process variation, three samples were measured as shown in Fig. 6.13(b). The mean trace shows a fundamental rejection of more than 35 dB across 11 to 20 GHz while the third-harmonic rejection is better than 30 dB above 12 GHz. The consistent measurement results across the three samples confirm a good odd-harmonic rejection from the frequency-doubler circuit. As seen from Fig. 6.13(b), between 15 to 20 GHz the second harmonic power at the output of the doubler is relatively higher than the lower frequency end. This is because of the output matching circuit of the doubler is not perfectly matched over the entire output frequency range.

6.5.2 Input power sweep

The magnitude of the harmonics at the output of the frequency doubler is dependent on the balance of the differential signal, the symmetry of the layout and the similarity of the two transistors in the doubler core. Apart from these conditions, the magnitude of the harmonics at the output of the frequency doubler is also dependent on the input power level. Theoretically, the magnitude of the harmonics increases with increased input power, so the input power is varied from -5 dBm to 10 dBm. The harmonics corresponding to 12 GHz, 16 GHz and 20 GHz input are measured. The measurement results of the three samples for each of these frequencies are shown in Fig. 6.14, Fig. 6.15 to investigate the process variation.

From the measurement results, it can be seen that the fundamental rejection corresponding to 12 GHz and 16 GHz inputs is approximately 35 dB across the input power sweep from -5 dBm to 10 dBm. For 20 GHz input, the fundamental rejection across the input power sweep is around 30 dB. The third-harmonic rejection for 12 GHz input

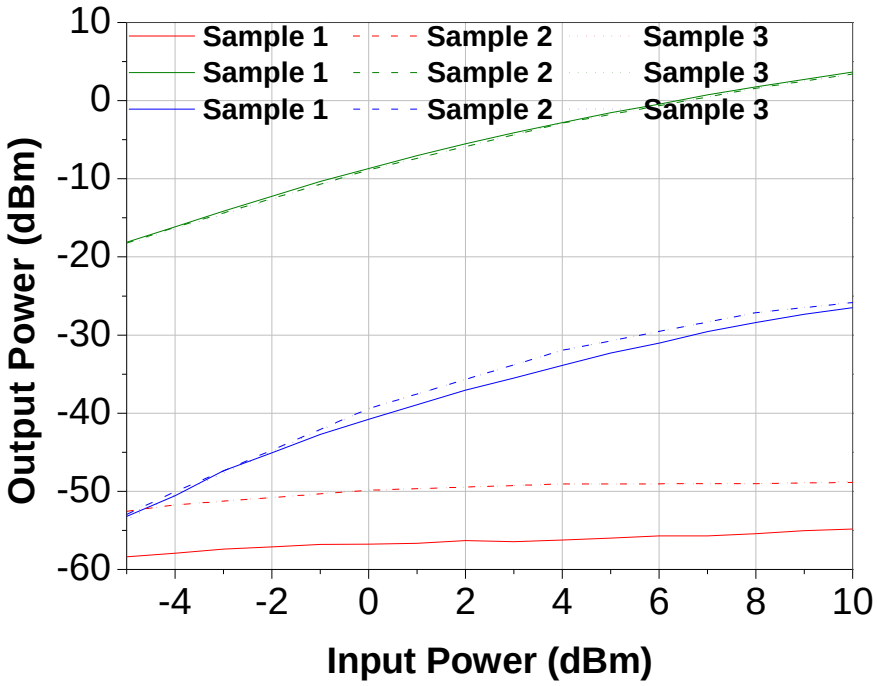
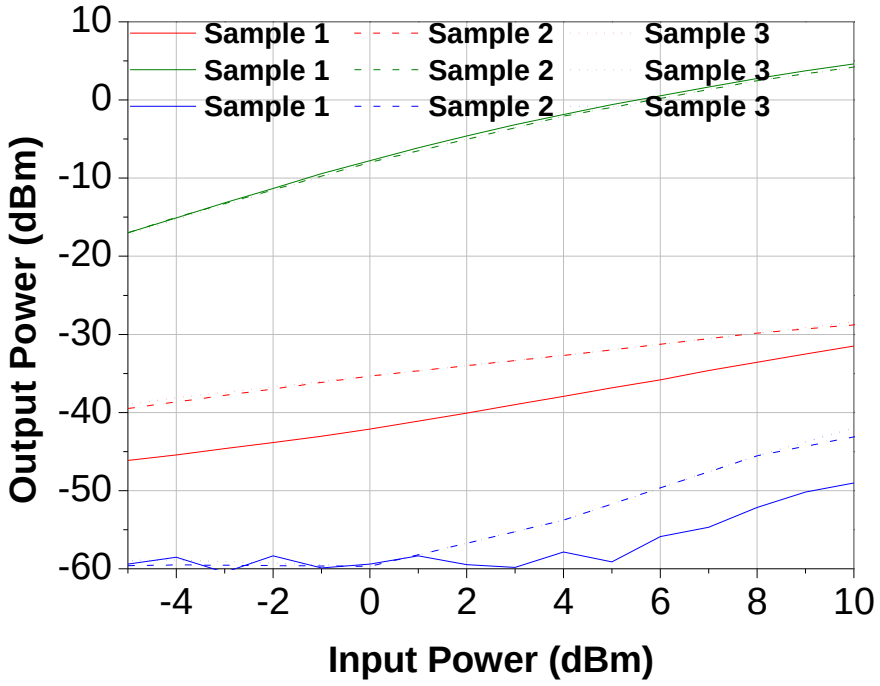


Figure 6.14: Output power of harmonics as a function of input power sweep from -5 dBm to 10 dBm for 12 GHz input across three samples; fundamental (red line), second harmonic (green line)and third harmonic (blue line).

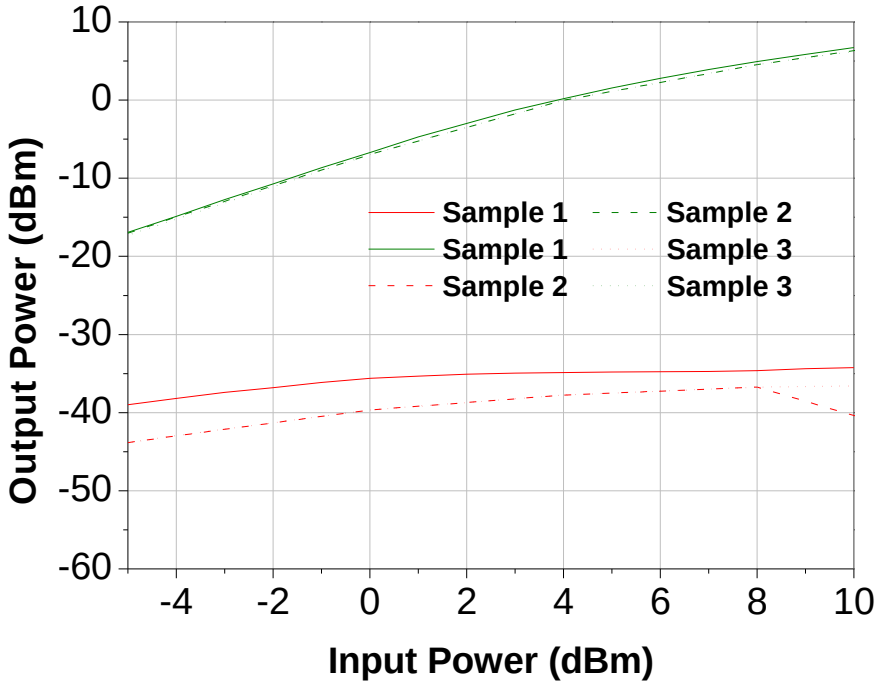
is better than 35 dB and for 16 GHz input the rejection is better than 40 dB across the input power sweep of -5 dBm to 10 dBm. Due to the limitations of the measurement instrument, the third harmonic for the 20 GHz input cannot be measured.

As observed from Fig. 6.14, Fig. 6.15, the output power of the second harmonic is quite low for low input power level like -4 dBm input. Gradually the conversion gain of the second harmonic improves with an increase in the input power level. These results indicate that the push-push frequency doubler in the PP10-10 process can be used with an amplifier at the output of the doubler, for low input power level (such as -4 dBm). For 5 dBm input power, the second harmonic output power is approximately 0 dBm at the mid band.

The performance of the designed frequency doubler and a comparison with other state-of-the-art designs are summarised in Table 6.2.



(a)



(b)

Figure 6.15: Output power of harmonics as a function of input power sweep from -5 dBm to 10 dBm across three samples: (a) for 16 GHz input, (b) for 20 GHz input; fundamental (red line), second harmonic (green line) and third harmonic (blue line).

Table 6.2: Performance summary of the designed frequency doubler and comparisons with other state-of-the-art designs

Parameters	[65]	[67]	[149]	**This work**
Fund. rejection [dB]	15	13	30	35
Bw. [GHz]	3−50	30−50	17% (mid-band 38 GHz)	22−40
Power consumption [mW]	600 (DC)	-	86 (at 10 dBm)	45 (at 5 dBm)
Area [mm^2]	3	1.5	2.25	0.72
Tech. [μm]	0.2 GaAs pHEMT	0.15 GaAs pHEMT	0.15 GaAs pHEMT	0.1 GaAs pHEMT

6.6 Discussion and Conclusion

The frequency-doubler design implemented in the PP10-10 GaAs pHEMT process is presented in this chapter. First, the design of a K-Ka band balanced doubler (using the push-push topology) with 11-20 GHz input and 22-40 GHz output is shown. The transformer balun implemented in the PP10-10 GaAs pHEMT process (shown in Section 4.6) with good balance performance is used with the balanced frequency doubler. The description of the circuit, details of the design flow and layout challenges are discussed. Symmetry in the layout of the frequency doubler is important for achieving large odd-harmonic suppression. As the doubler circuit presented in this chapter is self-biased, and identical circuit elements are used for both the transistors ($M1$ and $M2$), the bias voltages are identical for each of the transistors. Hence tuning of bias voltages is not applicable in this case, unlike the doubler in the SG13S SiGe HBT process for which the bias voltages are tuned (as in Section 5.5.2). The input power is varied from -5 dBm to 10 dBm to measure the harmonics for different input power levels. Also three samples are measured to investigate the process variation. The measured results show a fundamental rejection of approximately 35 dB across the band and more than 35 dB third-harmonic rejection across the output band. This indicates that the balance in the differential signals is crucial for odd-harmonic suppression at the output of the

frequency doubler. Agreement between the simulation and the measurement results justifies the design flow.

Based on the measurement results obtained from the frequency doubler in the SG13S SiGe HBT process (shown in Chapter 5) and in the PP10-10 GaAs pHEMT process (shown in this chapter), the two processes will be compared in terms of their linearity, which is the topic of discussion in the next chapter.

7

Comparison of SG13S and PP10-10 processes

7.1 Introduction

Since the invention of transistors in 1947, semiconductor electronics has evolved rapidly over seven decades, and is still evolving. These seven decades have witnessed the development of high-frequency transistors manufactured in various semiconductor materials. Advancements in devices have revolutionised the semiconductor industry over the years. The reduced dimensions and improved performance of mobile phones testify to the advancements in devices. For wireless communication systems, the demand for a higher data rate is increasing constantly. To cater to these demands, high-frequency circuits in the microwave and millimetre-wave range are explored. HBTs and HEMTs

have played an instrumental role in improving the high-frequency performance of high-speed devices. Not only the devices, but the process itself, play an important role in implementing a circuit in the microwave and millimetre-wave range. Therefore, selection of a particular process technology becomes an important decision for circuit designers. One of the primary objectives of this dissertation is to compare the suitability of two prominent technologies, SiGe and GaAs, for an overall system-level performance of microwave and millimetre-wave radio designs in terms of linearity. For this purpose, a frequency-doubler circuit is considered as an effective indicator of process linearity. Among the passive structures, a balun is considered as the test structure, as it complements a frequency doubler when the linearity of a process is considered.

Traditional MMIC circuits using the GaAs process have been paramount for microwave and millimetre-wave designs for the last few decades. But the recent advancement in silicon-based processes such as SiGe has made it possible to design circuits at microwave frequencies with a reasonable performance, with integrated digital logic and at a much lower cost than with GaAs. The f_T and f_{max} of current SiGe HBTs, and the predicted f_T and f_{max} in the future, indicate that the future of the SiGe process in the field of microwave and millimetre-wave circuits is promising. This chapter focuses on a comparison of the two process technologies, SG13S SiGe HBT and PP10-10 GaAs pHEMT, that are used for the implementation of the circuits.

WIN Semiconductor's PP10-10 process offers high-performance 0.1 μm GaAs pHEMTs with targeted applications in backhaul communication systems and radars for airport surveillance [25] (process overview in Section 2.3). This process is an extension of WIN's successful PL15 technology platform with an optimised device structure. The f_T and f_{max} of the pHEMTs in the PP10-10 GaAs pHEMT process are 130 GHz and 180 GHz respectively. The substrate thickness for this process is 50 μm. It has only two metal layers M1 and M2. There is a continuous ground plane below the substrate. All the interconnecting metal lines in this process are modelled as microstrip lines.

IHP's SG13S process is a 0.13 μm SiGe BiCMOS process which provides HS-HBTs (process overview in Section 2.2). As the HBTs are used for the circuit implementation, this process has been referred as the SG13S SiGe HBT process (as mentioned in Chapter

2). The f_T and f_{max} of the HS-HBTs available in this process are 250 GHz and 300 GHz respectively. The substrate thickness is 200 μm. In contrast to the PP10-10 GaAs pHEMT process, the SG13S SiGe HBT process offers a stack of seven metal layers, with two thick metal layers (TM2 and TM1) and five thin metal layers (M5 to M1). There is no ground plane underneath the substrate, so the interconnecting metal lines cannot be treated as microstrip lines. More details on both processes can be found in Chapter 2.

7.2 Circuit design differences

A frequency-doubler circuit is implemented in both the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes, to study the linearity that could be achieved from both the processes. A balanced topology is selected for the circuit implementation because it inherently rejects the odd harmonics without filtering. This is crucial for the overall linearity of a system such as a wireless transmitter or receiver. Device specifications and the process itself influence the design in a particular process. These differences in the circuit design in the two processes are discussed in this section.

7.2.1 Baluns

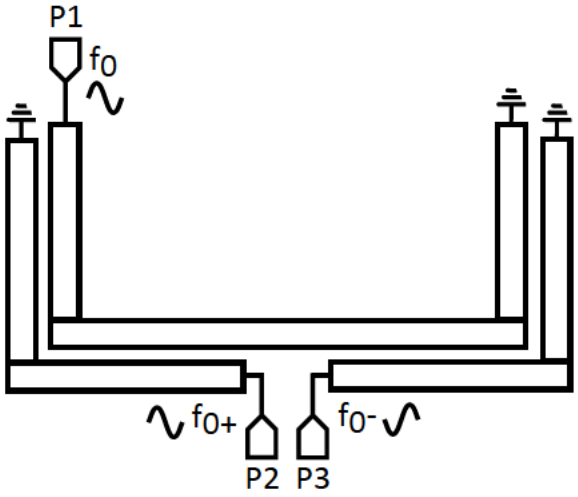


Figure 7.1: Schematic representation of transformer balun implemented in the PP10-10 GaAs pHEMT process.

A passive transformer balun is selected for driving the balanced frequency doubler (discussed in Section 4.3). Two different topologies can be used for the design of a transformer balun: edge-coupled and broadside-coupled. In the edge-coupled design, the primary and the secondary coils lie side-by-side, whereas in the broadside-coupled design the primary and the secondary coils are stacked on top of each other. Only two metal layers are available in the PP10-10 GaAs pHEMT process. Moreover, the M2 layer is not used independently, as it is usually enclosed by the M1 layer. The PP10-10 GaAs pHEMT process is therefore not suitable for implementing broadside-coupled designs. The coupling between the primary and the secondary coils is less in edge-coupled baluns than in broadside-coupled baluns. The coupling coefficient is dependent on the width of the metal lines and on the separation between the primary and the secondary coils (discussed in Section 4.6 in detail). The schematic of the edge-coupled transformer balun implemented in the PP10-10 GaAs pHEMT process is shown in Fig. 7.1.

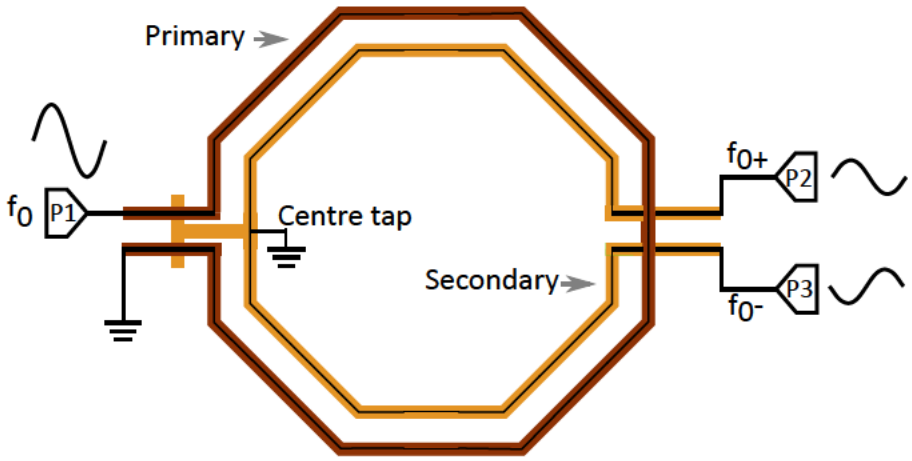


FIGURE 7.2: Schematic representation of transformer balun implemented in the SG13S SiGe HBT process.

A silicon-based process, such as SiGe, offers a stack of different metal layers. As mentioned in Chapter 2, the SG13S SiGe HBT process offers a stack-up of seven metal layers. This makes it suitable for implementation of broadside-coupled structures, and the transformer balun implemented in the SG13S SiGe HBT process is based on the broadside-coupled technique. It is also easy to implement cross-overs in the SG13S SiGe

HBT process, as several metal layers are available. The schematic of the transformer balun implemented in the SG13S SiGe HBT process is shown in Fig. 7.2 for reference (discussed in Section 4.5 in detail).

7.2.2 Frequency doublers

Theoretically, a balanced topology can cancel odd harmonics inherently. Therefore, a push-push topology is used to implement the balanced frequency doubler with a transformer balun, in both the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes (as shown in Chapters 5 and 6).

SG13S SiGe HBT process

In the SG13S SiGe HBT process, a pair of identical HS-HBTs is used to design the core of the push-push frequency doubler. To provide the required bias at the base of the transistor pair, Q_1 and Q_2, a current-mirroring technique is used. If the transistors are biased at different voltages, then the harmonics generated in the collector current are different in magnitude. This effect can be seen at the output of the frequency doubler. In a practical implementation of the circuit, it is not possible to measure the base voltages from the fabricated circuit. Hence, the bias line is not shared with the transistors Q_1 and Q_2, instead two separate bias lines are used. It gives a control to the designer to tune the bias voltages such that a null point is found, at which the base bias voltage of the two transistors will be the same. This gives rise to harmonics of the same magnitude in the collector currents of the two transistors. As the collectors of the two transistors are joined together, the odd harmonics are cancelled.

This bias tuning is helpful to mitigate the effect of any asymmetry in the electrical and physical aspects of the layout. For example, in the layout of the frequency doubler in the SG13S SiGe HBT process, as shown in Section 5.4, the bias lines for the two transistors are routed through different lengths. This is illustrated in Fig. 7.3, in which the red and the green lines show the path of the two bias lines. As the DC pads are aligned on the same side, the bias lines need to be routed differently and symmetry

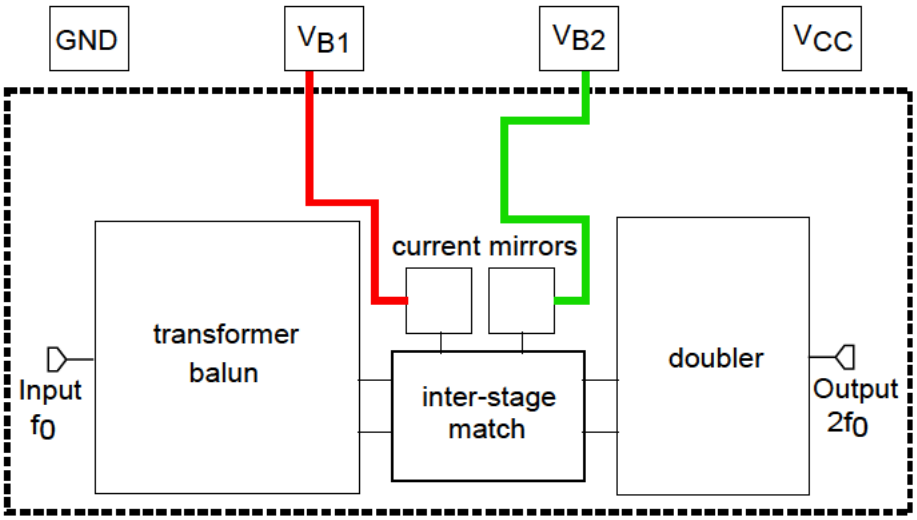


FIGURE 7.3: Representation of the two bias lines (red and green) in the layout of the frequency doubler in the SG13S SiGe HBT process.

cannot be maintained. This might lead to slightly different bias voltages at the bases of the two transistors of the push-push pair. The bias-tuning technique gives the flexibility to correct the bias voltages. Although symmetry in the layout is maintained, an additional odd-harmonic suppression of up to 2 dB is measured.

PP10-10 GaAs pHEMT process

According to the analysis presented in Chapter 3, a balanced frequency doubler implemented using identical pHEMTs will inherently cancel odd harmonics at the output if the input differential signal is perfect. In the PP10-10 GaAs pHEMT process, two identical 0.1 μm pHEMTs are used to implement the balanced frequency-doubler circuit (details in Chapter 6). The appropriate size of the pHEMTs is selected by changing the UGW. Similar to the SG13S SiGe HBT process, a push-push configuration is used but the biasing circuit is different. The transistors are biased at V_{GS} of -0.85 V. This is implemented using a self-biased circuit. The gates of the transistor pair M_1 and M_2 are connected to ground through two resistors. The drains are joined together for odd-harmonic cancellation. The sources of M_1 and M_2 are also tied together and connected to ground through a resistor and a bypass capacitor. The schematic for the biasing circuit of the frequency doubler is shown in Fig. 7.4.

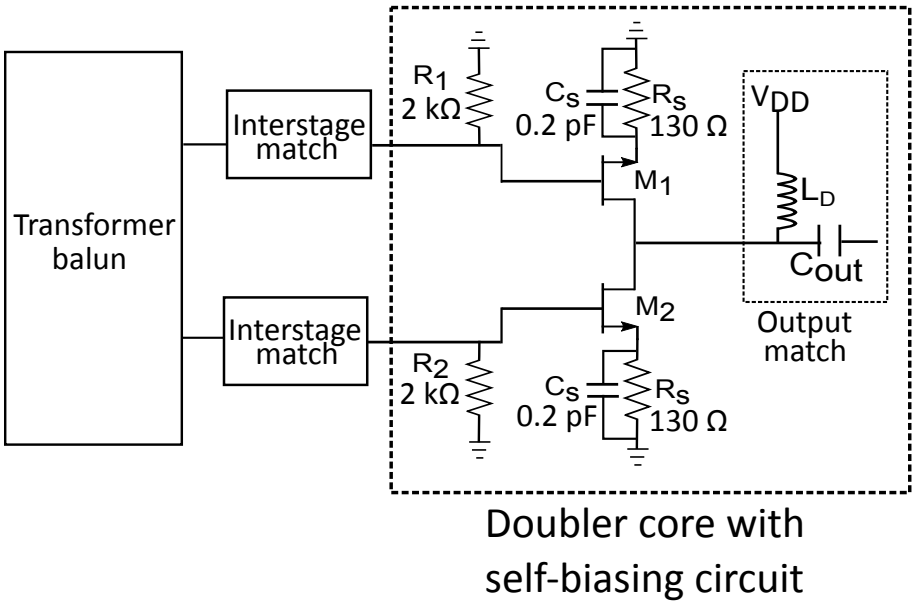


Figure 7.4: Schematic of the self-biasing circuit of the frequency doubler in the PP10-10 GaAs pHEMT process.

The DC pads are aligned on one side of the circuit as in the frequency-doubler circuit in the SG13S SiGe HBT process. Unlike the frequency-doubler circuit in the SG13S SiGe HBT process, it is possible to maintain the symmetry in the layout of the biasing circuit for the doubler in the PP10-10 GaAs pHEMT process. This is because additional bias lines do not need to be connected to the DC bias pads, as the self-biasing technique is used for the designed circuit in the PP10-10 GaAs pHEMT process. To maintain perfect symmetry in the biasing circuit, the resistor and the bypass capacitor connected with the sources of M_1 and M_2 are split into two (layout shown in Chapter 6). As symmetry is maintained in the electrical and physical aspects of the layout of the biasing circuit, the bias-tuning technique is not applicable in this case.

7.3 Implementation differences

At first the general circuit-implementation challenges in both the processes, the SG13S SiGe HBT and the PP10-10 GaAs pHEMT, are discussed in this section. Then the performances of the frequency doublers implemented in the two processes are compared with respect to the design parameters listed in Section 2.5.

7.3.1 Layout complexity

It is important to think about the layout simultaneously with designing the circuit. The layout methodologies in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process are very different from each other. In the SG13S SiGe HBT process, seven metal layers are available, rendering the layout very complicated, while in the PP10-10 GaAs pHEMT process only two metal layers are offered, and the layout is relatively simple.

In the SG13S SiGe HBT process, the whole chip is filled up with metal density fillers by the foundry. This makes the layout even more complicated as the designer needs to carefully use specific no-filler metal layers in the layout. If it is not done appropriately, then there is a chance of making unwanted short-circuit connections in the designed circuits. In contrast to the SG13S SiGe HBT process, this is not a problem in the PP10-10 GaAs pHEMT process.

In the PP10-10 GaAs pHEMT process, a continuous ground plane is present beneath the substrate. Therefore, the interconnecting metal lines can be simply treated as microstrip lines. Moreover, ground connections can be easily implemented using the back-via. In the SG13S SiGe HBT process, there is no ground plane at the bottom of the substrate. It is difficult to implement ground connections. Usually, a ground ring is used surrounding the sub-circuits and a metal layer is drawn beneath the sub-circuits which are connected to the ground ring, which creates a ground plane. The interconnecting metal lines are also surrounded by a ground ring and a ground plane beneath (discussed in Section 5.3.3).

7.3.2 Exploration of different topologies

Although the layout in the SG13S SiGe HBT process is complicated, it has a few advantages. As seven metal layers are present, different topologies for the passive and active circuits can be easily explored, such as a broadside-coupled balun, a Gilbert-cell design. Cross-overs of the metal layers are easily implemented in the SG13S SiGe HBT process, as there is an option of seven different metal layers. In the PP10-10 GaAs

pHEMT process, not all design topologies can be explored easily due to unavailability of the extra metal layers which makes the routing difficult. In the SG13S SiGe HBT process, as no ground plane is present underneath, unlike the PP10-10 GaAs pHEMT process, there is a problem with the current return path in structures such as a balun. The ground connections are established using the ground rings and sometimes a metal layer is also used beneath a passive structure (as in the transmission line shown in Section 5.3.3).

7.3.3 Compactness of layout

There is no continuous ground plane at the bottom of the substrate in the SG13S SiGe HBT process and the interconnecting metal lines cannot be modelled as microstrip lines. The dimensions of the lines need not be absolutely dependent on the wavelength. The layout can be made compact by utilising different metal layers and implementing stacked structures. On the other hand, in the PP10-10 GaAs pHEMT process the interconnecting metal lines are modelled as microstrip lines. The dimensions of the metal lines are dependent on the wavelength of the design. Stacked structures cannot be implemented easily in this process, therefore the layout is spread over one plane.

As demonstrated in Section 5.3.3, ground rings are often used in the SG13S SiGe HBT process. All the circuit elements lying on the RF signal path are bounded by ground rings to isolate them from any interference from the surrounding metal structures. The circuit elements can be closely spaced. This also helps in making the layout compact as compared to the PP10-10 GaAs pHEMT process. In the PP10-10 GaAs pHEMT process, ground rings are not available, but sufficient space is maintained between the circuit elements to avoid interference from the surrounding metal structures. Therefore, the layout of the circuits requires more area.

A comparison of the performance of the frequency doublers implemented in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes is presented in Table 7.1.

TABLE 7.1: Comparison of the performance of the frequency doublers implemented in the PP10-10 GaAS pHEMT and the SG13S SiGe HBT process.

Parameter	**SG13S SiGe HBT**	**PP10-10 GaAs pHEMT**
Bandwidth [GHz]	14-30	22-40
Power consumption [mW]	23.5 (at 0 dBm input power)	45 (at 5 dBm input power)
Output power at $2f_o$ [dBm]	-3.8 (at midband, for 0 dBm input power)	0 (at midband, for 5 dBm input power)
Area [mm^2]	0.24	0.72

7.4 Linearity performance comparison

Selection of a particular process is crucial for circuit designers for successful implementation of the circuits. For high-frequency circuit designs, comparing only the f_T and f_{max} of the circuits is not sufficient, but it is important to know how much linearity can be obtained from a process, or how much the onset of non-linearity can be avoided. This is particularly useful for applications when designing receivers and transmitters for high-performance.

A frequency-doubler circuit is considered as an archetype for non-linear circuits that allow the study of harmonics as discussed in Chapters 5 and 6. For a frequency doubler, a balanced topology is selected as it cancels the odd harmonics inherently. A balun is required to generate the differential signals to drive the frequency doubler. This allows the study of imbalance in a balun which complements a balanced frequency doubler and affects the harmonics.

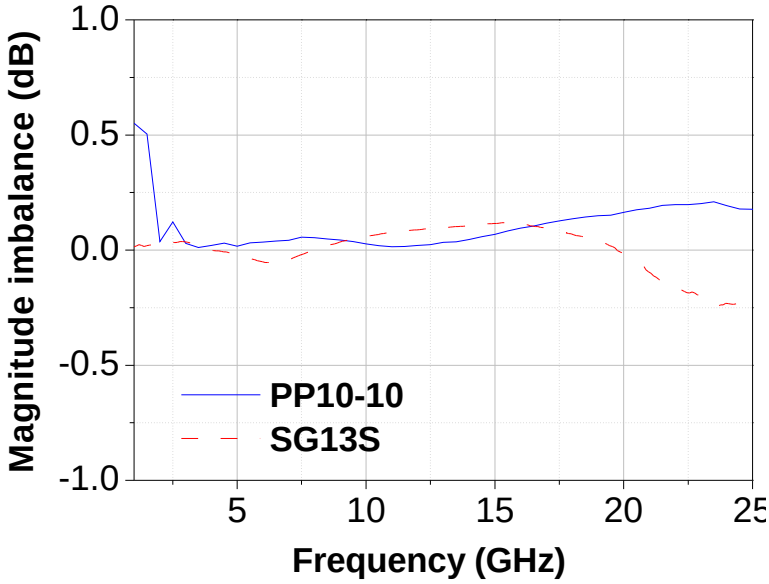
The analysis of a balanced frequency doubler using SG13S SiGe HBTs and PP10-10 GaAs pHEMTs is presented in Chapter 3. From the presented analysis, it is found that PP10-10 GaAs pHEMTs are more linear than SG13S SiGe HBTs. For the same bias conditions and the same gain, the harmonics generated in PP10-10 GaAs pHEMTs are significantly lower than in SG13S SiGe HBTs. The level of the odd harmonics at the output of the frequency doubler are dependent on three main factors: the match between the two transistors, symmetry in layout and balance of the differential signals, as mentioned in [87]. Among these factors, a good balance of the differential signal

is a significant determinant of the level of odd harmonics present at the output of the frequency doubler, as inferred from the analysis presented in Chapter 3.

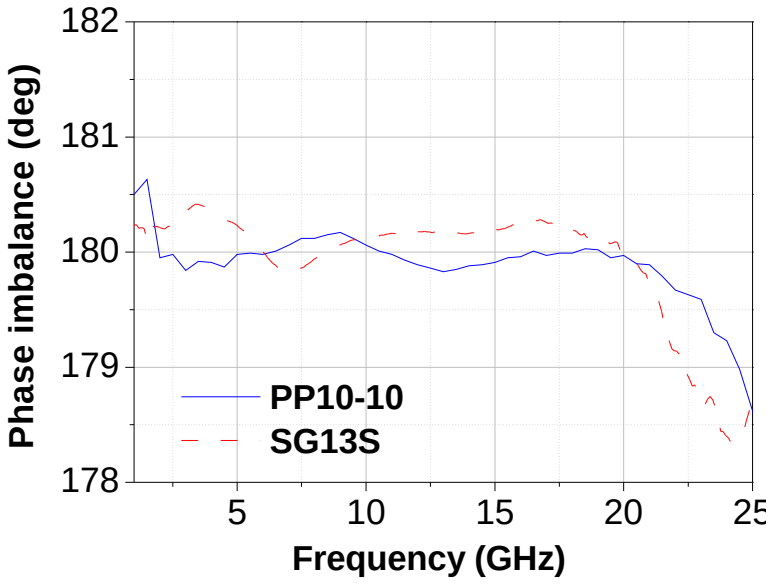
To investigate the imbalance of the baluns implemented in the two processes, the SG13S SiGe HBT and the PP10-10 GaAs pHEMT, a passive balun is selected (discussed in Chapter 4). For this application, a passive balun is favoured over an active balun which can add distortion to the generated signals. Transformer balun designs in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process are presented in Chapter 4. Five samples were measured for each of the baluns, to investigate the process variation. The balun in the SG13S SiGe HBT process is designed to drive a frequency doubler with 7 to 15 GHz input (shown in Section 4.5). The mean trace shows a magnitude imbalance of less than 0.13 dB, and a phase imbalance of less than 0.4^o, from 7 to 15 GHz. The transformer balun implemented in the PP10-10 GaAs pHEMT process is designed for a frequency doubler with 11 to 20 GHz input (shown in Section 4.6). The mean trace shows imbalances of less than 0.2 dB from 1 to 25 GHz and 1.5^o over 1 to 20 GHz. A comparison of the magnitude and phase imbalances of the transformer baluns in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process up to 25 GHz is depicted in Fig. 7.5.

The design and implementation of the frequency doubler in the SG13S SiGe HBT process is discussed in Chapter 5. A push-push topology is selected to implement the balanced frequency doubler. The input frequency range of the doubler in the SG13S SiGe HBT process is from 7 to 15 GHz and the output frequency range is from 14 to 30 GHz. As discussed in Section 5.5.2, one of the input biases is tuned to improve the odd-harmonic rejection. The measured fundamental rejection is better than 35 dB and the third-harmonic rejection is better than 40 dB across the output band.

Chapter 6 focuses on the design and implementation of a frequency doubler in the PP10-10 GaAs pHEMT process. The frequency doubler is designed using 0.1 μm pHEMTs in the K-Ka band range. The input frequency range of the doubler is from 11 to 20 GHz while the output is from 22 to 40 GHz. The measured fundamental rejection is better than 35 dB and the third-harmonic rejection is better than 35 dB across most

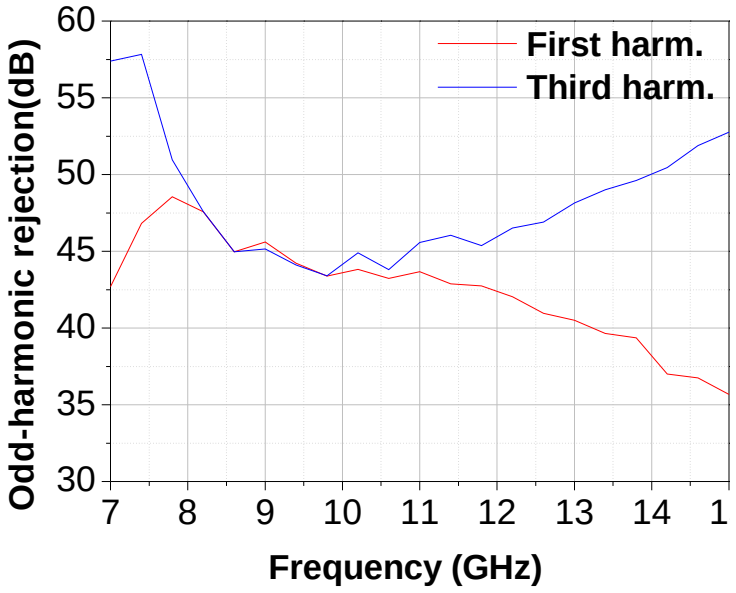


(a)

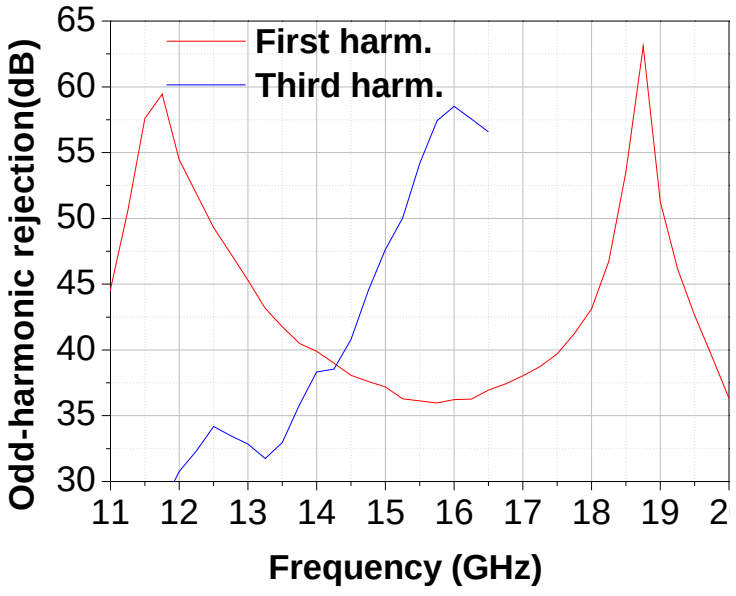


(b)

FIGURE 7.5: Comparison of imbalances of the transformer baluns in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes: (a) Magnitude imbalance, (b) Phase imbalance.



(a)



(b)

Figure 7.6: Odd-harmonic rejection at the output of the frequency doubler for, (a) the SG13S SiGe HBT and (b) the PP10-10 GaAs pHEMT processes.

of the output frequency range (due to instrument limitations the output could only be measured up to 50 GHz). The odd-harmonic rejections for the implemented frequency doublers in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes are shown in Fig. 7.6.

From the frequency-doubler results obtained in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process, it can be stated that it is possible to achieve comparable odd-harmonic rejection, over a similar bandwidth, from both processes.

7.5 Application to higher frequency

The demand for high-data-rate wireless communication systems is increasing day by day. To cater to the growing demands of high-speed communication systems, network operators are constantly seeking alternative frequency spectrum. The lightly licensed E-band is emerging as useful for high-capacity point-to-point communication. E-band offers technological and economic advantages over the existing systems. It is predicted to be the next-generation wireless backhaul spectrum.

The frequency-doubler designs in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes (presented in Chapters 5 and 6) are implemented in the K-Ka band range. With the successful implementation of the designs, as is evident from the good agreement between the simulation and measured results, these designs can be replicated for E-band applications. This would also justify the design flow established in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes. The transformer balun designs in both the processes for driving E-band frequency doublers are presented here.

7.5.1 E-band balun in the SG13S SiGe HBT process

Design details

The transformer balun design implemented in the SG13S SiGe HBT process over the 7-15 GHz range (shown in Section 4.5) is followed for the high-frequency balun. The

targeted input frequency range for the balun is from 30 to 50 GHz to be able to drive an E-band frequency doubler.

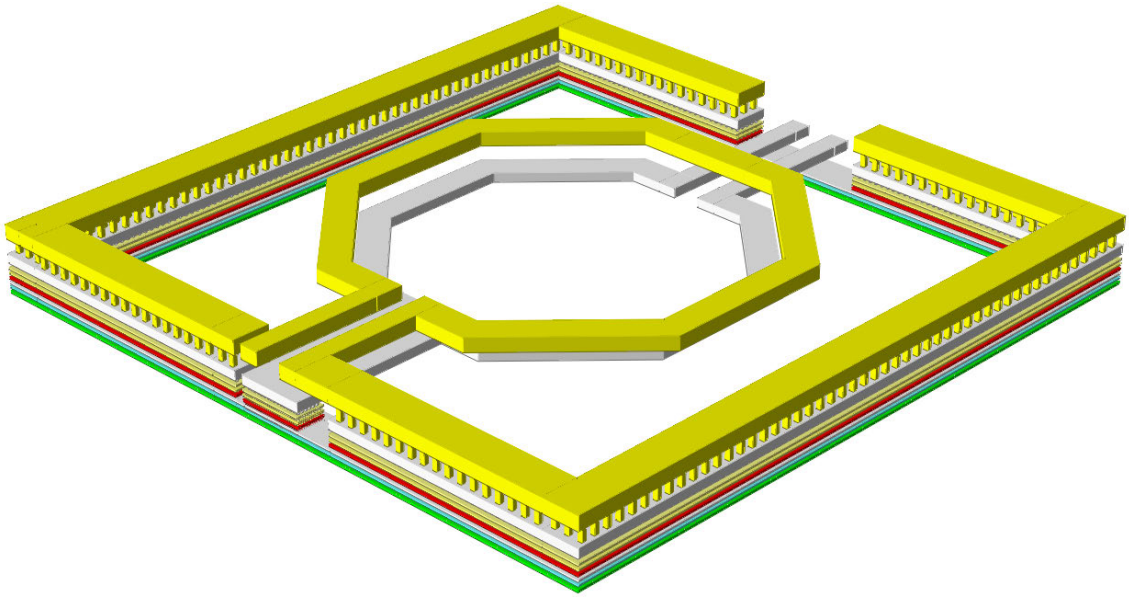


Figure 7.7: Schematic representation of the transformer balun for an E-band doubler.

As before, broadside coupling is used for the transformer balun design. The primary and secondary coils of the designed balun are implemented in the thick metal layers TM2 and TM1 respectively. Thick metal layers minimise metal losses and reduce the coupling to the lossy substrate. The schematic of the balun is shown in Fig. 7.7. The centre tap of the secondary coil is grounded, as this reduces the imbalance. To further improve the magnitude and phase balances, an offset of 6 μm is maintained between the primary and the secondary coils. A ground ring surrounding the balun is used to provide shielding from surrounding metal interference, also it aids the electromagnetic simulation by providing a ground reference for the excitation ports. Combinations of series and parallel capacitors are used at the input and output for matching.

Simulation results

The simulated S_{11} of the designed balun is better than -10 dB between 33 GHz and 50 GHz as shown in Fig. 7.8.

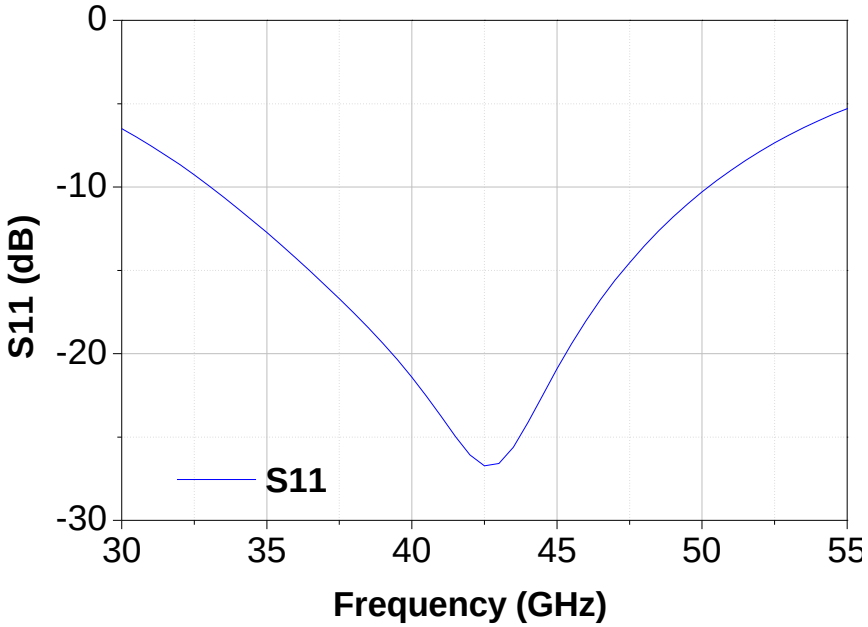


FIGURE 7.8: Simulated S_{11} of the transformer balun.

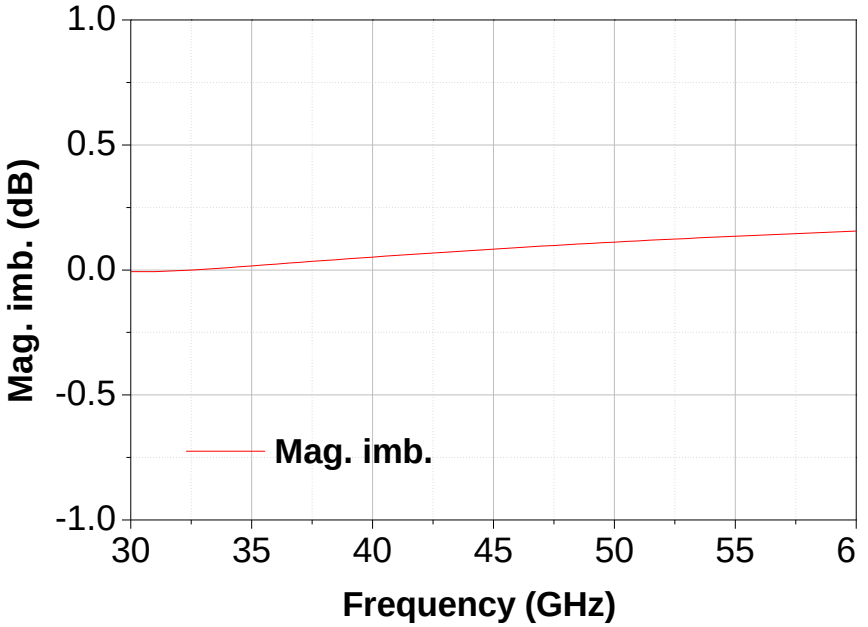


FIGURE 7.9: Simulated magnitude imbalance of the transformer balun.

The simulated insertion loss at the mid-band is 1.5 dB. The simulated magnitude imbalance of the balun is less than 0.15 dB over 30 to 60 GHz. The simulated phase imbalance is less than 1^o from 33 to 60 GHz. The simulated imbalances of the balun

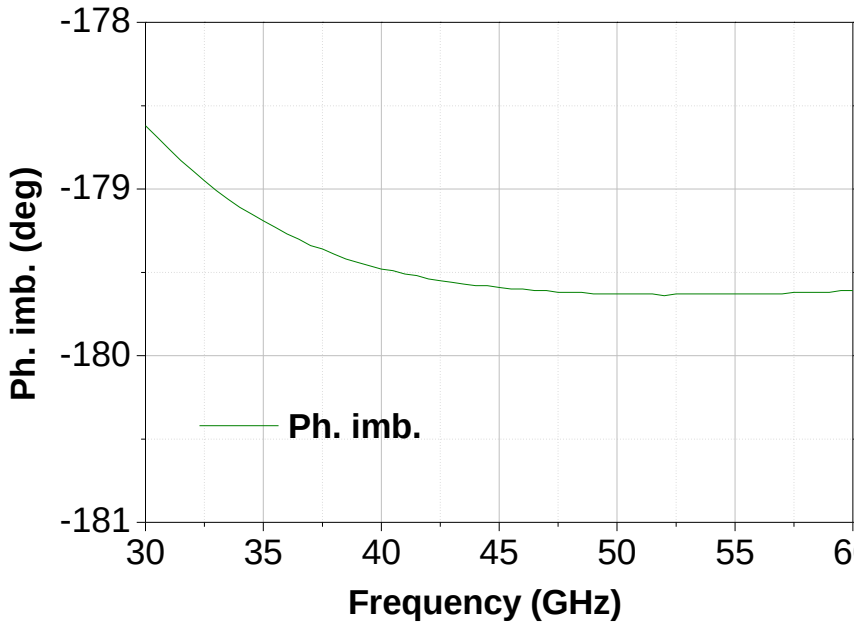


Figure 7.10: Simulated phase imbalance of the transformer balun.

are shown in Fig. 7.9 and Fig. 7.10.

7.5.2 E-band balun in the PP10-10 GaAs pHEMT process

Design details

The design principle followed for the 10 to 20 GHz transformer balun design in the PP10-10 GaAs pHEMT process is adopted. The intended input frequency range of the transformer balun is from 30 to 50 GHz for driving the E-band doubler. The details of the transformer balun design in the PP10-10 GaAs pHEMT process are presented in Section 4.6. The edge-coupled technique is used for implementation of the balun.

The primary and the secondary coils lie side by side. A double metal layer is used for implementing the primary and the secondary coils to minimise the metal losses, and so permit more current. As this is an edge-coupled structure, the primary and the secondary coils are kept at the minimum separation of 5 μm (according to the design rule limit) to increase the coupling coefficient.

The secondary coil is placed on the outer side of the primary coil. This enables a

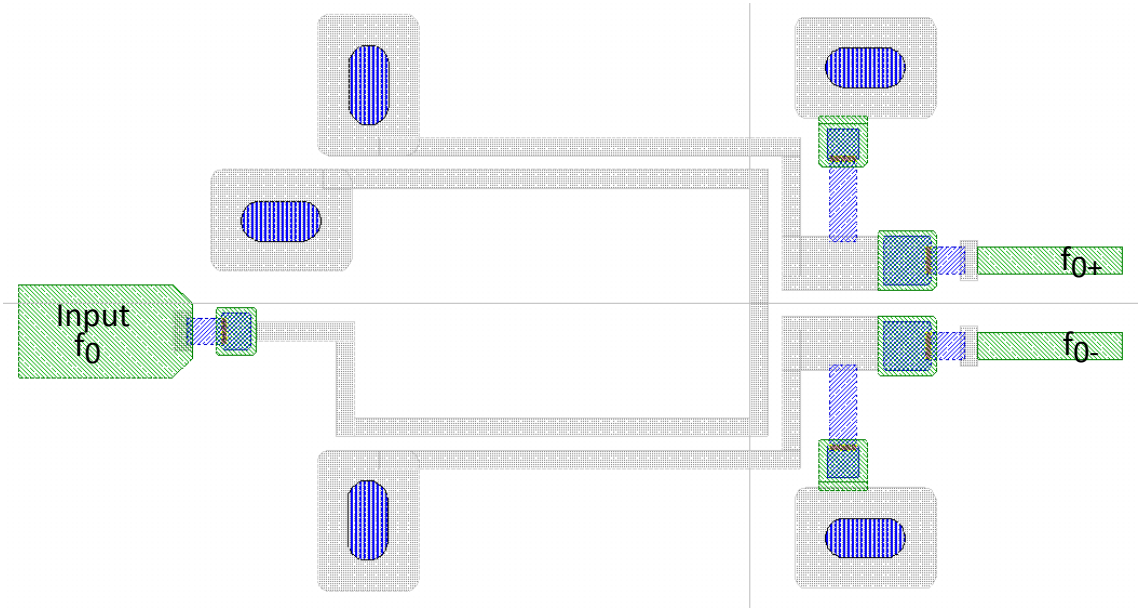


FIGURE 7.11: Schematic representation of the transformer balun for an E-band doubler.

symmetric layout without any cross-over of the metal lines. The centre tap is grounded to minimise the imbalances. As mentioned in Chapter 4, the position of the ground affects the phase imbalance [87]. To improve the matching, a combination of series and parallel capacitors is used. The total area of the structure is approximately 0.07 mm^2. There is a design-rule limit for the minimum dimension of the back-via as described in Section 6.4. At this high frequency the dimension of the back-via affects the overall size of the structure. The schematic of the designed balun is shown in Fig. 7.11.

Simulation results

The simulated S_{11} of the designed balun is better than -10 dB between 29 GHz and 47 GHz as shown in Fig. 7.12.

The simulated insertion loss at the mid-band is 1.5 dB. The simulated magnitude imbalance of the balun is less than 0.1 dB from 30 to 50 GHz and 0.28 dB up to 60 GHz. The simulated phase imbalance is approximately 1.2^o from 30 to 50 GHz and up to 1.5^o at 60 GHz. The simulated magnitude and phase imbalances of the balun are shown in Fig. 7.13 and Fig. 7.14.

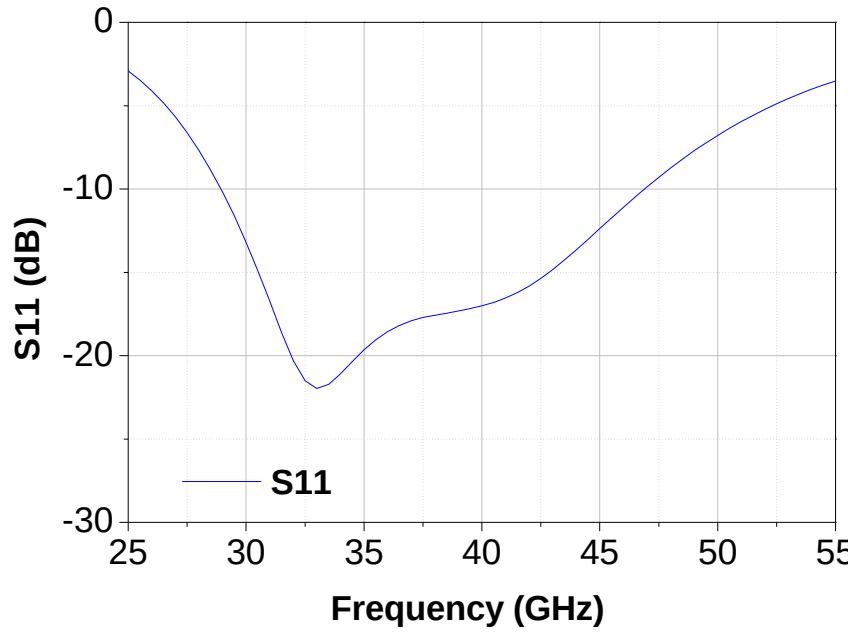


Figure 7.12: Simulated S_{11} of the transformer balun.

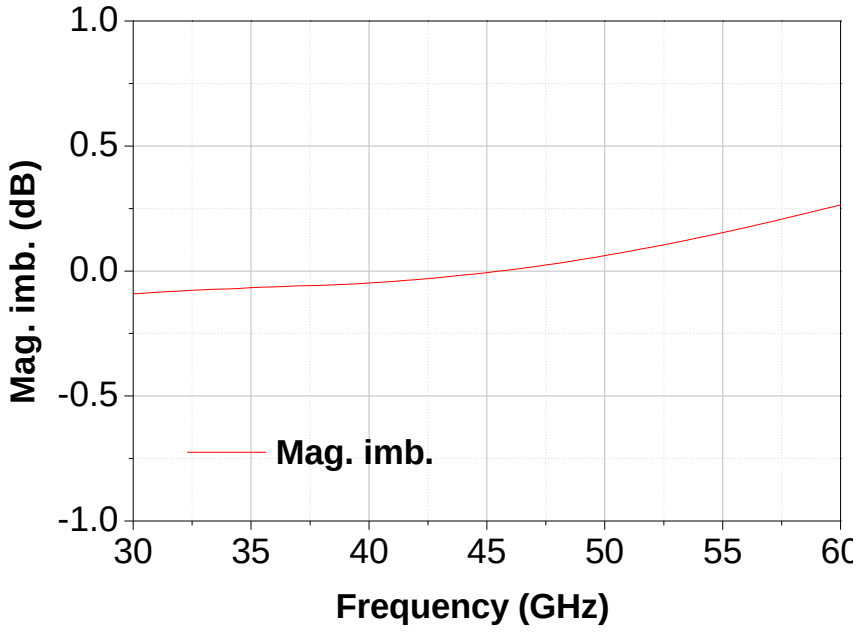


Figure 7.13: Simulated magnitude imbalance of the transformer balun.

The simulated results of the transformer baluns for E-band frequency doublers, in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes, are comparable to each other. These results look reasonable compared to the reported performances of baluns in the literature.

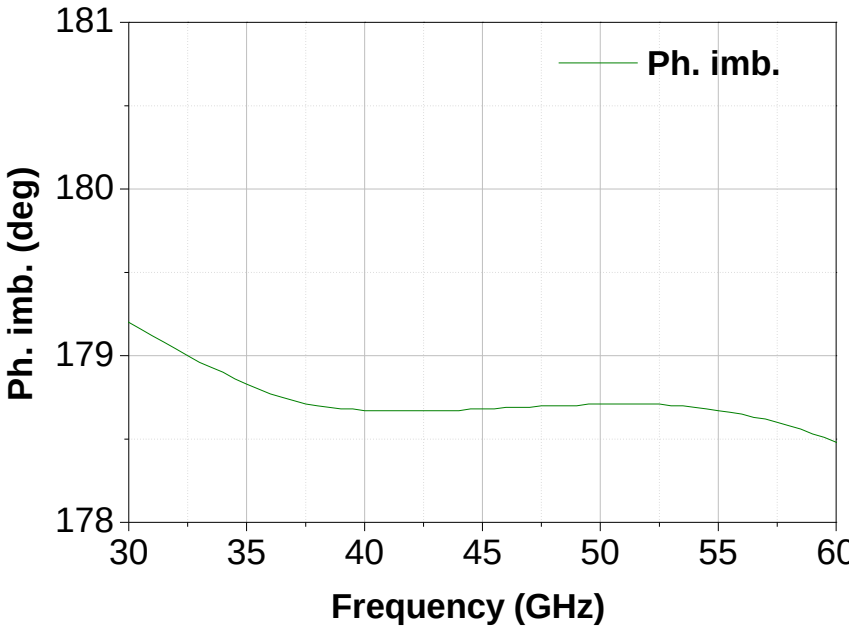


FIGURE 7.14: Simulated phase imbalance of the transformer balun.

7.6 Discussion and conclusion

The specifications of the 0.1 μm pHEMTs in the PP10-10 GaAs pHEMT process and the HS-HBTs in the SG13S SiGe HBT process show that both of these devices can be used for high-frequency applications. It is important to study the inherent linearity of a particular process, to be able to successfully implement circuits such as frequency multipliers, mixers, amplifiers with high performance. To compare the suitability of the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes in terms of linearity, a frequency-doubler circuit is considered as the archetype of non-linear circuits. The performance of the frequency doubler generally limits the overall linearity of a receiver or transmitter by its non-ideal harmonic generation. Analysis of the harmonics in PP10-10 GaAs pHEMTs and SG13S SiGe HBTs shows that PP10-10 GaAs pHEMTs are inherently more linear than SG13S SiGe HBTs. Despite the differences in the inherent linearity in the two processes, it has been demonstrated that it is possible to achieve good odd-harmonic rejection from the frequency doublers implemented in the two processes. In other words, with careful circuit design and analysis, it is possible to achieve comparable linearity from both the processes over a similar bandwidth. Apart

from the linearity, other design parameters such as power consumption, available output power, and the noise figure of the circuits implemented in the two processes should be considered before selection of a particular process for the desired application.

8

Conclusion

The non-ideality of the active and passive circuits can limit the overall linearity of a system such as a wireless transmitter or receiver. The key question in this context, is what level of QAM system can be supported by a particular technology. This thesis topic was proposed by industry partner MACOM as part of this ARC Linkage Project and is directly derived from a question of profound industrial importance: at what point is the up-and-coming SiGe-based IC technology a viable replacement for the GaAs-based incumbent in MACOM's most advanced products. Two process technologies, the SG13S SiGe HBT and the PP10-10 GaAs pHEMT, are considered for comparison of process linearity. A frequency-doubler circuit is used as an archetype of non-linear circuits which allows the study of harmonics. A balanced topology of the frequency-doubler circuit is found to be suitable for this study which also allows the

study of a balun. A transformer balun has been used as an archetype of passive structures. Frequency-doubler circuits and transformer baluns are implemented in both the processes for the purpose of comparison. This chapter provides a conclusion to the dissertation with a discussion of the main project outcomes and suggestions for future work.

8.1 Scope of Project

With the development of the semiconductor industry over the years, a circuit designer now has the option to exploit different devices in different semiconductor materials. Given the different available options, a circuit designer needs to select the appropriate process technology for successful implementation of a circuit. The two main driving factors for circuit designers are the high performance of the circuits and low cost of fabrication.

At microwave and millimetre-wave frequencies, the GaAs process has been dominant over the silicon-based technologies for higher performance over the last few decades. Silicon is known for its device density, low-cost volume production and integration of RF, analogue, and digital functionality. Also, recent advancements in silicon-based processes make it suitable for microwave and millimetre-wave circuits. The f_T and f_{max} of different processes cannot be the deciding factor in selecting a particular technology; it is important to determine the inherent non-linearity of a particular process. This is because the overall system linearity is limited by the inherent non-linearity of the transistors and the non-idealities of the passive circuits that disrupt the ideal performance of balanced architectures. It is particularly important for system-level designs such as transmitters and receivers. The aim of this dissertation is to study the non-linearity of two processes (GaAs and SiGe), or in other words how much linearity could be obtained from a particular process. For this purpose, a frequency doubler is considered as an archetype of a non-linear circuit.

With the growing demands of wireless communication systems and the availability

of high-frequency devices, recent research is constantly being pushed to the millimetre-wave range and above. Gradually passive structures are also being integrated on-chip. For high-frequency applications, to ensure good overall system performance, it is essential to integrate the passive structures on-chip to provide a system-on-chip solution. Therefore, it is also important to characterise the passive structures in a particular process. A transformer balun is considered as an archetype of a passive structure. Also, it complements a frequency-doubler circuit when a balanced architecture is used for the doubler. The aim of this dissertation is also to study the non-linearity of a passive balun in terms of its imbalance, to identify the cause of the imbalance and to find out ways to improve the balance of the balun.

For the purpose of comparison, the above-mentioned circuits are implemented in two different processes, the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process, and tested. To establish a methodology or a design flow in both the processes for reliable circuit implementation falls within the scope of this dissertation. It has been found that it is important to model the transistors to improve the accuracy of the simulation results with respect to measurements, but the accurate modelling of the transistors is out of the scope of this dissertation.

8.2 Project Outcomes

This dissertation is covered in eight chapters. The motivation for this work is presented in Chapter 1 and the background and literature review are presented in Chapter 2. The contributions of the dissertation are presented in Chapters 3 to 7.

8.2.1 Demonstrate frequency doubler as an indicator of process linearity

The purpose of this project is to compare the suitability of the two common process technologies: GaAs and the silicon-based process, for high-frequency circuit design. Among the silicon-based processes, SiGe technology has been selected based on the

advanced device performance. The development of the devices (pHEMTs and HBTs) available in these processes is studied in a literature review. The motivation of the performance comparison in these two processes came from the comparable device features available in today's technology and the attraction of SiGe's ability to integrate with analogue and digital functionality, assuming that the RF performance is comparable. A comparative study of the circuit design in both processes will help a circuit designer to make a decision in selecting a particular process based on their requirements.

Generally, GaAs is used for high performance at high frequency, whereas silicon-based processes are preferred for a low cost. In Chapter 1, the parameters of the devices, pHEMTs in GaAs and HBTs in SiGe, are compared. Future predictions for the development of these devices are studied from the literature and the parameters reported by the manufacturing companies. The study on the device parameters presented in Chapter 1 provided the motivation of the proposed work presented in this dissertation.

For the process comparison, it is not sufficient to compare the performances of the available devices, but it will be useful to have an insight of the process itself. Study of the behaviour of a non-linear circuit will provide useful information as the linearity of an overall system is affected by the inherent non-linearity of the transistors and also the non-idealities of passive structures used in balanced architectures. Moreover, there are some inherent differences between the pHEMTs and the HBTs. Therefore, a simple frequency-doubler circuit is proposed as an archetype of non-linear circuits in the presented work as it allows the study of harmonics. Furthermore, a balun is proposed as an archetype of a passive structure that will highlight the performance of passive structures that can be achieved in these two processes. Also, one key reason to study the balun is to see how a preferred balun architecture for a given technology (SiGe or GaAs) contributes to phase and amplitude imbalance which affect the overall linearity of a system. As a balun complements a balanced frequency doubler, this study will reflect the performance of the system-on-chip solution available in these two processes.

8.2.2 Analyse effect of topology on linearity

For this project, the PP10-10 GaAs pHEMT process and the SG13S SiGe HBT process technology are selected to implement the circuits for the purpose of establishing a methodology for an actual comparison of the inherent linearity from a particular process.

Based on frequency doublers reported in the literature, there are two main categories : active and passive. The passive doublers suffer from several disadvantages such as conversion loss, large input power drive, narrow band and susceptibility to any small changes in the circuit parameters. An active frequency doubler using transistors is more relevant for this project as it allows the study of the harmonics generated from a GaAs pHEMT or a SiGe HBT. Single-ended, balanced and Gilbert-cell multipliers are reported in the literature for the implementation of a frequency doubler. For our work, a balanced frequency doubler is selected, as it cancels the odd harmonics inherently, and gives an opportunity to investigate a balun. A balanced topology can be used for broad band designs. Hence, a balanced topology is selected for the frequency-doubler design.

8.2.3 Frequency-doubler analysis

A simple balanced topology of a frequency doubler is selected using a push-push pair. Chapter 3 presents the analysis of the harmonics of a frequency doubler using a push-push pair. At the beginning of Chapter 3, an analysis of the frequency doubler using SG13S SiGe HBTs is presented. The harmonics generated in the collector current of a bipolar transistor are determined. Some correction factors are introduced to the bipolar transistor analysis to represent the harmonics of a SG13S SiGe HBT. Then the harmonics at the output of the doubler are predicted, considering an ideal balanced signal at the input of the push-push pair. A step-by-step analysis of the harmonics is given, considering first only amplitude imbalance, then only phase imbalance and finally both amplitude and phase imbalance in the input differential signals. A similar set of analyses is shown for the frequency doubler using PP10-10 GaAs pHEMTs. At first,

the harmonics in a single FET are predicted. Then correction factors are introduced to modify the equation to represent the harmonics in a PP10-10 GaAs pHEMT. Then the harmonics at the output of the frequency doubler using PP10-10 GaAs pHEMTs are shown, for different cases of imbalances in the input differential signals. For the purpose of comparison of the harmonics in the collector current of a SG13S SiGe HBT and the harmonics in the drain current of a PP10-10 GaAs pHEMT, the gate bias voltage, the load and the multiplication factor of the pHEMT are set in such a way that the same DC bias current flows through it as for the SG13S SiGe HBT and the same voltage gain is obtained in both cases.

From the analysis presented in Chapter 3, it is found that PP10-10 GaAs pHEMTs are inherently less non-linear than SG13S SiGe HBTs. It has been found that the amplitude and phase imbalances of the differential signals at the input of the balanced frequency doubler in both the processes, degrade the odd-harmonic rejection. This analysis is verified by comparing MATLAB plots with the AWR simulation. From this analysis, it has been inferred that imbalance in the differential signals at the input of the balanced frequency doubler is a significant determinant of the odd-harmonic rejection. This makes the balun design critical in both the processes, the SG13S SiGe HBT and the PP10-10 GaAs pHEMT.

8.2.4 Balun analysis

The analysis of the baluns is presented in Chapter 4. From the frequency-doubler analysis in Chapter 3, it is inferred that balance of the differential signals is crucial for good odd-harmonic rejection at the output of the doubler. Also, for practical implementation, it is desirable to design baluns with compact size.

An active balun can add distortion into the generated differential signals. As the purpose of our project is to study the harmonics, a passive balun is a default choice. Mainly two types of passive baluns, Marchand baluns and transformer baluns, are studied. As a conventional Marchand balun consists of quarter-wavelength coupled lines, their physical size is large, especially at a lower frequency. The dimensions of a transformer balun are not dependent on quarter-wavelength coupled lines and it is

compact in size. Using the coupled-line models, it has been shown that the bandwidth of the Marchand balun is larger than that of the transformer balun. The MATLAB simulations are also verified with EM simulation in AWR. Further, it has been found from the EM simulations that, for the same length of coupled-line structures, the balance of the transformer balun is better than that of the Marchand balun (shown in Section 4.3.3).

8.2.5 Critical components of circuit implementation

The design and implementation of the baluns in the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process are presented in Chapter 4 and the frequency-doubler circuits in the two processes are presented in Chapters 5 and 6. A push-push topology is selected to implement the balanced frequency doublers.

Baluns

The designs of transformer baluns in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes are shown in Chapter 4. According to the frequency-doubler analysis presented in Chapter 3, balance in the differential signals is a critical parameter for the frequency-doubler design.

In the SG13S SiGe HBT process, broadside-coupled transformer baluns are implemented, being supported by this process technology. It has been found that the best way to minimise the imbalance in the differential signals is to ground the centre tap of the secondary coil. Also, an offset between the radii of the primary and the secondary coils is introduced to further minimise the imbalances. The transformer balun in the SG13S SiGe HBT process is designed to drive a frequency doubler with 7 to 15 GHz input (shown in Section 4.5). The mean trace shows a magnitude imbalance of less than 0.13 dB, and a phase imbalance of less than 0.4^o, between 7 and 15 GHz. The results of the transformer balun implemented in the SG13S SiGe HBT process have been published as a conference paper:

- S. Chakraborty, L. E. Milner, L. T. Hall, X. Zhu, O. Sevimli and M. C. Heimlich, "Characterisation of a Transformer Balun for a 7-15 GHz SiGe Frequency

Doubler", *Australian Microwave Symposium (AMS 2016)*, Adelaide, Australia.

In the PP10-10 GaAs pHEMT process, only the edge-coupled technique can be used due to the process limitations. It has been found that the ground at the centre tap of the secondary coil is crucial for minimising the imbalances in the differential signals. To avoid cross-over of the metal layers, the secondary coil is placed on the outer side of the primary coil. The position of the back-via for implementing the ground connection affects the imbalance. The transformer balun implemented in the PP10-10 GaAs pHEMT process is designed for a frequency doubler with 11 to 20 GHz input (shown in Section 4.6). The mean trace shows imbalances of less than 0.2 dB over 1 to 25 GHz and 1.5^o over 1 to 20 GHz.

The results of the transformer balun implemented in the PP10-10 GaAs pHEMT process are currently being considered for publication and the manuscript is in progress.

Different techniques for minimising the imbalances in the transformer baluns in both processes are discussed in Chapter 4 in detail. The results of the transformer baluns in both the processes are better than for state-of-the-art designs (shown in Chapter 4).

Frequency doubler in the SG13S SiGe HBT process

Minimising non-idealities in a doubler

The input frequency range of the doubler designed in the SG13S SiGe HBT process is from 7 to 15 GHz and the output frequency range is from 14 to 30 GHz. For this broadband frequency doubler, as the fundamental and the third harmonics fall into the desired output band, the odd harmonics cannot be suppressed with the help of a filter. It has been found that a balanced topology is useful to suppress the odd harmonics over a broad band. As shown in the frequency-doubler analysis in Chapter 3, the balance of the input signals is found to be crucial for odd-harmonic rejection. The transformer balun (shown in Section 4.5) is used with the balanced frequency doubler. A stagger-tuning technique is used between the transformer balun and the frequency doubler to achieve a flat second-harmonic response at the output. As the SG13S SiGe HBTs are

inherently non-linear, it is possible to drive the frequency doubler with 0 dBm input power for which the second harmonic power of -3.8 dBm is measured at the mid band. The total power consumption at 10 GHz for 0 dBm input power is 23.5 mW from a 1.7 V power supply.

Design flow and layout

Symmetry in the layout and identical transistors are also important for minimising unwanted harmonics. One of the input biases is tuned to compensate for any asymmetry in layout and mismatch between the transistors (as discussed in Section 5.5.2). Bias tuning improved the odd-harmonic rejection by up to 2 dB. The measured fundamental rejection is better than 35 dB and the third-harmonic rejection is better than 40 dB across the output frequency band. P-cells are used to make the layout fast and efficient. Once a library of P-cells is developed they can be used repeatedly in the layout. In the SG13S SiGe HBT process it is particularly difficult to manage all the seven metal layers and the via connections. Use of P-cells makes it easy to implement the layout. In the proposed design flow (Section 5.3.2), a methodical approach is followed that allows the circuit designer to complete the schematic simulation, EM simulation and the layout efficiently. Good agreement between the simulated and the measured results validates the design flow. The results of the frequency doubler implemented in the SG13S SiGe HBT process have been published as an article.

- S. Chakraborty, L. E. Milner, X. Zhu, L. T. Hall, O. Sevimli and M. C. Heimlich, "A K-band Frequency Doubler with 35-dB Fundamental Rejection Based on Novel Transformer Balun in 0.13 μm SiGe Technology", *IEEE Electron Device Letters*. vol. 37, no. 11, pp. 1375-1378, Nov. 2016.

Frequency doubler in the PP10-10 GaAs pHEMT process

Minimising non-idealities in a doubler

The input frequency range of the doubler designed in the PP10-10 GaAs pHEMT process is from 11 to 20 GHz and the output frequency range is from 22 to 40 GHz.

Based on the analysis of the frequency doubler presented in Chapter 3, a balanced topology is found to be the best way to implement the broad-band frequency doubler. Similarly to the frequency-doubler design in the SG13S SiGe HBT process, a push-push topology is used for the implementation of the frequency doubler. The transformer balun with good balance performance (shown in Section 4.6) is used with the balanced frequency doubler.

As the PP10-10 GaAs pHEMTs are inherently less non-linear than the HBTs, large input power is required to drive the frequency doubler as compared to the doubler in the SG13S process. For 5 dBm input power, the measured second-harmonic power at mid band is 0 dBm. The total power consumption at 15 GHz is 45 mW at 4 V supply.

Design flow and layout

Due to the requirement of the biasing conditions of PP10-10 GaAs pHEMTs, a self-biasing technique is used. The layout is symmetrical in this case, unlike the frequency doubler in the SG13S SiGe HBT process, in which asymmetry is introduced due to routing of bias lines through different lengths. Hence the bias tuning technique is not applicable for this frequency doubler. It is important to maintain symmetry in the overall layout (shown in Section 6.4). The design flow (Section 6.3.2) adopted in the PP10-10 GaAs pHEMT process proposes one single EM structure for the whole design, unlike the design flow adopted in the SG13S SiGe HBT process, which takes a longer time for a larger circuit. But this method is used as ground rings are not used as in the SG13S SiGe HBT process, and one single EM block helps to capture the interference from the adjacent circuit elements. The measured fundamental rejection is approximately 35 dB across the output frequency range, and the third-harmonic rejection is better than 35 dB up to 50 GHz (due to instrument limitations the output could only be measured up to 50 GHz). Good agreement between the simulated and the measured results validates the design flow.

The results of the frequency doubler implemented in the PP10-10 GaAs pHEMT process are being considered for publication.

8.2.6 Selection of a suitable process

The literature review on the SG13S SiGe HBT and PP10-10 GaAs pHEMT processes, frequency doublers and baluns are presented in Chapter 2. From the literature review of the silicon-based processes, it has been found that BiCMOS technologies are being used for microwave and millimetre-wave applications nowadays. According to the European DOTFIVE project, among the different companies who manufacture HBTs in the SiGe process IHP is a leader in terms of device performance. The predicted ITRS roadmap for the f_T and f_{max} of IHP's HBTs in the future looks promising. IHP's SG13S process has a HS-HBT with f_T and f_{max} of 250 GHz and 300 GHz respectively (for devices with an emitter length of 2 μm). The β of the transistor at a V_{BE} of 0.7 V is 900 and the collector-emitter breakdown voltage is 1.7 V. Both the β and the f_T make SG13S very attractive to millimetre-wave circuit designers.

From the literature review on the GaAs process, it has been found that several companies such as WIN Semiconductors, Wavetek, Triquint manufacture high-performance GaAs pHEMTs. WIN Semiconductor's PP10-10 process offers 0.1 μm pHEMTs with f_T and f_{max} of 130 GHz and 180 GHz respectively. To the best of the author's knowledge, this is the highest reported f_T and f_{max} of GaAs pHEMTs from any merchant manufacturer or pure-play foundry. The drain-to-gate breakdown voltage is 9 V.

From the frequency-doubler results obtained with the SG13S SiGe HBT process and the PP10-10 GaAs pHEMT process, it can be stated that it is possible to achieve comparable odd-harmonic rejection, over a similar bandwidth, from both processes despite the inherent differences between the devices, PP10-10 GaAs pHEMTs and SG13S SiGe HBTs. In other words, it is possible to minimise the non-idealities from a frequency doubler, which will help to achieve the required linearity in the overall system. In this respect the balun design is crucial in both the processes as the frequency doublers are sensitive to the balance of the differential signals. But critical challenges exist in each of the processes for successful circuit implementation.

8.3 Future Opportunities

The analysis of the frequency doubler, analysis of the baluns, details of the design and implementation of the frequency doublers in the two processes SG13S SiGe HBT and PP10-10 GaAs pHEMT are presented to investigate the inherent non-linearity in these two processes and hence the linearity that could be achieved in these processes. However a few points were noted during this project which are out of the scope of this dissertation, but these issues can be explored in future.

8.3.1 Models for the HBTs

The difference in the measured and the simulated power levels of the harmonics of the frequency doubler in the SG13S SiGe HBT process is larger than that for the PP10-10 GaAs pHEMT process. In the SG13S SiGe HBT process, aluminium pads are used, unlike the gold pads in the PP10-10 GaAs pHEMT process. It is found that the measurements with the aluminium pads are more difficult than with gold pads, as the aluminium pads get oxidised very quickly. The measurement results depend on the probe landing position. Nickel-tipped probes are used to make the measurement more reliable.

The author thinks that the models of the SG13S SiGe HBTs could be improved for high-frequency applications, for a better match between the simulated and measured results. For the frequency-doubler design in the PP10-10 GaAs pHEMT process, the foundry models of the transistors were not used. Improved device models developed by MACOM Technology Solutions, North Sydney design centre were used. Accurate modelling of the SG13S SiGe HBTs at higher frequencies could provide better predicted results through EM simulation.

8.3.2 Improvement of balun models

An analysis of the Marchand balun and the transformer balun is presented in Chapter 4. The equations for the S-parameters are derived using the coupled-line models. From the derived equations, the variation of the bandwidth with the coupling coefficient is shown

for both the Marchand balun and the transformer balun. An analysis of the magnitude and phase imbalances for both baluns is presented using EM simulation. The equations derived from coupled-line models cannot capture the effect of the magnitude and phase imbalances. These models can be improved to capture the effect of imbalance.

8.3.3 Improvement of power level of second harmonic

The frequency doublers implemented in the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes provide large odd-harmonic suppression. The level of the harmonics also depends on the input power level. Good odd-harmonic suppression is maintained with respect to an input power sweep. But the power levels of the second harmonic could be improved, important for driving the next stage.

For the frequency doubler implemented in the SG13S SiGe HBT process, a second-harmonic power of -3.8 dBm is obtained at the mid band for 0 dBm input power (shown in Section 5.5). For the design implemented in the PP10-10 GaAs pHEMT process, the second-harmonic power at the output is around 0 dBm for an input power of 5 dBm (shown in Section 6.5). A simple push-push configuration is used to implement the balanced topology of the frequency doubler, in order to study the harmonics at the output. The frequency-doubler circuit can be modified to get conversion gain. The author thinks that a balanced cascode topology should be explored to get conversion gain, and at the same time, good odd-harmonic suppression can be maintained.

8.3.4 Implementation of a E-band doubler

One of the aims of this dissertation is to establish a good design flow in both the SG13S SiGe HBT and the PP10-10 GaAs pHEMT processes for efficient circuit implementation. The successful implementation of the frequency doublers in both processes justifies the design flow followed in both processes. In order to verify it further, designs can be implemented at a higher frequency, such as E-band. As the lightly licensed E-band is emerging as useful for high-capacity point-to-point communication and it

offers technological and economic advantages over the existing systems, frequency-doubler designs can be replicated at this frequency band. The simulation results of the transformer baluns in both processes for driving E-band doublers are presented in Section 7.5. The simulation results indicate that good balance can be obtained from these transformer baluns. Similarly, the frequency-doubler circuits can be implemented at this high-frequency range to further test the design flow.

A

Appendix A

A.1 Energy Band Diagram

Herbert Kroemer, in his Nobel Lecture, Quasi-Electric Fields and Band Offsets: Teaching Electrons New Tricks, 8 December 2000, at Aula Magna, Stockholm University, mentioned:

"Whenever I teach my semiconductor-device physics course, one of the central messages I try to get across early is the importance of energy-band diagrams. I often put this in the form of Kroemer's Lemma of Proven Ignorance:

If, in discussing a semiconductor problem, you cannot draw an Energy Band Diagram, this shows that you don't know what you are talking about,

with the corollary

If you can draw one, but don't, then your audience won't know what you are talking

about."

A.1.1 SiGe HBT

Importance of Germanium doping

The dynamic performance of transistors is often characterised by f_T and f_{max}. These two parameters are dependent on transistor resistances, capacitances and carrier transit times as described in equations 1.1-1.2. To reduce the carrier transit times in the base of silicon bipolar transistors, the width of the base is shortened. But if it is pushed to the limit, short-channel effects come into play. With the help of bandgap engineering, the f_T of the transistors is improved by selective incorporation of Germanium into the base of the silicon bipolar transistor. This led to the development of SiGe HBTs which also increased the process complexity [110], [111], [112]. This bandgap grading in a SiGe HBT results in an accelerating drift field which facilitates the minority-carrier transport through the base. Extensive study on the Germanium doping profile for minimising the base transit time has been reported in the literature, for example [114], [115], [116], [117]. Also the base grading profile in SiGe HBTs improves transistor parameters such as β, g_m compared to silicon BJTs [113].

Doping profile

The effect of the Ge doping in the base of a SiGe HBT can be explained by an energy-band diagram. For an NPN HBT, the emitter and collector are n-type and the base is p-type doped with a SiGe layer. The conduction band in the base bends upward as it is p-type whereas the conduction bands at the emitter and collector bend downward. Due to the Ge doping in the base, the band gap in a SiGe HBT is less than for Si BJTs. As delineated in Fig. A.1 [7], the conduction band in the base of a SiGe HBT is lower than that of a Si BJT. A graded Ge doping profile is used in the base of the HBT, with a higher concentration at the emitter end than at the collector end. This results in a downward slope of the energy bands from the emitter to the collector, which creates an accelerating field for the electrons. Therefore the base transit time is reduced and

f_T is increased [17].

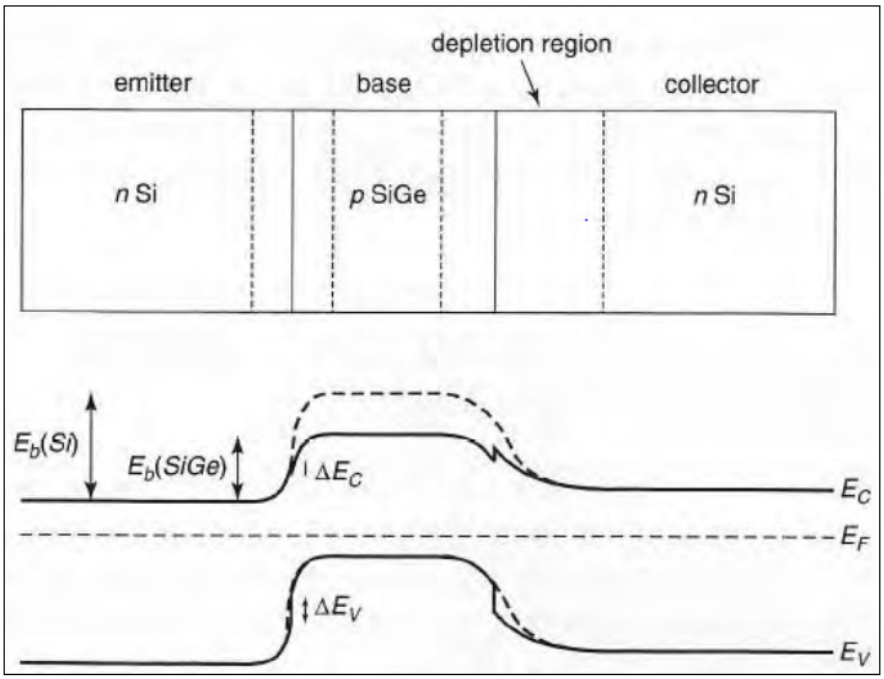


Figure 4. Band diagram of a SiGe HBT vs. a traditional Si BJT highlighting the narrowing of the bandgap energy in the base (5).

Figure A.1: Energy-band diagram of a SiGe HBT (solid line) with respect to a silicon BJT (dotted line).

A.1.2 pHEMT

Background

In order to satisfy the demands of high frequency applications, devices with high transit frequency f_T are needed. Transit frequencies of FETs can be improved by reducing the channel length, increasing the current I_{DS} and transconductance g_m, and increasing the saturation velocity of the FETs. These device parameters need to be optimised for a high-speed FET. But it is difficult to realise a high carrier concentration and a high saturation velocity at the same time in MESFETs. Increasing the dopant density reduces

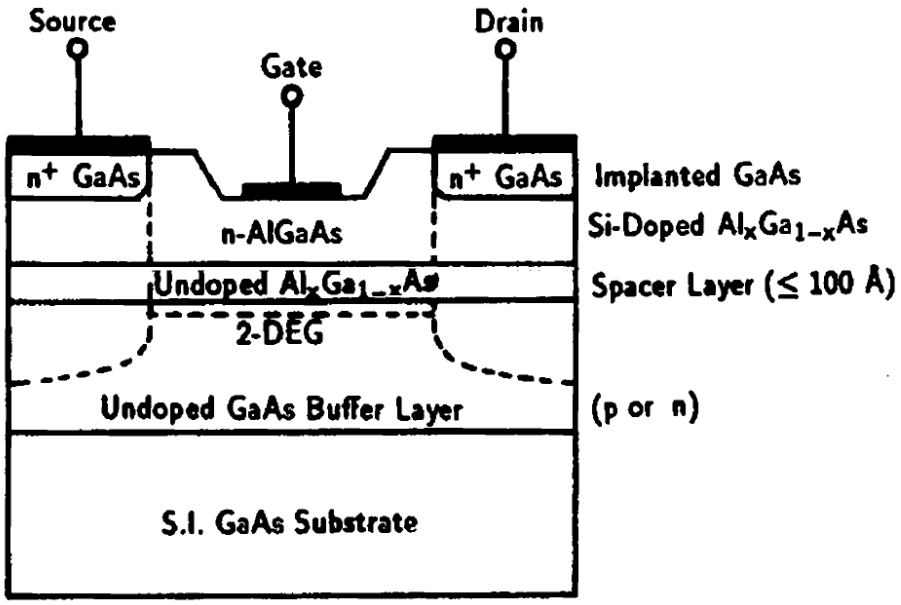


FIGURE A.2: Structure of a HEMT.

the saturation velocity as a result of ionised impurity scattering. To mitigate this problem, HEMTs were developed. Fig. A.2 shows the cross-section of an AlGaAs/GaAs HEMT. As shown in the figure, the HEMT structure is grown on a semi-insulating GaAs substrate. Layers of undoped GaAs buffer, undoped $Al_xGa_{1-x}As$ spacer and Si-doped n+ doped $Al_xGa_{1-x}As$ are grown on the semi-insulating GaAs substrate. A Schottky-barrier contact is formed at the metal gate and a doped $Al_xGa_{1-x}As$ interface between the source and the drain contacts. As the bandgap energy for $Al_xGa_{1-x}As$ is larger than for GaAs, the energy level of the conduction band (EC) of $Al_xGa_{1-x}As$ is higher than that of GaAs. Therefore the electrons flow from the EC of $Al_xGa_{1-x}As$ to the EC of GaAs by diffusion. These electrons are trapped at the heterointerface of AlGaAs/GaAs. A triangular potential well (quantum well) is formed on the undoped GaAs buffer layer. A two-dimensional electron gas (2-DEG) sheet charge is developed on the undoped GaAs layer at the AlGaAs/GaAs interface, which creates a conducting channel for the HEMT devices. The density of the 2-DEG sheet charge carriers is modulated by the applied gate voltage. Therefore, HEMTs are also known as MODFET (modulation doped FET), TEGFET (2-DEG FET), SDFET (selectively doped FET), identified with different device characteristics.

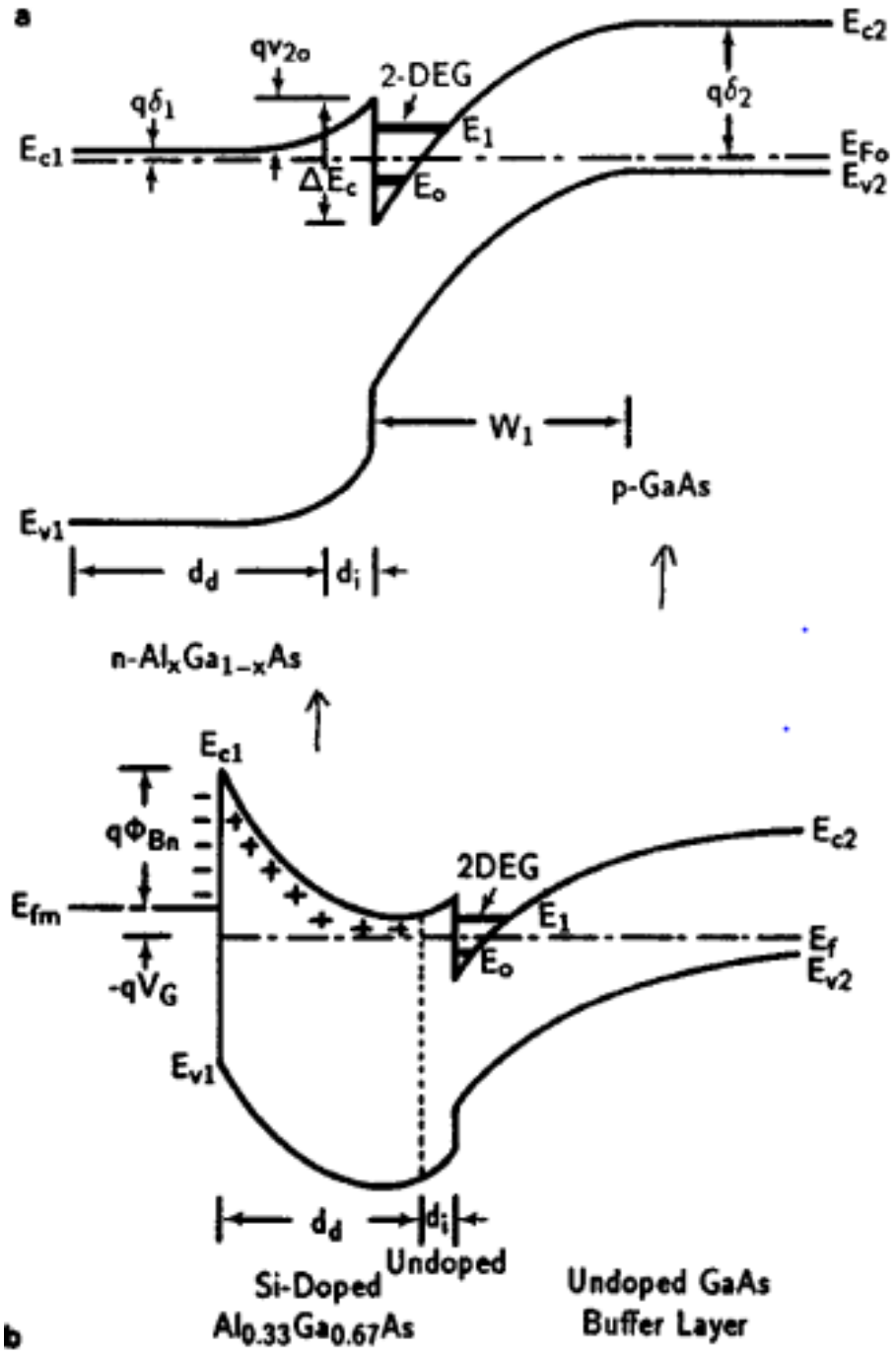


Figure A.3: Energy band diagram of a HEMT.

Doping profile

The channel conduction in the HEMT is primarily due to the 2-DEG sheet charge which is ensured by depleting the free electrons from the AlGaAs layer. The 2-DEG sheet charges in the quantum well do not experience ionised impurity scattering as they are spatially separated from the ionised donor impurities in the doped $Al_xGa_{1-x}As$ by an undoped $Al_xGa_{1-x}As$ spacer layer. This results in both high electron velocity and high electron mobility in the device channel and consequently to improved device performance compared to MESFETs. The gate length of HEMTs has been reduced over the years, which further improves the f_T and the low-noise performance of the device. Short-channel effects are observed for 0.1 μ gate length HEMTs. These undesirable short-channel effects are primarily due to the carrier injection into the undoped GaAs buffer layer under the channel. It causes a shift of the pinch-off voltage. Pseudomorphic HEMT structures are developed to overcome this problem in which AlGaAS/InGaAs/GaAs layers are grown by molecular-beam epitaxy (MBE). The InGaAs layer helps to confine the charge carriers in the potential well. Introduction of InGaAs into the HEMT structure creates large conduction-band discontinuities between the AlGaAs spacer and the GaAs layer, and improves the carrier transport in the InGaAs channel. Therefore pHEMTs offer high electron velocity and 2-DEG sheet charge density. The energy-band diagram of a pHEMT is shown in Fig. A.4.

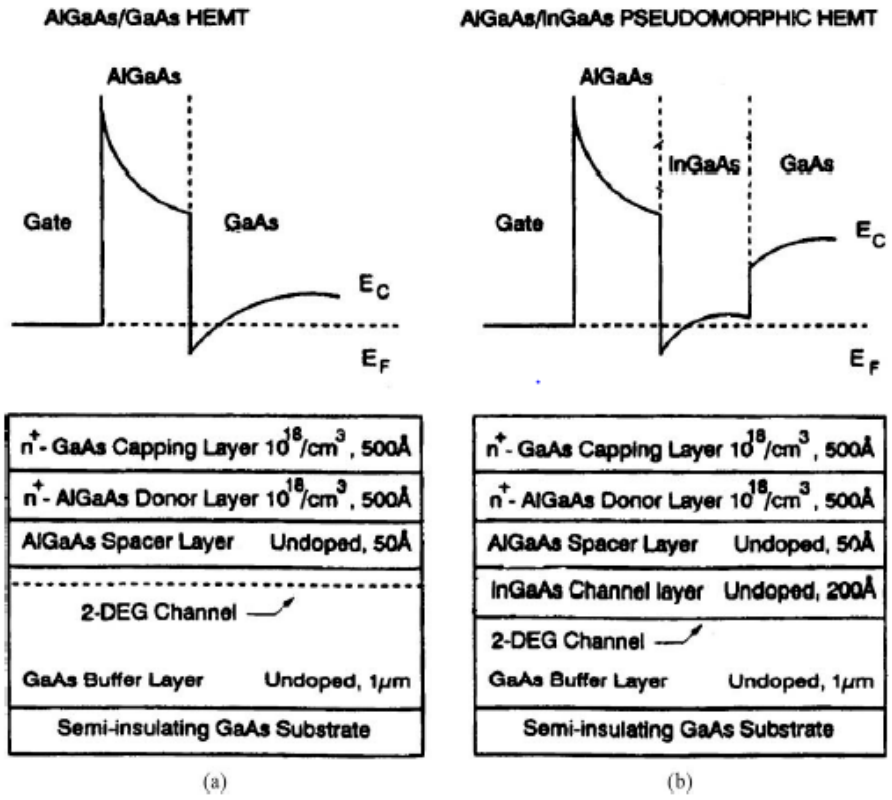


Figure A.4: Energy-band diagram of a PHEMT.

B

Appendix B

B.1 SG13S process specification

The IHP's SG13S is a high performance BiCMOS technology with 0.13 μm CMOS process. It supports two types of bipolar devices HS-HBT and HV-HBT. The f_T and f_{max} of the transistors are 250 GHz and 300 GHz respectively. This process provides 2 gate oxides: a thin gate oxide for the 1.2 V digital logic and a thick oxide for a 3.3 V supply voltage. The backend offline option offers a stack-up of 5 thin metal layers (from M1 to M5) and the two thick metal layers (TM1 and TM2). Passive components such as poly silicon resistors and MIM capacitors are available. The detailed cross-sectional view of the metal layers is not shown here due to the NDA with the foundry.

The maximum current densities in different metal layers are listed in the Table B.1.

TABLE B.1: Summary of the maximum current densities in the metal layers in the SG13S process

Parameters	**Unit**	**Max**
Metal1	mA/μm	1
Metal2	mA/μm	1
Metal3	mA/μm	1
Metal4	mA/μm	1
Metal5	mA/μm	1
TopMetal1	mA/μm	15
Topmetal2	mA/μm	16
Contact	mA/Cnt	16
Via1	mA/Via	0.2
Via2	mA/Via	0.2
Via3	mA/Via	0.2
Via4	mA/Via	0.2
TopVia1	mA/Via	1
TopVia2	mA/Via	15

The details of the bipolar transistor used for the frequency doubler design is presented in Table B.2.

TABLE B.2: Summary of the maximum current densities in the metal layers in the SG13S process

Parameters	**Unit**	**Min**	**Target**	**Max**	**Comment**
Current Gain	-	400	900	1500	A_E= 0.12×0.48 μm^2
Early Voltage	V	15	25	-	A_E= 0.12×0.48 μm^2
Breakdown Voltage Emitter-Collector	V	1.5	1.7	-	A_E= 0.12×0.48 μm^2
Breakdown Voltage Collector-Base	V	4	5	6.5	A_E= 0.12×0.48 μm^2
Breakdown Voltage Emitter-Base	V	1.3	1.8	-	A_E= 0.12×0.48 μm^2
Collector current	μA	1.2	1.7	2.2	A_E= 0.12×0.48 μm^2
Max. Transit Frequency	GHz	210	250	-	A_E= 4×(0.12×0.48 μm^2)
Max. Oscillation Frequency	GHz	260	300	-	A_E= 4×(0.12×0.48 μm^2)

B.2 PP10-10 process specification

The PP10-10 process is a 0.1 μm single recess pHEMT process designed for ultra high frequency power and low noise products operating upto 4 V. This process is an extension of WIN Semiconductor's highly successful PL15 technology platform with an optimised device structure. Apart from the excellent power performance, the noise figure performance is also competitive in comparison with other pHEMT technology such as mHEMT (data taken from Process specification). The maximum current densities in different metal layers are listed in the Table B.3. The performance target for pHEMTs, capacitors and resistors in this process are summarised in the Table B.4.

TABLE B.3: Summary of the maximum current densities in the metal layers in the PP10-10 process

Parameters	**Unit**	**Max**
Metal1	mA/μm	4
Metal2	mA/μm	6
Double metal	mA/μm	10

TABLE B.4: Summary of the maximum current densities in the metal layers in the PP10-10 process

Parameters	**Unit**	**Target specification**
Gate length	μm	0.1
Pinch-off voltage (I_D= 1mA/mm)	V	-0.95
I_{DSS} (V_g= 0 V, V_d= 1.5 V)	mA/mm	520
I_{Dmax} (V_g= 0.5 V, V_d= 1.5 V)	mA/mm	760
Maximum g_m (V_d= 1.5 V)	mS/mm	725
Breakdown V_{DG} (I_g= 1 mA/mm)	V	9.5
f_T (V_d= 1.5 V)	GHz	130
f_{max} (V_d= 1.5 V)	GHz	180
MIM capacitor	pF/mm	400
TFR resistor	Ohm/square	50
EPi resistor	Ohm/square	135

C

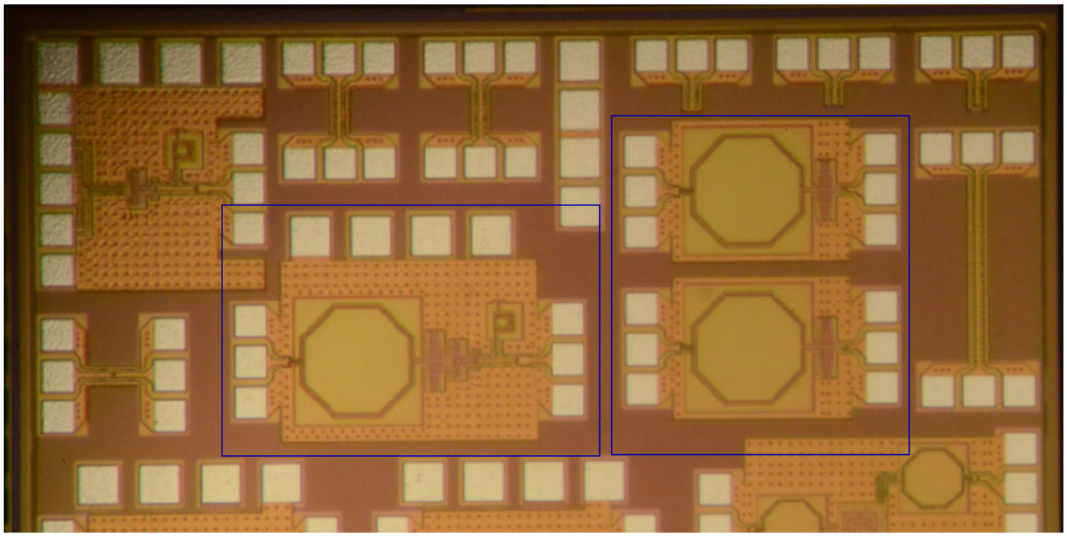
Appendix C

C.1 Fabricated circuits

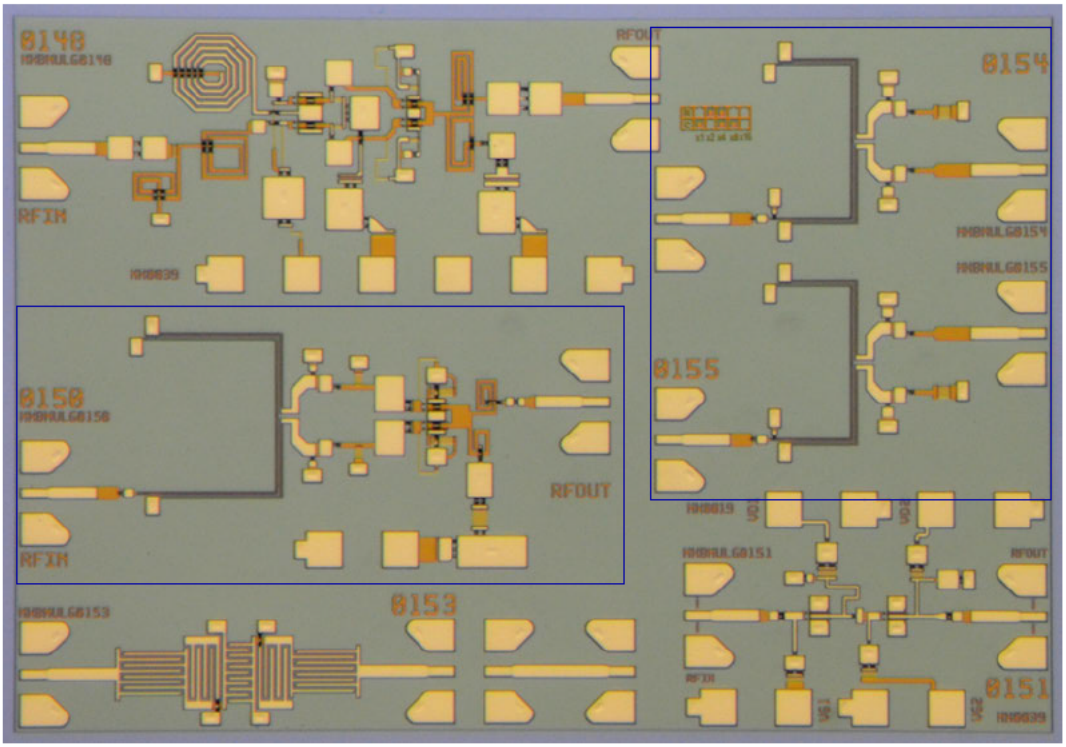
The frequency doubler and the transformer baluns implemented in the SG13S SiGe HBT process are manufactured by IHP through Europractice with the wafer identification number T323-0-S-a2.

The frequency doubler and the transformer baluns implemented in the PP10-10 GaAs pHEMT process are manufactured by WIN Semiconductors with the wafer identification number BP909.

The photographs of the fabricated wafers are shown in Fig. C.1(a) and Fig. C.1(b).



(a)



(b)

FIGURE C.1: Photographs of fabricated wafers (a)SG13S SiGe HBT process, (b) PP10-10 GaAs pHEMT process.

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