60 GHz Silicon Transmitters

by

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Abstract

The continual push for faster wireless systems in consumer devices is driven by the desire for higher performance media streaming, faster sync and better energy efficiency (lower energy per bit). The next generation of wireless links will be enabled by the wide unlicensed bandwidth available at mmWave frequencies and will provide multi-gigabit per second connections.

At the time the majority of the work in this thesis was done (2006-2010), there were no consumer wireless systems faster than a few hundred megabits per second. The work in this thesis aims to develop key components for a 60 GHz transmitter (TX) in Silicon as well as an architecture amenable to integration in a consumer device that can operate at a rate greater than 1 gigabit per second.

The first three chapters give an overview of Silicon technology for mmWave systems and cover theory for transmitters and phased arrays. Several optimisations for mmWave transmitters are shown in Chapter 4 including a method to calculate the optimal number of transmitters given a fixed power budget, why TX/RX switches are preferred and the asymmetry that can arise between devices in a mmWave ecosystem.

Chapter 5 presents a design flow for mmWave circuits that is based on careful modeling and the scaling of low frequency design techniques to mmWave. Two power amplifiers are shown. The first, a board level design at 1 GHz which won the high efficiency PA competition at 2007 IMS with an efficiency of 88%. The second is a 60 GHz SiGe transmission line based design which achieves a close match to simulation, wide bandwidth and is used in the single antenna transmitter presented in Chapter 7. The

outcomes from this work are a design flow for first time right power amplifiers (and mmWave circuits in general) as well as two PAs designed using this flow.

Chapter 6 builds on the mmWave PA design presented in Chapter 5. Two transformer coupled PAs are presented. The first a four stage design in SiGe that reduces the area required significantly compared to the transmission line design. A differential topology also enables higher output power by combining two out of phase signals into a single ended signal using an output balun. The second PA is designed in CMOS and achieved state of the art efficiency. It shows the benefit of neutralisation for transformer coupled designs and that the design methodology is equally valid in CMOS technology.

Chapter 7 ties the work from the previous chapters together and presents two transmitters for 60 GHz operation. The first transmitter is a single chip design with single antenna. The second design uses a novel architecture that enables the front-end to be placed at the end of a coaxial cable and allows for a scalable number of antennas. This architecture (co-invented with Leonard Hall) enables the optimal placement of 60 GHz antennas in devices.

Certificate of Originality

I certify that the work in this thesis entitled "60 GHz Silicon Transmitters" has not previously been submitted for a degree nor has it been submitted as part of requirements for a degree to any other university or institution other than Macquarie University.

I also certify that the thesis is an original piece of research and it has been written by me. Any help and assistance that I have received in my research work and the preparation of the thesis itself have been appropriately acknowledged.

In addition, I certify that all information sources and literature used are indicated in the thesis.

Michael J Boers

July 2014

Acknowledgements

The work in this thesis formed part of the GLIMMR project. I would like to extend a huge thank you to my advisor Professor Neil Weste and the other members of the radio team, especially Leonard Hall, James Howarth who I worked closely with on the Silicon designs. As a late arrival to the project, I was able to use the stable design environment and transmission line flow they created which saved countless hours debugging in an unfamiliar Sun environment. You taught me a lot.

It was great working with the other members of the GLIMMR team, especially Professor Cowley, Ian, Andre, Bala, Yingbo and Noorfazila who focused on other aspects of the system, thank you for all the stimulating conversations. I learnt a lot from you. Thanks also to my advisors at Macquarie University, Professor Anthony Parker, Professor Mike Heimlich and Associate Professor Linda Davis.

At Broadcom I was fortunate to continue working on 60 GHz radios, thank you to all the great engineers and management staff who supported and continue to support this work. It's really exciting being able to take this technology to market

Finally, thanks to my wife Jess and the rest of my family - I am fortunate to have won that lotto, you are an amazing bunch.

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Introduction

"A device called a transistor, which has several applications in radio where a vacuum tube ordinarily is employed, was demonstrated for the first time yesterday at Bell Telephone Laboratories..."

– New York Times, *1948*

1.1 Motivation

Since the demonstration of the first transistor in 1947 [1], integrated circuits (ICs) have ridden a wave of development and innovation unparalleled in our history. They power

the devices we use for entertainment, control our modes of operation, helped put man on the moon and enable us to talk with friends on the other side of the world.

Of all the IC technologies it is Silicon, primarily Complementary Metal Oxide Semiconductors (CMOS) with its generation to generation scaling (as observed by Moore [2]) which provides the platform for smaller, higher performance and lower cost circuits that enable these devices to get faster, smaller and cheaper each year. With this continual improvement comes a desire to push the boundaries and explore new applications at higher frequencies.

Until the 130nm CMOS and 180nm Silicon Germanium (SiGe) nodes, Silicon technology was limited to applications well below 60 GHz due to slow (relatively speaking) transistor speed. As each generation progresses past these nodes, millimetre wave (mmWave) circuits[1] that were once the domain of military applications [3] and point-to-point (PtP) links [4], and typically implemented using type III-V semiconductors such as Gallium Arsenide (GaAs) and Indium Phosphide (InP), are now able to be implemented in Silicon. Silicon implementations enable applications in mass-markets such as the personal computers (PCs) and cellphones due to the extremely low cost.

Table 1.1 shows a comparison of f_T and f_{max} for several SiGe and CMOS nodes [2].

The opening of 7 GHz contiguous bandwidth at 60 GHz and the performance of advanced CMOS [7] and SiGe [8] nodes pave a clear path to 60 GHz adoption for several applications.

[1] mmWave refers to frequencies from 30-300 GHz where the wavelength can be measured in millimeters (10-1mm)

[2] f_T and f_{max} are useful to understand the high frequency performance of a technology and will be discussed in more detail in Chapter 2.

Technology	f_T (GHz)	f_{max} (GHz)
Jazz SiGe 0.25µm	75	
Jazz SiGe 0.18µm	150	
Jazz SiGe 0.13µm	200	
ST SiGe 0.13µm	220	290
ST CMOS 65nm LP	175	325

Table 1.1: *Overview of Silicon processes [5, 6].*

The motivation for this thesis is the Silicon implementation of gigabit per second communication systems for both consumer wireless local area networks (WLANs) and low cost PtP links at 60 GHz. This thesis focuses on mmWave transmitters and a key transmitter component - the power amplifier.

1.2 Applications

Many of the devices we use today employ wireless technology. With each generation of new devices there is a desire for higher throughput to reduce download time, increase performance and provide bandwidth for new applications. WLANs were first implemented in the early 2000's. At inception they supported a few Mbps (11g) and have scaled to nearly 1 Gbps (11ac) today. The performance of 2.4 GHz and 5 GHz WLAN systems will continue to improve but due to the low available bandwidth, Multiple-Input and Multiple-Output (MIMO) systems that achieve a high spectral efficiency will be required for speeds greater than 1 Gbps. At some point, due to the much wider bandwidth at 60 GHz. mmWave systems will offer better efficiency (measured in energy per bit) for many high speed applications. mmWave systems will complement existing 2.4 GHz and 5 GHz WLAN transceivers in future devices.

60 GHz systems provide higher throughput at a much lower spectral efficiency than

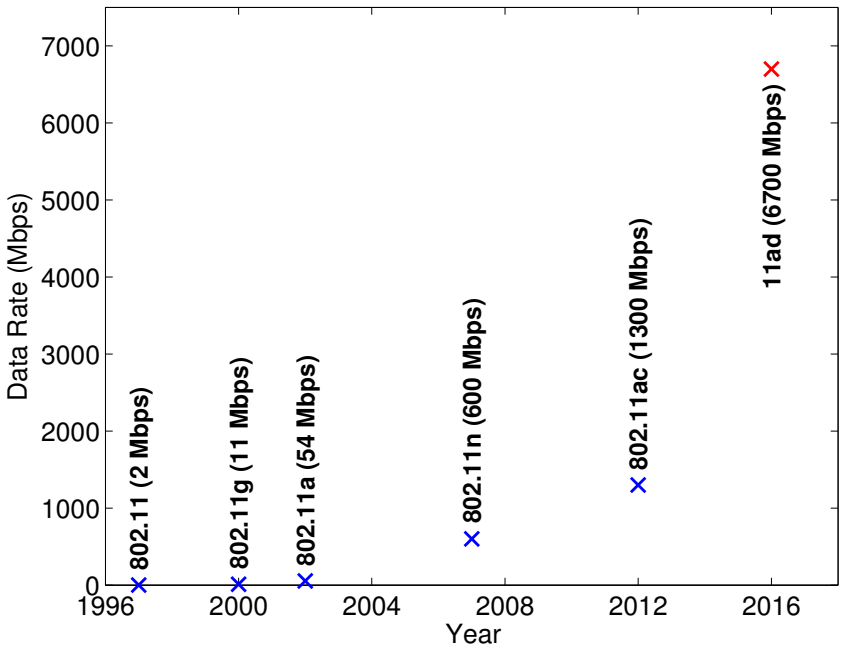


Figure 1.1: *The 802.11 wireless evolution 11g to 11ad. The y-axis shows the highest PHY rate specified in the standard.*

existing wireless systems. The 802.11ad specification provides for data rates up to 6.7 Gbps on 2 GHz wide channels [9]. There are several applications which can benefit from this high data rate, they are outlined in the following sections.

Wireless docking

60 GHz technology will enable wireless docking by providing a high bandwidth connection for video, connectivity to high speed internet and peripheral devices. Figure 1.2 shows a desktop environment with a 60 GHz wireless desktop bus. In this distributed mode, there is no central hub. In other implementations a central hub can be used with connectors to attach to the local area network, Universal Serial Bus (USB) and other devices.

Figure 1.2: *60 GHz for wireless docking [10].*

Multimedia streaming

Due to the high data rate, 60 GHz can be used for uncompressed or lightly compressed High Definition (HD) video streaming applications. Future mobile phones will enable full HD capture and a 60 GHz link would enable high speed transfer of the video to a television or live streaming. Video streaming also enables applications where a different screen to the device screen can be used. For example in an airplane, video could be streamed to a monitor in the back of the seat.

Figure 1.3: *60 GHz for wireless video streaming [11].*

Point-to-point links

PtP links are increasingly being used for wireless backhaul, and small-cell cellular applications. They can be installed alongside, or as a back-up for fibre links. Uses are envisaged in stadiums or other events like the Olympics where additional capacity is required over a short time period.

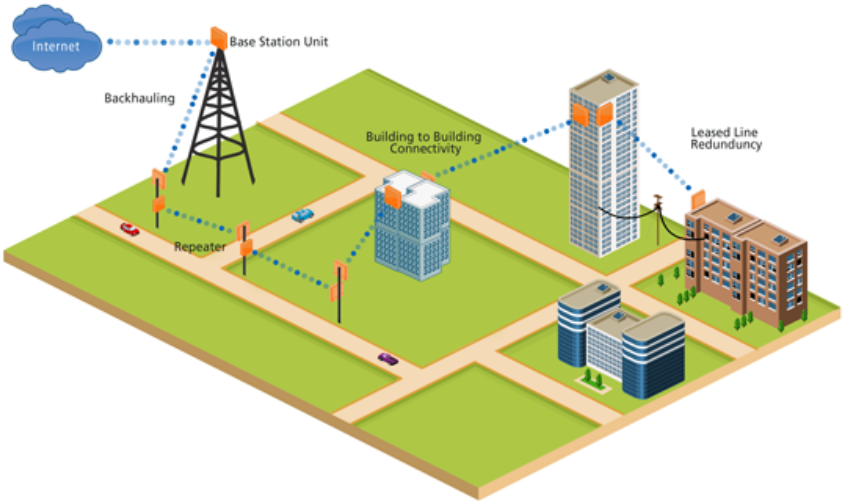


Figure 1.4: *60 GHz for wireless backhaul [12].*

1.3 Communication at 60 GHz

Up to 7 GHz contiguous bandwidth is available worldwide for license free communication at 60 GHz [3], a comparison of the unlicensed spectrum available at 60 GHz and other frequencies is shown in Figure 1.5. The capacity of a channel is a product of the bandwidth and the signal to noise ratio (SNR) [13]. Increasing the bandwidth enables high capacity at reasonable SNR levels as shown by Shannons capacity theorem.

[3]The exact allocation varies by country. In Australia 57-66GHz, US 57-64GHz, EU 57-66GHz and Japan 59-66GHz.

$$C = BW \times log_2(1 + SNR)b/s \tag{1.1}$$

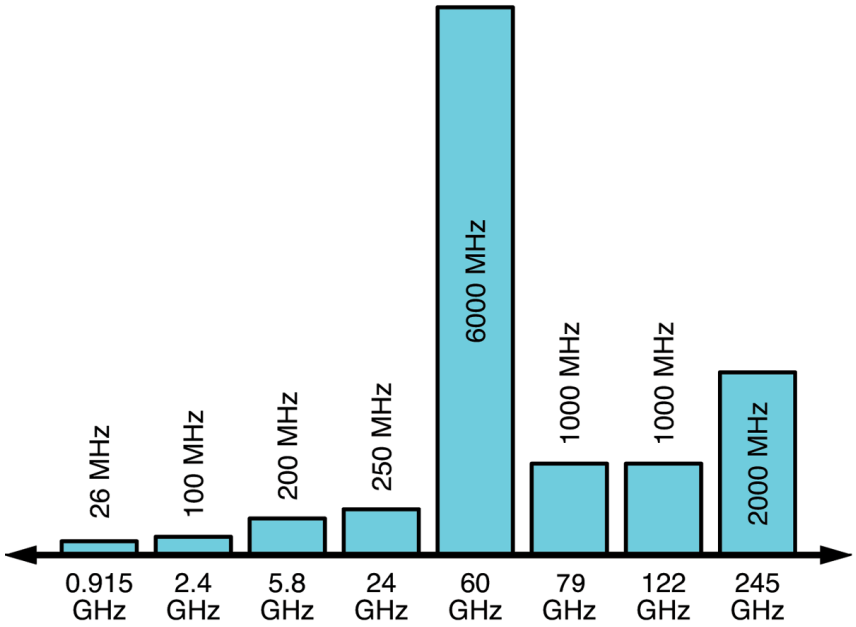


Figure 1.5: *Unlicensed channel bandwidths.*

The reason for the large allocation of bandwidth at 60 GHz is that it lies in one of the oxygen absorption bands. At sea level the attenuation due to oxygen is 15 dB/km [14] which is not a problem for in room operation or outside links up to a few hundred meters but restricts the use beyond that. Rain also has an effect on performance of 60 GHz outdoor PtP links. The free space path loss for a 60 GHz link and effects of Oxygen and rain are shown in Figure 1.6 and Table 1.2.

In addition 60 GHz is highly attenuated by common building materials [15, 16] (see Table 1.3). For indoor uses, this may limit the application to in room rather than whole house. When 60 GHz is looked at as a complementary technology to 2.4 and 5 GHz this high attenuation is not usually seen as a compromise, rather a feature as it enables higher spectral re-use.

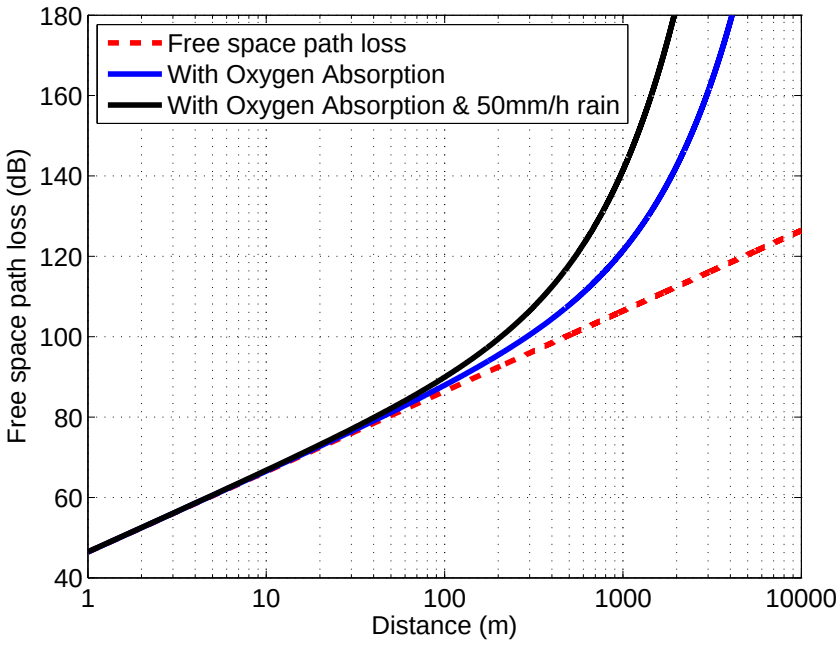


Figure 1.6: *Free space path loss at 60 GHz. The loss including Oxygen absorption and rain is also shown (Rain fall data from [14]).*

Rate (mm/h)	60 GHz Loss (dB/km)
0.25	0.2
1.25	0.8
5	3
25	10
50	20
100	30
150	40

Table 1.2: *Additional loss due to rainfall at 60 GHz [14].*

Material	Thickness (mm)	Loss (dB)
Drywall	25	6.0 +/- 3.4
Whiteboard	19	9.6 +/- 1.3
Clear glass	3	3.6 +/- 2.2
Mesh glass	3	10.2 +/- 2.1
Human	100	30 +/- 10

Table 1.3: *60 GHz propagation loss through objects [15, 16].*

1.4 GLIMMR

The GLIMMR (Gigabit low-cost integrated mmWave radio) project was a collaborative research effort started in 2005. It consisted of researchers from the University of South Australia, Adelaide University, Macquarie University and was led by NHEW R&D Pty Ltd (Neil Weste) in a linkage grant with the Australian Research Council.

The objective of the project was to design low-cost Silicon ICs and implement a system capable of >1 Gbps at 60 GHz. The project was supported by Cadence Design Systems, Jazz Semiconductor, Peregrine Semiconductor, Intel Corporation, and AWR Corporation.

The work in this thesis was carried out as part of the GLIMMR project and focused on the design of the transmitter for this system. Three SiGe tapeouts were undertaken; GLIMMR test-chip 1, 2 and 3 (GTC1, GTC2, GTC3) [4].

1.4.1 System Partition

The system was divided into separate blocks and split between researchers. James Howarth was responsible for the receiver design, Leonard Hall for a separate receiver, EM modeling and antenna design as well as overall project lead, Yingbo Zhu and Noorfazilla Kamal worked on the phase locked loop (PLL) and the author was responsible for the TX design. The work focused on in this thesis is highlighted in blue in Figure 1.7.

[4] Appendix C contains pictures of the three test-chips.

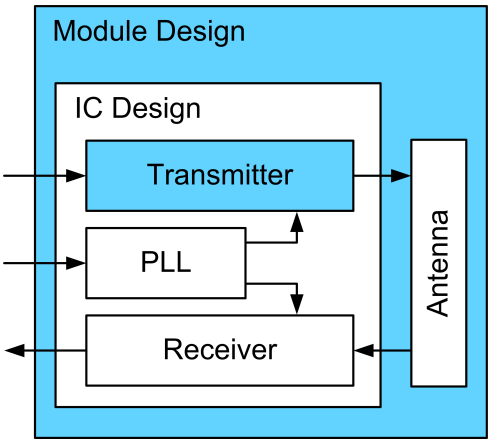


Figure 1.7: *System partition showing the focus for this work.*

1.5 Scope

The primary objective of this thesis is the design of 60 GHz transmitters in Silicon technology for next generation WLAN and PtP systems. The PA is a key component in wireless transmitters and forms a core part of the work done in this thesis.

The receiver, PLL and local oscillator generation (LOGEN) circuits along with the antenna are not shown in this thesis, they were worked on by others in the GLIMMR project.

The work in this thesis concentrates on the transmitter from the I/Q interface to the 60 GHz output.

1.6 Contributions

The work in this thesis was done over 6 years from 2005-2010, originally as a fulltime student at Macquarie University with the GLIMMR project and finally as an employee

with Broadcom. There is a time lag between some of the results presented in this thesis and when they were originally designed. Some parts of this thesis were published and these publications are outlined at the end of this section.

Chapter 4 outlines a 60 GHz system design. A link budget and specifications are built up for two transmitters in Sections 4.2, 4.3 and 4.4, this work was a collaborative effort by the GLIMMR team and was led by Neil Weste. Section 4.5 outlines several 60 GHz specific system level optimisations such as whether to use shared or seperate antenna arrays, the optimal number of antennas for a transmitter given a fixed power budget and the concept of asymmetric links in a 60 GHz ecosystem.

Chapter 5 opens with a review of PA fundamentals. A design methodology is presented in Section 5.3 for 60 GHz PAs (and mmWave circuits in general) which borrows techniques from low frequency RF design. This builds on earlier work done during the GLIMMR project, specifically the transmission line design and layout flow by James Howarth and Leonard Hall. A 1 GHz PA using a high speed GaN HEMT device which uses this design methodology is presented and resulted in first time right design of a high efficiency PA. Incidentally, this PA won the 2007 IMS student PA competition with the highest measured efficiency of 88%. The PA design layout and testing was done by the author, devices and device models from CREE were used. The fabrication was done by Macquarie University engineering services team. A second PA is presented, this time at 60 GHz. but using the same design methodology and transmission line matching approach. This PA was designed in 0.18 µm Jazz SiGe and the measured results closely match simulation validating the design methodology. The author was responsible for the design, layout and testing of the PA.

As the GLIMMR project progressed, there was a desire to reduce the size and power

consumption of the transmitter. Chapter 6 builds on the mmWave PA design presented in Chapter 5. Two transformer coupled PAs are shown. The first a four stage design in SiGe that reduces the area required significantly compared to the transmission line design. A differential topology also enables higher output power by combining two out of phase signals into a single ended signal using an output balun. The second PA is designed in CMOS and was presented at RFIC 2010. It achieved state of the art efficiency for a 60 GHz design. It shows the benefit of neutralisation for transformer coupled implementations and that the design methodology is equally valid in CMOS technology.

Chapter 7 outlines the design of two 60 GHz transmitters (I/Q analog input to 60 GHz output), both targeted at use in the GLIMMR system. The first transmitter (GTC2-TX) is a single antenna transmitter for short range applications. The author was responsible for the TX chain design including the I/Q up-convertor, RF mixer and PA. The author also designed the test printed circuit boards (PCBs) used for testing the chip. Leonard Hall worked on the characterization of transmission lines and provided EM support. He was also responsible for the bond-wire antennas used in this implementation.

The second transmitter outlined in Section 7.3 (GTC3-TX) uses a novel split sliding IF architecture. To the author's knowledge, this implementation (taped out in early 2009) was the first of its kind. The architecture was a joint invention of the author and Leonard Hall. The author was responsible for the architecture definition and the transmitter chain design including the I/Q modulator, RF mixer and PA. The author also designed the test boards used to characterize the transmitter. These boards include embedded chip to board wire-bond transition (modeled in HFSS) and 1.8mm coaxial connectors.

List of Publications

[17] - J. A. Howarth, A. P. Lauterbach, M. J. Boers, L. M. Davis, A. Parker, J. Harrison, J. Rathmell, M. Batty, W. Cowley, C. Burnet, L. Hall, D. Abbott, and N. Weste, *"60 GHz radios: Enabling next-generation wireless applications,"* in TENCON 2005 IEEE Region 10, pp. 16. - In this publication, the author was responsible for the PA design outlined in Section VIII-E. The design was done at Macquarie University and manufactured by Jazz Semiconductor.

[18] - M. Boers, A. Parker, and N. Weste, *"A GAN HEMT amplifier with 6W output power and >85% power-added efficiency [student designs],"* Microwave Magazine, IEEE,vol. 9, no. 2, pp. 106110, 2008. - In this publication, the author was responsible for the design, layout and testing of the amplifier. This publication was the result of winning the 2007 IMS high efficiency PA design competition. The design was done at Macquarie University and manufactured by Macquarie Engineering and Technical Service.

[19] - M. Boers, A. Parker, and N.Weste, *"A 60 GHz transmitter in* 0.18 µm *silicon germanium,"* in Wireless Broadband and Ultra Wideband Communications, 2007. AusWireless 2007. The 2nd International Conference on, pp. 3636. - In this publication, the author was responsible for the design of the SiGe transmitter. The design was done at Macquarie University and manufactured by Jazz Semiconductor.

[20] - M. Boers, *"A 60 GHz transformer coupled amplifier in 65nm digital CMOS,"* in Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE, pp. 343346. - In this publication, the author was responsible for the design of the PA. The PA was designed at Broadcom and manufactured by TSMC.

Related Publications

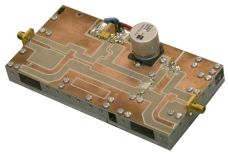
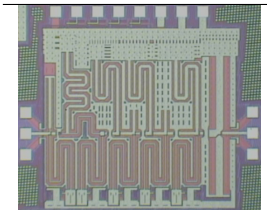
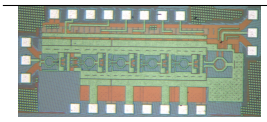
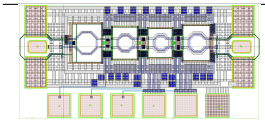
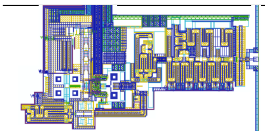
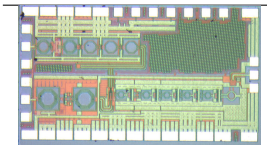
These are not specifically covered in this thesis but contain related work so are included here for completeness.

[21] - V. Bhagavatula, M. Boers, and J. Rudell, *"A transformer-feedback based wideband if amplifier and mixer for a heterodyne 60 GHz receiver in 40nm CMOS,"* in Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE, pp. 167170, 2012.

[22] - M. Boers, I. Vassiliou, S. Sarkar, S. Nicolson, E. Adabi, B. Afshar, B. Perumana, T. Chalvatzis, S. Kavadias, P. Sen, W. L. Chan, A. Yu, A. Parsa, M. Nariman, S. Yoon, A. Besoli, C. Kyriazidou, G. Zochios, N. Kocaman, A. Garg, H. Eber- hart, P. Yang, H. Xie, H. Kim, A. Tarighat, D. Garrett, A. Blanksby, M. K. Wong, D. Thirupathi, S. Mak, R. Srinivasan, A. Ibrahim, E. Sengul, V. Roussel, P.-C. Huang, T. Yeh, M. Mese, J. Castaneda, B. Ibrahim, T. Sowlati, M. Rofougaran, and A. Rofougaran *"A 60 GHz TX/RX 802.11ad transceiver with single coaxial cable and polarization diversity,"* in ISSCC 2014.

[23] - M. Boers, I. Vassiliou, S. Sarkar, S. Nicolson, E. Adabi, B. Afshar, B. Perumana, T. Chalvatzis, S. Kavadias, P. Sen, W. L. Chan, A. Yu, A. Parsa, M. Nariman, S. Yoon, A. Besoli, C. Kyriazidou, G. Zochios, J. Castaneda, B. Ibrahim, T. Sowlati, M. Rofougaran, and A. Rofougaran *"A 60 GHz TX/RX 802.11ad transceiver with single coaxial cable and polarization diversity,"* in Journal of Solid State Circuits Dec 2014.

List of Designs

	1 GHz high efficiency GAN HEMT board level PA. The PA uses a GAN HEMT device. The boards were manufactured by Macquarie Engineering and Technical Service.
	60 GHz 0.18 µm SiGe transmission line based PA, used in GTC2-TX. Manufactured by Jazz Semiconductor.
	60 GHz 0.18 µm SiGe transformer coupled PA, used in GTC3-TX. Manufactured by Jazz Semiconductor.
	60 GHz 65nm LP CMOS transformer coupled and neutralised PA. Manufactured by TSMC.
	60 GHz 0.18 µm SiGe 1 element transmitter - GTC2-TX.
	0.18 µm SiGe modular 60 GHz front-end transmitter for split IF single coaxial cable system - GTC3-TX.

1.7 Organisation

This chapter provides an introduction and motivation for the work in this thesis. The scope and contributions are also shown as well as a list of designs resulting from this thesis.

Chapter 2 reviews Silicon technology for mmWave applications. Both CMOS and SiGe

are investigated and key parameters, process information and performance are outlined. Passive devices are reviewed as well as an overview of packaging technologies for mmWave circuits.

Transmitters and phased arrays are introduced in Chapter 3. The fundamentals of radio transmitters are reviewed. Two transmitter architectures are analysed as well as several impairments. Phased arrays are important at 60 GHz due to the high free space path loss. Their application to 60 GHz systems is reviewed along with several key concepts.

Chapter 4 shows a 60 GHz link budget and outlines TX specifications for two transmitters. The first a single antenna system and the second a multi-element phased array. Some 60 GHz system level optimisations are also reviewed.

Chapter 5 demonstrates a design methodology for RF and mmWave design which results in the first time correct design of two PA's at 1 GHz and the other at 60 GHz.

Two transformer coupled PAs are shown in Chapter 6, transformer coupled PAs have several advantages over transmission line designs such as lower area and the ability to combine the differential output using a BALUN.

Chapter 7 highlights the design and measurement results for two SiGe 60 GHz transmitters. The first transmitter is a simple I/Q analog input to 60 GHz RF output integrated on a single chip. The second transmitter is a dual chip architecture which is designed to enable simple placement in a consumer device.

A conclusion and recommendation for future work is outlined in Chapter 8.

2

Silicon Technology

2.1 Overview

Historically mmWave systems have been implemented as hybrids, using type III-V compound semiconductors like GaAs. Over the last decade research into Silicon based technologies for mmWave communication [24, 25, 26, 19, 27] has ramped up. SiGe and CMOS technology have both reached nodes which provide high performance at mmWave frequencies and enable the integration of full transceivers. This chapter gives an overview of Silicon technology for mmWave applications.

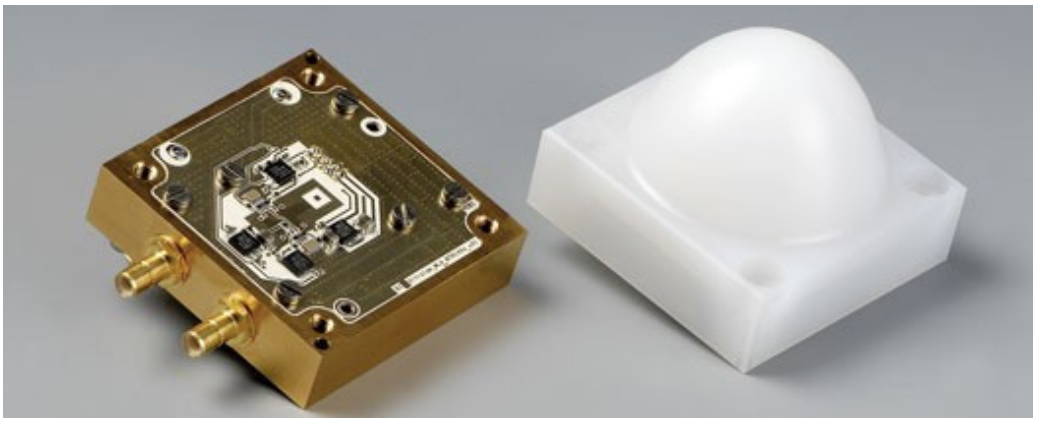


Figure 2.1: *A mmWave GaAs hybrid [28].*

Why Silicon?

Silicon is the second most abundant element in the earth's crust (27.7%) after oxygen (46%) and is the most common metalloid [29]. It is found in the environment combined with oxygen, predominantly silica (quartz) and other silicates (clay, feldspar, granite, asbestos). These silicon bearing compounds make up over 75% of the earth's crust [30]. The abundance of Silicon along with a host of favourable properties [31] have contributed to its dominance as a semiconductor over the last 50 years.

CMOS field-effect transistor (FET) technology and SiGe heterojunction bipolar transistor (HBT) technology are two processes which use a Silicon wafer as a substrate. In order to reach mass market with a reasonable cost, transceivers must be implemented in Silicon. The remainder of this section looks at CMOS and SiGe in detail and outlines key performance trends related to mmWave.

2.2 Choosing A Technology

CMOS and SiGe are both contenders for low-cost mmWave transceivers. This chapter reviews the cost, performance, reliability and other integration concerns for both technologies.

Of the Silicon based semiconductor processes, CMOS is by far the most popular making up 95% of globally produced integrated circuits [32]. The popularity of CMOS stems from the ease at which it can be manufactured, the high level of integration it achieves and the generation-to-generation scaling trend which has to date, followed Moore's law [2].

CMOS is a cost efficient process that was originally developed for digital systems, if an RF designer had a choice based purely on performance, CMOS FETs would most likely not be used. It is only when the economics are looked at that it becomes much more attractive, the key now is designing a system using a lower performing RF process which meets the application requirements.

CMOS is implemented on a silicon substrate and FETs are used as the active devices. Increased performance in FETs (higher f_T, f_{max} and lower NF_{min}) occurs primarily due to the lateral scaling of the devices each generation [33]. With better lithography smaller gate lengths can be implemented which reduces the gate transit time (electrons have less distance to travel), in addition, reduced dimensions also reduce the parasitic capacitances in the intrinsic device.

FETs are majority carrier devices where drift current (the result of an applied electric field) between the drain and source is dependent on the voltage at the gate terminal.

SiGe is a type-IV compound semiconductor. SiGe HBT technology is effectively a hetero-junction bipolar process implemented using a strained silicon-germanium epitaxy layer for the base of the transistor. The HBT NPN structure consists of a Si-N to SiGe-P junction emitter-base and a SiGe-P to Si-N base-collector junction [31]. The introduction of Germanium into the base of the HBT improves the performance of the device as it has a smaller band-gap than Silicon, improves the carrier transport parameters and can be graded to accelerate the carriers through the base [31].

SiGe offers several advantages over CMOS, it has lower 1/f noise, higher output resistance and higher voltage handling capacity than the equivalent (in speed) CMOS process [6] but it does not provide as high digital integration, achieve as low power consumption or cost as CMOS.

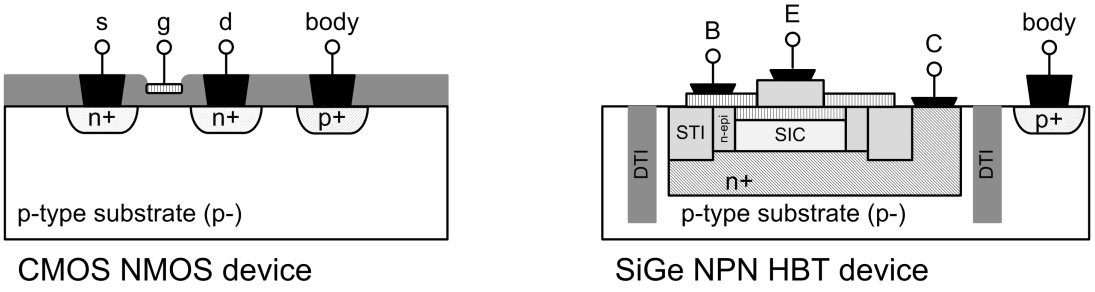


Figure 2.2: *Cross section of NMOS (left) and NPN HBT (right) [34].*

2.2.1 Material Properties

There are several material properties which define performance limits for mmWave devices [35, 34].

- Electron mobility (SiGe >Si)
- Hole mobility (SiGe >Si)

- Saturation velocity (Si ≈ SiGe)
- Thermal conductivity (Si >SiGe)[1]

2.2.2 Cost

The cost of manufacturing an integrated circuit can be broken down into the fixed costs (e.g. mask cost), and the per unit cost of the materials and manufacturing process to make the wafer.

At large volumes the cost of manufacturing Silicon is extremely cheap and can be anywhere from 50c to 5c per mm^2. The mask cost depends on the technology (minimum feature size) as well as the number of masks that are required.

Table 2.1 shows a rough price for SiGe and CMOS.

Technology	**Cost of Mask Set** (\$)	**Cost** (\$/mm^2)
SiGe 180nm	100,000	30
SiGe 130nm	200,000	30
CMOS 65nm	400,000	15
CMOS 40nm	800,000	15

Table 2.1: *Example pricing for SiGe and CMOS technologies.*

2.2.3 Performance

If we compare CMOS and SiGe technologies that have a similar f_T, we can observe that they match in speed at approximately 2 generations apart, 0.18 µm SiGe is equivalent to 90nm GP CMOS and 0.13 µm SiGe is equivalent to 65nm GP CMOS.

[1] this is not really a concern given the tiny amount of Germanium used in SiGe devices

The device f_T and f_{max} are both useful measures of a device performance [34, 36]. f_T is the frequency at which the current gain ($H21$) of the device is equal to one. f_{max} is the frequency at which the maximum available gain (assumes ideal input and output match) (G_{max}) is equal to one.

For mmWave designs, f_{max} is usually a better measure as it takes into account additional parasitic elements which impact the performance of the device.

CMOS

A FET with parasitics is shown in Figure 2.3. The intrinsic device sets the maximum speed and performance characteristics and the parasitics of the device reduce this. Some of the parasitics have more of an impact on performance than others. The equations below show that for high f_{max} the gate resistance R_g and gate-to-source C_{gs} capacitance need to be reduced as well as R_d and R_s.

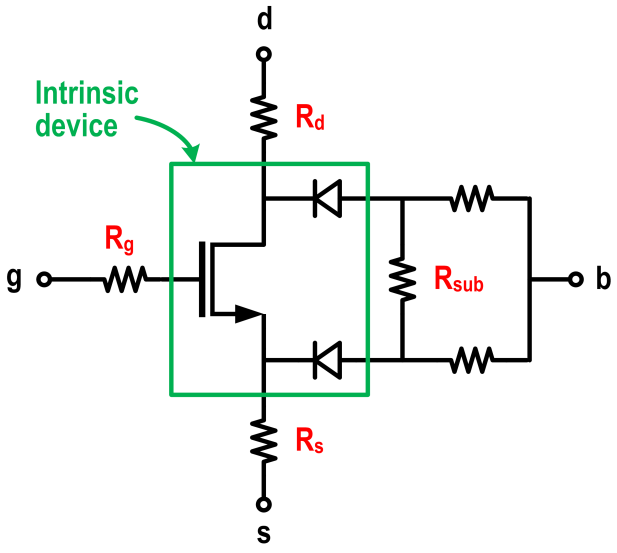


Figure 2.3: *CMOS device f_T and f_{max} shown below [37, 38].*

$$f_T = \frac{g_m}{2\pi\left[C_{gs} + C_{gd}\left(1 + gmR_s\right)\right]} \tag{2.1}$$

$$f_{max} = \frac{f_T}{2\sqrt{R_g\left(g_m C_{gd}/C_{gg}\right) + \left(R_g + r_{ch} + R_s\right)g_{ds}}} \tag{2.2}$$

SiGe

The f_{max} of a SiGe device is also affected by parasitics however they usually have less of an impact due to the much higher current density per area of transistor for HBTs resulting in less fingers and smaller metal to metal parasitics in the layout of a device. The backend in SiGe processes also has higher lateral and vertical spacing resulting in less parasitics. Care still needs to be taken to reduce the base resistance R_b as well as the base to collector capacitance C_{bc} as they have the largest impact on high frequency performance.

Equation 2.3 shows the f_T and Equation 2.4 shows the f_{max} of a SiGe HBT [38, 34].

$$f_T = \frac{1}{2\pi\left[\frac{nKT}{qI_c}\left(C_{be} + C_{bc}\right) + \left(R_E + R_C\right)C_{be} + \tau_b + \tau_c\right]} \tag{2.3}$$

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_b C_{bc}}} \tag{2.4}$$

Summary

Both SiGe and CMOS achieve high f_T and f_{max}. SiGe is less affected by layout parasitics than CMOS due to the higher current density per transistor and the larger spacing between metals. The table below shows the speed for some advanced SiGe and CMOS nodes.

Technology	f_t **(GHz)**	f_{max} **(GHz)**
Jazz SiGe 0.25 µm	75	
Jazz SiGe 0.18 µm	150	
Jazz SiGe 0.13 µm	200	
ST SiGe 0.13 µm	220	290
ST CMOS 65 nm LP	175	325

Table 2.2: *Overview of Silicon processes [5, 6].*

2.2.4 Noise

Noise in active devices can be separated into broadband noise such as thermal noise and shot noise and low frequency noise such as $1/f$ (or flicker) noise.

The thermal noise generated in a resistor is given by [39]:

$$\overline{e_n{}^2} = 4kTR\Delta f \tag{2.5}$$

All the terminal resistances in FETs and HBTs generate thermal noise.

Shot noise occurs when a current flows across a potential barrier such as the band-gap present at the PN-junction interface. It is the randomness of carrier transitions across

the interface which generates this noise. Like thermal noise, shot noise is white in nature [39].

The shot noise can be described by [39]:

$$\overline{i_n^2} = 2qI_{DC}\Delta f \tag{2.6}$$

In HBT's both base and collector junctions contribute to shot noise. As the base current is multiplied by the transistor gain, it dominates. In FETs, only the leakage across the gate junction generates shot noise but this is at a very low level due to the small current.

Flicker noise has a $1/f$ power density spectrum and the exact physical origins are not completely understood [34]. $1/f$ noise is higher in CMOS devices and while being low frequency in nature is up-converted around the fundamental frequency in VCOs.

NF_{min} is a useful figure of merit (FOM) which can be used to compare the noise of two technologies, NF_{min} is the minimum possible noise figure obtainable at the specified operating condition. NF_{min} is never practically achieved due to tradeoffs in the noise / gain match as well as losses associated with any matching networks.

CMOS

The NF_{min} for a CMOS device is given by [37]:

$$NF_{min} = 1 + 2\frac{f}{f_T}\sqrt{\frac{\overline{i_{dn}^2}}{4kT}\left(R_g + R_s + \frac{\overline{i_{dn}^2}}{4kTg_m^2}\right)} \tag{2.7}$$

SiGe

The NF_{min} for a SiGe device is given by [34]:

$$NF_{min} = 1 + \frac{n_F}{\beta} + \frac{f}{f_T}\sqrt{\frac{2I_C}{V_T}(r_E + R_b)\left(1 + \frac{{f_T}^2}{\beta f^2} + \frac{{n_F}^2{f_T}^2}{\beta f^2}\right)} \tag{2.8}$$

2.2.5 Reliability

The mechanisms for device degradation and breakdown are different in CMOS and SiGe due to the different structure of the active devices.

CMOS - Time Dependent Dielectric Breakdown

Time dependent dielectric breakdown (TDDB) is the breakdown of the insulating gate oxide in the CMOS device leading to a conduction path between the gate and the device substrate. Without this insulating layer the device no longer operates as a FET where current flow is dependent on the electric field [40].

Even though the gate dielectric is a good insulator, a small current still flows. The mechanism for this current flow is often attributed to Fowler-Nordheim tunnelling [41]. TDDB can be characterised by the total charge required to breakdown Q_{BD} which can be defined as [41]:

$$Q_{BD} = \int_0^{T_{BD}} I(t)dt \tag{2.9}$$

Foundries provide safe operating levels which will reduce the impact of TDDB, by following these rules the impact of TDDB can be mitigated.

CMOS - Hot Carrier Injection

Hot carrier injection (HCI) is the injection of a carrier (electron or hole) from the channel to the gate dielectric which generates an interface state [42]. HCI occurs in short channel devices under high electric fields (i.e. high V_{DS}). HCI affects the performance of the device, in particular it can cause an increase in the threshold voltage [43] which over time will reach a level that will not allow current to flow in the channel rendering the device un-fit for operation. HCI is not a sudden breakdown process, rather a degradation in the performance of the transistor over time.

HCI is the biggest concern for minimum feature size CMOS devices in mmWave circuits.

SiGe - Avalanche Breakdown

Avalanche breakdown is the primary concern for reliability in SiGe devices. This breakdown occurs at high base-collector voltages where the electric field in the junction exceeds the breakdown field of the device [34]. This type of breakdown is characterised by a sudden increase in collector current.

Operating below the BV_{ceo} of the device will ensure Avalanche Breakdown does not occur.

Summary

SiGe devices can handle much larger voltage swings than CMOS devices and do not degrade slowly over time as is the case with HCI effects in CMOS transistors. For high power applications that operate constantly across a long period of time, higher efficiency can be achieved in a SiGe process.

2.2.6 Digital Integration

For a complete transceiver, the integration of data converters and digital processing also needs to be considered. High performance ADC's have been shown in both SiGe and CMOS technologies [44, 45, 46, 47], there does not seem to be a clear advantage to using SiGe, it may offer slightly better matching due to V_{be} versus V_t matching (In SiGe V_{be} matching is controlled by doping profiles which is getting better with each generation and in CMOS V_t is controlled by the doping as well as the device dimensions which are decreasing each generation), however, with power on calibration, this point is moot.

The power of DAC's is typically dominated by the output stage. Neither technology offers a clear advantage for the output driver but CMOS is superior for the digital driver circuitry in the DAC.

CMOS provides superior digital integration and performance so is the clear choice if a single chip is required. In the case of split-chip architectures SiGe can be considered for the front-end IC.

2.2.7 Conclusion

There is no clear winner. For high volume applications CMOS will always be the economic choice. For low to medium volumes, SiGe is a contender, especially for demanding performance specifications which would benefit from a larger signal swing such as voltage controlled oscillator (VCO) phase noise or transceiver linearity.

If an SoC is required, CMOS will provide better performance and lower power for the digital portion of the design.

2.3 Passive Devices

Passive devices are extremely important in RF circuit design. They can be used to couple adjoining stages, provide a load and path for direct current (DC) to flow, they are used in impedance matching circuits in order to maximise the power transfer between circuits.

2.3.1 Capacitors

Capacitors are used to AC couple a signal, effectively blocking DC at the expense of a reduction in bandwidth. They can be used as resonant elements, tuning a circuit's impedance or resonating with an inductor in the tank of a VCO. They can also be used to decouple a local power supply from the rest of a system or provide a local reservoir of energy in an inductive power supply. There are several capacitor types depending on process availability; metal-insulator-metal (MIM), metal-to-metal (MTM) and MOS

capacitors. MIM capacitors require one or more additional process steps in the fabrication process adding extra cost. MTM capacitors are implemented using only the metal that is available in the process.

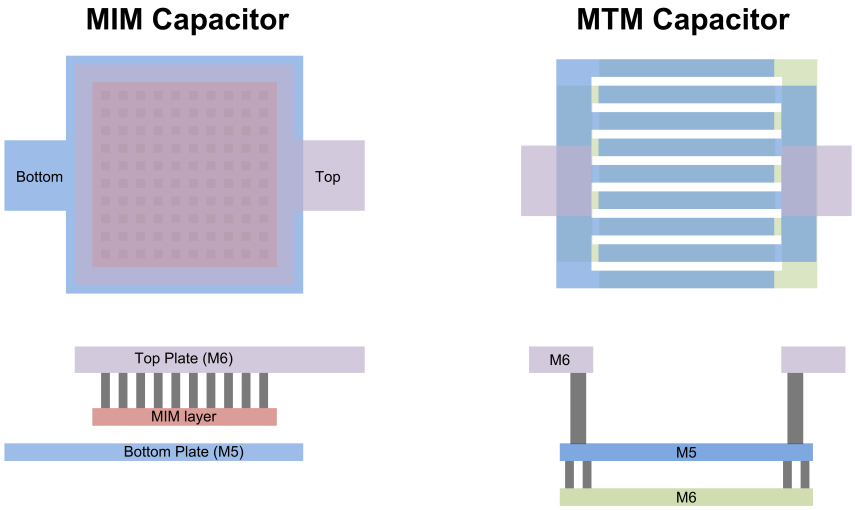


Figure 2.4: *MIM and MTM capacitors in a Silicon technology.*

MIM capacitors

MIM capacitors are implemented as parallel plate capacitors and typically use one of the standard metal layers in the process as one of the parallel plates [48, 49]. An insulator is deposited between this plate and an additional plate that is spaced above or below but much closer than the next standard metal layer.

MIM capacitors provide a high quality factor (Q). The insulator is designed to have a low loss tangent and high dielectric constant in order to increase the capacitance per square. Capacitance values on the order of 1-2 fF/μm^2 can be easily achieved. Capacitance to the substrate is usually an order of magnitude less than that of equivalent MTM capacitors. Due to their layout, mainly square or rectangular, MIM capacitors exhibit low lead inductance and perform well into mmWave frequencies.

Using MIM capacitors requires an additional mask and processing steps which increases the cost. Most CMOS processes do not use MIM capacitors for this reason and high capacitances are available at advanced nodes due to the small metal to metal spacing.

MTM capacitors (inter-digital / finger / comb)

MTM capacitors are created with the standard metal available in the Silicon process. They are typically used in sub 90nm CMOS processes where minimum geometry sizes allow the implementation of MIM comparable capacitors without the need for any additional process steps [50]. As MTM capacitors rely on the capacitance between metal, (sidewall, plate-to-plate or both), the capacitance is limited by the minimum space allowed by DRC rules as well as the dielectric constant. In 65nm, 40nm and below, low-k dielectric constant materials (~3.0) are used in the lower metal stack in order to reduce coupling between traces. While this has the desired effect of reducing capacitance between routing, it also reduces the achievable capacitance.

MOS capacitors

In both CMOS and SiGe processes, MOS capacitors are available. MOS capacitors use the capacitance between the gate and drain plus source nodes. By biasing the device in different regions, the capacitance can be varied. MOS caps are useful as varactors in VCOs, or as decoupling capacitors combined with metal caps to increase the capacitance density per unit.

2.3.2 Inductors

Inductors can be created from the metal layers in Silicon processes. They have been studied from 30-100GHz in [51]. They can be used as part of matching networks, to tune out parasitic capacitances in RF switches and to supply bias currents. Inductors can be implemented as short sections of transmission line, as a line inductor or as single / multiple turn structure. Modelling is important in order to capture the self-resonant frequency.

In single-ended designs, correct modelling of the ground return path is extremely important as it can impact the tuning and stability of the devices.

For the transformers and inductors used in the designs in this thesis, a solid ground loop is simulated as part of the passive device structure. This has two benefits. Firstly, the ground return path is clearly modelled by being included in the EM simulation, secondly, circuitry outside of this area does not have a large impact on the performance of the passive device. [2]

2.3.3 Transformers

Transformers are useful passive components for RF design. They have more degrees of freedom than inductor or capacitor and provide an extremely compact way to provide inter-stage coupling and matching between two stages of a differential circuit. They can also be used to couple stages in a mixer providing DC separation between the switching ang g_m stages. Transformers are used extensively in the power amplifier

[2] but we still need to be careful about coupling to nearby magnetic devices

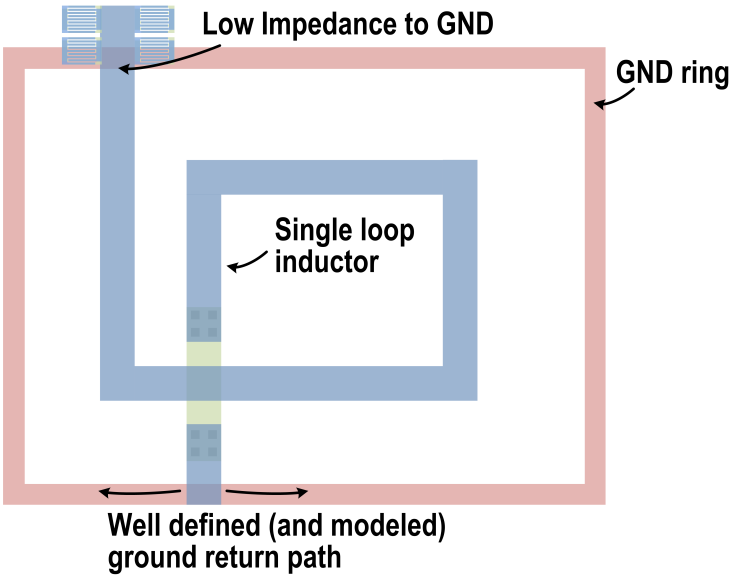


Figure 2.5: *Inductor showing main loop, ground ring and decoupling capacitors.*

designs in Chapter 4.

Due to the magnetic coupling between coils, a transformer forms a higher order network than two separate inductors. This can be seen by the T model equivalent for the transformer shown in Figure 2.6 [38].

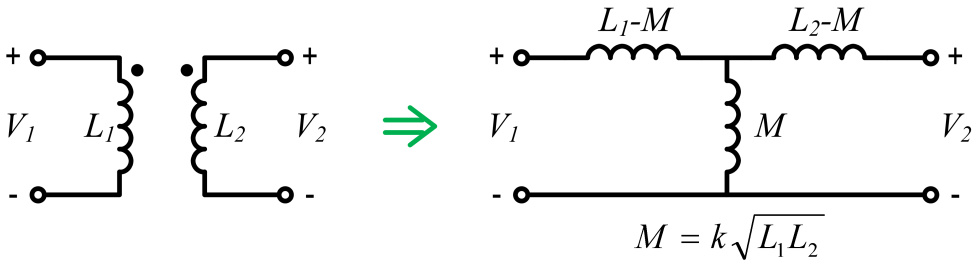


Figure 2.6: *T model for a transformer [38].*

G_{max} is a useful figure of merit for a transformer - it shows the minimum loss possible due to losses in the transformer itself (resistive loss in the metal, loss due to coupling into the substrate). The G_{max} can be described as a function of the coil Q and coupling factor k [38].

$$G_{max}(Q,k) = 1 + \frac{2}{Q^2k^2} - 2\sqrt{\frac{1}{Q^4k^4} + \frac{1}{Q^2k^2}} \tag{2.10}$$

2.3.4 Transmission lines

Transmission lines are required at frequencies where the routing distance is in the order of a fraction of a wavelength ($\lambda/15$), this applies for 60 GHz on chip where the wavelength in free space is 5mm and routing on chip can be multiple millimetres.

Transmission lines for the GLIMMR project were simulated in HFSS and implemented in Cadence by Leonard Hall and James Howarth. A library of single ended and differential lines was created with several characteristic impedances from 30ohms to 90ohms.

While transmission lines can be used for matching in mmWave circuits, they are much larger than inductors and transformers and result in an area penalty compared to other approaches (as shown in Chapter 4).

2.3.5 Metal stack comparison

There are different metal stacks available within a technology and between different technologies. The type (usually Aluminium or Copper) of the metal, the number of layers, thickness and height above the substrate all impact the performance of passive devices such as capacitors, inductors, transmission lines and transformers.

Several figure of merit's (FOMs) can be used to compare the metal stack for a given

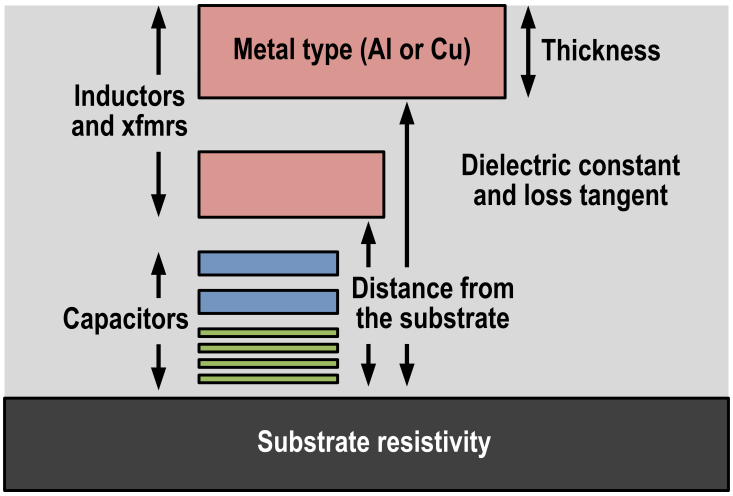


Figure 2.7: *The left shows the metals used for different passive devices. The right highlights some of the main metal stack parameters which impact performance.*

process. Transmission line loss in dB/mm depends on the metal, spacing, loss tangent and dielectric constant of the process. It is also implementation dependent - in some processes microstrip lines may perform better than coplanar waveguide (CPW) lines for example.

An example of the different performance of CPW transmission lines in Copper and Aluminium backend is shown in the table below. This data was simulated in AWR microwave office.

Metal	Thickness (um)	Loss (dB/mm)
Aluminium	1	1.9
Copper	2	1.3

Table 2.3: *Table showing loss in dB/mm for two different CPW implementations.*

Transformer G_{max} is a good measure of the loss through a transformer. This is mainly dependent on the geometry, metal type and loss of the substrate. Capacitors and inductors can be judged based on their Q factor and self resonant frequency.

Processes with thick copper metals and higher spacing between the top layer metals

and the Silicon substrate give better performance.

2.4 Packaging At 60 GHz

Packaging is an important step for mmWave circuits, the key consideration is reducing the loss from the PA output (or LNA input) to the antennas, as well as providing a stable substrate for the device, low warp, temperature, moisture.

Wirebond and bumped die are two different methods which can be used.

2.4.1 Wirebond Package

In a wirebond package, pads are placed around the edge of the chip and the connection to package, board or module is done using fine pieces of wire, typically Gold or Aluminium. A wirebond transition is shown in Figure 2.8. Wirebonding suffers from higher variability due to manufacturing tolerances [52], this is especially a problem for 60 GHz signals. It usually has higher losses than other methods as well.

2.4.2 Bumped Die

In a bumped die, solder balls (as small as 75 µm in diameter) are used to connect a die to package, module or board. This is shown in the following Figure 2.9. The manufacturing tolerances for bumped dies are much smaller than wire-bonding due to the consistent size of the solder bump, the self alignment due to surface tension of the solder bumps [53] and the small size relative to 60 GHz wavelength.

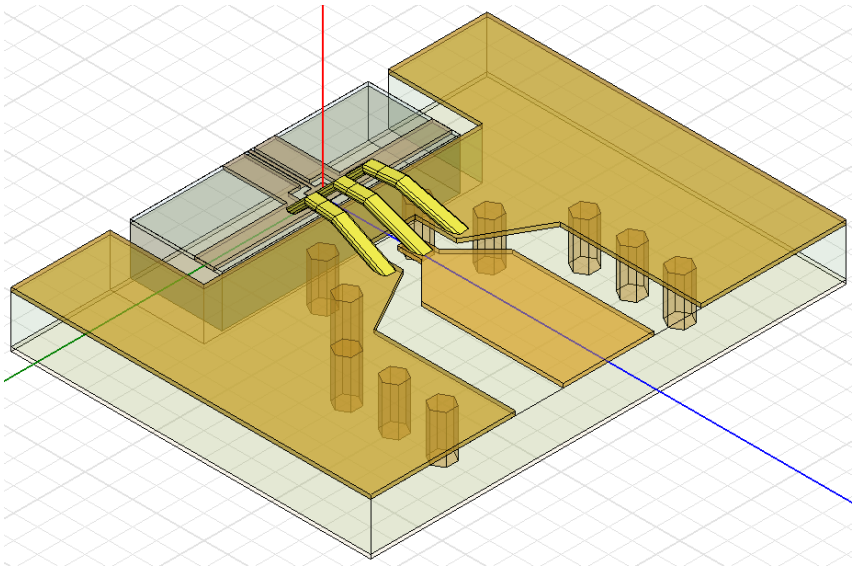


Figure 2.8: *High frequency bond-wire transition.*

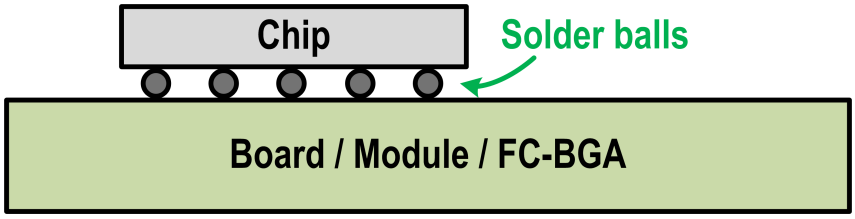


Figure 2.9: *Solder balls from chip to board, module or FC-BGA package.*

2.5 Summary

This chapter gave an overview of two Silicon technologies SiGe and CMOS. Material properties, cost, performance, noise and reliability for both technologies was reviewed. For equivalent nodes, SiGe is the performance winner due to higher voltage handling capability and faster devices. CMOS is useful if cost and power consumption are the most important factors.

Passive devices including capacitors, transmission lines, inductors and transformers were described and an overview of a typical Silicon metal stack was given.

Packaging is an important part of 60 GHz development. Two different packaging methods (flip-chip and wire-bond) were outlined. Flip-chip is preferrable for mmWave designs due to the smaller transition and better manufacturing tolerances. If wire-bonding is required, GSG transitions with ribbon cable can be used.

3

Transmitters and Phased Arrays

"... in the microwave area, structures included in the definition of integrated electronics will become increasingly important. The successful realization of such items as phased-array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar."

– Gordon Moore, *1965*

3.1 Introduction

RF systems are responsible for the conversion between a baseband signal and a signal modulated around a carrier. There are many different types of RF systems, this thesis is focused on transmitters for mmWave applications.

Phased array systems use multiple antennas to achieve higher performance over a single antenna system. At mmWave frequencies phased arrays provide an efficient way to help close the link budget, and unlike lower frequencies are easily implementable due to the small wavelength.

This chapter starts with a comparison of 5 GHz and 60 GHz communication links and reviews the fundamentals of transmitters and phased arrays for mmWave applications.

3.2 A comparison of 60 GHz and 5 GHz systems

WLAN links at 2.4 and 5 GHz are probably one of the most pervasive communication technologies in the world today, they are used in the home, office and to connect the internet of things. There are several key differences between operation at 60 GHz and 5 GHz and these are outlined below:

1. The channel capacity of a 60 GHz system is higher due to a wider available bandwidth. At 5 GHz, up to 160 MHz wide channels are used versus 2 GHz wide channels at 60 GHz [9, 54]. In terms of capacity, this results in an 2000/160 = 12.5 improvement in speed for the same SNR. Alternatively, the same speed can be achieved with reduced SNR at 60 GHz.

2. At 60 GHz. the free space path loss for an additive white gaussian noise (AWGN) channel is higher by $20 \times \log_{10}(\frac{60}{5}) = 21.5dB$ resulting in a 12× reduction in range.[1]

3. Due to a smaller wavelength (5mm at 60 GHz vs. 60mm at 5 GHz), more antennas can fit in a given area.

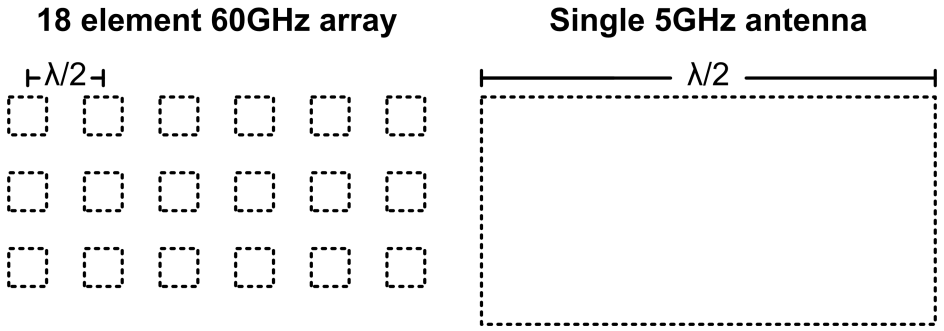


Figure 3.1: *Simple comparison of size between 60 GHz and 5 GHz antennas*

To achieve the increased capacity offered by the wide bandwidth of a 60 GHz implementation some of the losses associated with reduced wavelength need to be overcome. This is possible by using multiple elements in a phased array. Figure 3.1 shows 18 elements at 60 GHz in the same area as a simple 5 GHz antenna.

In addition to increasing the 60 GHz link budget, high gain antennas provide:

- The ability to steer away from sources of interference.

- More efficient use of the spatial channel (multiple links can operate on the same channel at the same time).

[1]The loss is even higher due to oxygen absorption of 60 GHz of 15dB/km but this of little consequence for short-range links. [17]

The remainder of this chapter gives an overview of transmitters and phased arrays and quantifies some of the concepts introduced here. It is not exhaustive, for more details the reader is referred to [55, 56].

3.3 Transmitters

3.3.1 Architectures

Radio transmitters are responsible for the up-conversion of a baseband signal to RF. For amplitude and phase modulated systems two architectures are commonly used: direct conversion and dual conversion (with a sliding or fixed IF).

Direct Conversion Transmitter

A direct conversion transmitter is shown in Figure 3.2. In direct conversion transmitters the baseband signal is directly up-converted around the local oscillator (LO) frequency using a single quadrature mixing stage. The direct conversion architecture is relatively simple and takes up less area than an equivalent super-heterodyne implementation, however it's often more difficult to meet performance with this architecture in practice.

One challenge with direct conversion transmitters is the generation of the quadrature LO directly at the RF carrier, this is especially difficult for 802.11ad systems due to the high channel frequencies (58-63 GHz). The generation of a quadrature LO at 60 GHz can be high power and also have high mismatch. A second common concern in

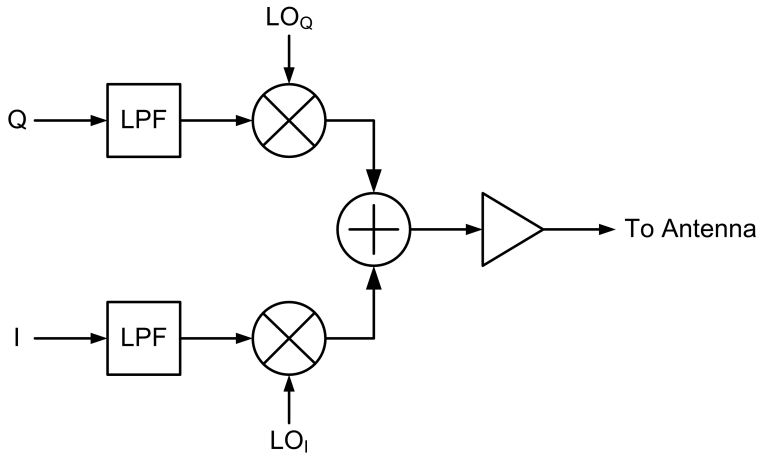


Figure 3.2: *Direct-conversion transmitter.*

high power, low frequency direct conversion transmitters is LO pulling. LO pulling occurs when the power amplifier couples into a fundamental frequency VCO or the LO generation circuit (through the circuit itself or the power supply) and modulates the transmitted signal with the transmitted waveform. This results in a degradation of output error vector magnitude (EVM) due to corruption of the LO signal. The concern of LO pulling at 60 GHz is reduced since the output power is low and losses in the coupling paths are high at 60 GHz.

Several direct conversion transseivers have been demonstrated at 60 GHz [57, 58]. In [57] a CMOS direct conversion transmitter is shown which uses quadrature oscillators to help ease the burden of LO generation at 60 GHz.

Figure 3.3 shows the up-conversion of a complex baseband signal to RF in a direct conversion transmitter. The up-converted signal contains an in-band image which can be seen as the reversed signal on top of the RF signal.

Figure 3.3: *Up-conversion in a direct conversion transmitter. The complex (I/Q) signal at baseband (BB) is up-converted directly to RF using an LO at the centre of the RF channel.*

Dual Conversion Transmitter

Figure 3.4 shows a simple dual conversion transmitter. In this architecture the baseband signal is first up-converted to an IF frequency then a second stage of mixing up-converts the IF to RF. The first mixer uses quadrature conversion to reject the image. An image is present after the second up conversion stage however this is usually architected so that it is far enough away from the RF that a simple filter (or the inherent filtering in the TX) attenuates it to a desired level.

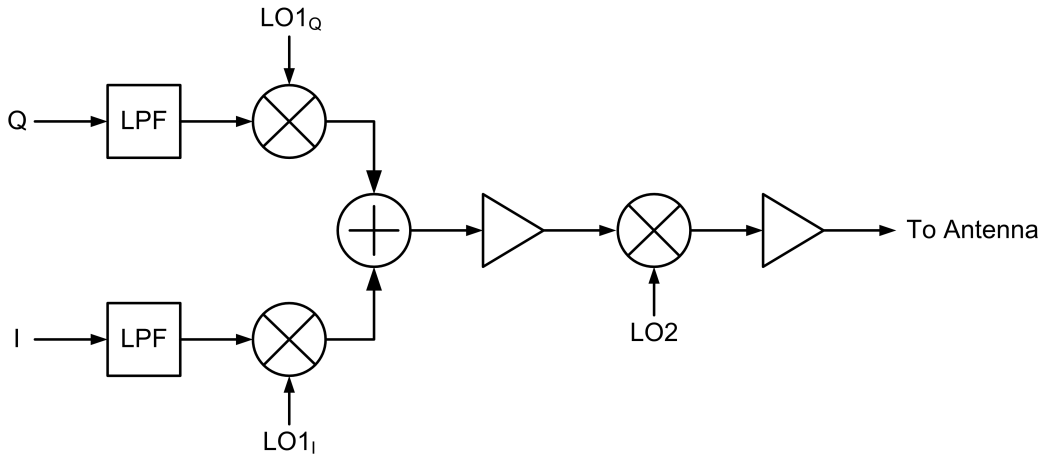


Figure 3.4: *Dual conversion transmitter.*

Dual conversion transmitters reduce the frequency required for quadrature LO and enables gain to be spread between more stages (this is more beneficial for the RX than

TX). In a spilt chip architecture, super heterodyne enables the front-end to be implemented on a separate chip to the IF radio.

There are different types of dual conversion systems and can be classified based on how the IF is implemented.

Sliding IF

In a sliding IF architecture, LO1 (IF mixer quadrature LO) and LO2 (RF mixer single phase LO) are related to each other and can be generated from the same PLL. An example of a sliding-IF is the architecture used in GTC2 (see the next chapter). In this architecture a 12 GHz LO1 and 48GHz LO2 are used. When the RF channel changes, both of the LO's move together.

Fixed IF (Super Heterodyne)

In a fixed IF architecture, LO1 is fixed and LO2 changes to move between channels. This places the lowest requirement on bandwidth for the IF path, it enables a fixed IF band-pass filter to be used for DAC image rejection in a Nyquist DAC system rather than baseband filters. It comes at the expense of VCO tuning requirement for the LO2 PLL.

Sliding IF (Fixed LO2)

In a sliding IF (fixed LO2) system, the IF to RF conversion LO (LO2) is fixed and LO1 (and the IF frequency) move to switch between channels. This architecture reduces the burden on the PLL used to generate the higher LO resulting in better phase noise

performance although it is rarely used as there is a large bandwidth requirement on the IF signal path. It needs to shift by the full RF channel spacing. At 60 GHz. this corresponds to a 6 GHz shift or 8 GHz bandwidth requirement.

Several dual-conversion transceivers at 60 GHz have been presented [59, 60]. In [59] present a super-heterodyne receiver which uses a 29 GHz VCO multiplied by 2 to get 58 GHz LO for the initial down conversion stage. The IF is 2 GHz. The low IF would make it challenging to filter the TX image if the same frequency plan is used for a transmitter. In [60] a super-heterodyne architecture with 7 - 13 GHz IF is used.

IF Frequency

The choice of frequency in a dual-conversion transmitter is an important consideration. We can refer to the two frequencies as the 'IF (intermediate frequency) LO' and the 'Second LO (local oscillator)' as shown in Figure 3.5. The IF LO is a quadrature signal which up converts the baseband signal to the IF band. The image of the baseband signal is rejected at this stage through the quadrature mixers and needs to be as it falls right on top of the IF frequency.

The IF LO should be high enough in frequency so that the second image that is created when the IF signal is mixed with the second LO is far enough away that it can be filtered by the RF front-end without requiring a second image rejection stage (along with a qudrature LO).

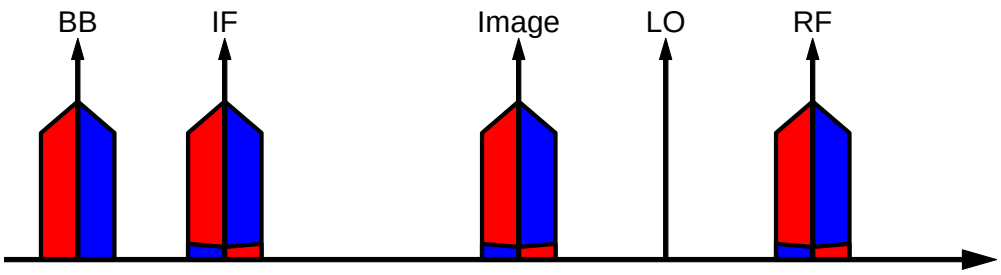


Figure 3.5: *Up-conversion in a dual conversion transmitter. The complex (I/Q) signal at baseband (BB) is first up-converted to an IF and then converted to RF using an offset LO.*

3.3.2 Error Vector Magnitude

The error vector magnitude (EVM) is a good measure of performance for a digitally modulated system [39]. In an ideal system transmitted and received constellation points would be the same. In a real system, noise, linearity and other imperfections move these constellation points. EVM is a measure of how far the constellation points are shifted from the ideal location. This is shown in Figure 3.6 the ideal constellation point is P_{ref} and the actual point is offset by P_{err}.

Equation 3.1 shows how EVM is calculated in dB and equation 3.1 shows the EVM calculation in percent.

$$EVM(dB) = 10 \times log_{10}\left(\frac{P_{error}}{P_{reference}}\right) \tag{3.1}$$

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{reference}}} \times 100\% \tag{3.2}$$

Transmit EVM is the EVM measured at the output of the transmitter after up-conversion

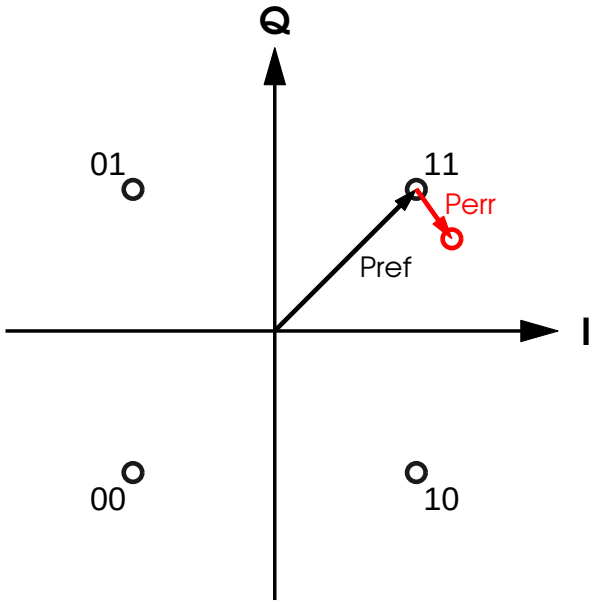


Figure 3.6: *A QPSK constellation with error vector shown in red.*

and amplification. Standards such as 802.11 [9, 54] specify the EVM requirement for the transmitter. EVM requirements for each single carrier modulation and coding set (MCS) in 802.11ad are shown in Table 3.1. While there are several contributors to EVM in a transmitter, to get the highest efficiency, the PA should dominate.

MCS Index	Modulation	Coding rate	EVM value (dB)
1	$\theta/2$-BPSK	1/2 with repetition	-6
2	$\theta/2$-BPSK	1/2	-7
3	$\theta/2$-BPSK	5/8	-9
4	$\theta/2$-BPSK	3/4	-10
5	$\theta/2$-BPSK	13/16	-12
6	$\theta/2$-QPSK	1/2	-11
7	$\theta/2$-QPSK	5/8	-12
8	$\theta/2$-QPSK	3/4	-13
9	$\theta/2$-QPSK	13/16	-15
10	$\theta/2$-16QAM	1/2	-19
11	$\theta/2$-16QAM	5/8	-20
12	$\theta/2$-16QAM	3/4	-21

Table 3.1: *Single carrier EVM requirements for 802.11ad [9].*

The worst-case (often pessimistic) transmit chain EVM can be approximated as the root mean square (RMS) sum of individual contributors, where it is assumed that each contributor is uncorrelated and adds as squares. Equation 3.3 shows this calculation, and the conversion to % is shown in equation 3.4.

$$EVM_{tx} = \frac{1}{\sqrt{\frac{1}{EVM_a^2} + \frac{1}{EVM_b^2} + \dots}} \tag{3.3}$$

$$EVM_{\%} = 10^{EVM_{dB}/10} \tag{3.4}$$

In 802.11ad EVM is calculated for SC transmitters using the following:

$$EVM = 10log_{10}\left(\sqrt{\left(\frac{1}{N_S P_{avg}} \sum_{i=1}^{N_S} \left[(I_i - I_i^*)^2 + (Q_i - Q_i^*)^2\right]\right)}\right) \tag{3.5}$$

where:

N_S = Number of symbols

P_{avg} = Average power per symbol

$I_i - I_i^*$ = Error in in-phase component

$Q_i - Q_i^*$ = Error in quadrature component

3.3.3 Impairments

In the previous section we discussed EVM as a good measure of transmitter performance degradation. In this chapter, we will discuss several impairments which impact the performance and therefore have an effect on the transmitted EVM.

I/Q Phase and Amplitude Imbalance

I/Q phase and amplitude imbalance in the baseband and LO paths affect the suppression of the side-carrier (image) [61]. In a quadrature up-convertor the image is mirrored around the LO and falls on top of the wanted signal. There are two types of imbalance, fixed and frequency selective. Frequency selective phase imbalance is another form of degradation in transmitters [62], this type of degradation is more challenging to correct in the digital domain. Fixed phase and amplitude mismatch are easily correctable in the digital baseband of the transmitter as they only need a single phase and amplitude correction factor.

The effect of phase and amplitude imbalance is visualized in Figures 3.7 and 3.8.

Figure 3.7 is generated using the following equation [63]:

$$y_{phase} = exp\left[j \times \left(-0.5 \times \pi \times \frac{I_P}{180}\right)\right] x_r + exp\left[j \times \left(\frac{\pi}{2} + 0.5 \times \pi \times \frac{I_P}{180}\right)\right] x_i \qquad (3.6)$$

Figure 3.8 is generated using the following equation [63]:

$$y_{amplitude} = 10^{\left(0.5\times\frac{I_A}{20}\right)} \times x_r + j\left[10^{\left(0.5\times\frac{I_A}{20}\right)}\right] \times x_i \tag{3.7}$$

where:

I_P, I_A = Phase imbalance (degrees), amplitude imbalance (dB)

x_r, x_i = real part of x, imaginary part of x

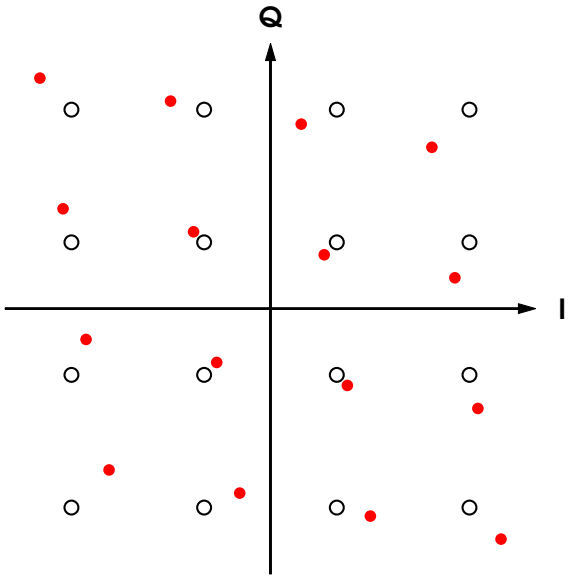


Figure 3.7: *16-QAM constellation with 20 degrees phase imbalance in I/Q paths.*

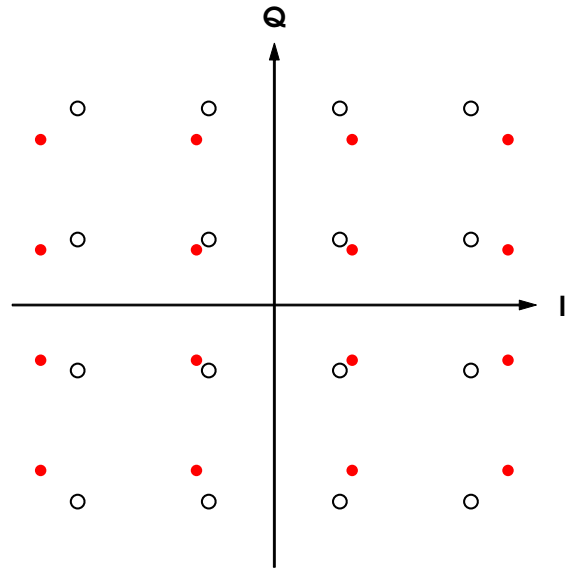


Figure 3.8: *16-QAM constellation with 3dB amplitude imbalance in I/Q paths.*

Phase imbalance is usually generated in the LO path from mismatch or variation in a polyphase filter, hybrid or quadrature divider. Amplitude variations in a hard switching LO do not have as large an impact as variations in gain in the analog baseband or DAC output amplitude mismatch. Sideband suppression (SBS) is a function of these phase and amplitude imbalances and is given by the following formula. Figure 3.9

shows the amplitude versus phase imbalance curves for different sideband suppression targets.

Equation 3.8 is used to generate the sideband suppression plot.

$$SBS(dBc) = 10 \times log_{10}\left(\frac{G^2 - 2Gcos\phi + 1}{G^2 + 2Gcos\phi + 1}\right) \tag{3.8}$$

where:

G = Amplitude imbalance

ϕ = Phase imbalance

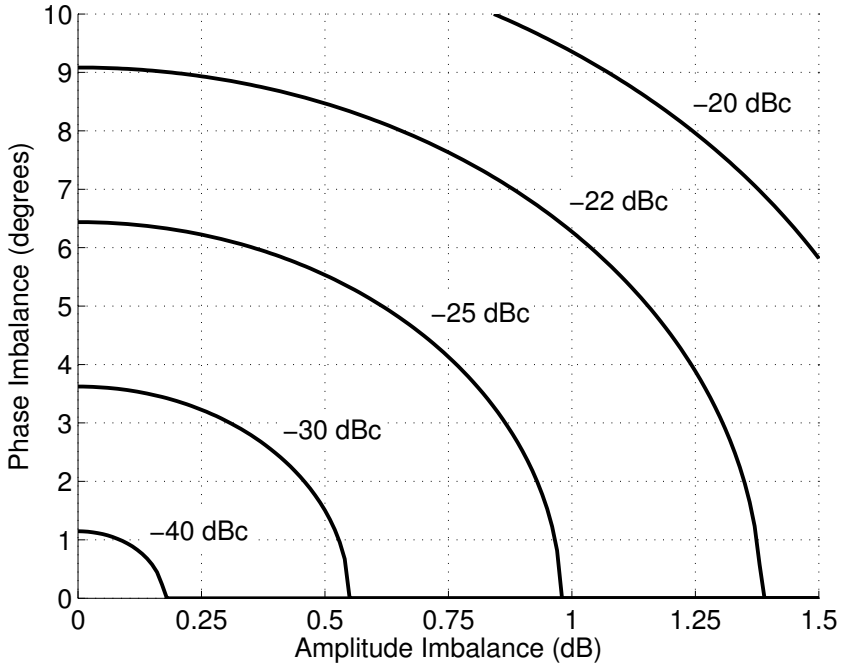


Figure 3.9: *Amplitude (dB) and phase (degree) imbalance curves for different sideband suppression (dBc) levels.*

The EVM contribution from IQ mismatch is equal to the sideband supression [64], this is shown with the following equations:

$$EVM_{IQmm}(dB) = SBS(dBc) \tag{3.9}$$

$$EVM_{IQmm}(\%) = 10^{\frac{SBS(dBc)}{10}} \tag{3.10}$$

DC Offset

DC offset between the I and Q paths shifts the constellation directly in the I or Q direction by the amount of the offset. DC offset is one of the primary contributors to local oscillator feedthrough (LOFT).

The 802.11ad standard requires less than -23dBc LOFT. The amplitude of the baseband signal directly impacts the DC offset requirements. Since LOFT is the ratio of average signal swing to DC offset, higher swing increases the tolerance to DC offset at the expense of transmitter power for increased linearity [65].

The following formula shows the maximum DC offset V_{max_DC} for a desired LOFT $LOFT(dBc)$ and baseband amplitude V_{rms}.

$$V_{max\_DC} = \frac{V_{rms}}{20log10(\frac{LOFT(dBc)}{10})} \tag{3.11}$$

To achieve better than -30dBc LOFT with a baseband signal swing of 600mV, the al-

lowable baseband offset is 22.mV as show in the following equation.

$$\frac{0.6/2\sqrt{2}}{20log10(\frac{30}{10})} = 22.2mV \tag{3.12}$$

Figure 3.10 shows the impact of DC offset on the transmitted constellation.

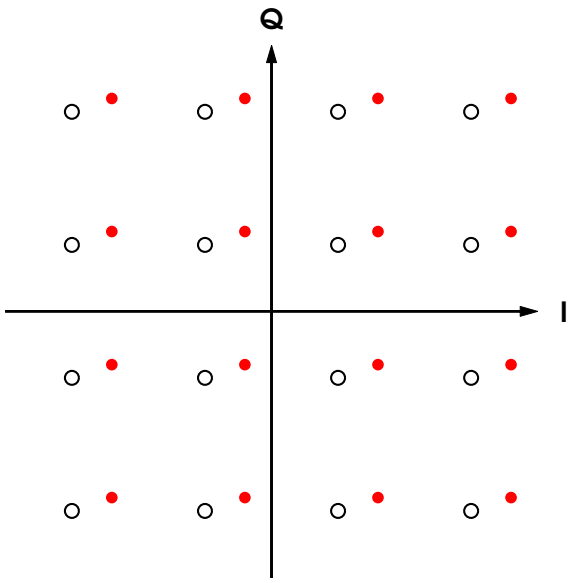


Figure 3.10: *DC offset translates the I/Q constellation.*

Noise

There are several noise sources in the transmitter. These include quantisation noise in the digital to analog convertor, AWGN noise floor and noise added by the TX noise figure and PLL/LO noise.

In the absence of non-linear effects (i.e. at a backoff from TX Op1dB), phase noise from the VCO should be the dominant source of EVM degradation in the TX.

Phase noise is the result of jitter in the LO signal. Inside the loop bandwidth of the PLL the external reference dominates the noise, above this the VCO dominates and in the far out specrum the LO generation circuits set the noise floor.

Figures 3.11 and 3.12 shown a 16-QAM constellation with phase noise and additive white gaussian noise added. The phase noise exhibits a circular shift around the origin and primarily has an impact on the phase of the constellation. AWGN noise affects both the phase and magnitude of the transmitted symbol. Phase noise can be tracked and corrected using pilot tones [66].

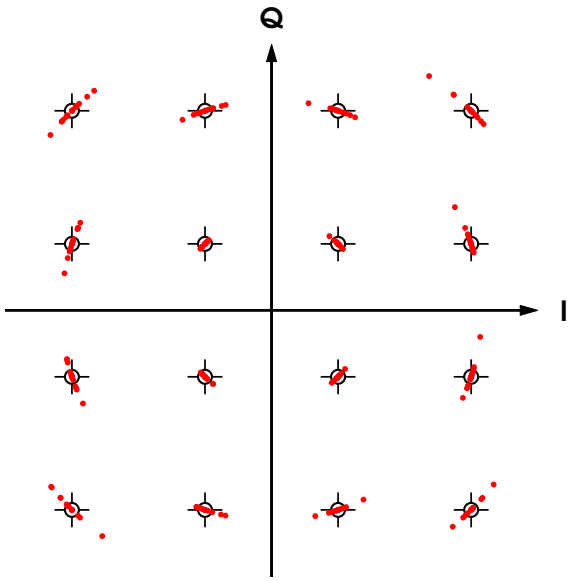


Figure 3.11: *16-QAM constellation with phase noise.*

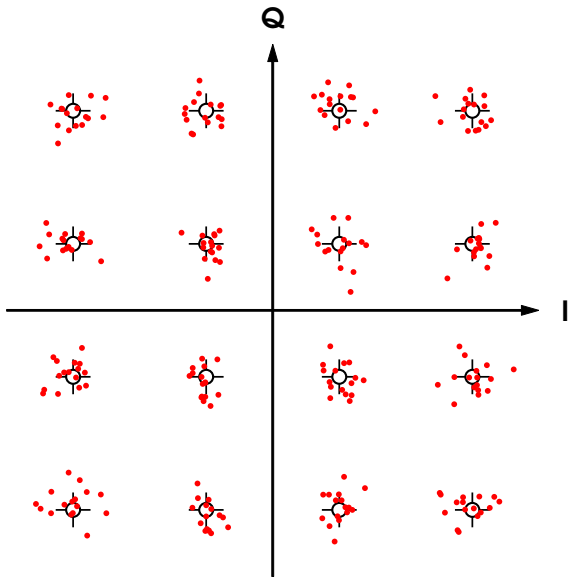


Figure 3.12: *16-QAM constellation with 10dB TX SNR.*

Non-linear distortion

Non-linearity can occur at any point in the transmit chain but to get the highest efficiency, the non-linear effects should be dominated by the PA. Memory-less non-linearity can be defined using two characteristics: amplitude to amplitude conversion

(AM-to-AM) and amplitude to phase conversion (AM-to-PM).

AM-to-AM conversion is the compression in power as the output signal is increased. AM-to-AM conversion in an amplifier is usually quantified by the 1dB compression point as shown in Figure 3.13.

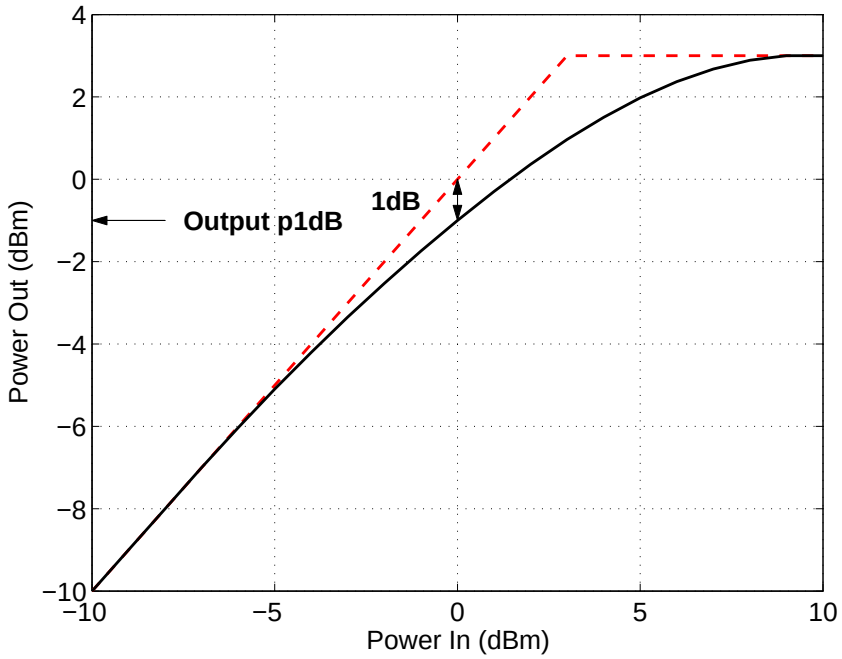


Figure 3.13: *Output 1dB compression point definition.*

AM-to-PM conversion is the modulation of output phase based on the size of the input signal. AM-to-PM conversion is shown versus input power in Figure 3.14.

A constellation showing the effect of pushing the power amplifier into hard compression is shown in 3.15. In this figure, the power of the constellation is normalized so that the total constellation power is equal to one. The effect of both AM-to-AM and AM-to-PM effects can be seen.

Figure 3.16 shows the degradation in transmitter EVM as the transmitter is pushed into saturation. The TX EVM starts at -40dB and is degraded to -10dB at the highest

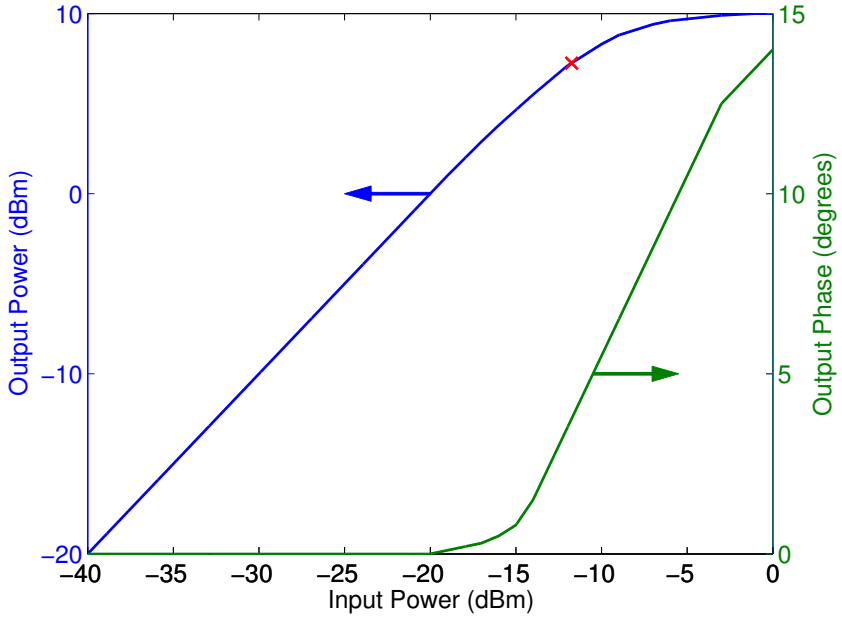


Figure 3.14: *Example plot of am-am and am-pm characteristics for a transmitter.*

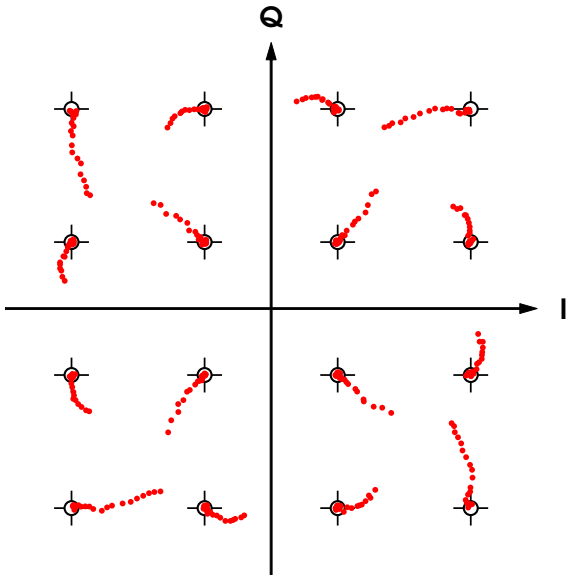


Figure 3.15: *16-QAM constellation pushed into hard compression. The PA is pushed to saturation. The power of each constellation is normalised.*

output power.

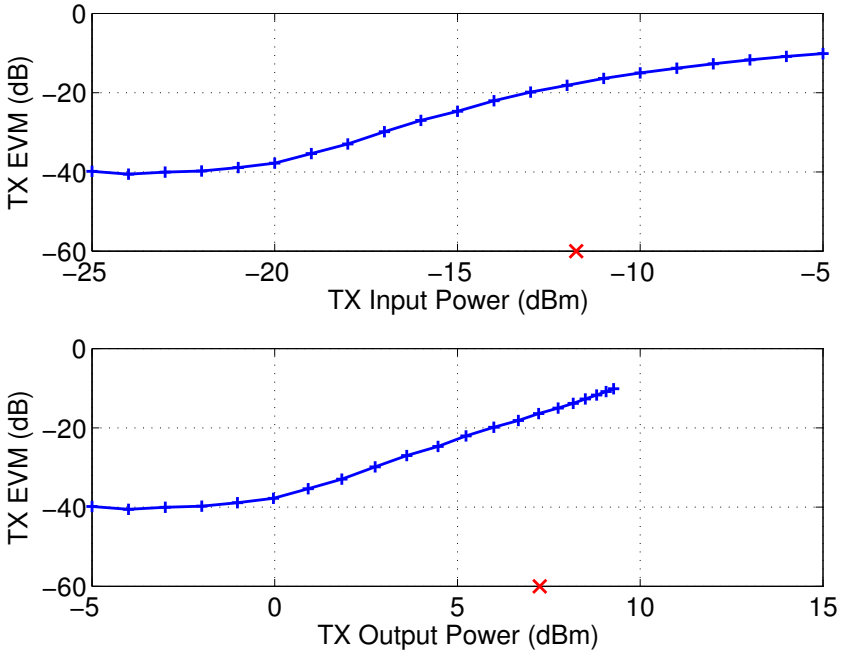


Figure 3.16: *Plots showing TX EVM versus input and output power. An EVM floor of -40dB is assumed.*

Intermodulation distortion

A second type of non-linear distortion called intermodulation distortion refers to the intermodulation of multiple tones. Intermodulation distortion can cause both in-band and out-of-band products in a transmitter. Figure 3.18 shows several of the modulated components from two input frequencies f_1 and f_2.

Spectral regrowth refers to the out-of-band frequency components generated in the transmitter. Spectral regrowth can be generated by non-linearity in the transmit chain, insufficient analog filtering of a Nyquist sampled DAC, insufficient digital filtering in an oversampled DAC or noise from the transmit chain on PLL but it should be dominated by the PA [65]. In a system where the PA dominates transmit power, allowing

the spectral regrowth to be PA dominated enables the transmitter to perform at peak efficiency.

Spectral regrowth is typically the limiting factor when increasing output power for lower order modulations where the EVM requirements are relaxed (QPSK, BPSK) and is limited by the transmit spectral mask. The 802.11ad spectral mask is shown in Figure 3.17.

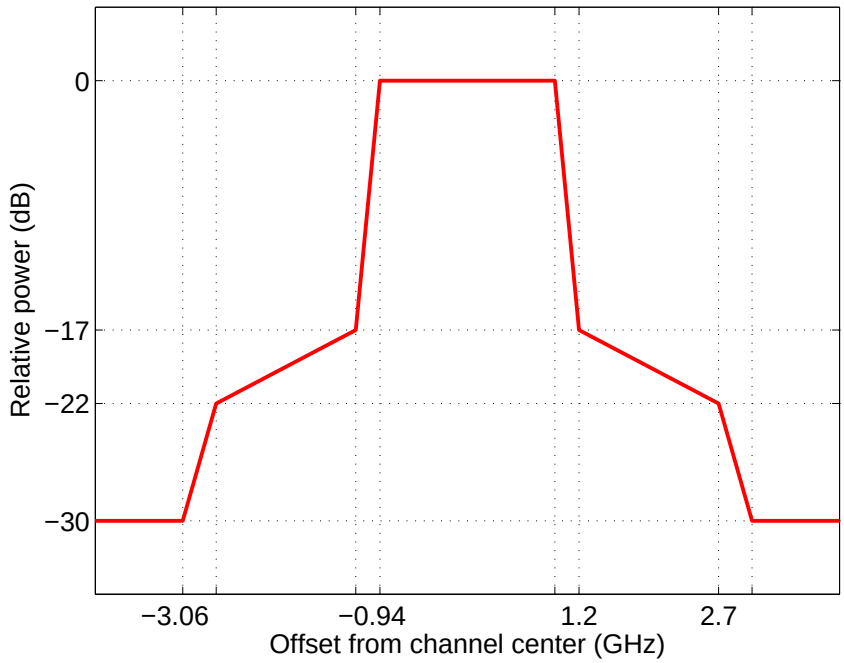


Figure 3.17: *802.11ad spectral mask [9].*

All Impairments

None of the TX impairments operate alone, they combine to distort the transmitted signal. Some are easy to correct with calibration in the digital baseband (I/Q phase and amplitude imbalance), in the analog domain (DC offset) and some are not easily reduced in a wide-band system (PA non-linearity). Figure 3.19 shows the combination

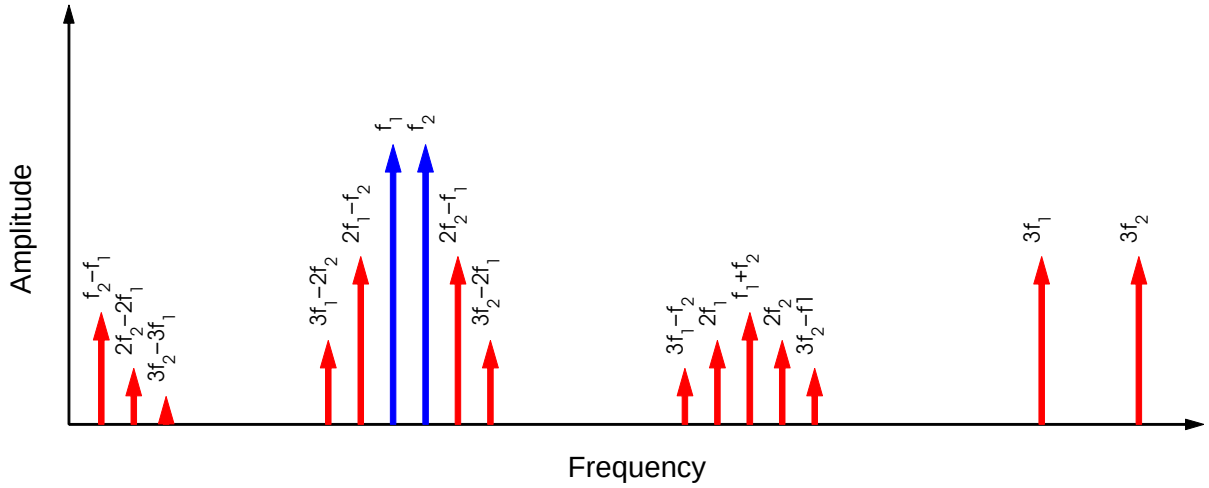


Figure 3.18: *Two input frequencies f_1 and f_2 inter-modulate to create many output components.*

of several impairments.

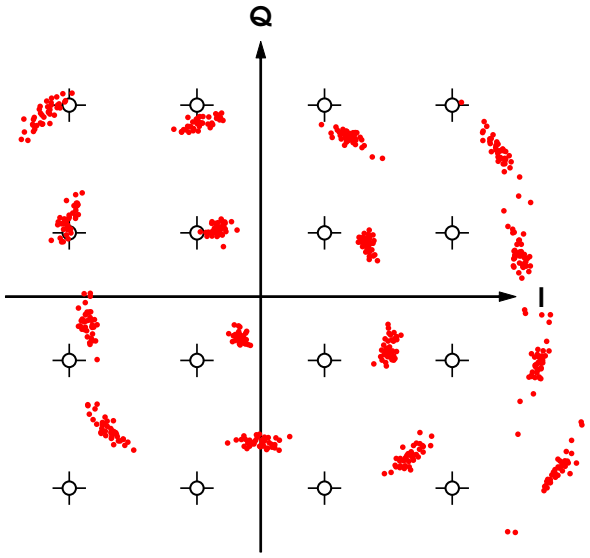


Figure 3.19: *TX output constellation showing a combination of TX impairments.*

3.4 Phased Arrays

Phased array systems have been used for RADAR [67, 68, 69], communication links [70, 71, 72] and satellite systems [73]. They offer several advantages over conventional single antenna systems and are especially attractive at mmWave due to the small wavelength. This section looks at why phased arrays are uniquely suited for mmWave transceivers, the benefits, some fundamentals, system level considerations and challenges.

Phased arrays are made up of 2 or more antennas which can be excited with specific phases to form a focused beam. Many applications can benefit from the focused transmission and reception of energy rather than using a broad beam. In an active phased array, changing the relative phases at each antenna enables the beam to be steered. The following properties control the performance of an array [74, 75]:

1. The position of each element
2. The excitation amplitude of each element
3. The excitation phase of each element
4. The antenna pattern (or unit pattern) of the elements

Phased arrays are required at mmWave frequencies due to the higher free space path loss. It is important to note however, that they are easily implementable at these frequencies due to the small wavelength that enables many antennas to be placed in a small area. For example, in the same area that a 5 GHz antenna occupies, 20 or more 60 GHz elements can be placed.

3.4.1 Array Pattern

The array pattern of a phased array is the summation of individual elements in the far field. In the case where identical elements are used, it can be defined at the product of the unit element pattern and the array factor [55]. If $\boldsymbol{d}_0, \boldsymbol{d}_1, \boldsymbol{d}_2, ...$ denotes the position of elements with relative feed coefficients $a_0, a_1, a_2, ...$ then the array factor can be given as [76]:

$$A(\boldsymbol{k}) = a_0 e^{j\boldsymbol{k}\cdot\boldsymbol{d}_0} + a_1 e^{j\boldsymbol{k}\cdot\boldsymbol{d}_1} + a_2 e^{j\boldsymbol{k}\cdot\boldsymbol{d}_2} + \cdots \tag{3.13}$$

The array factor for a linear array of elements is shown in Figures 3.20 to 3.23. In the 1 element case, there is no array, the array factor is a unit circle. For 2 elements the beam-width is reduced to 46.1° and 11.2° for 8 elements.

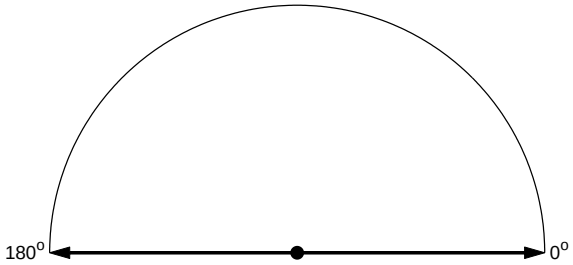


Figure 3.20: *1 element array factor*

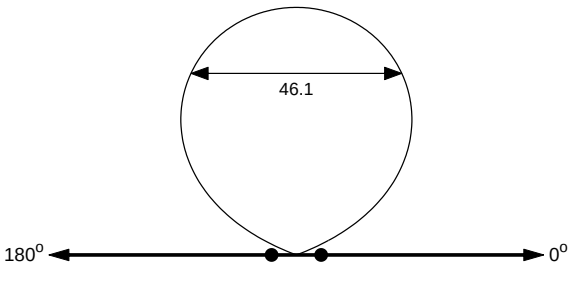


Figure 3.21: *2 element linear array factor, $\frac{\lambda}{2}$ spacing*

3.4.2 Array Gain

The array gain for a phased array is the increase in gain beyond a single element due to the array factor. Ideally, every doubling of antennas increases the array gain by 2×.

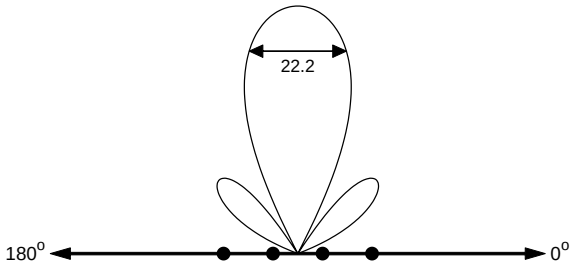


Figure 3.22: *4 element linear array factor, $\frac{\lambda}{2}$ spacing*

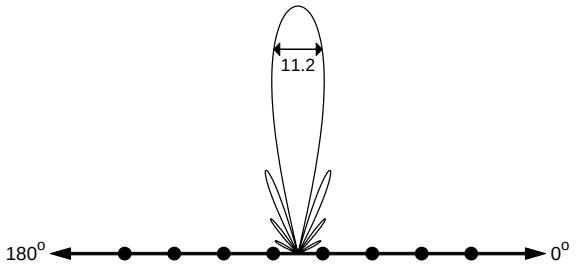


Figure 3.23: *8 element linear array factor, $\frac{\lambda}{2}$ spacing*

In decibels this can be expressed as an increase of $10 \times log_{10}(n)$ where n is the number of elements in the array.

3.4.3 Array Steering

Increasing the number of antennas to achieve higher gain is much more useful if the beam can be steered. In an active phased array, steering is achieved by adjusting the relative phase at each antenna. Side-lobe levels can be changed by adjusting the excitation amplitude as well as the phase. For communication systems that only make use of a small number (<32) of antennas, this is not usually done since reducing side-lobes can result in decreased power in the main lobe and maximising the link margin is more important than minimising energy elsewhere. A steered beam is shown in Figure 3.24.

3.4.4 Increase in Transmit EIRP

In a phased array transmitter, energy is radiated from multiple antennas and combined in space. Phased array transmitters not only benefit from the increase in antenna gain but also benefit from the spatial power combining of multiple power amplifiers. The

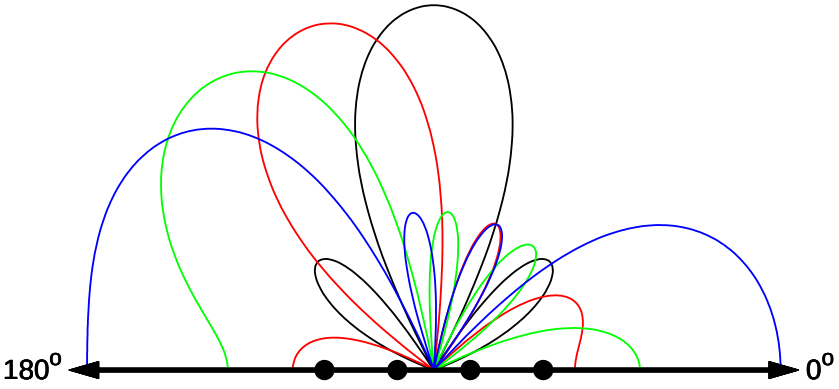


Figure 3.24: *4 element array, $\frac{\lambda}{2}$ spacing, steering from 90 to 150*

increase in effective isotropic radiated power (EIRP) beyond a single transmit chain is [77]:

$$10 \times log_{10}(n) + 10 \times log_{10}(n) = 20 \times log_{10}(n) \tag{3.14}$$

Figure 3.25 shows the increase in TX EIRP relative to a single antenna with increasing number of front-ends.

3.4.5 RX SNR Improvement

Compared to a single antenna receiver, multiple antennas improve the received signal SNR by:

$$10 \times log_{10}(n) \tag{3.15}$$

The SNR improvement is shown in the Figure 3.25.

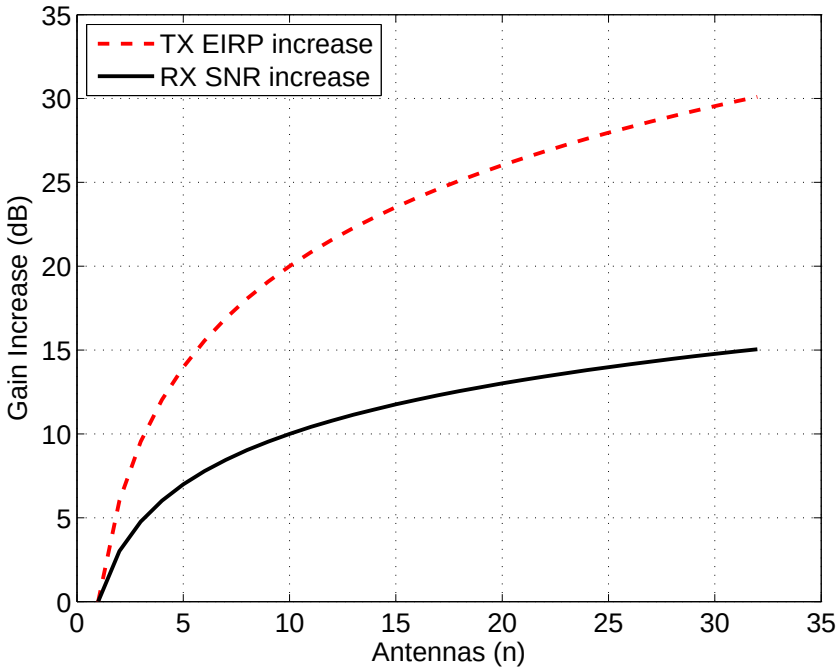


Figure 3.25: *TX EIRP and RX SNR increase vs. Antennas*

3.4.6 Phased Array Architectures

Figure 3.26 shows four different architectures for phased arrays.

Digital Combining

In digital phase combining systems the entire transceiver is duplicated for each antenna. These systems give the best performance and allow fine-grain control of the phase as well as more advanced MIMO methods such as BLAST [78]. Digital beam-forming is often used for military RADAR applications [79] but have the downside of high power and large area. Digital beam-forming systems are proposed for next generation mm-wave cellular applications, in [80] a hybrid approach is proposed where several digital beam-forming chains are connected to multiple RF front-ends.

LO Path Phase Shifter

Phase shifting in the RF path is simple to generate in a super-heterodyne system. In this architecture the RF mixers are duplicated and fed with a variable phase LO. This method decouples any phase adjustment from amplitude adjustment as amplitude changes in the LO path typically do not affect the RF path gain [2]. A CMOS LO phase shifter is shown in [81], in this design delay cells are used as the frequency of operation is less than 6 GHz.

RF Signal Path Phase Shifter

Phase shifting in the RF path enables the most compact implementation as the number of duplicated circuits is reduced. Several implementations have shown RF phase shifters at 60 GHz, these include [82, 83]. Implementing the phase shift in the RF path can have an impact on the transciever power if the loss is high and care needs to be taken to keep the amplitude mismatch between different phase shift settings as low as possible as unlike the LO phase shift approach, this directly impacts the gain of the RF path.

3.5 Summary

This chapter gave an overview of transmitters, transmitter architectures and typical transmitter impairments. EVM was outlined as a useful metric for TX design. These topics are useful to understand for the development of mmWave radios.

[2] This assumes a saturated LOGEN path

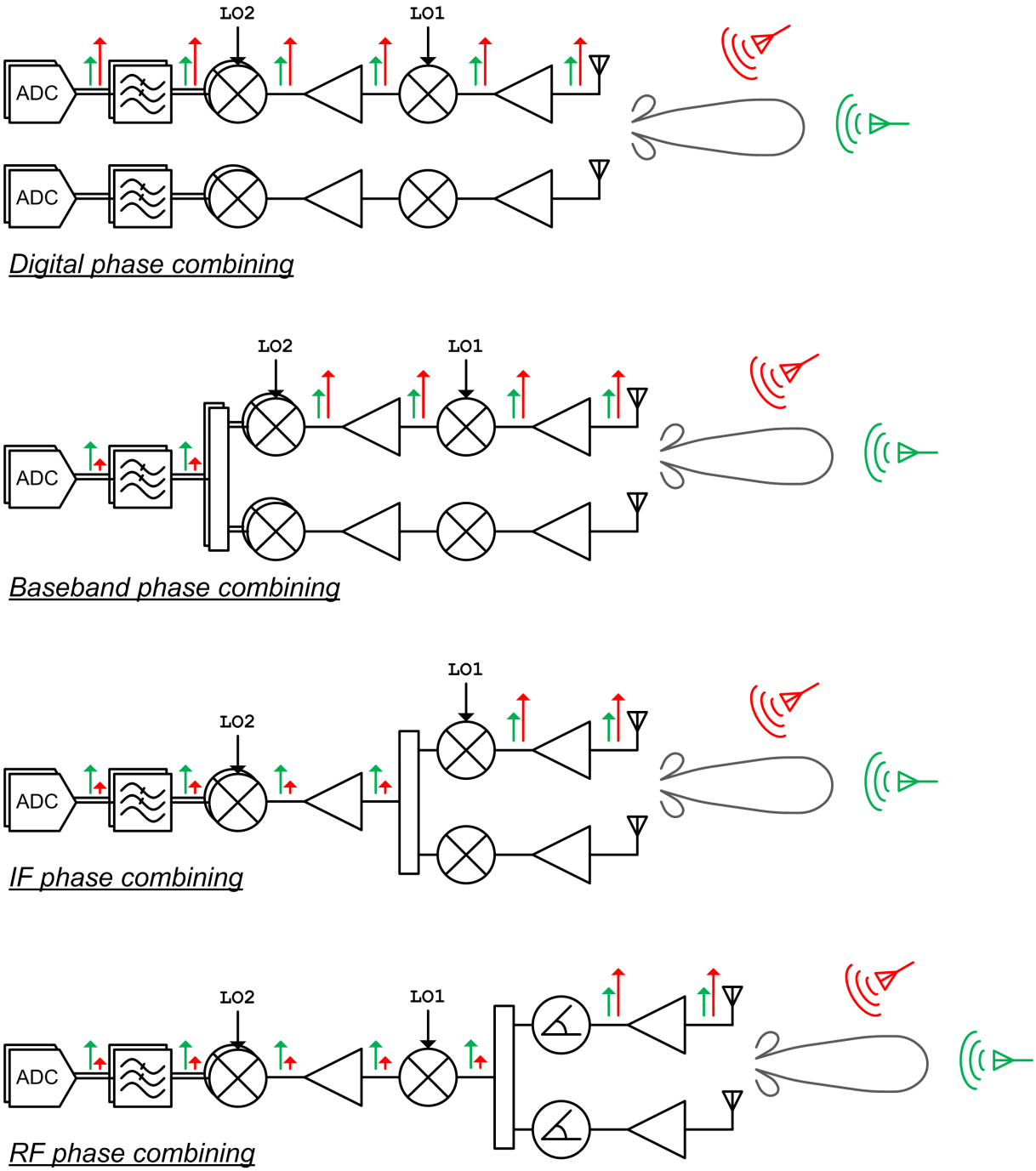


Figure 3.26: *Phased Array Architectures*

Phased array systems are implementable at 60 GHz due to the small wavelength (5mm). This chapter reviewed some of the fundamentals of phased array design including array pattern, array gain, steering, the increase in TX EIRP due to power combining and antenna gain as well as the improvement in SNR at the RX side. Different phased array architectures were outlined in the last section.

4

60GHz System Design

4.1 Introduction

This chapter outlines the system design for the two GLIMMR transmitters (GTC2-TX and GTC3-TX) and looks at some specific tradeoffs associated with the development of 60 GHz radios.

A link budget is built up for a 4 element system and this is compared to a single element system. Block level specifications are generated for both mmWave transmitters. Line-ups are also shown. These specifications form the basis for the PA and transmitter circuit designs later in this thesis.

4.2 Link Budget

A link budget is a useful calculation that accounts for all the gains and losses in a communication system. It can be used to calculate the maximum distance for a line of sight communication link given a required SNR or it can be used to calculate the SNR at a given distance.

A link budget for a 4TX, 4RX 60 GHz phased array system is built up below to show the procedure, at the end of this section the single antenna case is compared to the 4 antenna case.

The noise at the receiver input can be defined as:

$$N_{tot} = kT_0B \tag{4.1}$$

where:

$$k = 1.38e^{-23} Joule/^\circ C \text{ (Boltzmann's constant)}, \tag{4.2a}$$

$$T_0 = 270^\circ K \text{ (Receiver temperature)}, \tag{4.2b}$$

$$B = 1.86GHz \text{ (Receiver bandwidth)} \tag{4.2c}$$

For a 60 GHz 802.11ad single carrier system, the total noise at the receiver input is:

$$N_{tot} = 1.38e^{-23} \times 270 \times 1.86e^{9} \quad (4.3)$$

$$= -81.6dBm \quad (4.4)$$

Given a system noise figure of 10dB and 10dB SNR margin for QPSK demodulation, the receiver sensitivity is:

$$S_{min} = N_{tot} + NF + SNR \quad (4.5)$$

$$= -61.6dBm \quad (4.6)$$

The system sensitivity can be defined as the receiver sensitivity with antenna / system gain added. In the case of a 4 element system with 3dBi unit elements (average routing loss is included) the additional system gain is:

$$G_{rx} = 10 \times log_{10}(n) + G_{ant} \quad (4.7)$$

$$= 9dBi \quad (4.8)$$

$$RX_{sens} = S_{min} - G_{rx} \quad (4.9)$$

$$= -70.6dBm \quad (4.10)$$

(4.11)

At the transmitter, given 4 antennas with 7dBm output power each, the transmit EIRP can be given as:

$$TX_{eirp} = P + 20 \times log_{10}(n) + G_{ant} \quad (4.12)$$

$$= 22dBm \quad (4.13)$$

The link margin is the difference in TX_{eirp} and RX_{sens}:

$$LM = TX_{eirp} - RX_{sens} \quad (4.14)$$

$$= 92.7dB \quad (4.15)$$

In an AWGN channel, the range can be calculated from the free space path loss:

$$FSPL = \left(\frac{4\pi d}{\lambda}\right)^2 \quad (4.16)$$

$$d = \frac{\lambda\sqrt{FSPL}}{4 \times \lambda} = 17.1m \quad (4.17)$$

The resulting distance of $17.1m$ indicates the best case possible and different channel types, reflection loss, fading, margin for automatic gain control (AGC) and other system factors will reduce this. Figure 4.1 shows the difference in line of sight link

distance for an increasing number of antennas at the TX and RX sides. In this plot both TX and RX antennas = n.

4 TRX	**1 TRX**	**Units**	
-81.6	-81.6	dBm	$N_{tot} = kT_0B$
-61.6	-61.6	dBm	Add 10dB NF and 10dB SNR
-70.6	-64.6	dBm	Rx sensitivity with $10log_{10}n$ antenna gain
22.0	10.0	dBm	Tx EIRP with 7dBm TX and $20log_{10}n$ factor
92.7	74.6	dB	Link margin
17.1	2.1	m	LOS AWGN distance

Table 4.1: *Link budget for 1 and 4 antenna systems.*

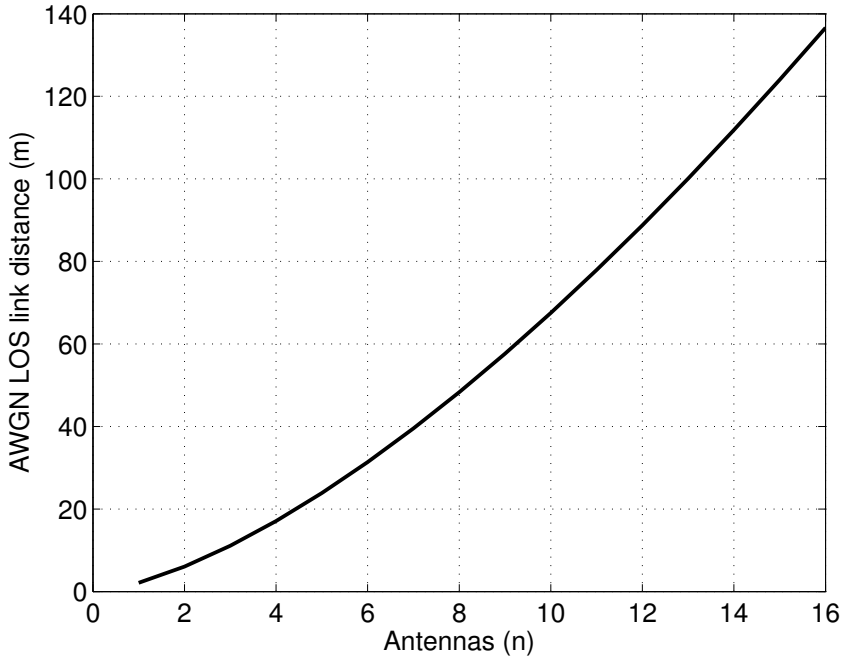


Figure 4.1: *LOS link distance in an AWGN channel for increasing antennas*

4.3 Block Level Requirements

4.3.1 Single Antenna TX

The block level requirements for the single antenna transmitter are shown below.

		BB PGA (offchip)	I/Q Mix	IF amp	RF Mix	PA
Gain	(dB)	0	-3	10	-3	26
NF	(dB)	20	15	10	15	10
Op1dB	(dBm)	0	0	3	0	10
Cascaded Analysis						
Gain	(dB)	0	-3	7	4	30
NF	(dB)	20	21.2	21.7	21.9	22.0
Op1dB	(dBm)	0	-4.8	0.9	-4.2	9.7

Table 4.2: *Block level specifications and lineup for GTC2.*

4.3.2 4 Antenna TX

The block level requirements for the multiple antenna transmiiter are shown below.

		BB PGA	I/Q Mix	interface	splitter	IF amp	RF Mix	PA
Gain	(dB)	3	-2	-4	-12	12	-2	30
NF	(dB)	20	15	4	12	10	10	10
Op1dB	(dBm)	0	0	20	20	3	0	10
Cascaded Analysis								
Gain	(dB)	3	1	-3	-15	-3	-5	25
NF	(dB)	20	20.6	20.7	21.6	26.3	26.5	26.8
Op1dB	(dBm)	0	-4.1	-8.1	-20.1	-8.5	-10.8	9.5

Table 4.3: *Block level specifications and lineup for GTC3.*

4.4 60 GHz System Optimisation

4.4.1 Blocked Links

The propagation of mmWave signals is significantly different to lower frequency signals. Unlike 2.4 GHz and 5 GHz which are composed of multiple waves coming from a primary and multiple secondary sources, 60 GHz can be viewed more like a quasi-optical signal. This is due to the small wavelength which results in reduced diffraction effects and sharp shadowing losses [84].

The modelling of 60 GHz links is typically done with ray tracing software which calculates the potential spatial paths between a transmitter and receiver and the losses due to reflection.

For mmWave links >10m, high gain, steerable antennas are used to close the link budget. The losses due to blockage by humans can be on the order of 20-30dB [16], in this case, steering around the blocked link by using a reflected path often results in better link performance. Reflection losses in typical office environments are on the order of 10dB [16].

Figure 4.2 shows a line of sight (LOS) link using a reflected path after being blocked by a human.

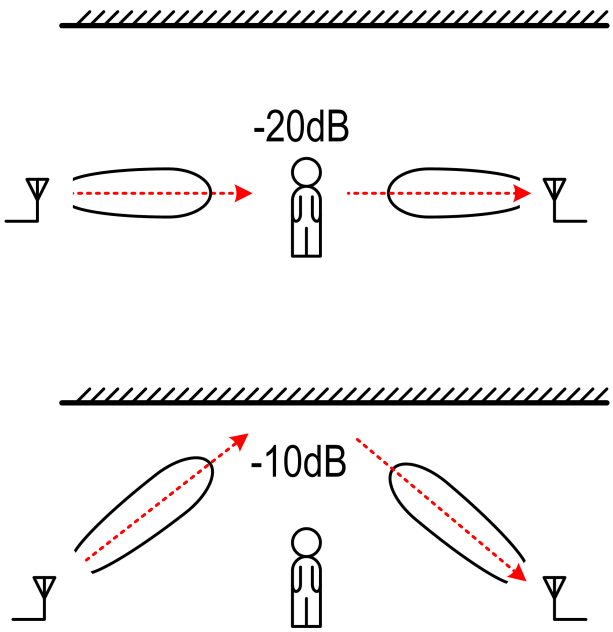


Figure 4.2: *A blocked LOS link is shown at the top. In this link, the blocker has 20dB loss. In a beam-formed system, it is better to steer around the blocker and use a reflected path. The loss due to reflection varies based on the material but 10dB has been found to be a reasonable approximation [16].*

4.4.2 Optimal Number of TX Antennas

In a real phased array system constraints such as maximum power dissipation and routing losses impact the optimal number of antennas. The EIRP of n antennas can be defined as:

$$EIRP(n) = 20 \times log_{10}(n) + P_{out} \tag{4.18}$$

A simple transmitter is shown in Figure 4.3. In a system constrained by a power limit, and assuming several overheads which cannot be reduced, the EIRP for the transmitter can be given by:

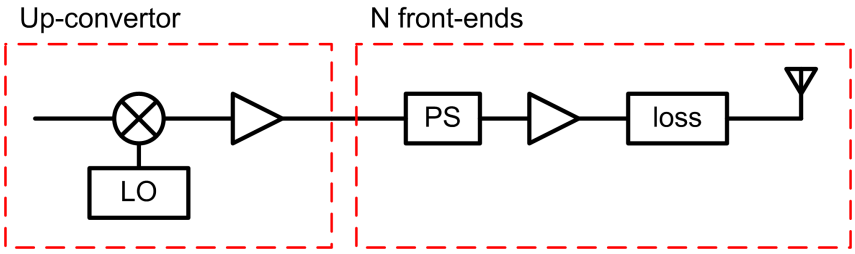


Figure 4.3: *Simple transmitter block diagram*

$$Pdc_{avail} = Pdc_{max} - Pdc_{core} - n \times Pdc_{fixed} \quad (4.19)$$

$$Pdc_{pa} = \frac{Pdc_{avail}}{n} \quad (4.20)$$

$$Prf_{out} = 10 \times log_{10}(Pdc_{pa} \times PA_{eff}) \quad (4.21)$$

$$EIRPconstrained(n) = 20 \times log_{10}(n) + Prfout - n \times 1.5 \times loss \quad (4.22)$$

where,

$$loss = \text{Routing loss to antenna in dB/mm} \quad (4.23)$$

$$n = \text{Number of front-ends} \quad (4.24)$$

Figure 4.4 shows this analysis for 600mW total power budget, core power of 300mW, a fixed overhead of 10mW per front-end and routing loss of 0.3dB/mm. In this analysis, it can be seen that around 8 antennas is optimal. Different system parameters and power consumption limits will result in different optimum.

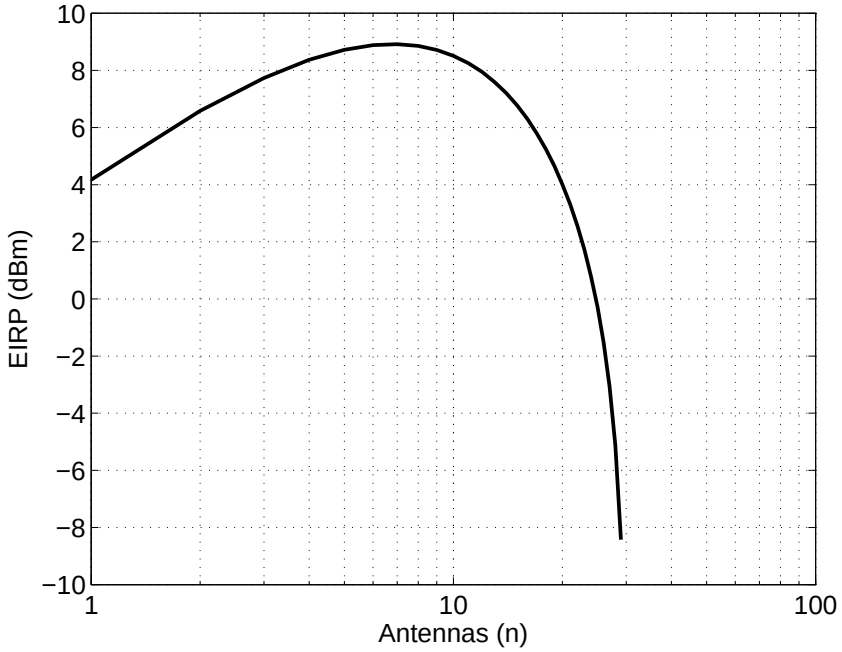


Figure 4.4: *Total EIRP vs. number of TX antennas for a fixed power budget*

4.4.3 TX/RX Switch

In most WLAN and Bluetooth systems a single antenna is used with a TX/RX switch. At 60 GHz the switch loss can be in the range of 1-2dB depending on technology and implementation [85]. Depending on the area available for the antenna array and the performance requirements of the system a choice can be made between separate TX and RX arrays or a single array with TX/RX switches. In almost all cases, a single array using shared TX/RX antennas which achieves the maximum aperture area with lowest routing losses is the most optimal.

For the case where 8 antennas are available, these can be partitioned as 4TX, 4RX or 8TRX.

The EIRP (given a fixed DC power) will be 3dB higher for 8TX antennas compared to

4TX. In this calculation, the factor is $10log_{10}n$ improvent, not $20log_{10}n$ as the output power for each antenna in the 8 element case is reduced by 3dB to stay at the same system DC power.

For the receiver, the SNR can be improved by an additional 3dB with an increase in DC power consumption.

For a switch loss of 1.5dB on each side, and keeping power consumption fixed there is no difference in system link budget. As the switch loss gets lower there is a clear benefit from sharing antennas between transmit and receive. If switch loss can be maintained at 1.5dB, there is still a valid argument for TX/RX switch as some extra margin is available in the reciever if the power can be increased slightly and number of front-ends increased.

4.4.4 Asymmetric Links

In the 60 GHz eco-system handheld devices will communicate with always powered (plugged in) devices such as routers, televisions, monitors and docking stations. In such an environment it is important to try and limit the power use by battery operated devices and push as much of the burden on the plugged in device. The limiting case is battery to battery communication such as cellphone to cellphone. If cellphone to cellphone (or tablet to cellphone) communication can be limited to LOS with the assumption that the user will help with orientation then an efficient system can be implemented.

In an ecosystem where different devices have different numbers of antennas, and assuming the power amplifiers on both sides of the link are the same, the forward and

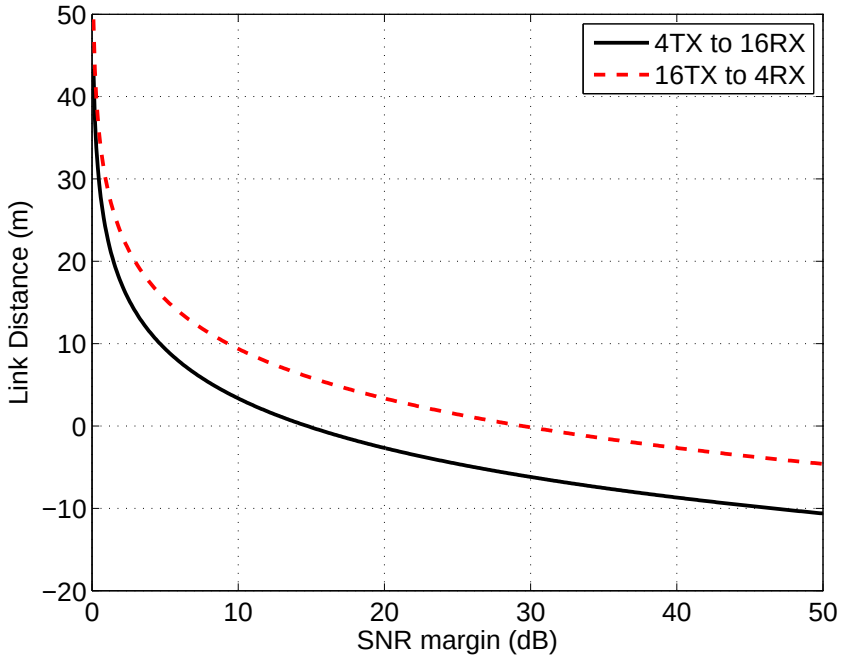


Figure 4.5: *Link SNR margin vs. distance for an asymmetric link setup*

reverse links have different margin. Figure 4.5 illustrates this. It shows the SNR margin versus distance for 4TX to 16RX (cellphone to TV) and 16TX to 4RX (TV to cellphone). In the first case the AWGN LOS distance is 15m and 30m in the second.

4.5 Summary

This chapter built up a link budget for 1x1 and 4x4 60 GHz systems. Block level specifications were generated from high level requirements. Several 60 GHz system aspects were also discussed.

5

Power Amplifier Design

5.1 Introduction

Power amplifiers (PAs) are a core component in RF transmitters. They are responsible for the efficient delivery of RF power to a load [39].

This chapter presents some fundamentals of high frequency PA (and circuit) design and a methodology which results in the first time right design of four PAs. The design methodology proposes a structured approach to the design and modelling of active and passive devices and make use of well defined interfaces and ground return paths. The methodology is based on RF board level design and is scaled to chip-scale designs.

The first PA presented is a low frequency, high efficiency design undertaken for the 2007 IMS student high efficiency PA competition, an annual event held at the IMS-RFIC conference. This PA won the competition with a measured efficiency of 88% [18]. While not a mmWave PA, many of the same modelling, simulation and design techniques apply on a board level hybrid as they do for a IC.

The second PA is a transmission line based design in Jazz 0.18 µm SiGe. This PA has a wide bandwidth with only 2.5dB variation from 57-64GHz. It achieves a peak gain of 30dB and has an output 1-dB compression point (Op1dB) of 8-9dBm. It suffers from a large area due to the transmission lines.

The outcome from the work in this chapter was a design methodology for first time right designs and an understanding of RF and mmWave design techniques.

5.2 Fundamentals

A simple transmitter with the integrated PA highlighted in blue is shown in Figure 5.1.

The PA is placed after the last up-conversion stage and connected to the output of the chip where it interfaces to the antenna. PA designs need to take performance, efficiency and reliability (due to electrostatic discharge (ESD), device stress and antenna mismatch) into consideration. This section reviews some system requirements, topologies and optimisation points for PAs.

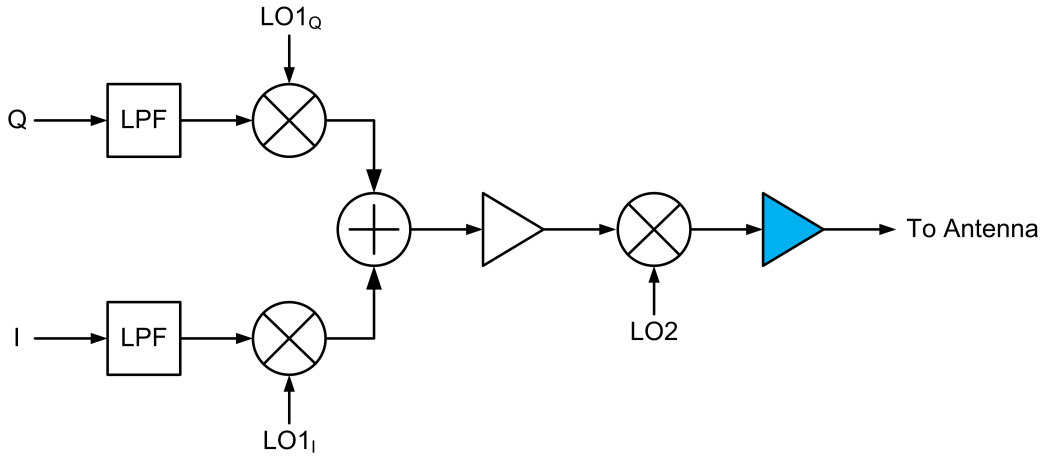


Figure 5.1: *Block diagram of a dual-conversion transmitter with the PA highlighted in blue.*

5.2.1 Key Parameters

Several key parameters for PAs are outlined below.

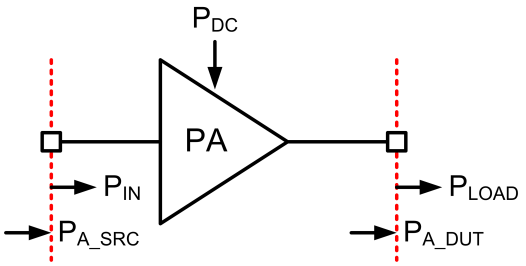


Figure 5.2: *PA with annotated power definitions.*

Power added efficiency (PAE) is a measure of efficiency which takes into account the gain of the device.

$$PAE = \frac{P_{LOAD} - P_{A\_SRC}}{P_{DC}} \tag{5.1}$$

Transducer gain (G_T) is the power delivered to the load divided by the power available from the source.

$$G_T = \frac{P_{LOAD}}{P_{A\_SRC}} \tag{5.2}$$

Power gain (G_P) is the power delivered to the load divided by the power available into the amplifier. It only takes into account output match.

$$G_P = \frac{P_{LOAD}}{P_{IN}} \tag{5.3}$$

Available gain (G_A) is the power available from the amplifier divided by the power available from the source. It only takes into account input match.

$$G_A = \frac{P_{A\_DUT}}{P_{A\_SRC}} \tag{5.4}$$

5.2.2 PA Efficiency

The power of a transmitter is often dominated by the PA. By increasing the efficiency of the PA the overall transmitter efficiency and system power can be improved.

In high power, low frequency systems like cellular base stations, the limiting factor is often thermal and cooling effects. Increasing the efficiency by even a few percent helps reduce the cost and complexity associated with cooling.

In mmWave transmitters the PAs operate at much lower power but with several in parallel. For consumer devices which operate from a battery, a peak power limit is imposed by the system architect. In this case, increasing efficiency either allows in-

creased output power (higher performance) or, if this is not required, results in an improvement in battery life.

The importance of efficiency is shown in Figure 5.3, for a required output power the normalised power consumption versus efficiency is shown. It can be seen that at very low efficiencies - which are characteristic of mmWave PAs, increasing efficiency only slightly makes a big difference in system power consumption.

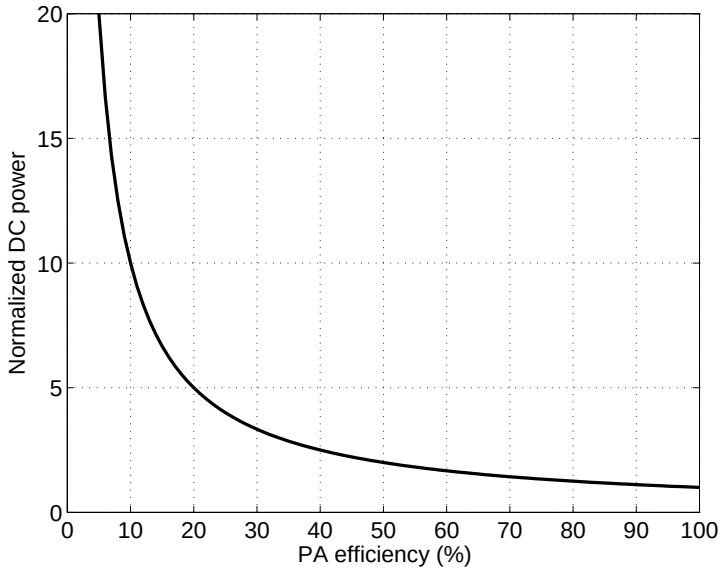


Figure 5.3: *Normalised DC power of a PA versus the efficiency.*

The maximum theoretical efficiency for a class-A PA with a lossless inductive tank is 50%, for a simple amplifier with 1V Vcc, 10mA quiescent bias current and 100ohm load, this is shown by the following equations.

$$
\begin{aligned}
P_{DC} &= V * I_Q \\
&= 10mW \\
P_{AC} &= \frac{V_{rms}^2}{R_L} \\
&= 5mW \\
Eff &= \frac{P_{AC}}{P_{DC}} \\
&= 50\%
\end{aligned}
$$

In real implementations, the theoretical efficiency is reduced by losses in the inductive tank, losses in the output matching network and limits on the voltage swing due to transistor turn-on voltage or reliability concerns.

Figure 5.4 shows a simple circuit for a linear PA and Figure 5.5 shows the reduction in maximum efficiency due to (a) losses in the output matching network, (b) resistance in the tank inductor, (c) limits on the voltage swing and (d) the PAE for different levels of gain. Class-A results are shown in Blue and Class-B results are shown with red dotted lines. This highlights the importance of modeling and reducing the losses in the design. It also illustrates why it is more difficult to get high efficiencies as the frequency increases.

The efficiency with an effective 6 Ohm resistive loss (in tank, ground and device and due to skin effect), 2dB loss in the output matching network, 0.2 Volt minimum swing and 6dB last stage gain is 12% for class-A and 20% for class-B. This is just the last stage efficiency, adding additional stages which is typically required due to low mixer linearity results in even worse efficiencies. Typical mmWave designs have peak efficiencies of 5-10% [86, 87, 88, 89, 90, 91].

Waveform engineering techniques [92] that involve increasing efficiency by terminat-

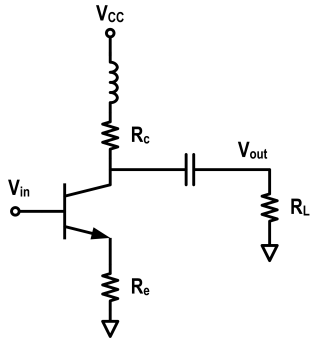


Figure 5.4: *Example linear PA schematic.*

ing specific harmonics of the amplifier with certain impedances to achieve class D, F, E (or their inverse) require the core transistor to have gain at these harmonics. For 60 GHz designs, the second harmonic is 120 GHz, third 180 GHz and fourth 240 GHz. With limited f_{max} the useful harmonics are limited.

The type of modulation used dictates how much distortion can be introduced by the PA. For 11ad systems with QPSK, 16-QAM and 64-QAM modulations, the EVM degradation from the PA can typically be in the range -10dB to -30dB. Reaching high EVM performance requires a linear PA with some back-off from the saturated output power level. Figure 3.16 in Chapter 3 shows this.

With the exception of the 1 GHz board level PA, the PAs in this chapter are linear designs which meet the distortion requirements for 11ad systems.

5.2.3 PA Optimisation for 60 GHz Systems

In multi-element phased array systems the output power from several PAs is combined in free-space. For a fixed EIRP target, this spatial power combining offers a benefit as the power from each PA can be reduced, this is shown in Figure 5.6. In technologies

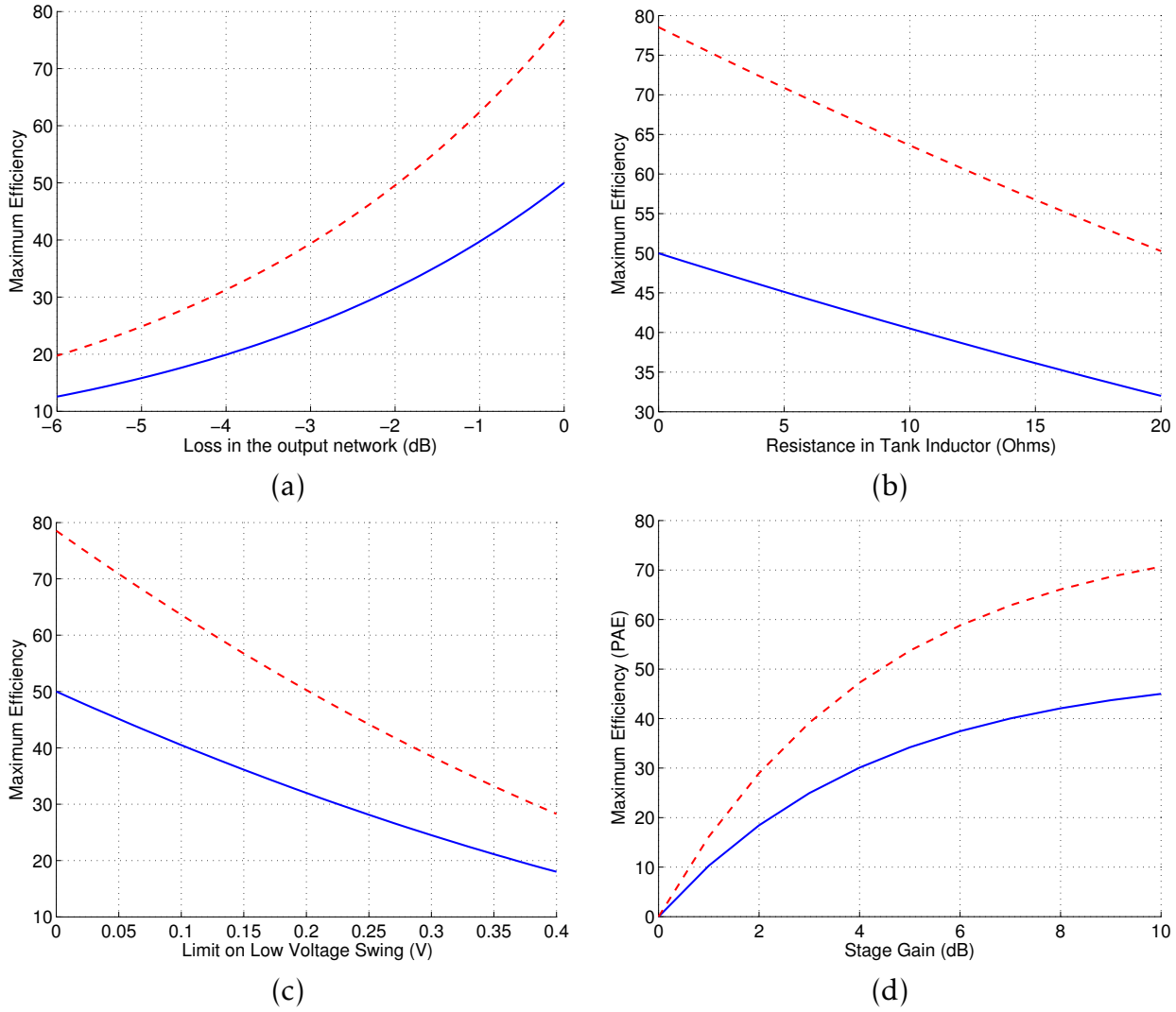


Figure 5.5: *This set of plots show the maximum efficiency of a Class A (blue) and Class B (red dots) with ideal implementation except for (a) loss in the output network (b) resistance in the tank Inductor (c) limit on the available swing (due to knee or reliability limits) (d) the gain of the stage (in this case PAE is plotted)*

like CMOS where a low voltage supply limits the reasonable output power it offers an elegant way to increase EIRP without resorting to lossy on-chip power combining [93].

It should be noted that Figure 5.6 shows an idealised case, actual implementations suffer from routing loss to antennas and there is usually a fixed overhead in with each additional transmitter that is used in parallel. Section 4.4.2 analyses this in some more detail and outlines a formula for the optimal number of TX antennas given a system power budget and specified fixed overhead per additional front-end.

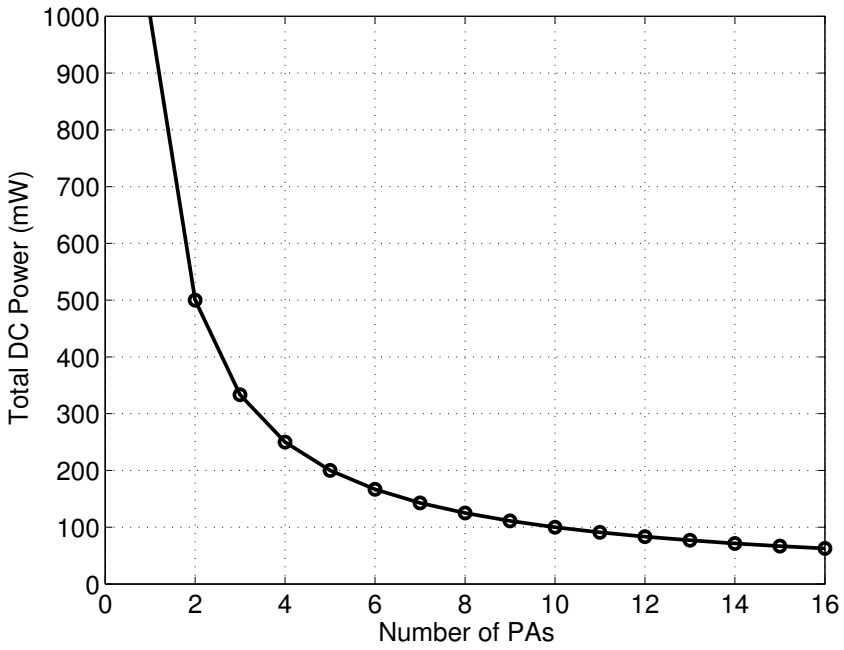


Figure 5.6: *Total power to achieve a 20dBm EIRP assuming 10% PA efficiency.*

The formula used to generate Figure 5.6 is below.

$$P_{DC} = \frac{10^{\left(\frac{20-20\times log_{10}(n)}{10}\right)}}{10\% \times n} \tag{5.5}$$

5.3 Design Methodology

A structured approach to design and modelling enables the first time right design of RF circuits including PAs. This chapter explores both 1 GHz and 60 GHz PAs and makes use of a similar design methodology scaled to higher frequency. It consists of: 1) validation of device models and device optimisation 2) simple RLC extraction for small interconnect much shorter than a wavelength 3) EM modelling and optimisation of custom passive devices. This is shown in Figure 5.7.

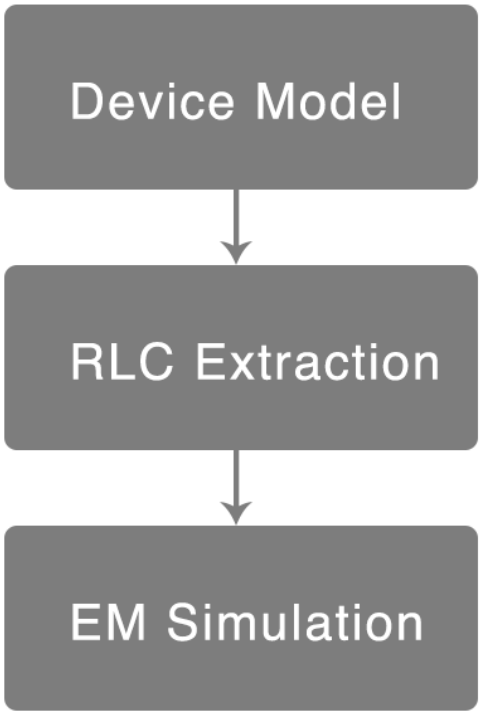


Figure 5.7: *Flow chart showing the design methodology.*

This design methodology was used for the PAs presented in this section as well as the other transmitter circuits in the following chapters.

5.3.1 Device modelling and optimisation

Device models are often provided by the manufacturer or foundry but need to be validated, especially if modifying the base layout. For all the designs in this thesis, test devices were taped out with calibration structures in order to check the models. Standard calibration and de-embedding methods were used. For board level designs, calibration is done to the SMA cables then on board de-embedding structures are used to move the reference plane to the device under test. The short, open, load, through (SOLT), layouts are shown in Figure 5.8.

Probes are used to measure on-chip devices. In this case, the probes are calibrated to the end of the probe tips using a calibration standard such as CS-5 from Cascade Microtech. On-chip SOLT structures shown in Figure 5.9 are used to move the reference place to the device [94].

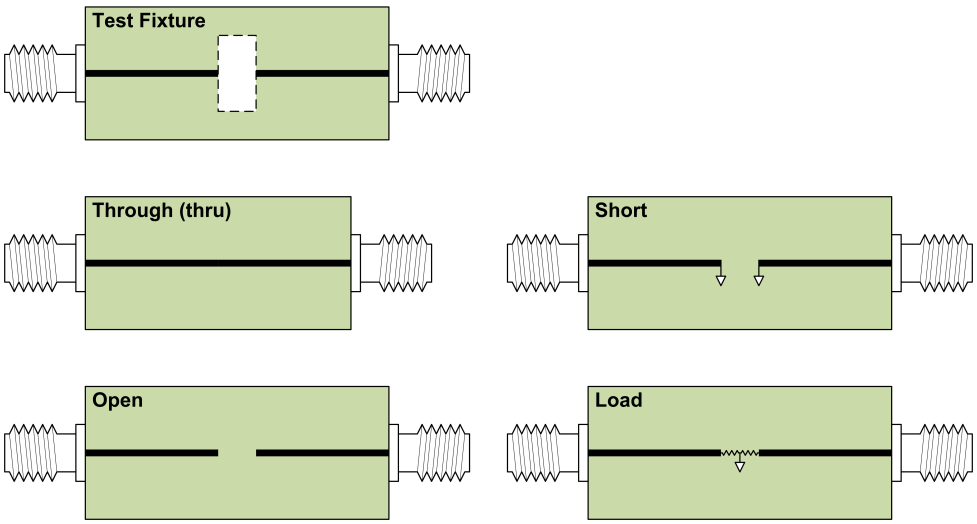


Figure 5.8: *Test fixture and SOLT structures for board level design.*

Transmission lines are also included in the de-embedding structures. Open short and TRL methods are both used for de-embedding and more details can be found in [95].

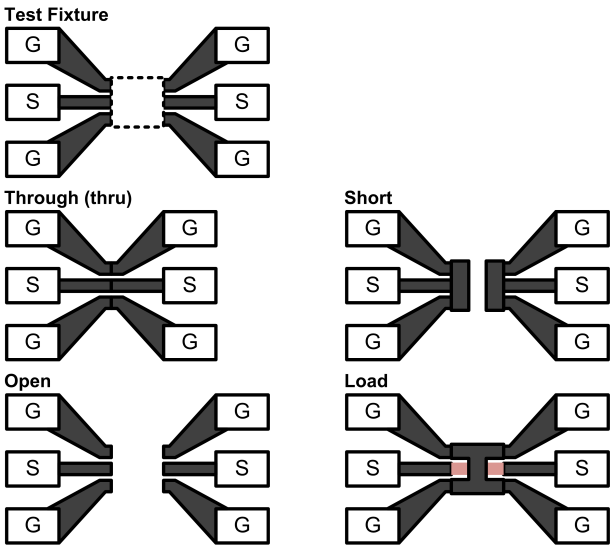


Figure 5.9: *Test fixture and SOLT structures for chip level design.*

Once the devices are validated, they can be optimised for operation in the design. If the device models are not accurate, bias dependent S-Parameter measurements can be used. If this is done, it's usually helpful if the reference plane for the device measurement and the RC extraction is the same. If measured models are used, step (2) can be skipped.

To get the best circuit performance the individual devices also need to be optimised.

CMOS Device Optimisation

The length, width and number of fingers need to be optimised as well as the device layout. The smallest length offered by the technology is used to reduce transit time. The total width is the device width multiplied by the number of fingers.

For 65nm LP technology a unit finger width of 1.0-1.5µm is used to maximise performance. This width offers the highest Gmax and peak ft for the device. Choosing the

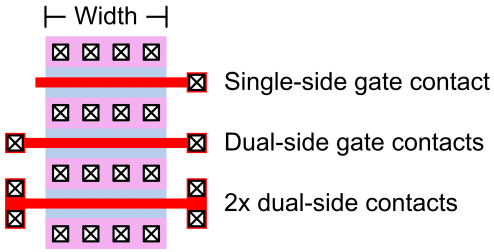


Figure 5.10: *Gate contact options.*

device width is a tradeoff between high R_g for fewer longer fingers and higher C_{gd} and other parasitics from many short fingers. The effect of device width versus maximum stable gain can be seen in figure 5.11.

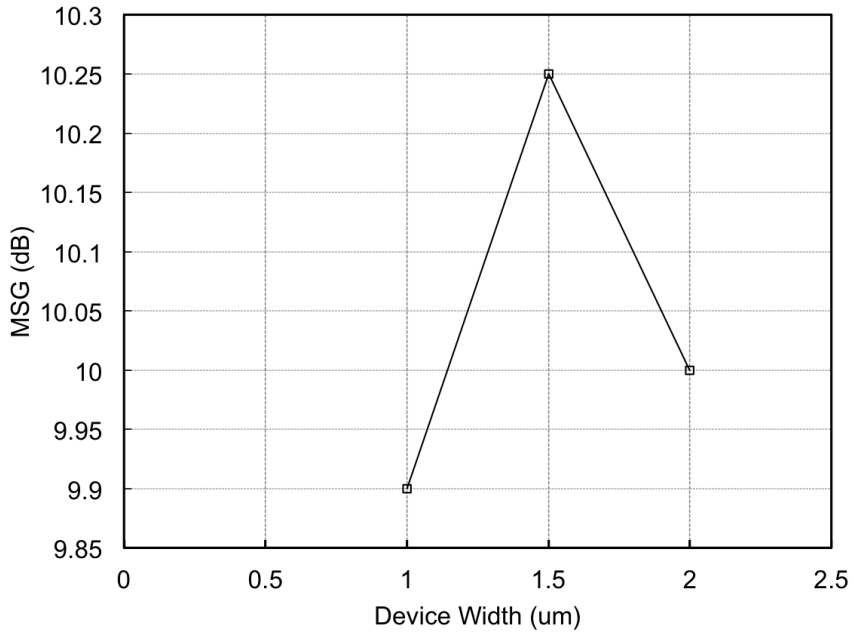


Figure 5.11: *Transistor MSG (dB) vs. device finger width (um). Total device size is constant (90um).*

The f_T, f_{max} of the transistor versus bias is shown in Figure 5.12.

The total device width is chosen based on the requirement for output power and the stage the device is in the design. The device should be biased at close to peak f_T, this usually corresponds to close to class-A operation. De-biasing the transistor for operation in more efficient classes is difficult at 60 GHz in 65nm CMOS as the gain and

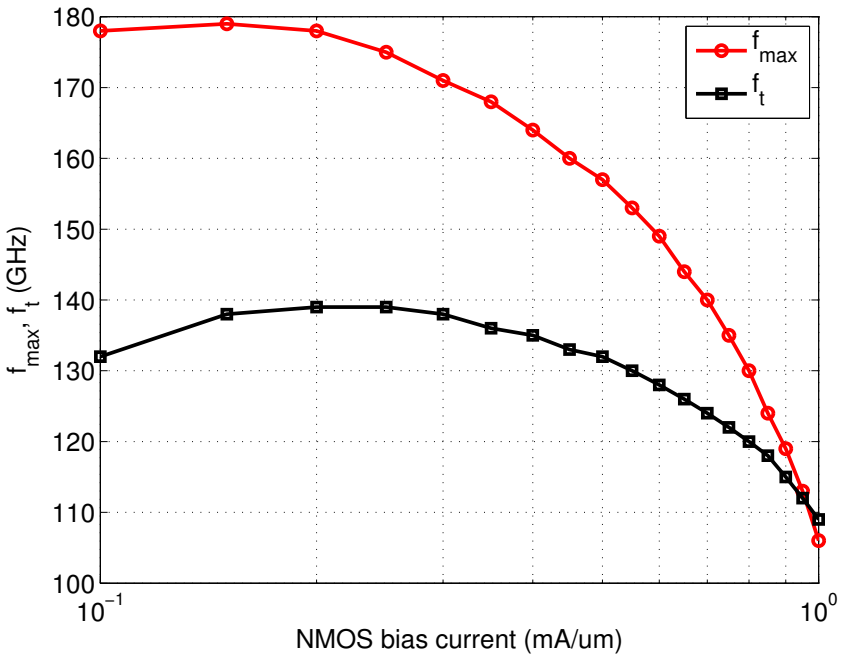


Figure 5.12: *CMOS device f_T and f_{max} versus bias current.*

f_T of the device drops as the current is reduced affecting the PAE (as seen in Figure 5.5 (d)). When operating at a significant fraction of the device f_T, the bias can be backed off without as much impact in performance and higher efficiencies can be achieved.

SiGe Device Optimisation

The best topology for SiGe devices when trying to maximise speed is three base and two emitter fingers. This configuration minimises the transit time of electrons between the emitter and collector while maintaining a large emitter area [96].

The optimisation of SiGe devices is simpler than CMOS as configurations are limited by the foundry, the sizes are bigger due to higher node for equivalent performance and less devices are required in parallel due to the higher current carrying cabability of HBT devices. The only degree of freedom is choice of base, collector and emitter

configurations, device area and layout of the metal interconnect.

The size of the SiGe device is chosen so that it meets the required output power. SiGe devices are usually biased at a higher current density than CMOS, typically around 3× higher.

5.3.2 Device RC extraction

For integrated designs, the core device up to the contact or first-layer metal is usually modelled by the foundry. The parasitic elements from interconnect and escape to the higher metal layers are not captured. Parasitic extraction is used to model these connections. It is important that a well defined reference plane is used to make sure interconnect is not double counted. Figure 5.13 shows a transistor in a test fixture with the reference plane defined in red.

All parasitics within the red boundary are extracted with parasitic extraction. Outside of this, EM modelling is used.

It is important that the RC extraction engine acurately extracts all the device capacitance and capacitance to ground. The device layout is done such that C_{gd} (or C_{bc}) capacitance are kept as small as possible. Reducing gate (or base) resistance is also important. The goal of the device layout is to meet electro-migration rules while limiting the most degrading parasitics. The RC extraction should be done on a scale which is much smaller than the wavelength. For Silicon designs, the effective wavelength on-chip is reduced due to the high dielectric constant of the substrate and dielectric layers as shown in the following equation.

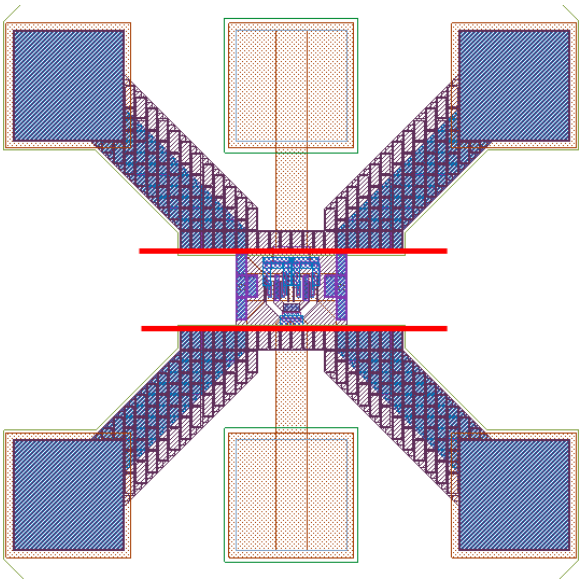


Figure 5.13: *Transistor shown in test structure with reference plane defined in red.*

$$\lambda = \frac{\lambda_o}{\sqrt{\epsilon_{eff}}} \tag{5.6}$$

For a dielectric constant (ϵ_{eff}) of 9, the wavelength is reduced by a factor of 3. 60 GHz signals have a wavelength of 5mm in a vacuum. This is reduced to 1.6mm on chip. If the interconnect is kept to much less than this (20× smaller) ~80um then the RC extraction will be valid.

5.3.3 Electromagnetic (EM) Modelling

Correct modelling of EM devices reduces the chance of frequency mismatch, in-stability and several other problems in PA design. A 2.5D or 3D simulator can be used. For the designs in this thesis, HFSS was used.

As shown in Chapter 2, Figure 2.5 a clear ground return path and boundary can

help with the device design. For single-ended designs the ground return is a critical part of the model and affects the inductance and Q-factor - it must be modelled. For differential designs, including this as part of the model can help reduce the impact of surrounding ground loops and sets a clear boundary for other parts of the layout to keep clear of.

The optimisation of EM devices for mmWave designs is challenging given the many degrees of freedom and the long time taken for a full 3D simulation.

In the initial design phase, a narrow band psuedo device model (impedance tuner) can be employed which exhibits reasonable Q (15-18 for 60 GHz). and simply matches the input and output to the impedances which give the best performance, this can be done for each stage in the chain.

Once these psuedo device models are found, the goal is to find the correct transmission line, inductor and capacitor or transformer which achieve this transformation, have the lowest loss (G_{max} is a good metric) and achieves the required band-width. Simple scalable equivalent circuit models are the best place to start and these can be generated from a parametric sweep of the chosen EM device. The models should be simple, capture the bandwidth of interest and scalable.

Once a close match is found full 3D simulations can be run to optimise the EM device and come up with the final circuit.

5.3.4 Summary

The design flow outlined in this section is used in the designs which follow. It can be used from low frequency RF to mmWave and has resulted in the first time right correct of several circuits for mmWave transmitters.

5.4 A GaN HEMT amplifier with 6 Watts output power and >85% PAE

While not a mmWave design, this was an interesting project investigating high efficiency PAs. Many of the techniques including modelling, EM simulation and design at a board and component level translate to mmWave at the chip and transistor level.

The 2007 IEEE MTT-S student PA competition requires students to design and fabricate a highly efficient PA. Recently published results show PAs in the low GHz range with efficiencies greater than 80% [97, 98]. This chapter presents the winning PA implemented with a GaN HEMT transistor and having power added efficiency greater than 85%. It will be shown that CAD simulation tools, accurate device models and sensible design rules can produce first-pass PA design success. An overview of design, fabrication and testing processes is presented here together with measured results. The design was published in Microwave Magazine [18].

5.4.1 Design

The transistor chosen for this design was a 10W RF Power GaN HEMT from Cree (CGH40010). The transistor used is available in a screw-down package and is not internally matched. It comes with an accurate non-linear model which is critical for the design of high-efficiency PAs. AWR's Microwave Office software was used for the design of the amplifier. It is an integrated environment that allows the design and simulation of PCB or IC RF circuits as well as providing seamless connection to EM simulators such as Sonnet.

The design and modelling strategies employed are similar to that presented in [99], but were adapted to deal with a non-linear amplifier rather than Class-A. Instead of using multi-match software to synthesise the input and output matching networks, an input and load termination optimisation method was used to obtain the maximum power-added-efficiency and matching networks were designed around these components. At the heart of any efficient amplifier is a switch. The switching action results in output currents or voltages that resemble a square wave. While the PAE calculation is concerned with power at the fundamental (and hence harmonics should be minimised), these harmonics need to be present otherwise the current and voltage waves cannot exist in any other form than a pure sinusoid. Due to this, impedances at all harmonics up to the fifth were included in the input and output matching tuners.

The amplifier was designed without a specific class. The main concern was what harmonic impedances could be provided at the input and output of the amplifier in order to obtain maximum efficiency. To model the effect of different terminations at the input and output of the transistor, an optimisation routine was setup where the impedance (magnitude and phase) presented to the input and output for 5 harmonics was a parameter as well as the bias and drain voltage. Loose convergence tolerances were set in the Harmonic Balance simulator and the goals of the optimisation were set to greater than 85% PAE with greater than 6 Watts output power at 1.2GHz. The efficiency generated by this method was 88% at 1.2GHz with an output power just above 6 Watts.

The next step is to take the ideal components (impedance tuners) at the input and output of the transistor and turn them into real matching networks made up of transmission lines and capacitors. The transistors are bilateral in this configuration so a change of output impedance affects the input impedance and vice versa. One of the advantages of using this method allows the input match to be designed with the out-

put matched in a condition that achieves high efficiency (i.e. with the ideal matching network). This reduces the amount of time re-optimising the input match as the output match is changed. As time was limited, a trial and error approach was used to transform the ideal impedance tuners into real matching networks. In the future, an automated method that takes the parameters from the source and load tuners and creates the matching networks could be employed. The resulting input matching networks are shown in Figure 5.14.

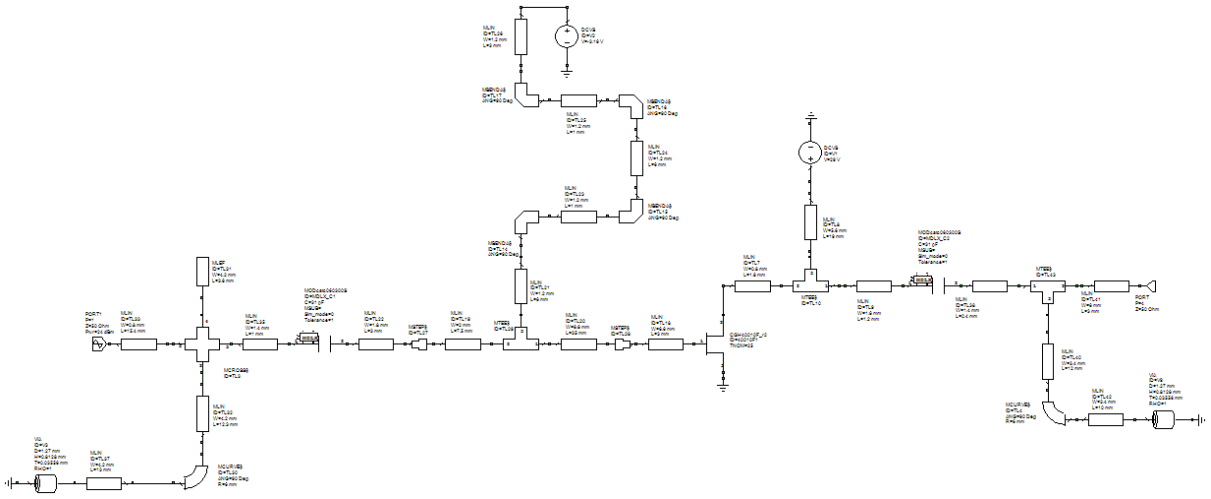


Figure 5.14: *Schematic for 1 GHz PA including transmission lines.*

As there are some significant steps in the matching networks, Sonnet was used to analyse them. Some of the reasons that this is needed are outlined in [100, 99]. This was done in four parts. Two EM networks were created for the input and two for the output. In order to have the ability to tune out any changes to the efficiency resulting from the enhanced modelling of the matching networks, the lines were shortened by approximately 5mm at each port and transmission line component was used. This allowed Sonnet to take care of any step and coupling effects and the variable transmission lines in the schematic are used to tune out any differences. Only one EM simulation was needed for each network taking a few minutes to simulate and providing a more accu-

rate model.

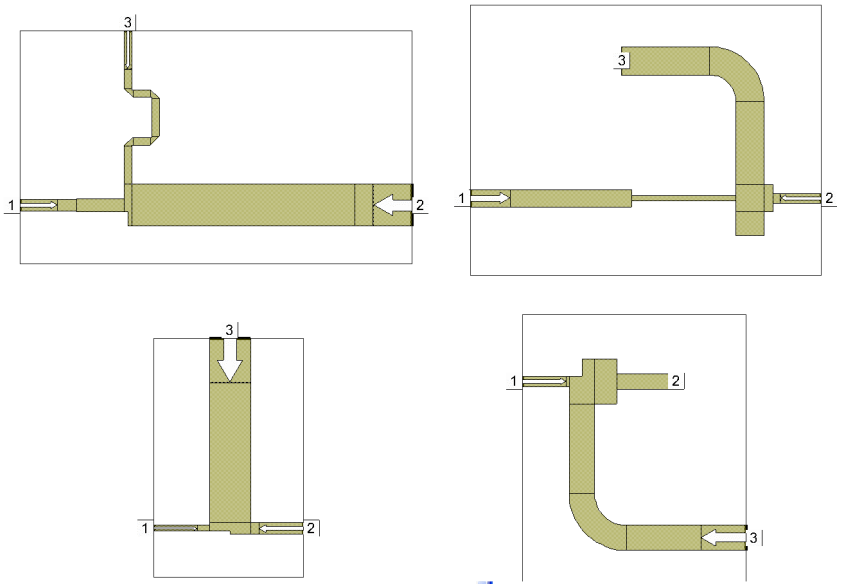


Figure 5.15: *Matching networks modelled in Sonnet.*

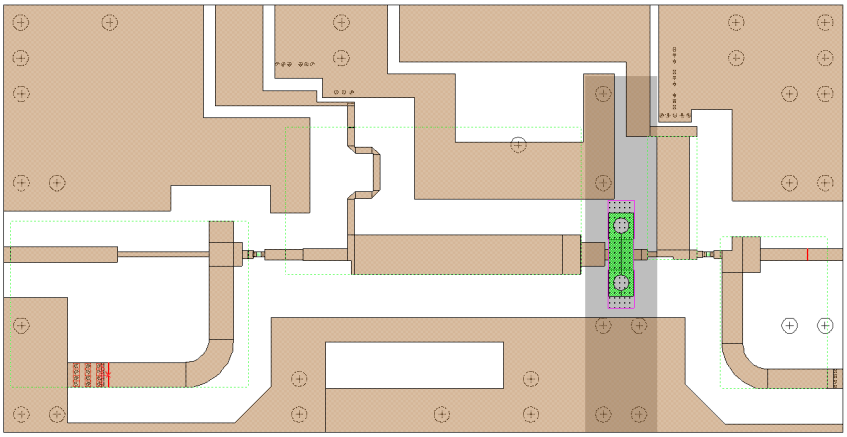


Figure 5.16: *Final layout for the amplifier.*

5.4.2 Results

The efficiency and output power levels were extremely close to specification especially across the frequency desired for this design. A slight error in the calibration shows the measured PAE to be slightly higher than that measured at the competition. The

simulated output current and voltage waves are shown in the figure below. It appears, due to the voltage peaking that this amplifier is operating in a quasi-F-1 mode. It is likely that there is a portion of class-E operation as well due to the output capacitance within the device and the capacitance added by the packaging. As mentioned in [101], "it is difficult to determine the class unless the output current and voltage waves can be directly measured".

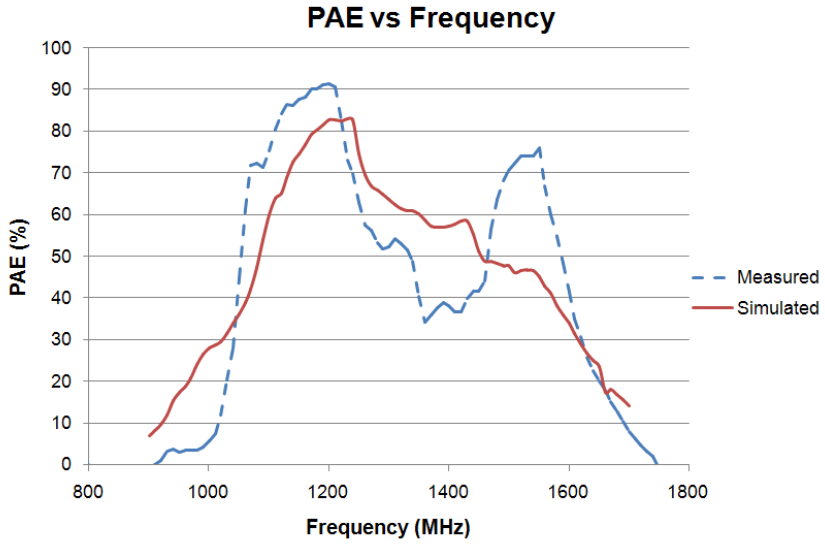


Figure 5.17: *PAE vs. Frequency*

The amplifier is shown in Figure 5.21, it achieves an efficiency of 85%.

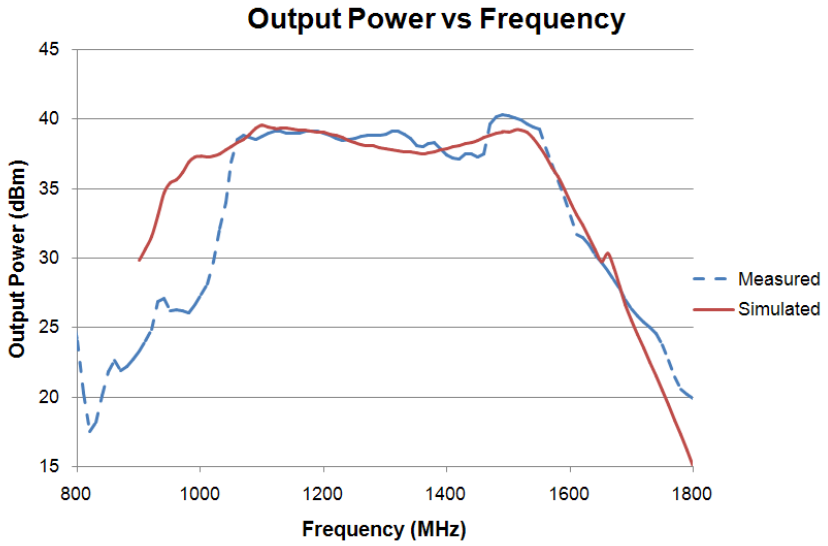


Figure 5.18: *Ouptut power vs. frequency.*

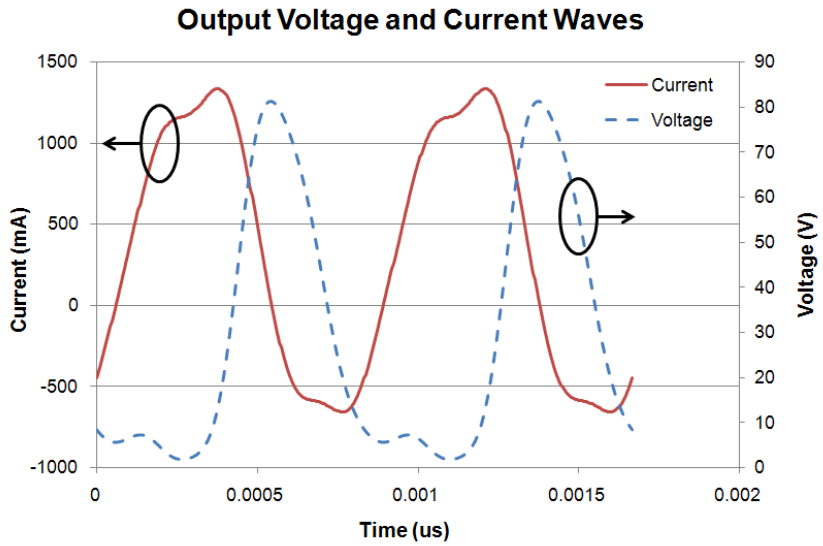


Figure 5.19: *Output voltage and current waves.*

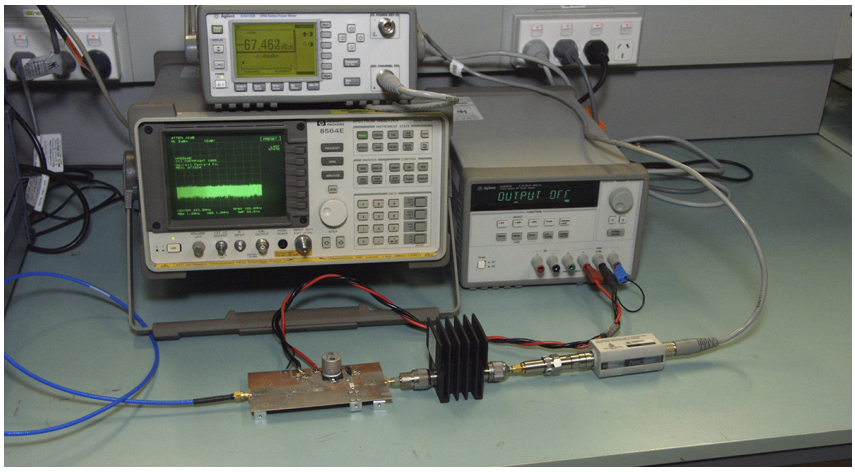


Figure 5.20: *Testing a prototype at Macquarie University (photo courtesy of Professor Anthony Parker). The board is implemented using a Rogers substrate.*

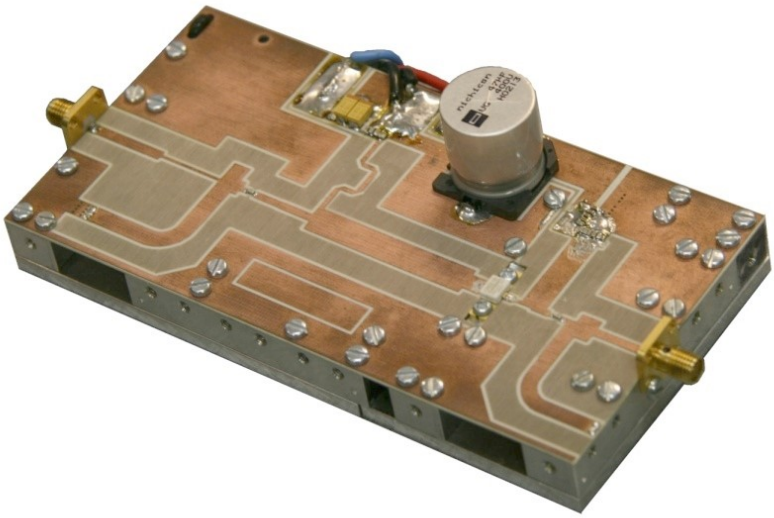


Figure 5.21: *Photo of the finished amplifier. The board is implemented using a Rogers substrate.*

5.5 A 60 GHz Transmission Line PA

This section outlines the design of a PA for the first GLIMMR transmitter. The PA is designed using 0.18 µm SiGe from Jazz Semiconductor.

The PA consists of 5 stages. A cascode input stage provides 8dB of gain. The final 4 stages are common-emitter amplifiers biased in Class A. Inter-stage matching is carried out using transmission lines and capacitors. The large-signal power gain for the PA is 30dB, it has a 3dB bandwidth of 11.5GHz, centered at 58GHz.

Each bias stage consists of a quarter wavelength transmission line connected to a current source, fed using a 4-bit current-mode DAC. The nominal DAC value is set for maximum gain and can be programmed to output current down to zero allowing the PA to be switched off if needed. The bias networks are cascaded and loadable via a serial control port.

The characteristic impedance for the bias lines was chosen to minimise RF loss and provide maximum isolation. Capacitors are used at the end of the bias lines for RF grounding. The transistors in the PA have three base and two emitter fingers. This configuration minimises the transit time of electrons between the emitter and collector while maintaining a large emitter area [96]. Using maximum (10.16um) sized fingers (for this process) in the output stages means that the parasitics in the feed structure can be kept to a minimum (fewer transistors are needed for the same effective emitter length).

Mismatch in a PA contributes to low efficiency, a worsened VSWR, higher die temperature for the same output power and is the cause of many other undesirable effects.

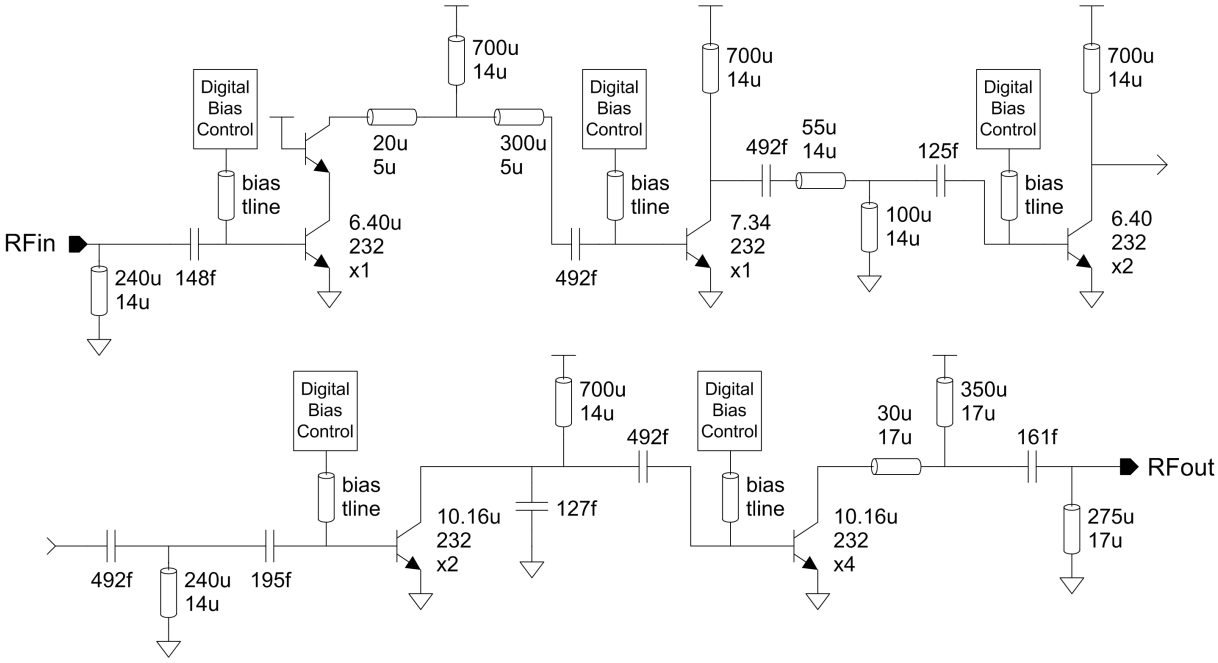


Figure 5.22: *Block diagram of the SiGe PA.*

It is not valid to match a PA using small signal S-parameters as the input and output characteristics of a HBT change under large-signal conditions. Matching must be done under large signal conditions using a Periodic Steady State (PSS) or Harmonic Balance (HB) simulator.

The problem with PSS and HB simulations is that they are time consuming when compared to an S-parameter analysis. A method was developed to counter this, it allows matching networks to be evaluated and optimised quickly; it is described in the following paragraphs.

For each stage of the design a frequency-domain large signal model of the transistors input impedance with matched output, and output impedance with matched input was created (as the transistors are bilateral in this configuration, mismatch on the output changes the input impedance and vice versa).

The approach is shown in Figure 3. Transistor 1 is to be matched to transistor 2. Circuit 3 is used to model the output impedance of transistor 1. It is generated using an optimisation routine, programmed in visual basic, (within Analog Office) that minimises the mean square error between the real and imaginary components of the large-signal impedance looking into Zout for circuit 1 (Ar) and circuit 2 (Am). The same method is used to model the input of transistor 2 with circuit 4.

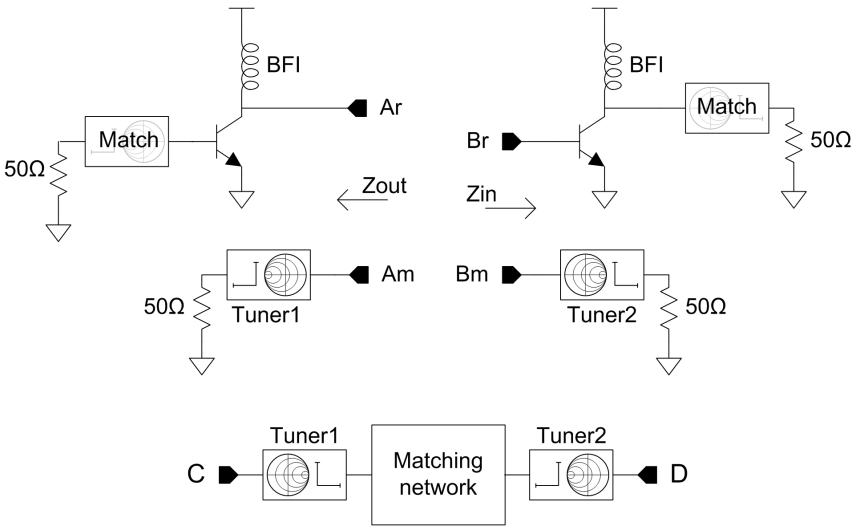


Figure 5.23: *A method proposed for matching high power devices.*

By creating these impedance models' we can determine the absolute effect of the matching network. To get the best performance out of the PA it is now a process of minimising the loss of the network with a simple simulation instead of undertaking a large-signal analysis of the whole amplifier.

On a stage-by-stage basis we can optimise the inter-stage match and see how it contributes to the overall frequency response of the PA. The matching networks were optimised using a gradient descent method for low loss (maximum gain). Other factors which were considered were tolerance to manufacturing parameters and low frequency stability. The output stage was optimised for maximum power transfer using

the load-pull wizard in AWR's Analog Office.

All the transmission lines in the PA are shielded micro-strip type with fixed shield and adjustable width, except for the output stage which employs micro-strip lines. Micro-strip lines are used in the output stage as they provide a lower DC resistance for the same characteristic impedance (a 50ohm micro-strip is 17um wide as opposed to 14um for the shielded type). The output match is the most critical [93].

Attention was focused on the design of each transistor's feed network. The two critical aims are reducing resistance in series with the base and reducing the base-to-collector capacitance. The resistance in series with the collector while not as critical, must be made as small as possible as it reduces the voltage available to the transistor. A distributed R+C+CC circuit for each transistor was extracted using Calibre (Mentor Graphics) within the Cadence layout environment.

The PA occupies an area of 0.870 x 0.930 mm^2.

5.5.1 Layout

The layout of the output stage transistor is shown in Figure 5.24. The input and output reference planes are highlighted in red. Within this boundary parasitic RC extraction is used. Outside this boundary, EM models are used.

The layout for the full PA is shown in Figure 5.25. The quarter wave transmission lines and bias DACs are on the bottom. The interstage and input / output matching are at the top.

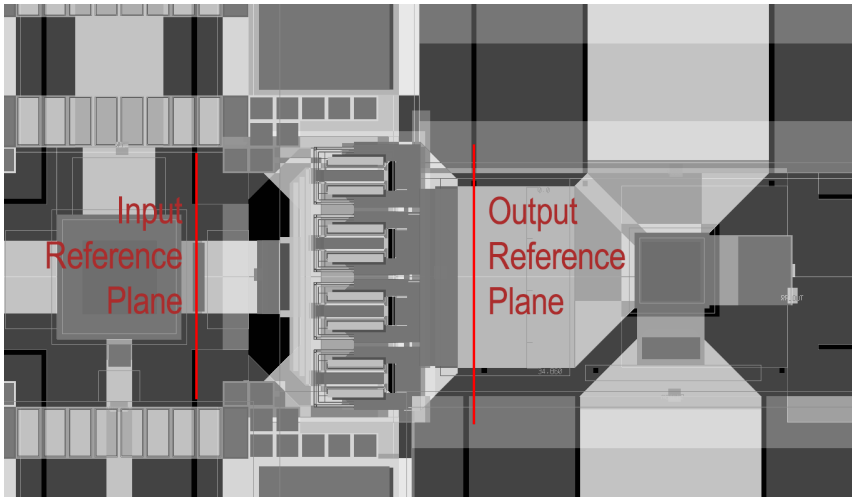


Figure 5.24: *Layout of the output stage transistors.*

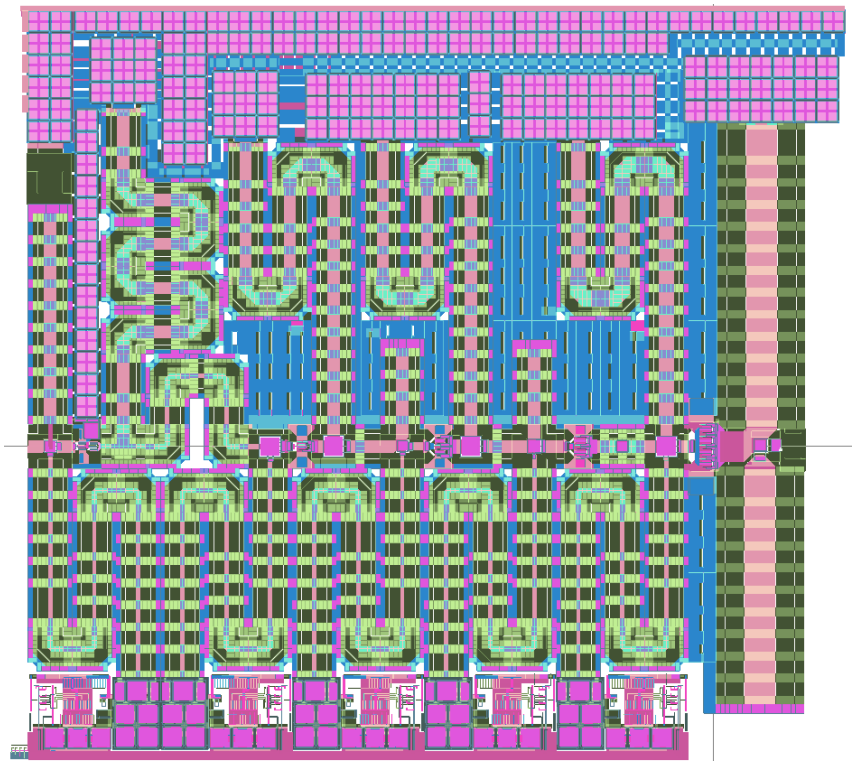


Figure 5.25: *Layout of the PA.*

5.5.2 Measurements

A summary of the PA performance is shown in Table 5.1. The bias of the PA is controlled using a digital bias block adjustable from 0 to 15. The bias settings for each stage are shown in the graphs e.g. _66776_ and they correspond to the bias setting for each stage. The optimal bias for peak f_{max} occurs around value 7.

Parameter	Units	Measurement
Gain	dB	25-30
S22	dB	<-10
S11	dB	<-10
Psat	dBm	12-13
p1dB	dBm	8-9
Power	mW	385

Table 5.1: *Measured results of GTC2 PA.*

Figure 5.26 shows the power gain of the PA over frequency. The design is well matched to the 60 GHz band and has a flat response. By adjusting the bias settings, the gain of the PA can be changed. The current consumption ranges from 214mA to 273mA from a 1.8V supply.

The PA input and output match are shown in Figures 5.28 and 5.27. Both the input and the output of the PA are well matched to 50 ohms. The output is better than -10dB across the band and the input is better than -15dB.

A comparison of the PA simulation results to measurement results is shown in Figure 5.29. This graph shows the close match between simulation (black curve) and measurement (red curve) across the frequency range from 20 GHz to 64 GHz. The input and output match also show similar characteristics between measurement and simulation.

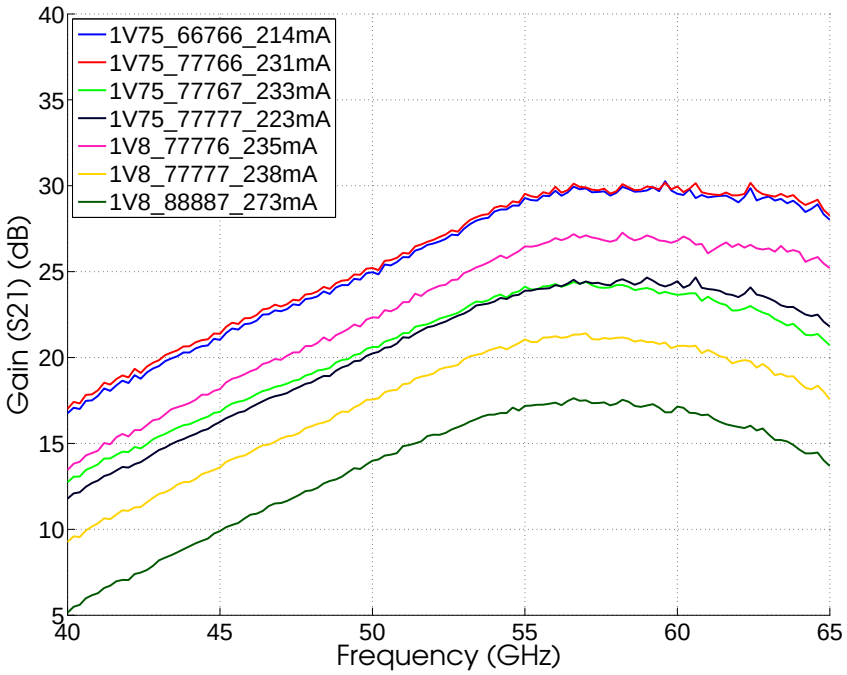


Figure 5.26: *GCT2 PA gain plot.*

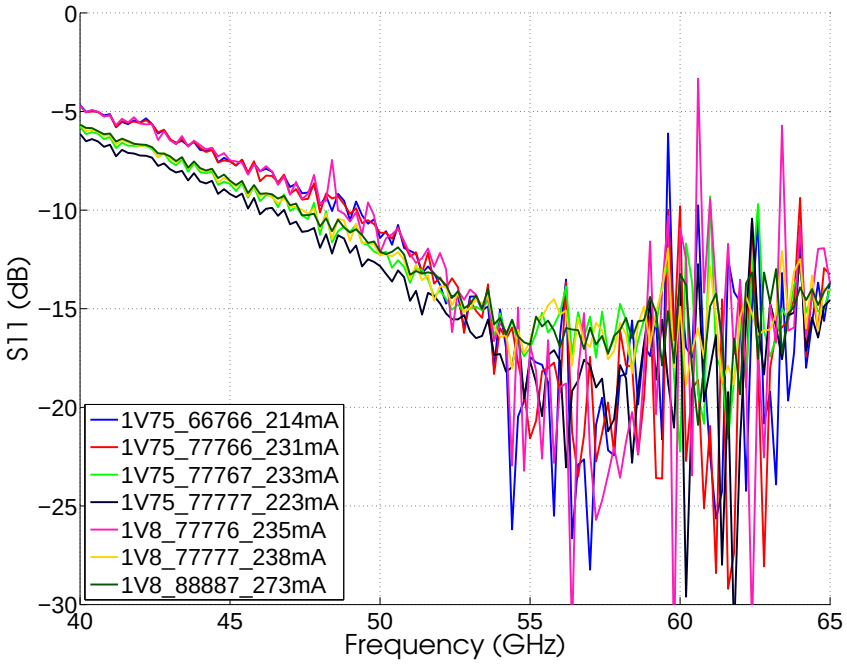


Figure 5.27: *GTC2 PA S11 plot.*

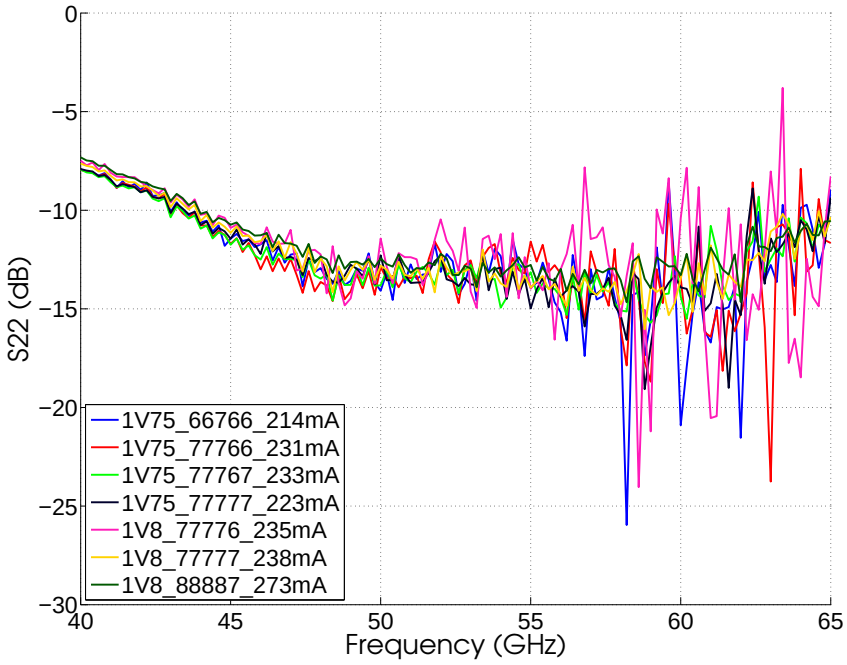


Figure 5.28: *GTC2 PA S22 plot.*

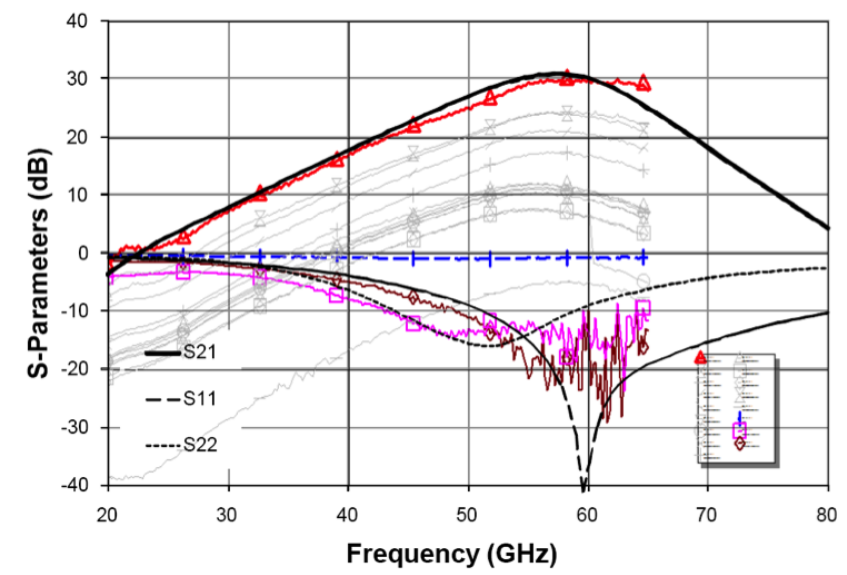


Figure 5.29: *GTC2 PA measured vs simulated plots (apologies for the poor graph).*

5.5.3 Discussion

A die micrograph of the PA is shown in Figure 5.30. The PA achieves 25-30dB of gain, output saturation of 12-13dBm a 1dB compression point of 8-9dBm. The PAE at 1dB compression is only 2.1%, at Psat the PAE is 5.2%. The area for this PA is also large, if it was to be integrated in a phased array nearly 1mm^2 would be needed for each PA. In the following two sections, two transformer based designs are shown which achieve higher efficiency and utilize much smaller area.

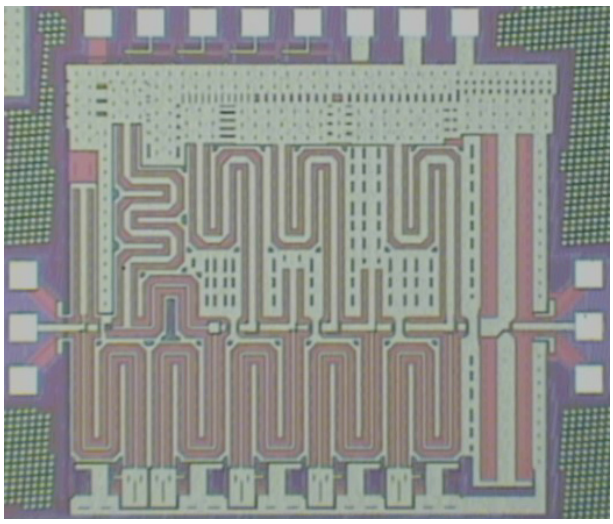


Figure 5.30: *Die photo of the implemented PA. Die size is approximately 1mm x 1mm.*

5.5.4 Testing the PA

The PA was tested using a probe station. The DC signal was provided with DC probes from the top, the input and output were measured with GSG probes. A picture showing the test setup is shown in Figure 5.31.

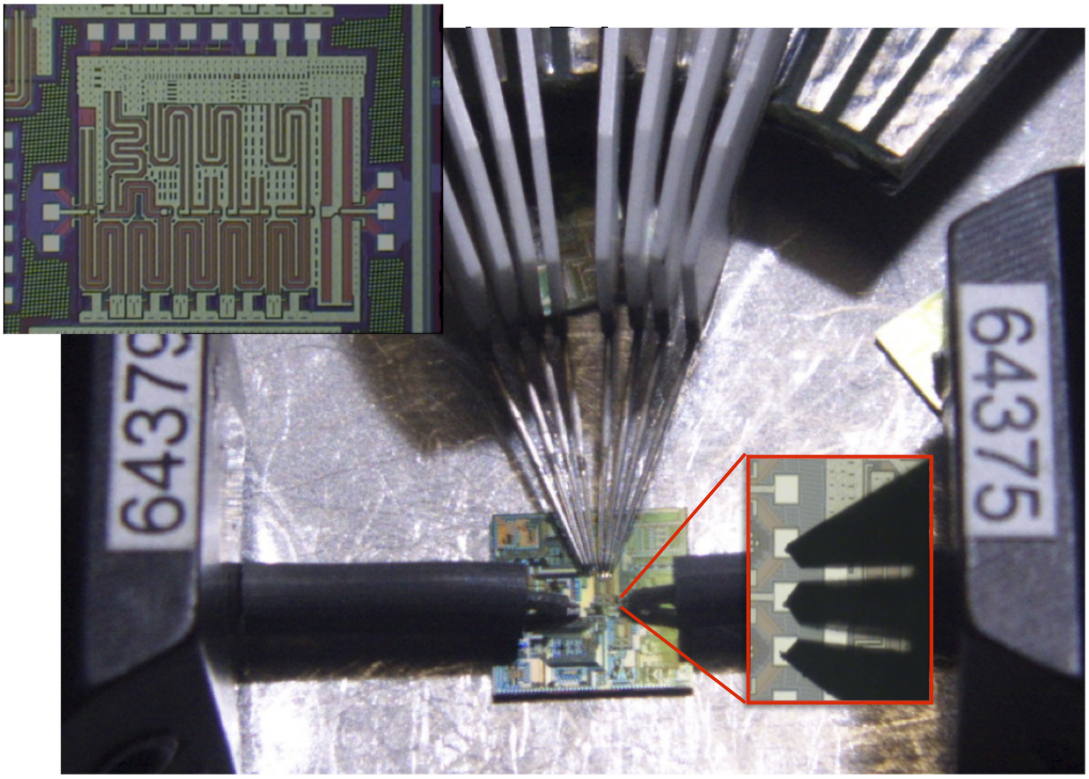


Figure 5.31: *Photo of GTC2 PA test setup at Macquarie University (photo by Professor Anthony Parker).*

5.6 Summary

This chapter presented a design methodology for RF designs from low frequency to mmWave which is based on three core aspects. 1) Accurate device models and optimisation, 2) an RC extraction for small interconnect much smaller than the on-chip wavelength, and 3) EM modelling and optimisation of passive devices. A flow is outlined for amplifier design which uses simple models to optimise performance followed by more accurate models later in the design.

The design flow was used to design two PAs. The first design was a low frequency, high efficiency design which achieved an efficiency better than 88% at 1 GHz. Achieving such high efficiency requires extremely accurate modelling and design. The second design was a 60 GHz transmission line PA which also matched simulation results closely.

6

60GHz Transformer Coupled PAs

6.1 Introduction

Published 60 GHz amplifiers typically fall into three different categories; transmission line based [90, 88, 89], lumped element based [102, 86] and transformer based [91, 87]. Transmission line amplifiers use typical MMIC design strategies and benefit from a well defined current return path. This aids accuracy; the tradeoff is the large area which these designs generally require. Lumped element and transformer based designs facilitate smaller layouts with the requirement of better modelling and design methodology to get close agreement between simulated and measured performance. In the case of differential designs, transformers are preferred as they allow a much

simpler layout.

With a large number of antennas in a phased array, the output 1dB compression point for each individual amplifier can be relaxed. In this type of system, the most important parameters to consider are power added efficiency (PAE) and the gain provided by each stage. High PAE is desired in order to decrease the system power consumption. Gain is required to amplify the low power output from the up-conversion mixer. Having a high gain per stage reduces the number of stages needed in the amplifier.

Two transformer based PAs for 60 GHz applications are presented in this chapter. These designs show that transformer based PAs can achieve high performance while using a much smaller area than their transmission line based counterparts. The first design, a four stage transformer coupled PA designed in 0.18 µm SiGe achieves the same performance as the transmission line design presented in Chapter 5, with a reduction in area of 4x and power. The second design, also a four stage design but in 65nm CMOS, achieves the same area saving and achieves a state of art efficiency of 7.7% at 1dB compression [20].

6.2 A 4-stage transformer based PA in 0.18 µm SiGe

In the second generation GLIMMR transmitter, there was a goal to reduce size and increase efficiency. The PA outlined in this section was used in GTC3-Tx and achieves better performance than the transmission line design, takes up one quarter of the area and uses transformers for input match, output match and inter-stage coupling. A comparison of the two PA layouts is shown in Figure 6.1.

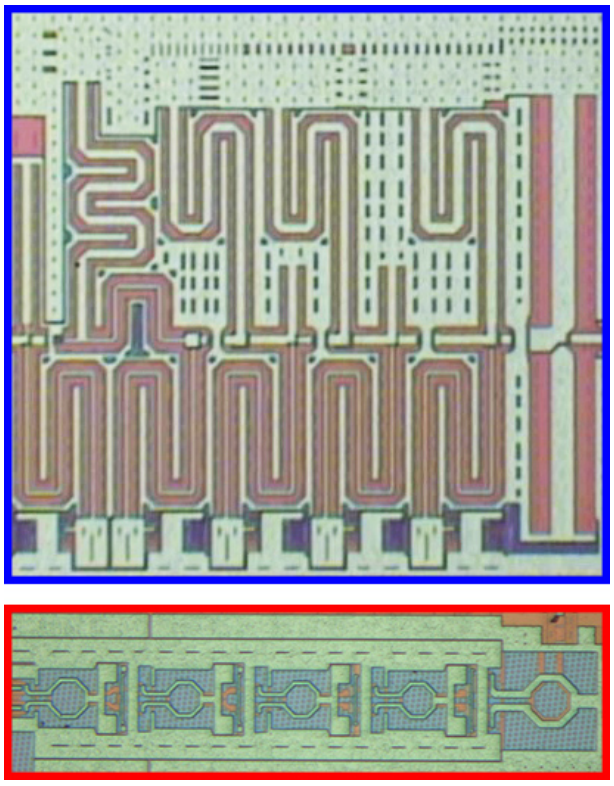


Figure 6.1: *Comparison of GTC2 (blue outline) and GTC3 (red outline) PAs*

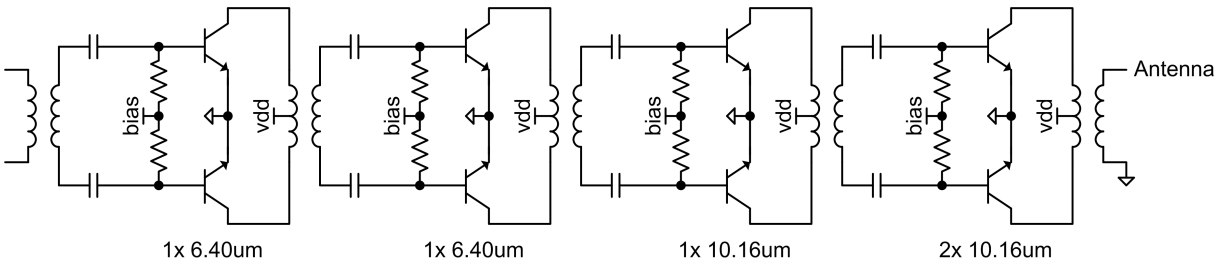


Figure 6.2: *Schematic of PA*

6.2.1 Specifications

The target specification for the PA is outlined in Section 4.3.2 and is repeated in Table 6.1.

		BB PGA	I/Q Mix	interface	splitter	IF amp	RF Mix	PA
Gain	(dB)	3	-2	-4	-12	12	-2	30
NF	(dB)	20	15	4	12	10	10	10
Op1dB	(dBm)	0	0	20	20	3	0	10
Cascaded Analysis								
Gain	(dB)	3	1	-3	-15	-3	-5	25
NF	(dB)	20	20.6	20.7	21.6	26.3	26.5	26.8
Op1dB	(dBm)	0	-4.1	-8.1	-20.1	-8.5	-10.8	9.5

Table 6.1: *Block level specifications and lineup for GTC3.*

6.2.2 Design

A four stage design was used to meet the gain requirement. A differential architecture is used and enables the output power of two devices to be combined using the output balun [87]. Interstage matching is provided with single loop transformers and series capacitors. The inclusion of the capacitor in the matching network adds another degree of freedom in the matching. The capacitors in this process are high-Q MIM capacitors. Bias is provided to transistors through the center of differential resistors at the device, it could also be supplied through the center-tap of the inter-stage transformer if series caps were not used.

A schematic of the design is shown in Figure 6.2.

The size of the transistors in each stage are scaled in order to achieve the best efficiency, the first two stages use 1x6.40um devices, the third stage uses 1x10.16um devices and

the output stage has 2x10.16um devices.

The design of the PA follows the design flow outlined in the previous chapter. 1) Accurate device models and optimisation, 2) an RC extraction for small interconnect much smaller than the on-chip wavelength, and 3) EM modelling and optimisation of passive devices.

For the last step, a scalable transformer model was created in HFSS. This was mapped to a parameterized equivalent circuit model in AWR and different radius, width and spacing was able to be swept.

The output of the device was matched using results from a load-pull simulation. An example load-pull curve is shown in Figure 6.3. In addition to peak output power curves, curves can be plotted for peak PAE at specific back-off which might be slightly different.

6.2.3 Layout

The layout of mmWave circuits is critical for the measured results to match simulation.

The input cascode stage is shown in Figure 6.4, the layout of the devices are done to minimise parasitics and meet electro-migration rules.

An inter-stage transformer is shown in Figure 6.5. The layout shows the overlapping loops, the well defined ground surrounding loop and reference planes between EM modelling and RC extraction.

The layout for the full PA is shown in Figure 6.6. The digital bias DACs can be seen

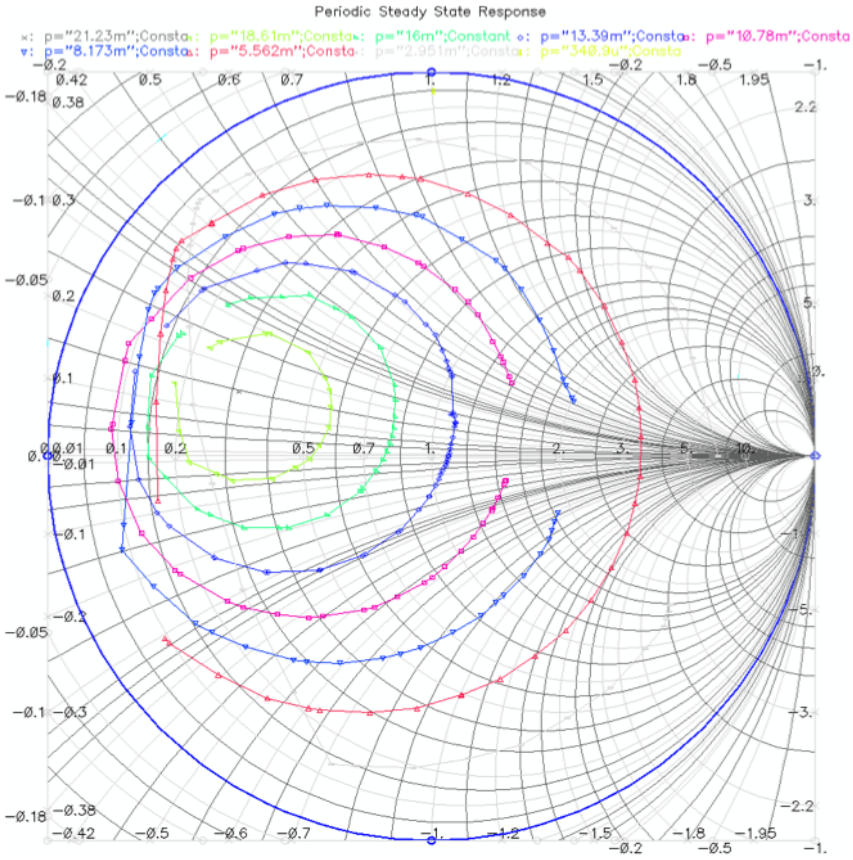


Figure 6.3: *GTC3 output stage load pull simulation.*

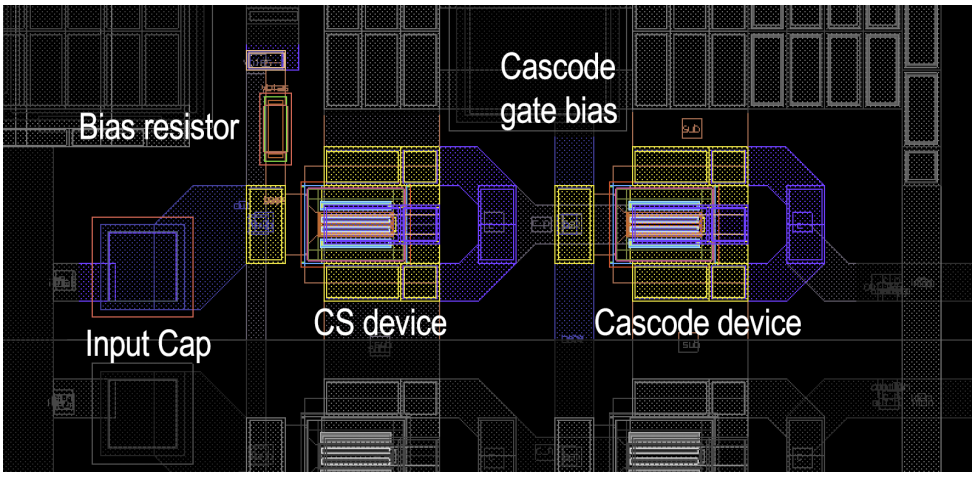


Figure 6.4: *GTC3 PA input cascode stage.*

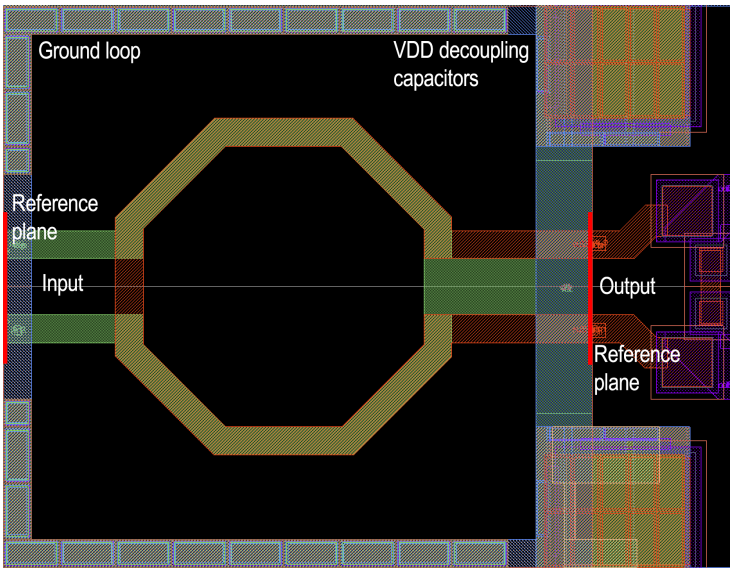


Figure 6.5: *Interstage transformer in GTC3 PA.*

along the top of the design, they supply a bias voltage to the base of the devices. A series of decoupling capacitors are used at the top and bottom of the PA. The metal cross-overs feed VDD into the center tap of the devices. The output uses a BALUN to convert the differential signal to single ended. The output transformer uses wider metal turns for low loss.

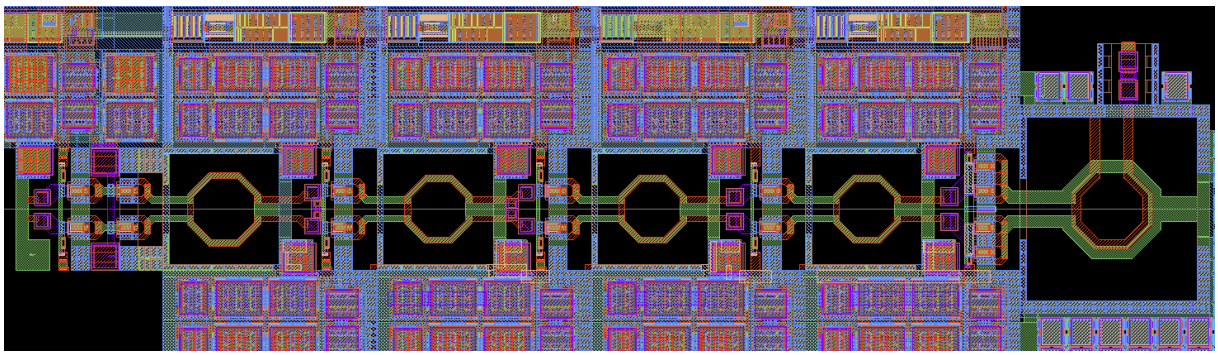


Figure 6.6: *GDS of GTC3 PA.*

6.2.4 Measurements

A standalone test structure shown in Figure 6.7 is used to test the PA. The test-structure is matched to 50Ω at the output. The input is matched to the output of the IF amplifier. To enable simple testing a single-ended to differential balun is used.

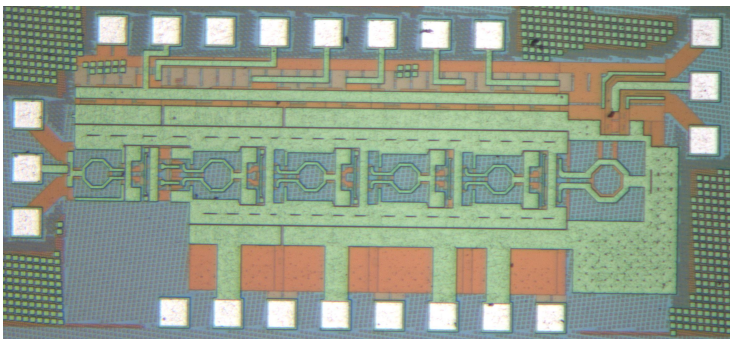


Figure 6.7: *Standalone PA for testing. Approx 1.1mm x 0.5mm.*

The PA is measured using a 67 GHz VNA. GSG probes calibrated to a CS-5 substrate are used to probe the input and output ports. The PA bias is controlled using an Arduino controller, the source code can be found in Appendix B.

The output of the PA is well matched, it achieves better than -10dB across the 802.11ad band (57-64GHz). The gain of the PA is better than 25dB across the same band. The output match (S22) can be seen in Figure 6.9 and gain (S21) in Figure 6.8.

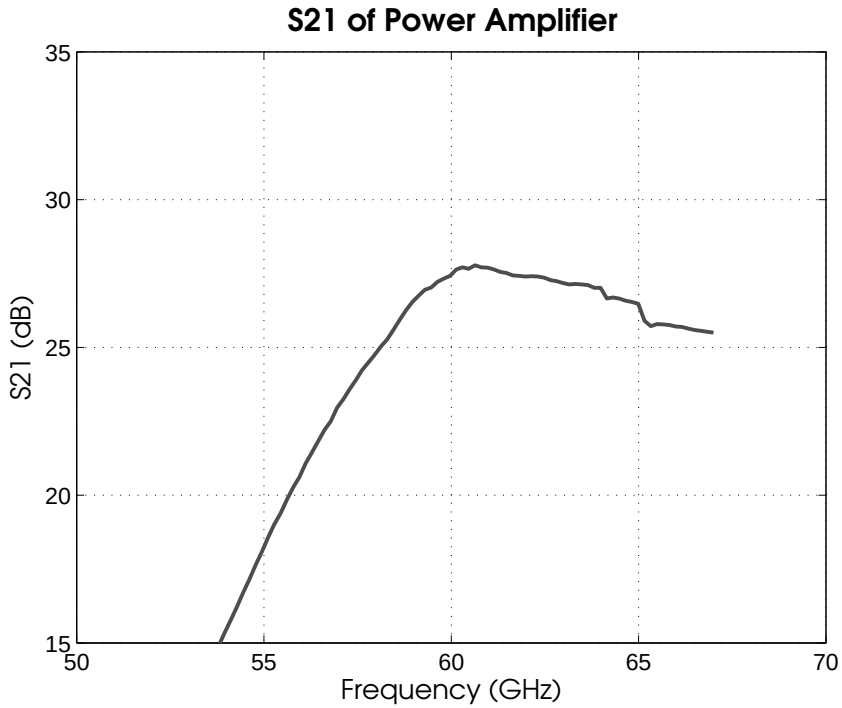


Figure 6.8: *Gain of PA*

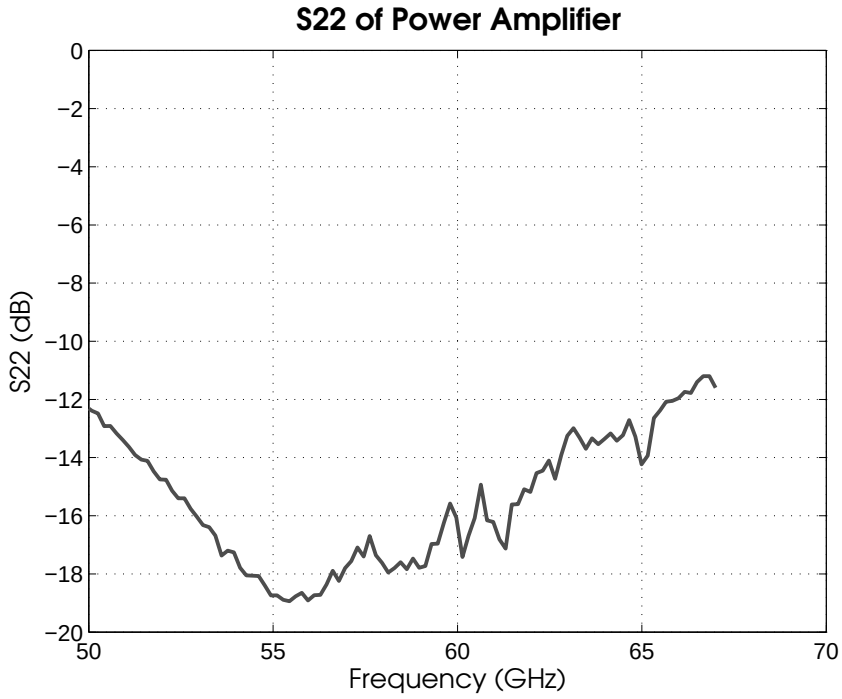


Figure 6.9: *S22 of PA*

6.3 A high efficiency 3-stage transformer coupled power amplifier in 65nm digital CMOS

A second transformer coupled power amplifier is presented in this section. In this design, a similar approach is taken to the SiGe PA presented in the previous section. In addition to using transformer coupling, neutralisation is used to boost the Gmax of the differential pair. The PA is designed in 65nm digital CMOS and achieves a high efficiency with a three stage design.

6.3.1 Methodology and implementation

The most important aspect of mmWave design is a structured design flow and a methodology that enables repeatable, first-pass correct design success. At the heart of the design flow is accurate transistor and passive models along with an accurate parasitic extraction engine.

The amplifier presented in this paper was designed using the BSIM4 transistor model with RF enhancements based on [103]. Passive devices were simulated in HFSS and mapped to a custom wide-band equivalent circuit model using Microwave office and Matlab. Post-layout parasitic extraction was done to capture interconnect and via parasitics. As the interconnect is very small compared to the wavelength at 60 GHz this lumped approach can be used.

6.3.2 Amplifier topology

A differential transformer based topology was chosen for a number of reasons. Compared to the transmission line approach, it saves a lot of area. Compared to the lumped element approach, it makes for a much easier and compact layout. The schematic is shown in Figure 6.10. Differential circuits are preferred over single-ended circuits as they possess greater immunity to common mode noise and have a well defined virtual ground which simplifies modelling. A differential topology splits the output between two transistors. If a single-ended output is desired, this power can efficiently be combined using a BALUN like in this design.

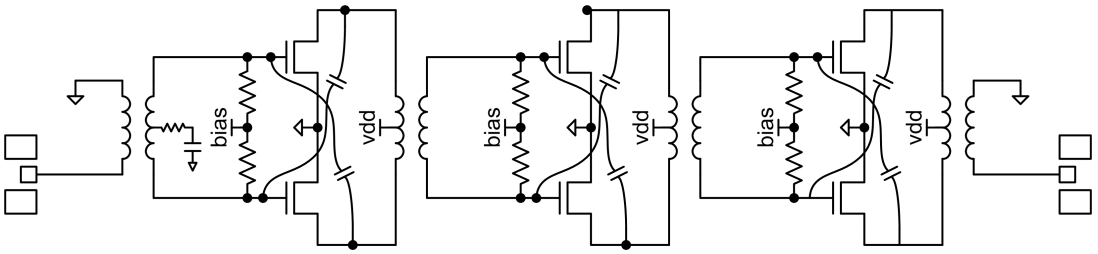


Figure 6.10: *Block diagram of the transformer-coupled CMOS PA.*

6.3.3 Transistor size and layout

Sizing the transistors for a mmWave amplifier is a tradeoff between power handling capability and f_{max}. Below a certain width, the layout parasitics associated with the routing dominate; at larger widths the gate resistance is dominant. Simulation including the parasitic components leads to an optimal gate width of 1um. Transistors are placed using custom P-Cells which include routing up to the highest metal. The P-Cell is designed to reduce the gate resistance and inductance, reduce C_{gd} and resistance between the channel and tie-downs. A 20x1um finger NMOS placed in an island

surrounded by substrate contacts has been used as the unit cell in this amplifier. Transistors are sized 2 x 20 x 1um, 3 x 20 x 1um, 4 x 20 x 1um for the first, second and final stages.

6.3.4 Transformer design

Transformers are used throughout the amplifier. At the input and output they provide a single-ended to differential transformation. At the input stage the secondary turns (connected to the transistor gates) centre-tap is decoupled to ground through an RC filter to reduce the possibility of common-mode oscillation. Between the stages, the transformers are used as matching networks, to provide VDD to the drains and couple the signal from the output of the previous stage to the input of the next.

The transformers are modelled using HFSS. Parameterised multi-port s-parameters are extracted for several loop widths, radii and overlaps. These s-parameters are input into a custom software module that creates equivalent circuit models for Cadence, ADS and AWR MWO. No substrate shielding techniques are used however a multi-metal ground ring is implemented around each transformer. This ground ring ensures that any metal outside the transformer perimeter does not affect the performance; it also allows ground to be distributed through the circuit with low impedance. The Gmax for the transformer is extremely low, -0.5dB at 60GHz. The transformers are implemented using the top 2 copper layers (0.9um thick).

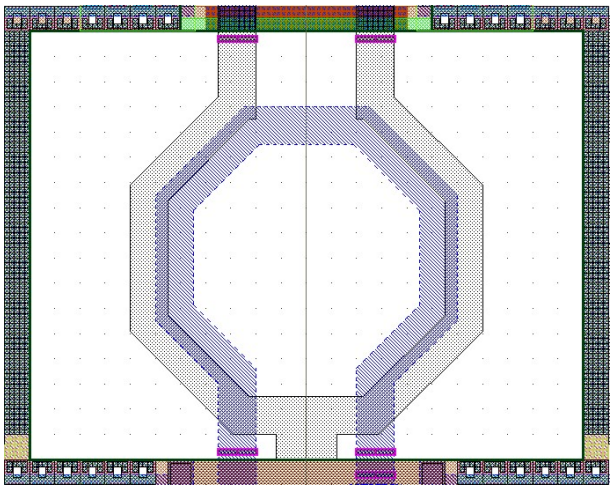


Figure 6.11: *Transformer design.*

6.3.5 Neutralisation

Common-source amplifiers at mmWave frequencies often suffer from gain degradation due to drain-gate capacitive feedback. This capacitance across a voltage gain node is magnified by the gain of the stage. In addition, this capacitance can de-stabilize the amplifier.

At lower frequencies a cascode topology is often employed to reduce the effect of the Miller capacitance. At mmWave frequencies, the capacitance associated with the drain and source nodes often creates a pole which needs to be removed with a series inductance. This inductance adds area and in an amplifier with limited headroom the cascode topology is not practical.

Neutralisation is a technique that aims to negate or reduce the effects of the drain-gate capacitance. It has been demonstrated recently at 60 GHz in [91]. It is easily achievable in a differential amplifier as out of degree phase signals are available. The neutralisation is accomplished by feeding back some of the output of the positive stage to the

input of the negative stage and vice versa. The feedback is implemented using a metal plate capacitor and varies depending on the stage from 15-30fF. The neutralisation is only useful across a narrow frequency range. To ensure stability at low frequencies where the transistors have a large amount of gain, high pass elements such as transformers or series capacitors need to be used. At high frequencies the quickly rolling off frequency response of the amplifier aids stability.

Compared to other stabilization techniques such as series RC networks the neutralisation technique does not degrade the performance of the amplifier. The benefit of neutralization on the G_{max} of the transistor is shown in Figure 6.12.

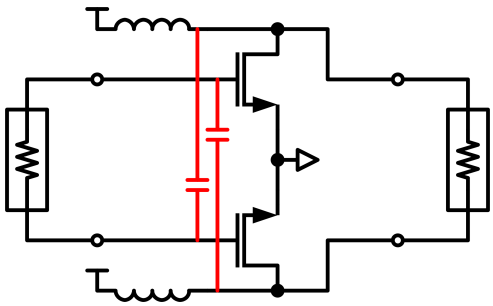


Figure 6.12: *Differential devices with neutralisation capacitors shown in red.*

6.3.6 Layout

The core of the amplifier (not including input balun which is only for testing) takes an area of 350um x 150um. The compact layout is due to the use of transformers through-out the design. Apart from the reduced cost, the small size also keeps routing between the transistors to a minimum improving performance and reducing the need for additional modelling steps.

The layout of the neutralized transistors is shown in Figure 6.14 and the layout of the

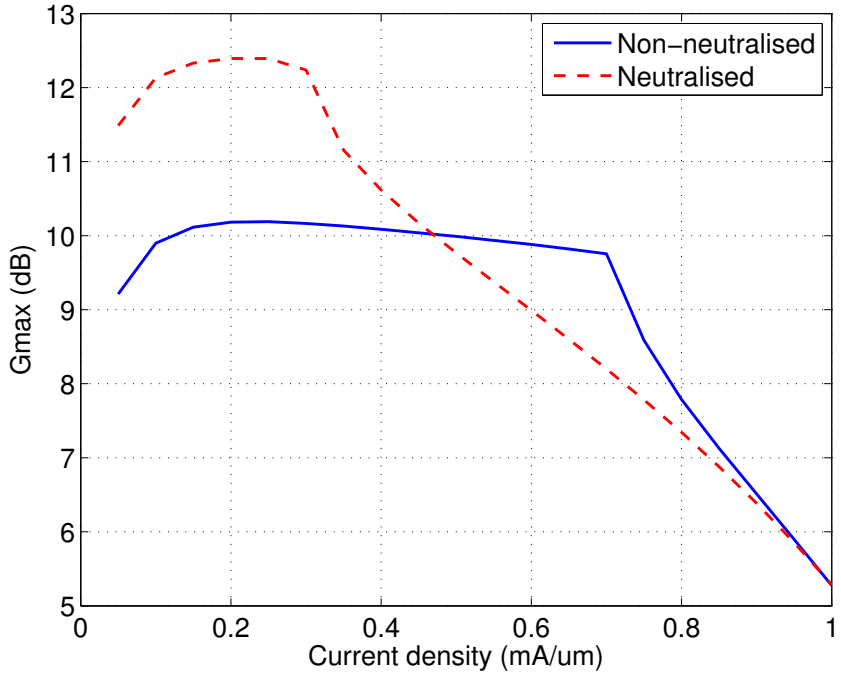


Figure 6.13: *The G_{max} for both a neutralized transistor and a common-source configuration is shown. The G_{max} of the transistor with neutralization is 2.5dB higher than without.*

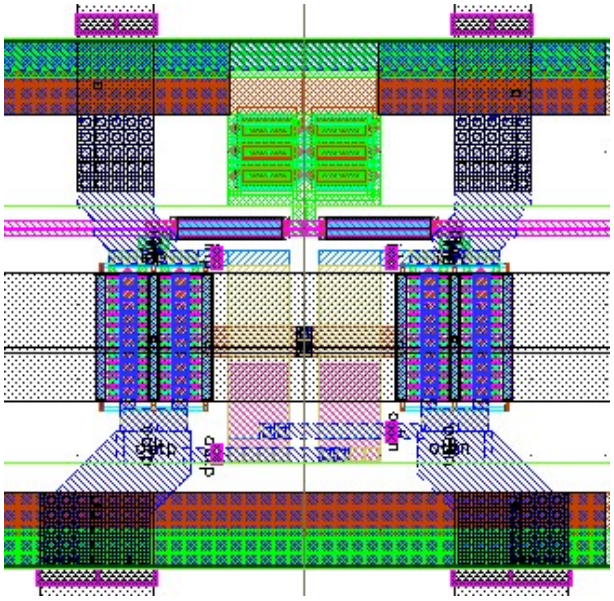


Figure 6.14: *Transitor layout showing neutralisation capacitors.*

entire amplifier is shown in Figure 6.15.

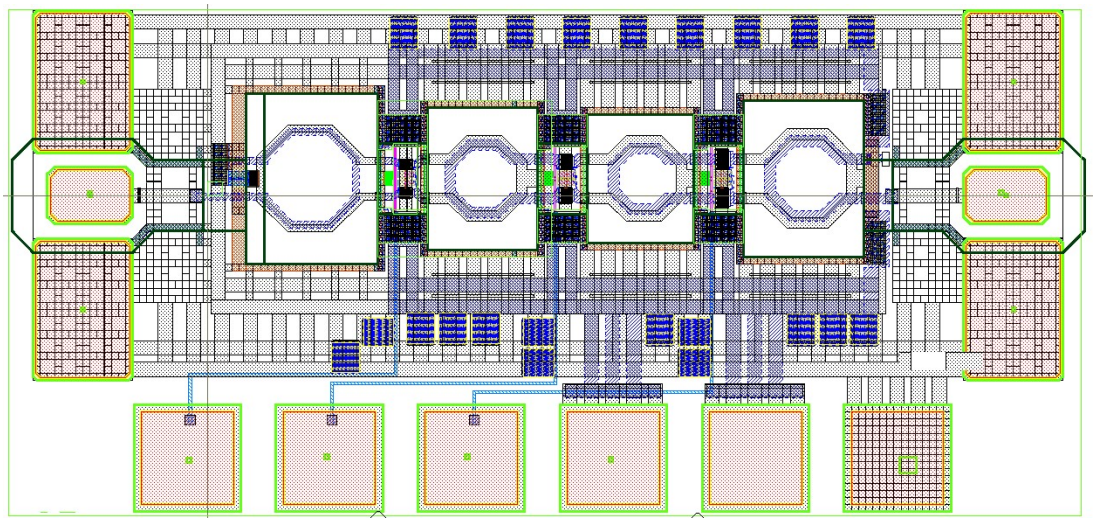


Figure 6.15: *Layout.*

6.3.7 Measurement Results

The amplifier presented in this section achieves a peak efficiency of 18% and a saturated output power of 10.5dBm (both limited by measurement). The gain is greater than 30dB from 61 to 65 GHz demonstrating the highest achieved gain per stage for any CMOS amplifier. The PAE at 1dB compression and 61GHz is 7.7%

Figure 6.16 shows the s21 of the amplifier across frequency for different temperature settings. The gates are biased with a constant voltage across temperature. With a temperature dependent bias network, the gain will be more constant across temperature.

Figure 6.17 shows the s22 of the amplifier and the output 1dB compression point of the amplifier across frequency and temperature is shown in Figure 6.18. The PAE is shown in Figure 6.19.

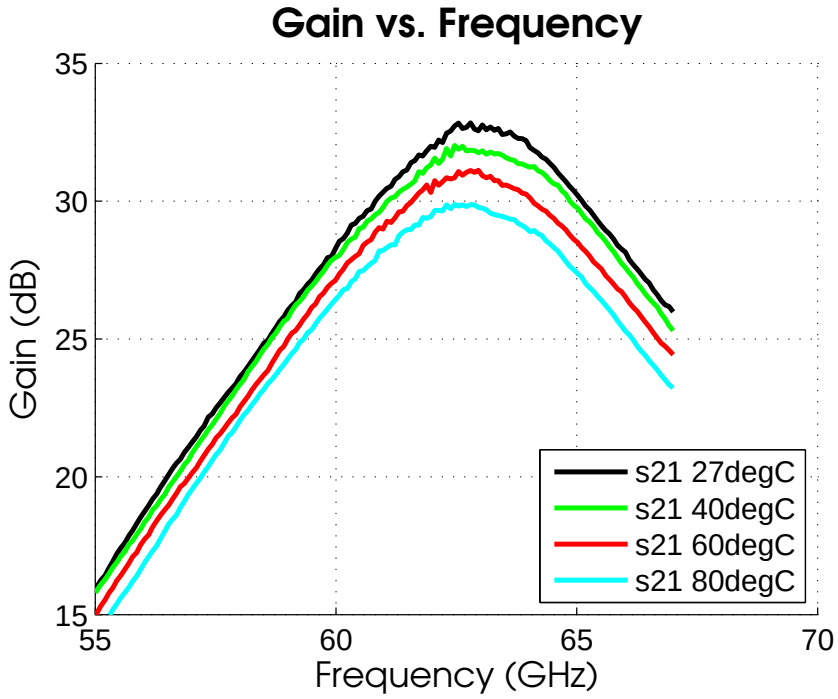


Figure 6.16: *Gain (S21) vs. frequency.*

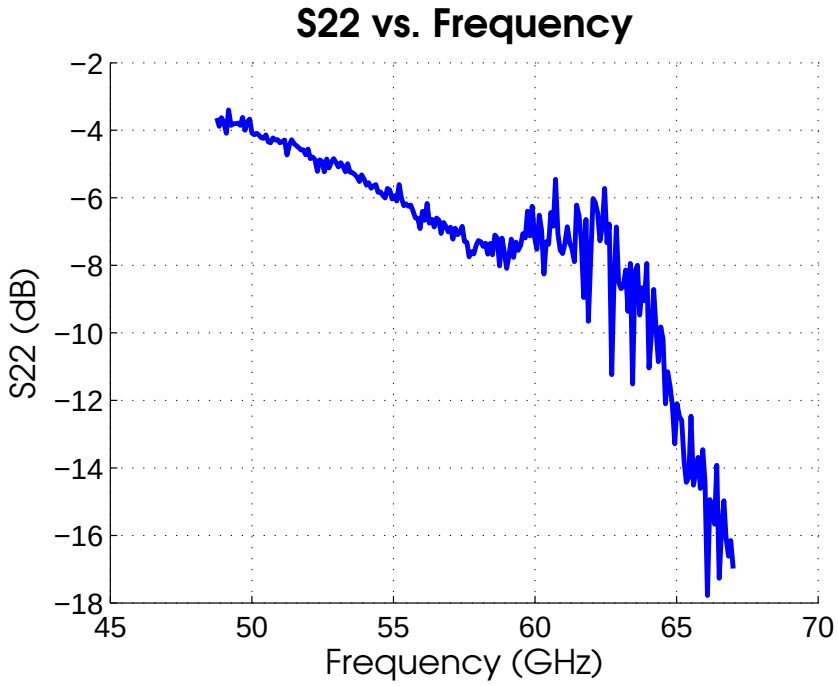


Figure 6.17: *S22 vs. frequency.*

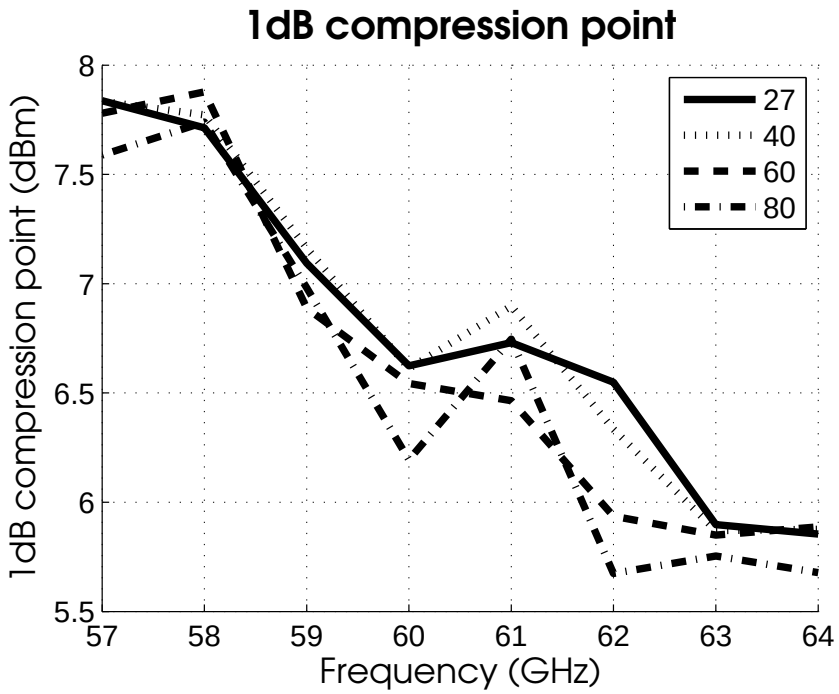


Figure 6.18: *Output 1dB compression point.*

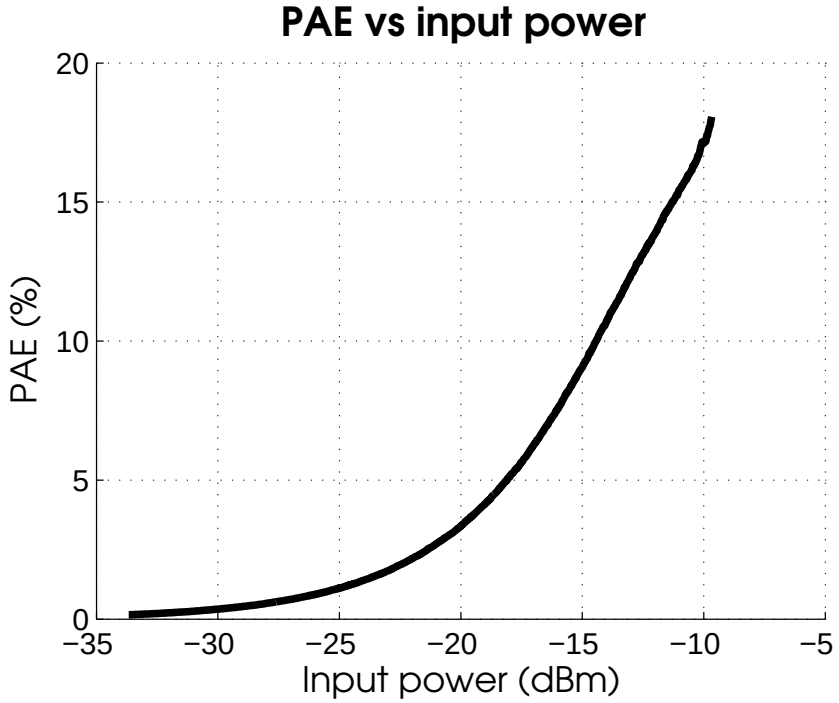


Figure 6.19: *PAE vs. input power.*

6.3.8 Comparison

Table 6.2 compares the amplifier presented in this chapter to other state of the art amplifiers published at the same time. In [86] a 3 stage L/C matched amplifier designed in 90nm CMOS is shown. This amplifier obtains a gain of 5.2 dB, showing the difficulty of designing 60GHz designs at 90nm node and PAE of 6.05%.

References [88, 89] and [90] all show power amplifiers at 60GHz which make use of transmissions lines for matching. The transmission line topoplogy typically results in a larger area and does not lend itself to a differential architecture. These PAs achieve a gain between 8 and 17 dB and peak efficiency up to 6.35%.

In [87] and [91] differential transformer coupled designs are shown. [91] shows one of the first neutralized designs at 60 GHz.

Ref	Year	Process	Stages	Topology	Pg	p1dB	Psat	Vdd	Pdc	PAE
[86]	2006	90nm	3	L/C	5.2	6.4	9.3	1.5	39.75	6.05
[87]	2008	90nm	2	xfmr	7.7	9.0	12.3	1	88	7.09
[88]	2008	90nm	4	tline	8.3	8.2	10.6	1.2	220	2.7
[89]	2008	90nm	3	tline	14.3	10.0	11.0	1.0	150	6.35
[90]	2008	90nm	3	tline	17	5.1	8.4	1.5	54	5.8
[91]	2009	65nm	3	xfmr	15.8	2.5	11.5	1	43.5	4.0
[102]	2009	45nm	3	L/C	19	7.9	1.2		6.4	
[20]	2010	65nm	3	xfmr	30	6.8	10.6	1	65	7.7

Table 6.2: *Comparison of CMOS power amplifiers, this work is shown in the last row.*

6.4 Summary

This chapter presented two transformer coupled PA designs at 60 GHz. The designs built on the knowledge and design methodology outlined in the previous chapter.

Transformer coupled power amplifiers provide several benefits. They occupy a small area, enable the output power from two differential devices to be combined into a single ended single at the output using a BALUN and reduce modelling complexity due to the well controlled virtual ground.

The SiGe PA was used in GTC3-Tx and the CMOS PA formed the basis of a design for the 40nm PA used in the Broadcom 60 GHz transceiver [22].

7

60GHz Transmitters

7.1 Introduction

This chapter outlines two transmitters designed for the GLIMMR project.

The first transmitter (GTC2-Tx) is a single chip sliding IF transmitter. This design is targeted for implementation in a mobile phone or small handheld device. It has only one transmit and one receive port and is not capable of beam-forming. It is suited for short range (within 1-2m) applications such as docking or desktop bus. Figure 7.1 shows a simple block diagram and target placement inside a phone. In this Figure, the RF chip is shown on the bottom right, it takes an analog I/Q signal as input and generates a 60 GHz output to drive an antenna. The author was responsible for

the transmitter design and the transmitter module design (excluding the bond wire antennas).

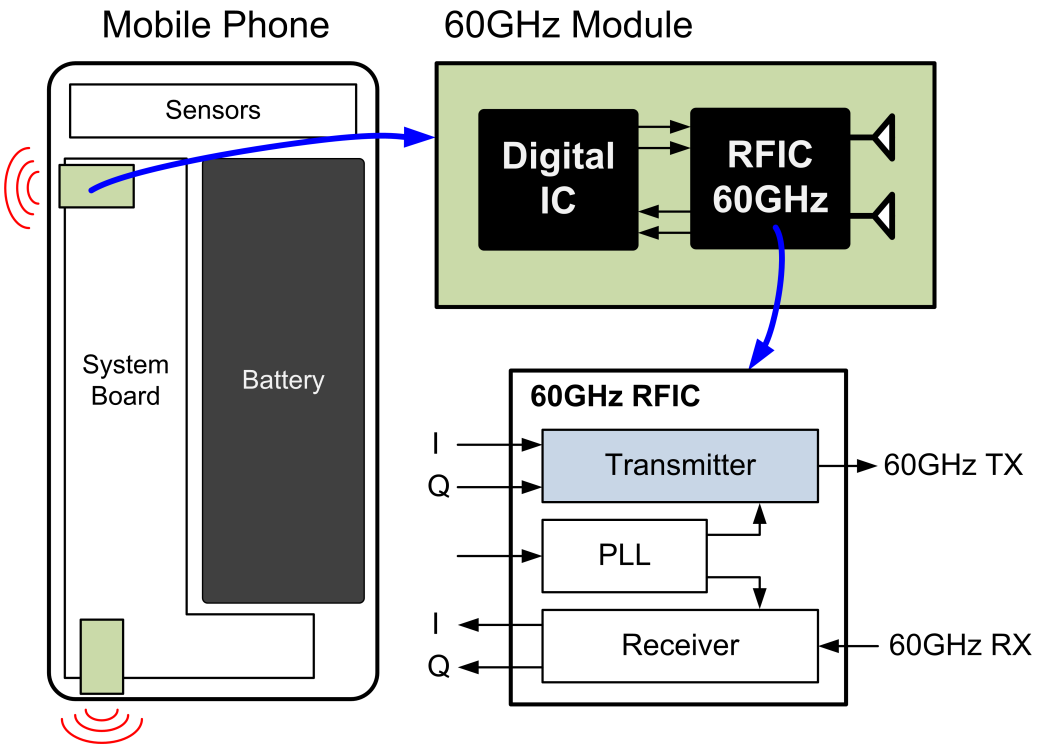


Figure 7.1: *A single chip implementation for 60 GHz and placement in mobile phones.*

The second transmitter (GTC3-Tx) is a novel, split sliding IF architecture which is designed to use a single coaxial cable between baseband and RF front-end module. The split is accomplished by using a 9GHz IF frequency and enables the baseband chip to be placed away from the RF front-end chip. The RF front-end is built in a modular fashion and several can be used together on a single module to form a phased array. Due to the multi-chip front-end architecture, an arbitrary number of antennas can be supported. The author was responsible for the transmitter and the high level architecture was a joint invention with Leonard Hall. This architecture is well suited for implementation inside a laptop or high powered router, and is shown in Figure 7.2.

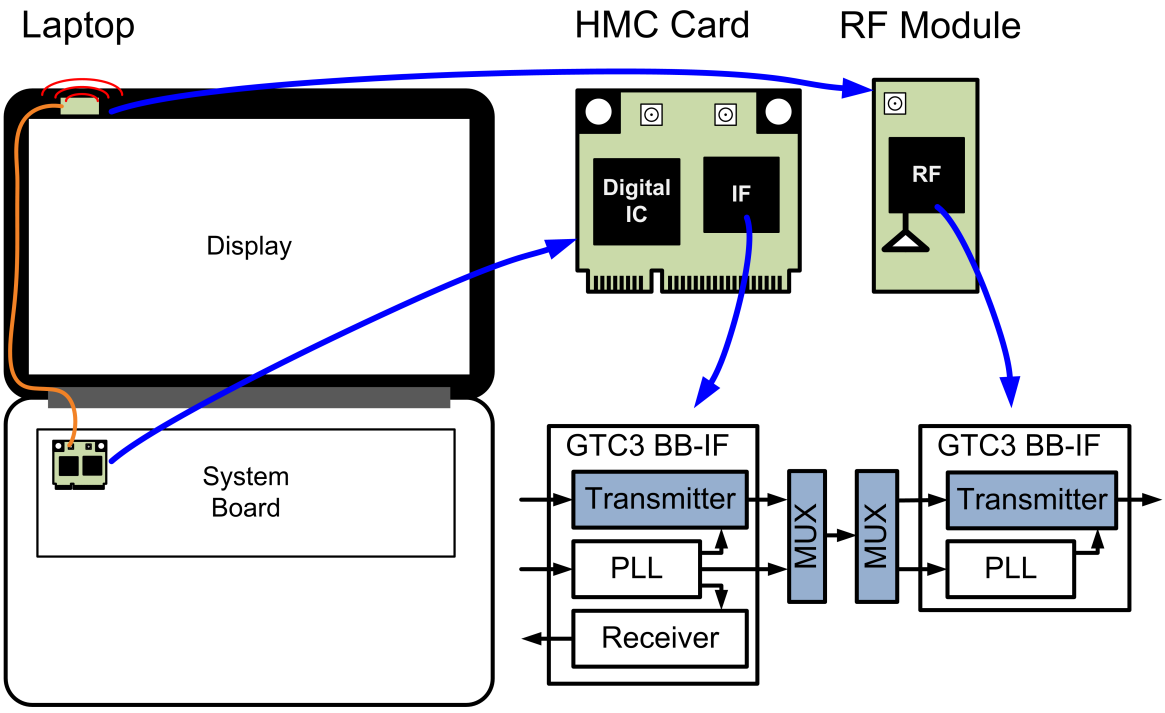


Figure 7.2: *A two chip implementation for 60 GHz and placement in laptops.*

7.2 GTC2-Tx: A 60 GHz +12dBm single-chip transmitter

7.2.1 Introduction

This chapter presents a simple sliding IF 60 GHz transmitter designed for the GLIMMR project (GTC2). The transmitter is implemented using Jazz Semiconductors' SBC18hxl SiGe process [104]. This process has 6 metallisation layers, MIM capacitors and planar inductors. An overview of the transmitter design strategy and simulation results is given in [19] and outlined below.

A high level block diagram of the 60 GHz GLIMMR transceiver is shown in Figure 7.3 with the author's contributions highlighted in blue.

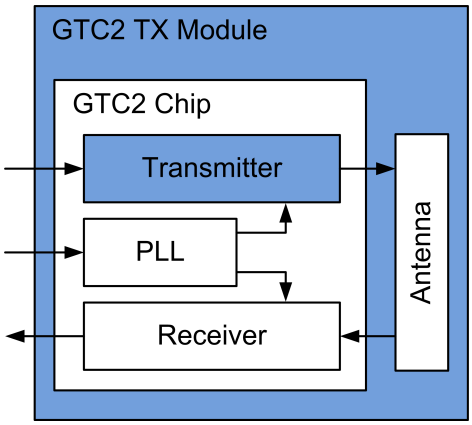


Figure 7.3: *Simple diagram of GTC2. The blue highlights show the work covered in this thesis.*

Link Calculation

This system is designed for short-range 1-to-1 operation or medium range 1-to-N operation.

Assuming a goal of 1 Gbps, transmit power of 9dBm (at p1dB point), losses to antenna of 2dB and 5dBi antenna gain the EIRP is 12dBm.

For a 1-to-1 implementation, 2Gbps can be achieved at just over 2 meters in an AWGN channel. Figure 7.4 shows the link margin (dB) vs. distance (m) for this configuration.

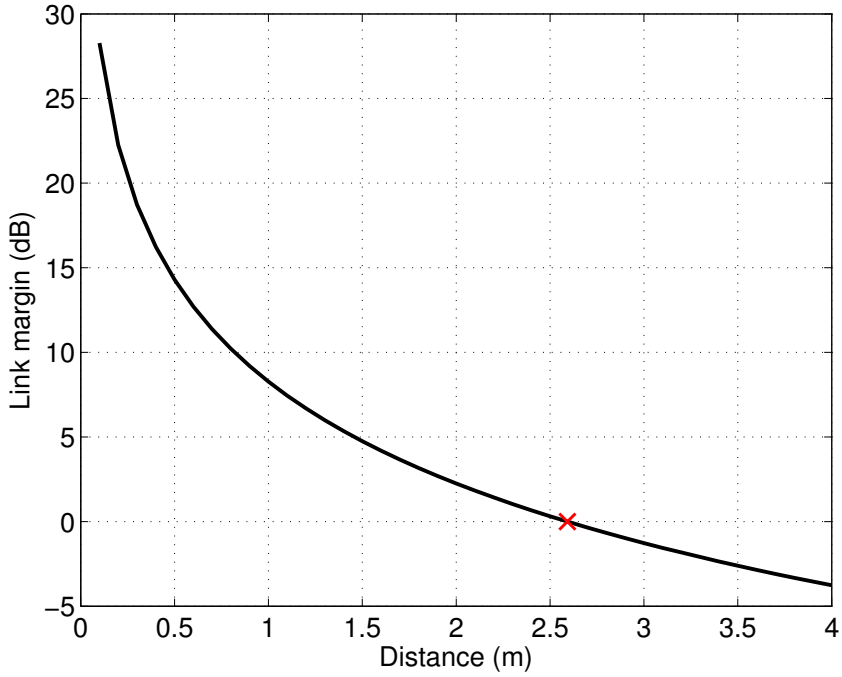


Figure 7.4: *AWGN link margin in dB versus distance for 1x1 QPSK 2Gbps link. TX EIRP 12dBm, antenna gain 3dBi each side, RX NF of 10dB, SNR requirement of 10dB.*

Specifications

The transmitter specifications are described in Section 4.3.1 and reproduced in Table 7.1.

		BB PGA (offchip)	I/Q Mix	IF amp	RF Mix	PA
Gain	(dB)	0	-3	10	-3	26
NF	(dB)	20	15	10	15	10
Op1dB	(dBm)	0	0	3	0	10
Cascaded Analysis						
Gain	(dB)	0	-3	7	4	30
NF	(dB)	20	21.2	21.7	21.9	22.0
Op1dB	(dBm)	0	-4.8	0.9	-4.2	9.7

Table 7.1: *Block level specifications and lineup for GTC2.*

7.2.2 Architecture

A sliding IF architecture is used for the transmitter, this offers some advantages over a direct-conversion system. For one, the generation and distribution of the LO signal is simplified. In this system, a 24GHz VCO is phase locked to an external 180MHz reference. The IQ mixer operates with an LO of 12 GHz which is obtained via a 24-12 GHz quadrature divider. The 48GHz LO for the second mixer is generated by a frequency doubler. The moving IF architecture simplifies the design of the frequency synthesiser and the high IF frequency reduces the need for image filtering as it is well out of the bandwidth of the transmitter (48GHz). A block diagram of the transmitter is shown in Figure 7.5.

7.2.3 Circuit design

7.2.3.1 Power amplifier

The power amplifier design is covered in more detail in Chapter 4. It consists of 5 stages. A cascode input stage provides 8dB of gain. The final 4 stages are common-

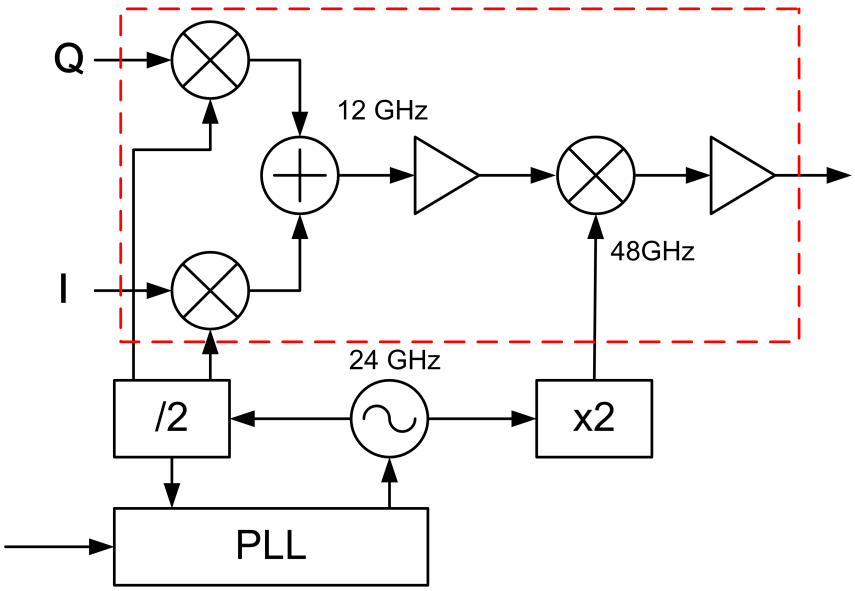


Figure 7.5: *GTC2 block diagram.*

emitter amplifiers biased in Class A. Inter-stage matching is carried out using transmission lines and capacitors. The large-signal power gain for the power amplifier is 30dB, it has a 3dB bandwidth of 11.5GHz, centred at 58GHz. Each bias stage consists of a quarter wavelength transmission line connected to a current source, fed using a 4-bit current-mode DAC. The nominal bias value is set for maximum gain and can be programmed to output current down to zero allowing the PA to be switched off if required. The bias networks are cascaded and loadable via a serial control port.

7.2.3.2 Baseband to IF Mixer

The first up-conversion stage employs an image-reject Gilbert cell mixer. To achieve infinite image-rejection the phase of the baseband (BB) I and Q signals must be perfectly quadrature and equal in amplitude. The LO must also have a 90 phase shift. Due to the tolerance and mismatch inherent in the manufacturing process this is not achievable. To maintain 25dB of image-rejection the phase error must be less than 5

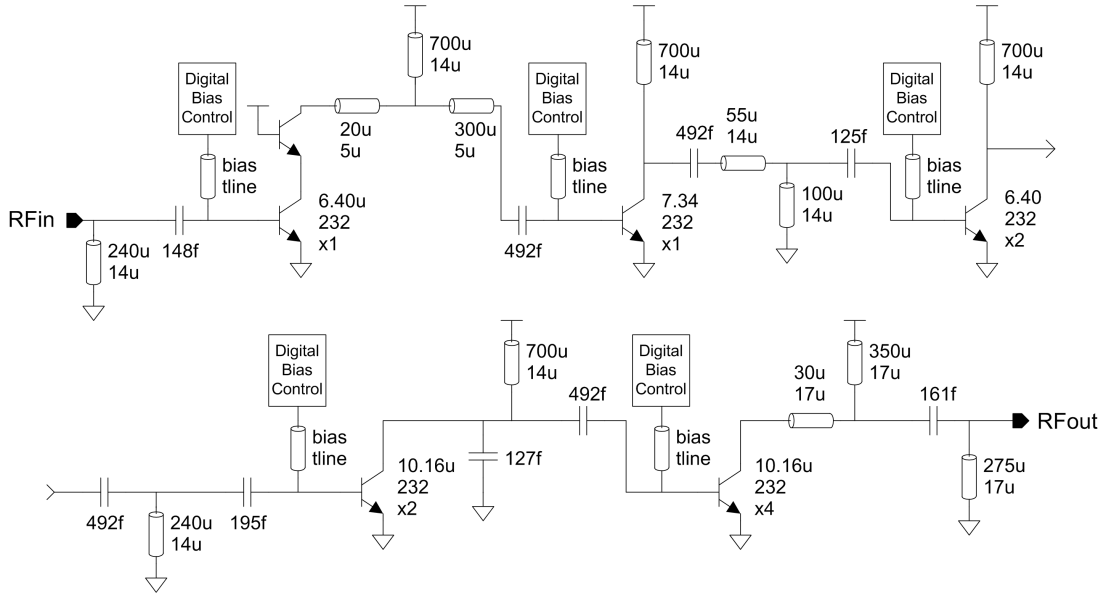


Figure 7.6: *Block diagram of* 0.18 µm *Jazz SiGe transmission line PA used in GTC2-Tx.*

and the amplitude error must be less than 5% [105]. Typically this is not obtained through analog matching and can be calibrated out using different methods, one procedure is outlined in [106].

The switching transistors are biased for maximum f_T. This results in a current density of approximately 1mA/um of emitter length. At this current density the transconductance stage would be twice the size of the switches in order to have the same f_T. However, they are sized 4x larger, this gives a lower noise figure and reduced gain which is optimal for the maximum 2 GHz input frequency. With sufficient LO drive the switching transistors act as ideal switches and do not contribute to the non-linearity of the circuit [107], the transconductance stage is the main non-linear element. To increase the linearity and reduce the gain, emitter degeneration resistors are used.

The transconductance stage is dc coupled to the input transmission lines. This allows the use of high value (1uF) off-chip capacitors for the BB signal or direct DC coupling. The input match is obtained using 100 ohm resistors between the differential signal

paths.

Inductors are used at the output. This keeps the voltage across transistors at an effective level, allows the output to be tuned to the 12 GHz IF frequency and matched to the following stage. As this design employs a moving IF, the low Q of the on-chip inductors is not a problem and allows a broadband match to be achieved. The inductors were chosen to resonate well away from their self resonant frequency (i.e. approximately 1/3 fsrf).

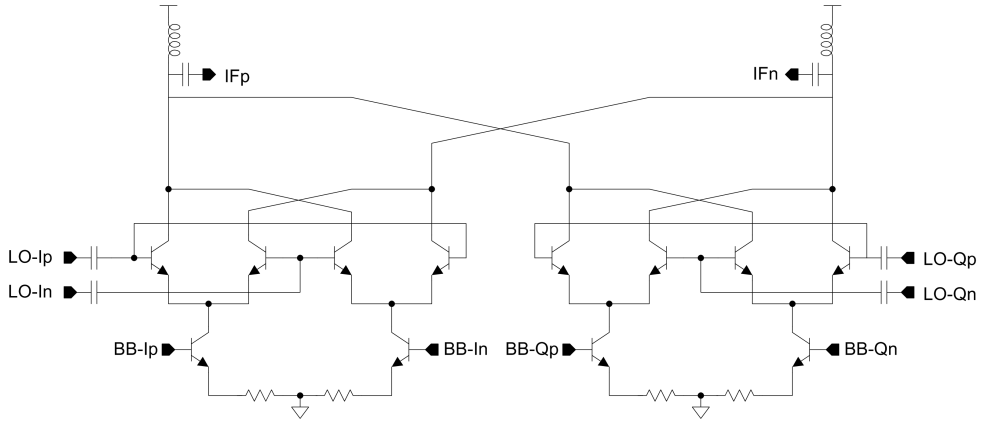


Figure 7.7: *Block diagram of SiGe I/Q mixer used in GTC2-Tx.*

7.2.3.3 RF Mixer

The second up-conversion mixer is a Gilbert cell with tuned input and output. The input is matched to the complex conjugate of the output of the previous mixer. The output is tuned to 50 ohms using a transmission line and capacitor as the passive balun (implemented by Leonard Hall) that follows this mixer was designed with 50 ohm single-ended ports.

The image for this mixer is centred around 36 GHz. The tuned output stage attenuates this signal. In the future a notch filter at 36 GHz will be employed to reduce this image

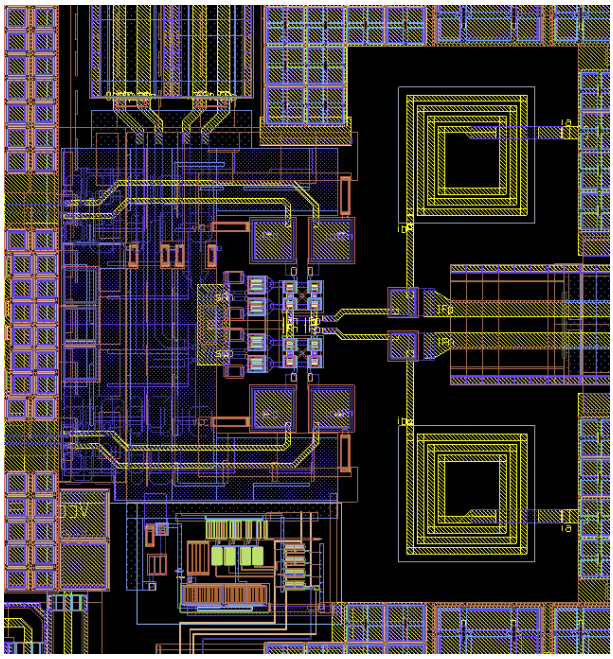


Figure 7.8: *Layout of the I/Q mixer*

further.

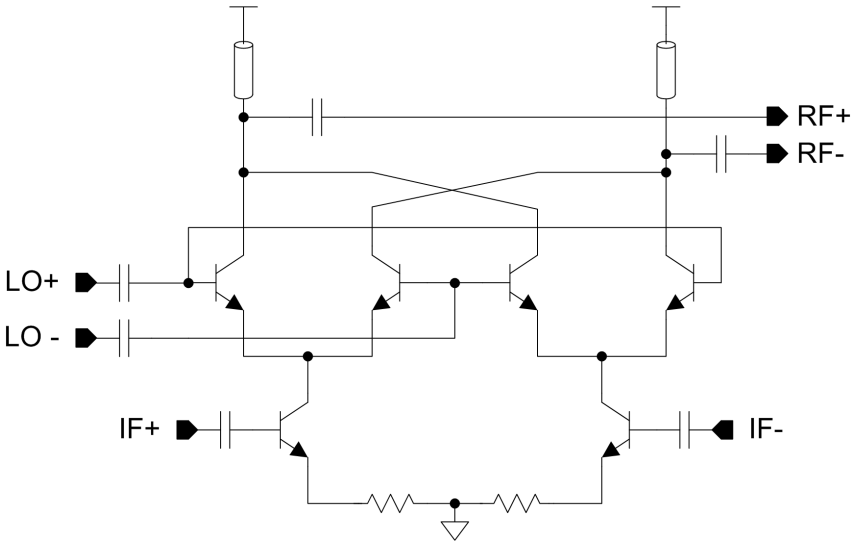


Figure 7.9: *Block diagram of SiGe RF mixer*

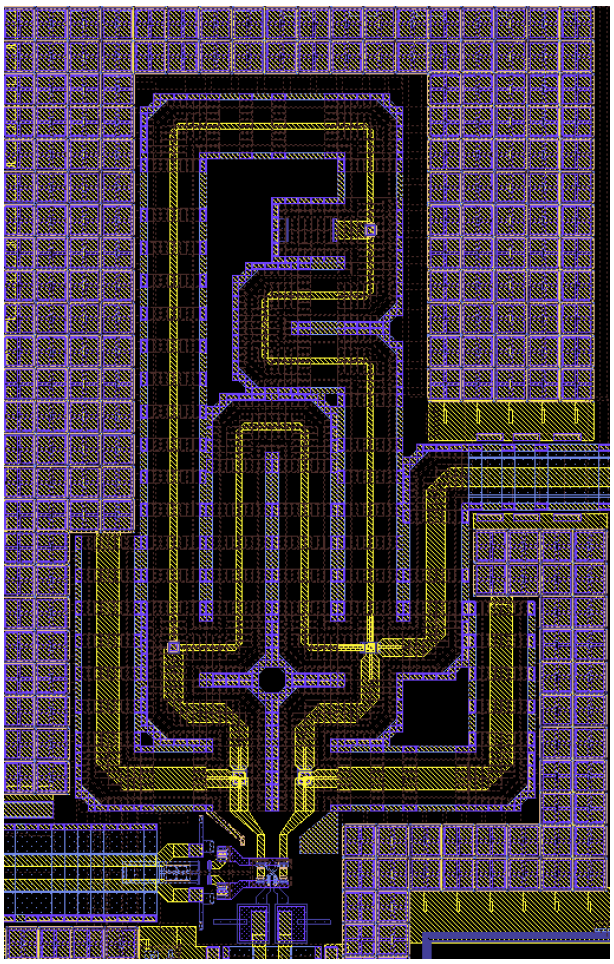


Figure 7.10: *Layout of the RF mixer. The output balun is a transmission line design implemented by Leonard Hall.*

7.2.4 Layout

The layout of the transmitter is shown in Figure 7.11. The pins are taken to one edge as the design was located on a multi-project wafer (MPW) and was not able to be sub-diced.

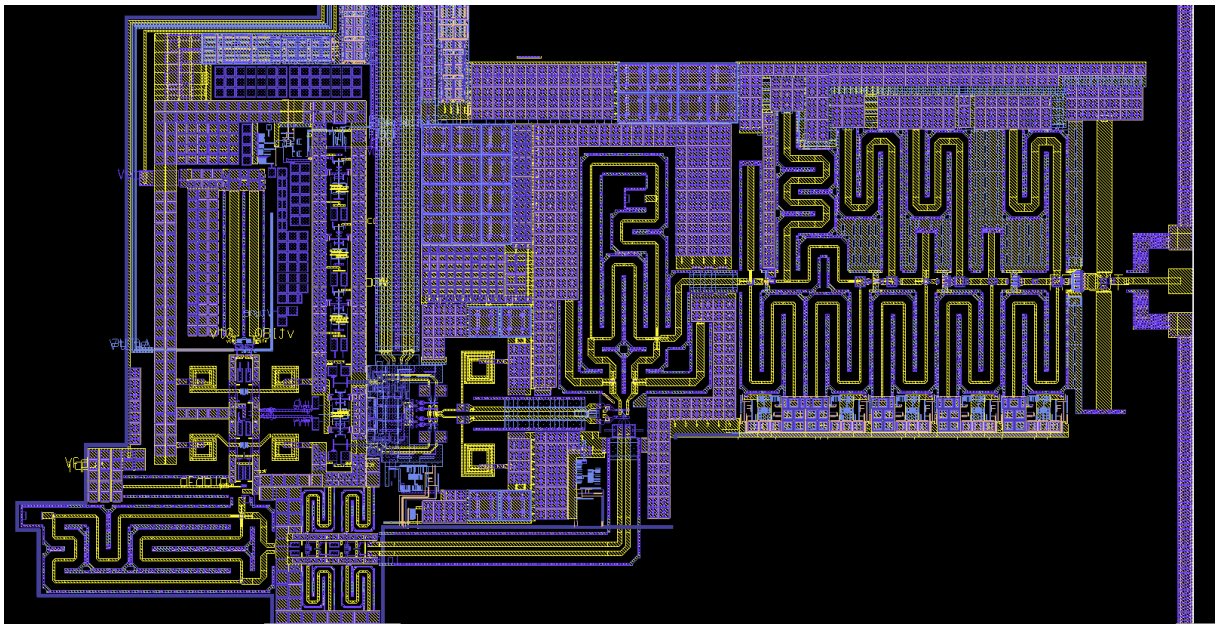


Figure 7.11: *Layout of GTC2 transmitter.*

7.2.5 Development Boards

Boards designed to test the transmitter are shown below. A bond-wire antenna (Weste and Hall) [108] was used at the output of the transmitter. The test setup consists of a master board which contains control logic (small micro-processor), voltage regulation, power supply conditioning and some baseband attenuation. The daughter boards we implemented on Rogers 4003 substrate and contain the chip, some decoupling capacitors and the bond-wire antennas. The chip is mounted in a cavity and bondwires are

used to connect to the PCB.

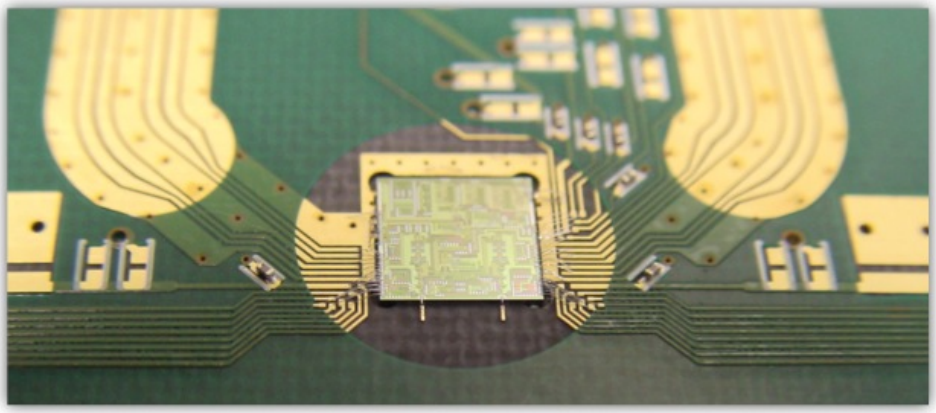


Figure 7.12: *RF daughter board for TX testing. Board designed by the author, antennas by Leonard Hall.*

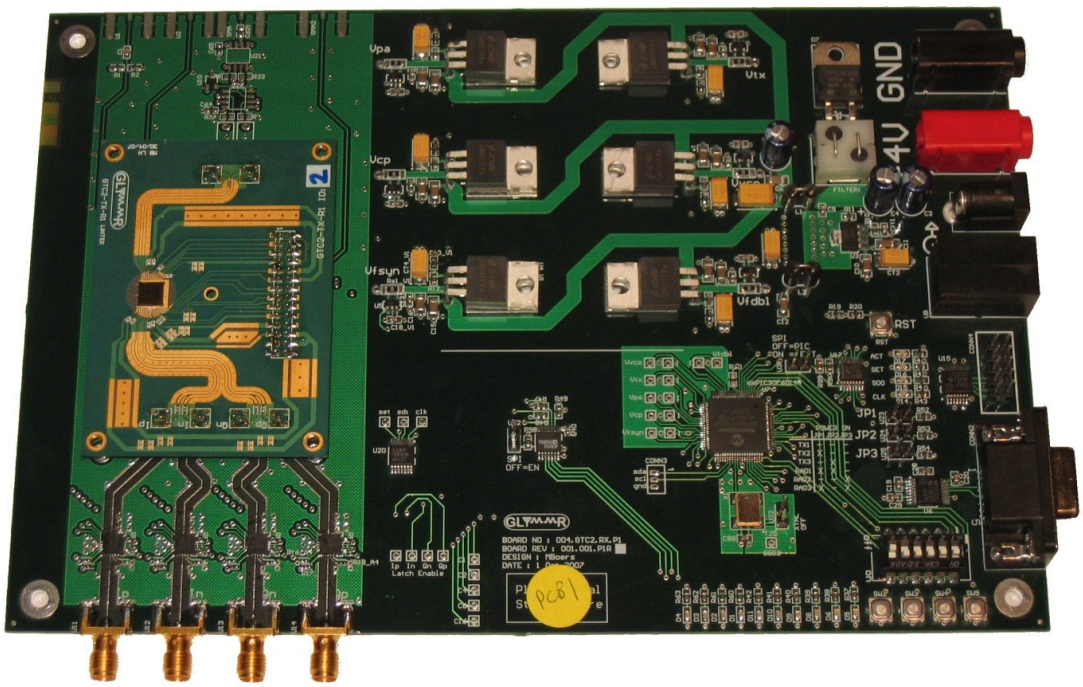


Figure 7.13: *Development boards designed for testing the transmitter*

7.2.6 Wire-bonding

This chip uses wirebonding to connect to the chip. Wire-bonding is feasible at 60 GHz however WLCSP packaging is preferred if available. To get the best performance at high frequency, a cavity is cut out of the PCB. The die is attached inside the cavity using thermal and conductive glue. Ideally the top of the chip will be slightly higher than the PCB and the wirebond will be as straight as possible. This is shown in Figure 7.14.

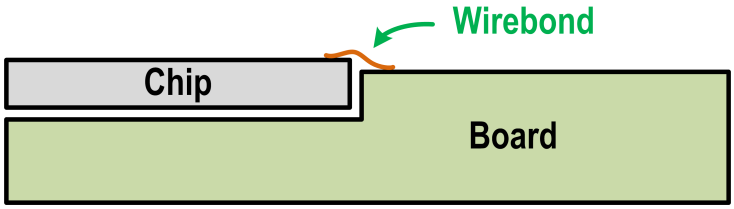


Figure 7.14: *The chip is inserted into a cavity on the PCB to reduce the length of the wirebond.*

Wirebonding requires a specific pressure to attach the bond to the pad. If too much pressure is used, the wirebond will be compacted onto the adjacent pads, if too little pressure is used, the wirebond will come away from the pad. We outsourced the wirebonding for this project, the results are shown in Figure 7.15.

7.2.7 Measurement Results

The transmitter's measured performance matched the simulated results closely. The output was tuned to the 60 GHz band (57-64GHz) and provided close to 30dB gain across this range.

A simple experiment was done with the transmitter transmitting across a room to a

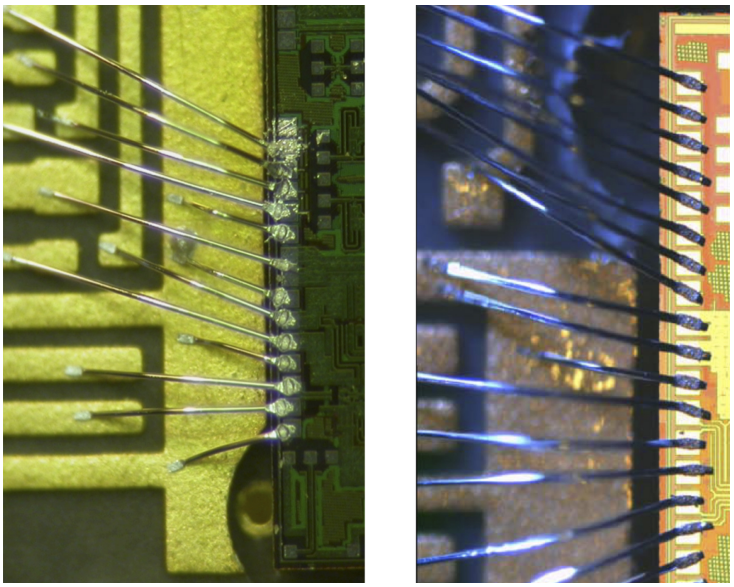


Figure 7.15: *On the left too much pressure was used for wirebonding, the right shows better bonds.*

horn antenna attached to a spectrum analyzer. The setup is shown in Figure 7.18 and the results in Figure 7.17. The results roughly show the 6dB drop off expected each time the distance is doubled.

7.2.8 Outcomes

This section outlined a transmitter designed for 60GHz. The performance matches simulation and validates the design methodology presented in Chapter 4.

The architecture shown here would be amenable to integration in a small form-factor device such as a cell phone and would enable up to 1Gbps over 1 meter.

In order to communicate over a longer distance, multiple antennas are required and a phased array with more front-ends should be implemented. An architecture which supports multiple antennas is presented in the next section.

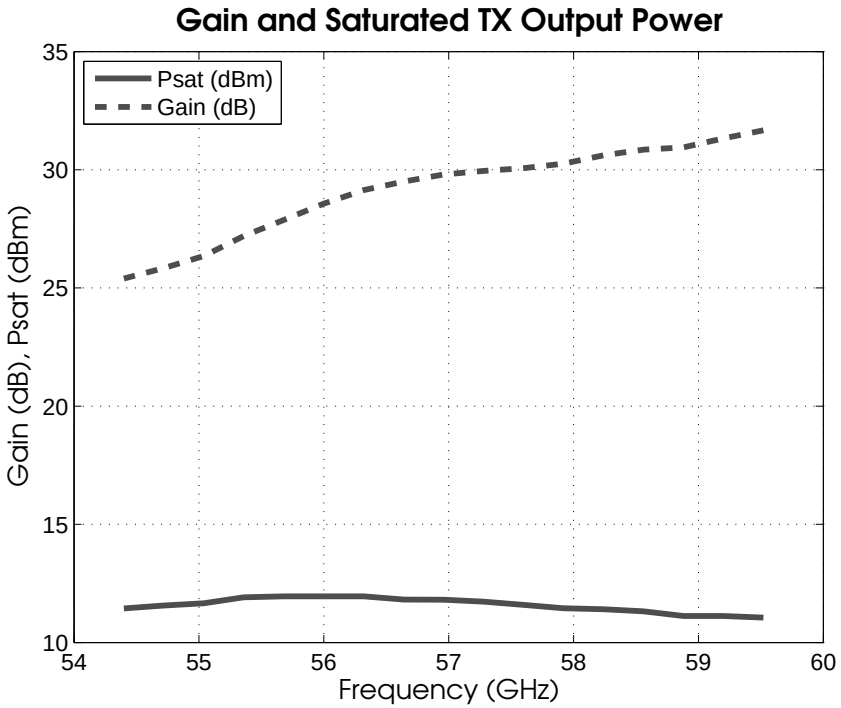


Figure 7.16: *Gain and Saturated Output Power for GTC2-Tx.*

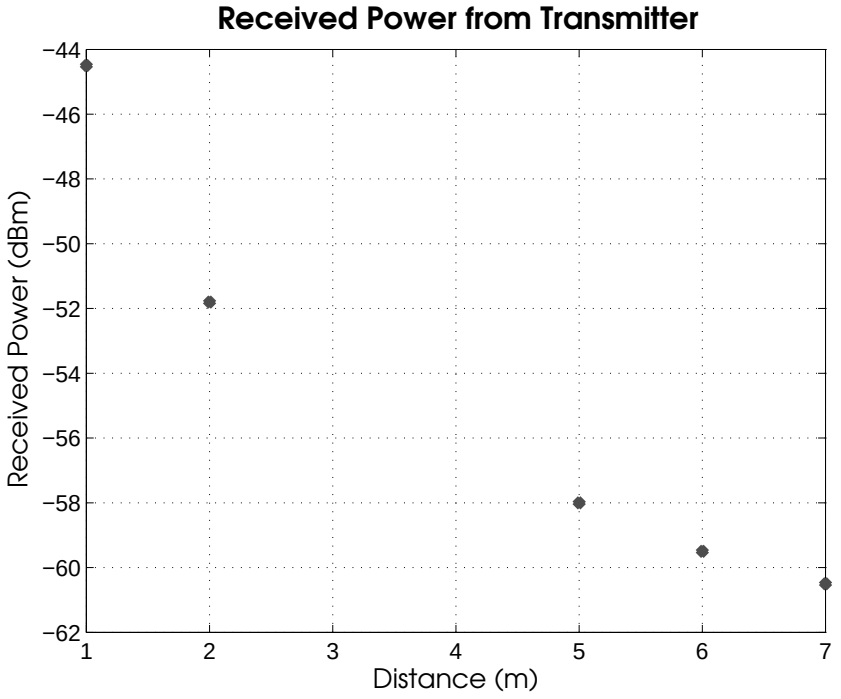


Figure 7.17: *Received power from the transmitter*

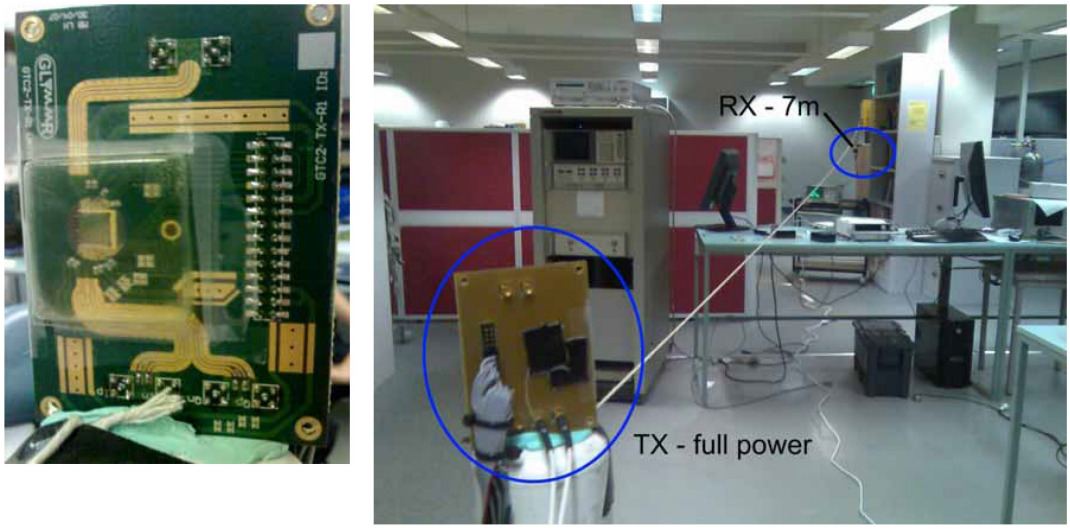


Figure 7.18: *Photo showing TX to Spectrum Analyzer link experiment*

7.3 GTC3-Tx: A Split-IF 60 GHz TX

This section presents a transmitter and architecture designed for GLIMMR test-chip 3 (GTC3). A block diagram of the system with the work covered in this thesis is highlighted in blue in Figure 7.19.

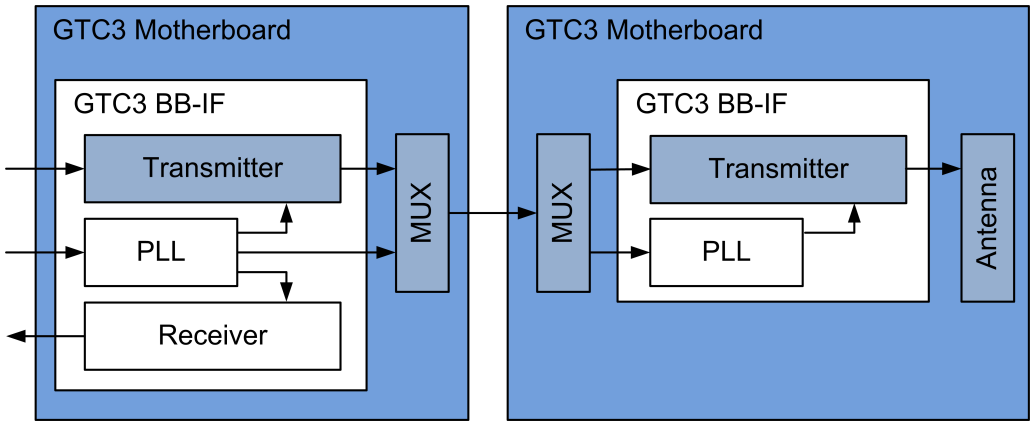


Figure 7.19: *Simple diagram of GTC3 showing the areas covered in this section.*

7.3.1 Introduction

The continual performance improvement, feature addition and size reduction makes the integration of millimetre wave transceivers in consumer devices challenging. Architectures used for WLAN and Bluetooth where the RF signal is routed over a coaxial cable to the antenna are problematic at 60 GHz due to high losses. Mounting the whole transceiver at the site where the antenna is located also poses difficulties due to large area of the module, high power dissipation and digital interference with LCD screens.

Figure 7.20 shows three architectures commonly used for wireless communication systems. In a laptop or television, the antennas can be up to 15cm away from the digital source (host processor).

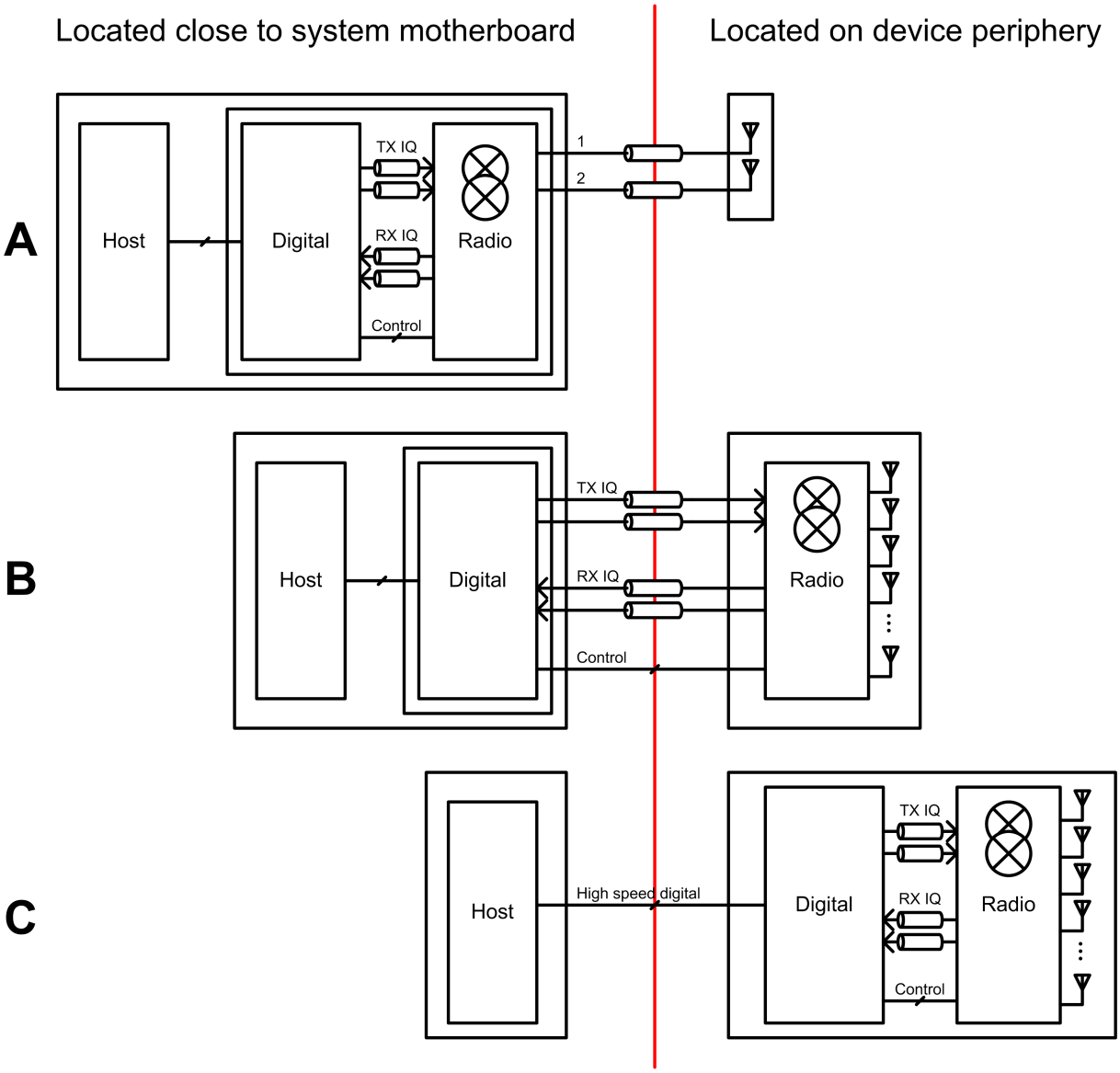


Figure 7.20: *Typical architectures for wireless communication systems*

RF Interface

Figure 7.20 (A) shows a typical setup for WLAN or Bluetooth where a passive antenna is separated from the radio and host platform via a long coaxial cable. This works well at lower frequencies for the following reasons. Only a few 2-4 antennas are required and the losses over the coaxial cable are low (less than a dB). At 60 GHz. the losses would be too high (several dB per cm).

Analog I/Q Interface

Figure 7.20 (B) shows a front-end module and antennas separated from the digital core at the analog I/Q interface. This architecture is challenging to implement over a long distance due to the large number of lines required between the two chips and the power penalty of the I/Q link.

Digital Interface

Figure 7.20 (C) shows the entire radio including digital baseband at the front-end. The radio is connected to the host using digital link (PCI-e) or other. In this architecture, there is some power penalty from routing the digital over an extended distance, the interface requires several lines which takes important realestate in a device and the noise from a digital interface may cause interference to other blocks.

A split sliding IF Architecture

In order to overcome some of the challenges outlined above, an alternative architecture is proposed here for 60 GHz systems. In this architecture the radio is split at an intermediate frequency and a single coaxial cable is used to route the intermediate frequency, LO frequency, DC and a control signal.

Figure 7.21 shows a high level system diagram. The digital and radio up to an intermediate frequency (IF) is close to the host processor. A second module which contains IF to RF conversion and the antennas is placed close to the device periphery.

The benefits of this architecture include the following:

1) The integration in a device is consistent with integration of lower frequency radios, with the major difference being an active front-end module.

2) The small size and flexible nature of a coaxial cable enables one or more front-ends to be placed at the desired place in a device without worrying about the routing of several analog or digital lines.

A simular architecture is shown in [109] [1].

[1] This patent was filed 4 years after the work in this thesis was done.

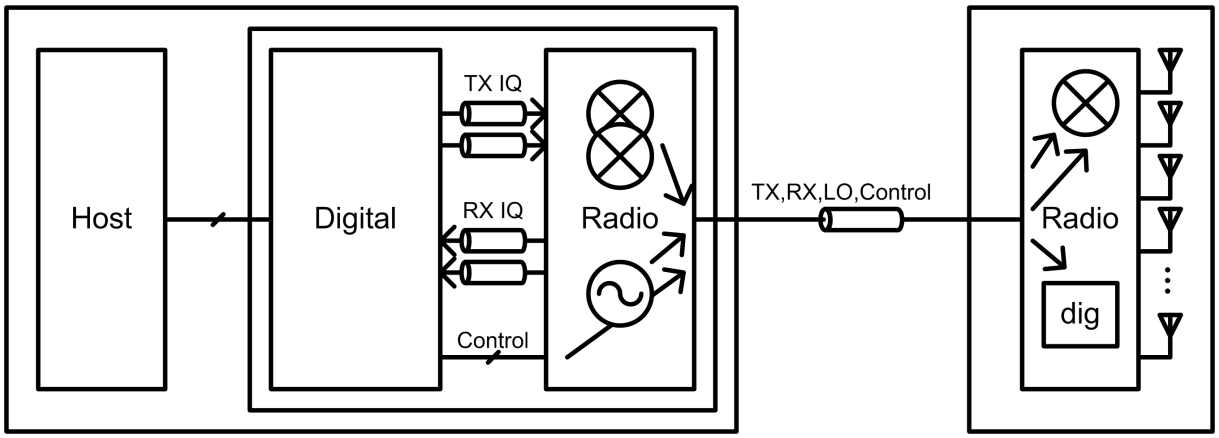


Figure 7.21: *Proposed Split-IF Architecture - Taped out in January 2009.*

7.3.2 System Design

Link Calculation

The target for this system is a single baseband chip with a scalable number of front-end chips. Assuming transmit and receive modules have specifications as outlined in Table 7.2, Figure 7.22 shows the distance for a 1 Gbps link versus number of antennas. Four antennas provides a reasonable link for in-room operation.

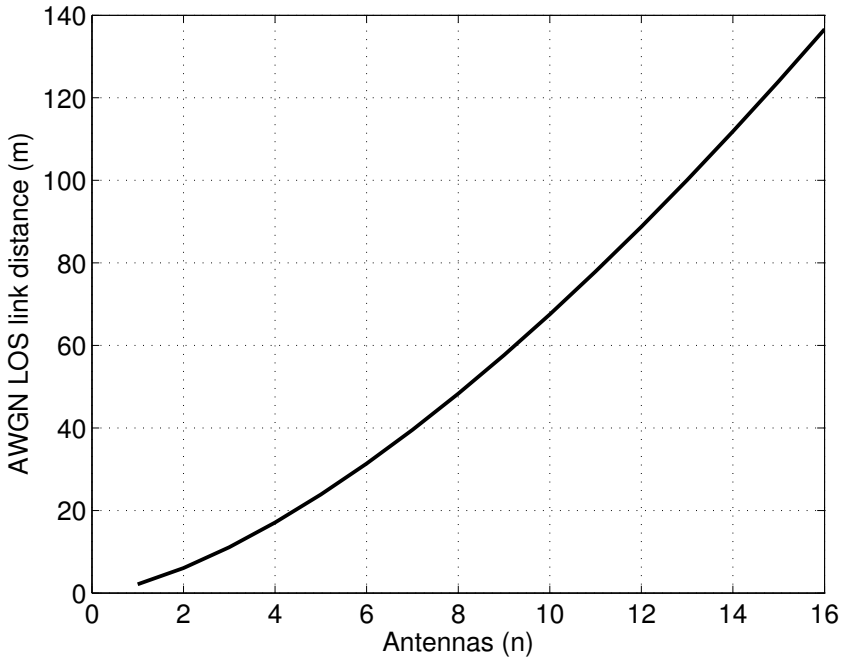


Figure 7.22: *Link distance versus number of antennas for a QPSK LOS 60 GHz link.*

Specifications

The specifications for the TX are outlined in Section 4.3.2 and repeated in Table 7.2.

		BB PGA	I/Q Mix	interface	splitter	IF amp	RF Mix	PA
Gain	(dB)	3	-2	-4	-12	12	-2	30
NF	(dB)	20	15	4	12	10	10	10
Op1dB	(dBm)	0	0	20	20	3	0	10
Cascaded Analysis								
Gain	(dB)	3	1	-3	-15	-3	-5	25
NF	(dB)	20	20.6	20.7	21.6	26.3	26.5	26.8
Op1dB	(dBm)	0	-4.1	-8.1	-20.1	-8.5	-10.8	9.5

Table 7.2: *Block level specifications and lineup for GTC3.*

Power over coax

The transfer of DC power over a coaxial cable to power an RF amplifier (LNA or PA) is a common technique used to improve the performance of systems at low frequencies (up to 5GHz) where the antenna would have to route several meters. It is used in remote HAM antenna installs, [110], has applications in wireless-LAN installations [111] where the antennas and amplifiers are placed on a mast and has also been used in low noise GPS receivers [112]. Most of these applications use off the shelf connectorised cables and bias tees to inject the DC signal. Bias tees are three port devices. One port is inductor coupled and contains only the DC signal (the inductor provides a high impedance to the RF), an RF port which is capacitor coupled and a DC+RF port.

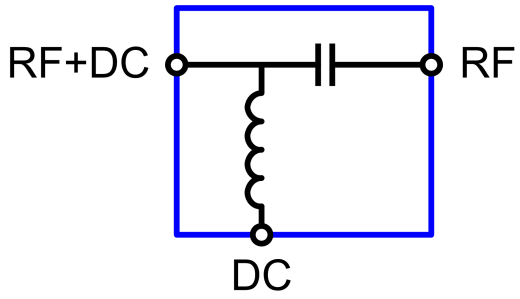


Figure 7.23: *A bias tee.*

One of the primary considerations when supplying DC over coax is the power lost in

the bias tee and cable due to resistive losses. A power budget for the coaxial link is shown below.

The resistance of the DC link is:

$$R_{tot} = 2 \times R_{bias\_tee} + 2 \times R_{connector} + R_{coax/m} \times L \tag{7.1}$$

If we include a switching regulator with efficiency = S_{eff}

$$P_{sw} = P_{out}/S_{eff} \tag{7.2}$$

$$V_{sw} = V_{in} - R_{tot} \times I_{sw} \tag{7.3}$$

$$V_{sw} = V_{in} - R_{tot} \times \left(\frac{P_{out}/S_{eff}}{V_{sw}} \right) \tag{7.4}$$

$$V_{sw}^2 - V_{sw} V_{in} + R_{tot} P_{out}/S_{eff} = 0 \tag{7.5}$$

Solving for V_{sw} we get

$$V_{sw} = V_{in}/2 + \frac{\left(V_{in}^2 - 4 R_{tot} P_{out}/S_{eff} \right)^2}{2} \tag{7.6}$$

and

$$P_{loss} = \frac{(V_{in} - V_{sw})^2}{R_{tot}} \tag{7.7}$$

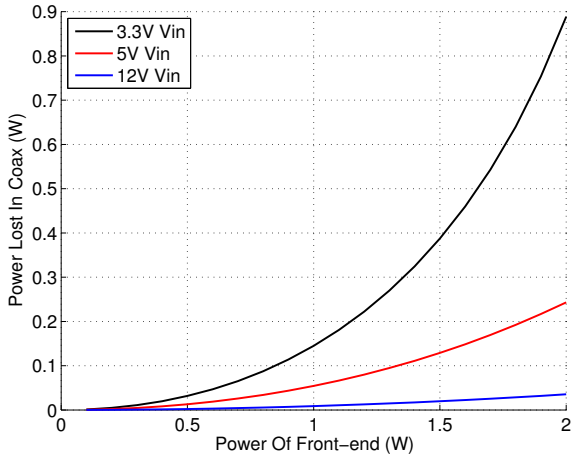


Figure 7.24: *Power lost over the coax cable, assumes fixed 1ohm R_{tot}*

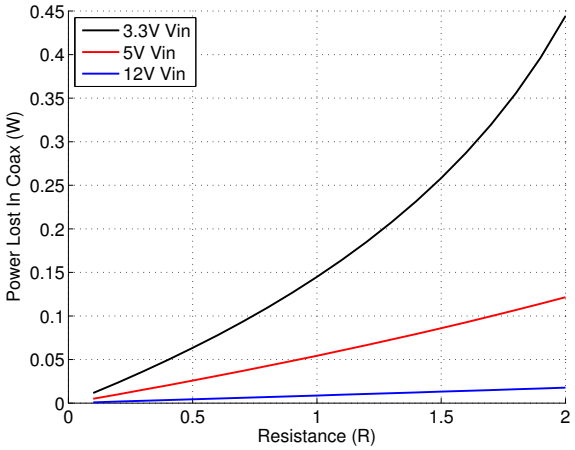


Figure 7.25: *Power lost over the coax cable, assumes fixed 1W front-end power*

These results show the importance of reducing the resistance of the coaxial cable and other resistive losses in the path and the benefit of operating at a higher voltage if possible.

IF over coax

Transmitting an intermediate frequency over coaxial cable is proposed in [112] for a remote GPS installation in order to reduce the losses of routing the RF signal. This architecture is also used in satellite ground stations and cellular base-stations.

The primary goal of transmitting the IF over a coaxial cable is to reduce the losses associated with routing a high frequency signal to the front-end. At 60 GHz the losses

over standard coaxial cable used in laptops for 5.8GHz systems would be too high (on the order of 20-30dB/m).

At 9GHz the losses are much lower and importantly, the losses do not degrade the receiver sensitivity or output power as they are before the PA in the transmitter and after the LNA in the receiver.

LO over coax

There are two options for sending an LO frequency over the coaxial cable. The first is to send a lower frequency signal (MHz range) and use that to lock a PLL on the front-end as shown in [22].

The second option is to send a harmonic component of the final LO and use frequency multiplication at the front-end. This is the option we use in this work. The frequency plan is shown next.

Frequency Plan

There are several considerations for the frequency plan in a multiplexed system. The IF frequency should be low enough that it does not have too much loss on low-cost coax. Harmonics of the LO and other components should not interfere with the IF and vice versa.

The frequency scheme chosen in this architecture is $VCO/2$ for LO1, and $VCO \times 3$ for LO2 resulting in a VCO range from 16-19GHz.

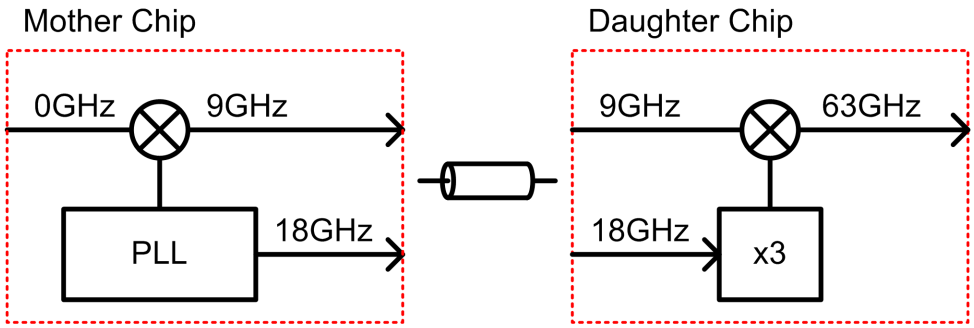


Figure 7.26: *Frequency Plan for Split-IF Architecture*

Channel	Frequency	IF Frequency	VCO Frequency	LO Frequency
1	58.32	8.33	16.66	49.99
2	60.48	8.64	17.28	51.84
3	62.64	8.95	17.90	53.59
4	64.8	9.26	18.51	55.54

Table 7.3: *Split-IF Radio Frequency Plan*

Control over coax

We did not implement the circuitry for control over coax on the chip - we envisaged a simple ASK or OOK system running at low GHz frequencies. This should operate in the linear region to reduce any harmonic and intermodulation content outside of the band. It should also be designed to be away from standard communication bands such as cellular, Bluetooth and Wireless LAN.

Block Diagram

The TX block diagram is shown in Figure 7.27. The two chips taped out are shown in blue highlight (some features removed for clarity). The left chip contains baseband to IF up-conversion as well as a PLL. The right chip contains IF to RF up-conversion mixer, a PA, a tripler and a phase shifter in the 18GHz LO path.

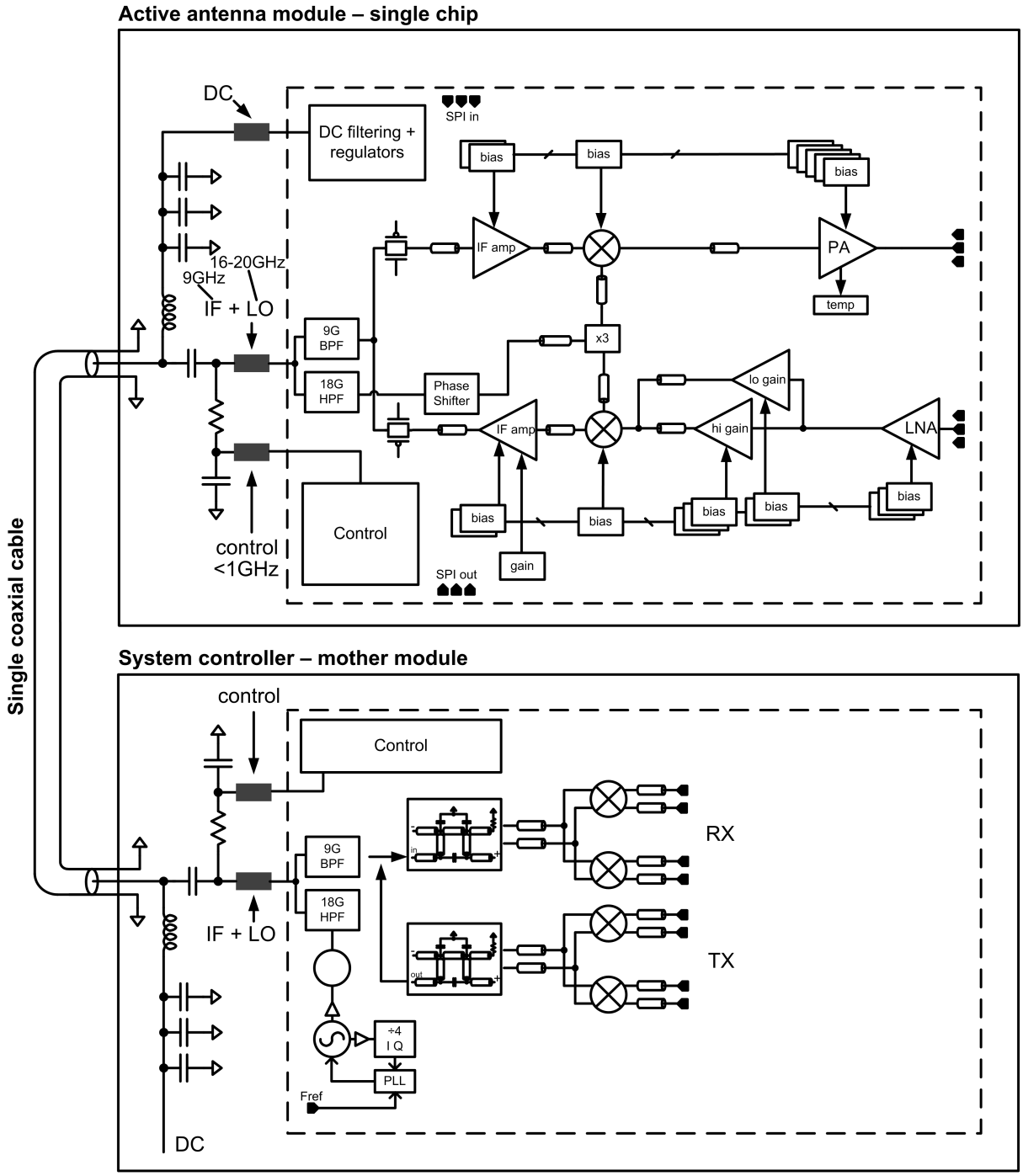


Figure 7.27: *High level block diagram for GTC3 system. The transmitter is covered in this chapter. The receiver was designed by Leonard Hall and James Howarth. The PLL was designed by Yingbo Zhu and Noorfazila Kamal.*

7.3.3 Circuit Design - TX Mother Chip

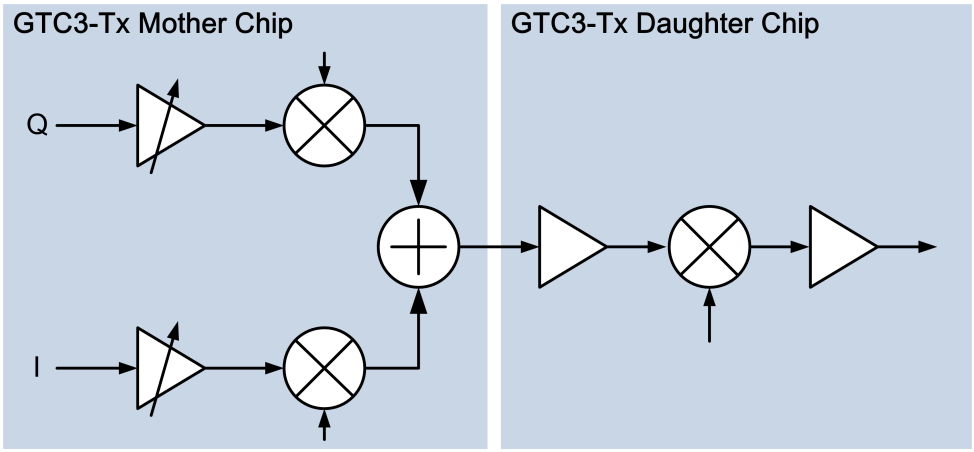


Figure 7.28: *Block diagram of the GTC3 transmitter.*

Baseband to IF mixer

The TX mother chip contains an I/Q up-conversion mixer, PLL and 9 GHz LOGEN. The I/Q mixer uses NMOS devices as a gm input stage and SiGe HBT switches for the up-conversion mixing. A schematic for the mixer is shown in Figure 7.29.

The baseband mixer uses NMOS transistors for the gm stage. The switching devices are SiGe HBTs. The output of the I/Q mixer is loaded with a 9 GHz transformer which is matched to 50 ohms.

The layout for the I/Q upconversion mixer is shown in Figure 7.30.

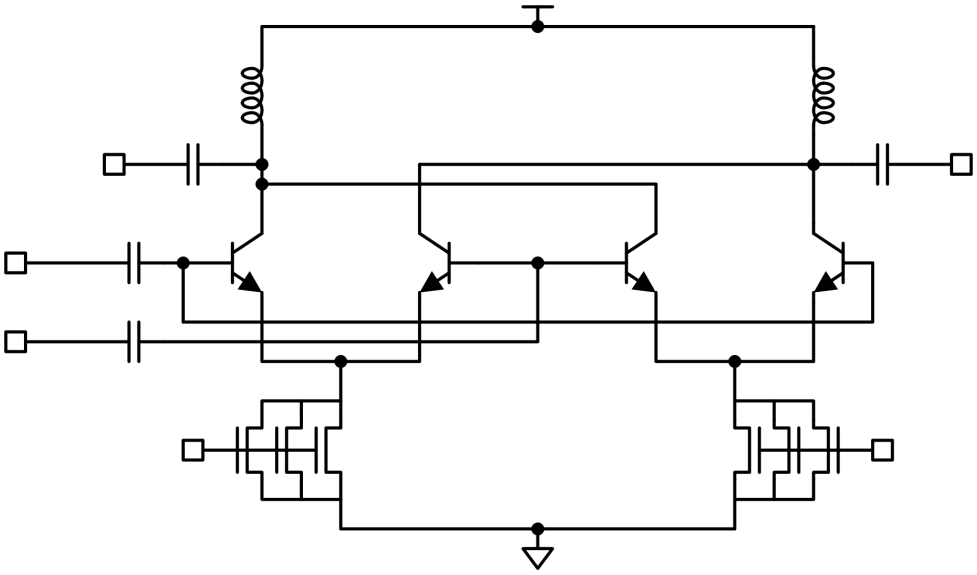


Figure 7.29: *Simple diagram showing a single side of the I/Q up-convertor.*

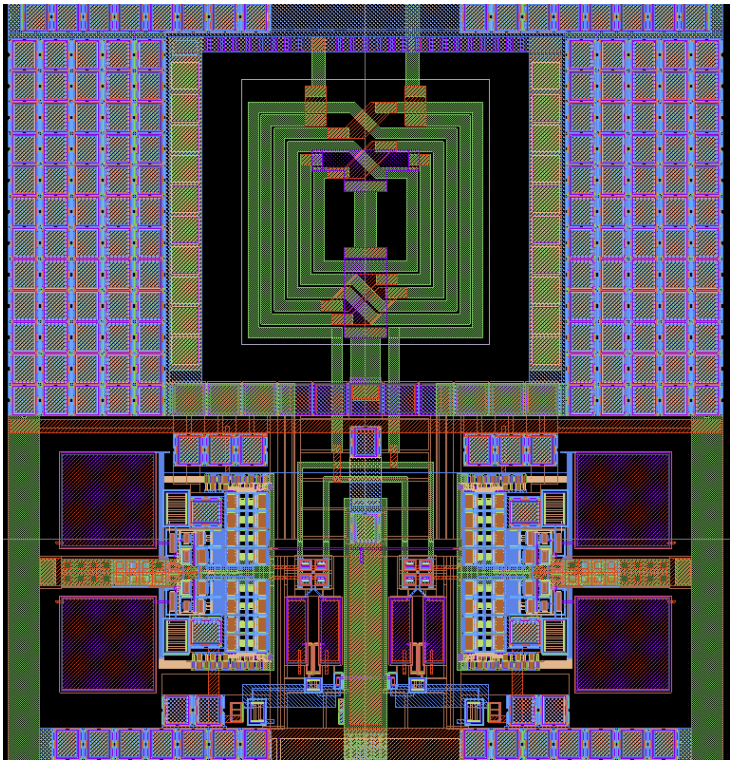


Figure 7.30: *Layout of the I/Q up-convertor.*

7.3.4 Circuit Design - TX Daughter Chip

The TX daughter chip contains an IF amplifier, RF mixer, PA and 18 GHz to 54 GHz LOGEN. Phase shifting is done in the LO path. RF phase shifters provide a lower power solution

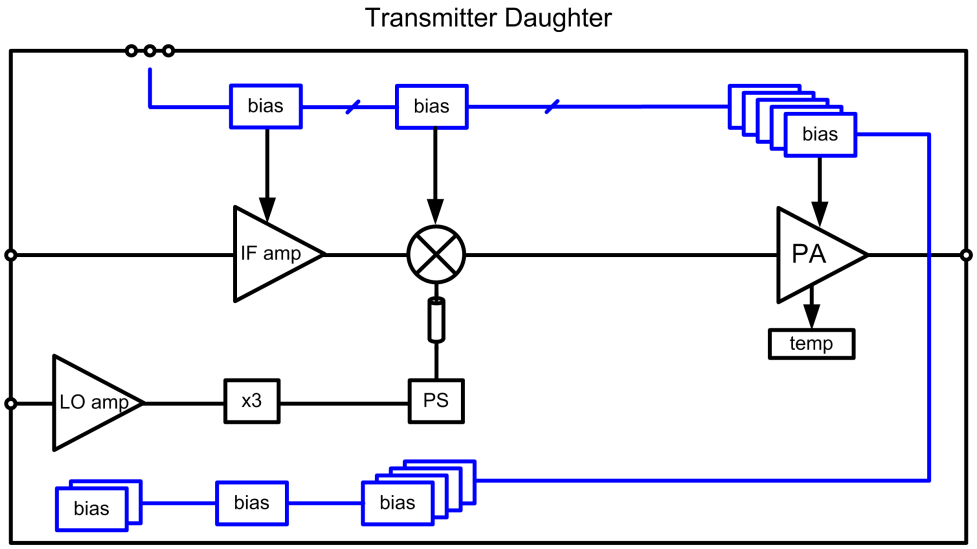


Figure 7.31: *TX Daughter Chip Block Diagram*

IF Amp

The IF amp is a 9 GHz amplifier using a single cascode gain stage. The amplifier is matched with transformers at the input and output. The input of the amplifier is matched to 50 ohms.

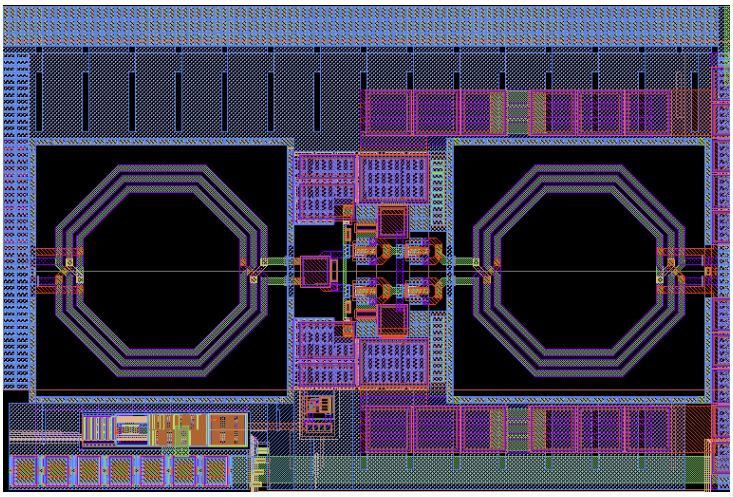


Figure 7.32: *Schematic of IF amplifier*

IF to RF mixer

The IF to RF mixer shown in Figure 7.33 is a simple Gilbert cell which is matched to the output of the IF amplifier and the input of the power amplifier. Rather than matching to a 50ohm impedance, the conjugate matching networks save area.

Power Amplifier

The PA is discussed in detail in the previous chapter. The schematic is shown in Figure 7.35. It is a four stage transformer coupled design which achieves 25-30dB gain and has a wide band-width.

7.3.5 Module Design

The front-end module for GTC3-Tx is shown in the figure below. It consists of an IF and LO input and a connector for 60 GHz output. The module is designed for wire-

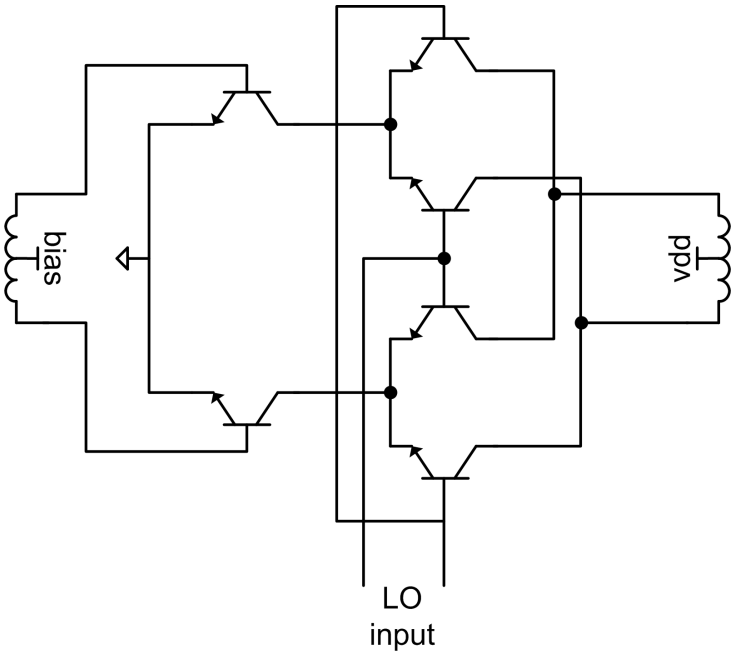


Figure 7.33: *Schematic of IF to RF mixer*

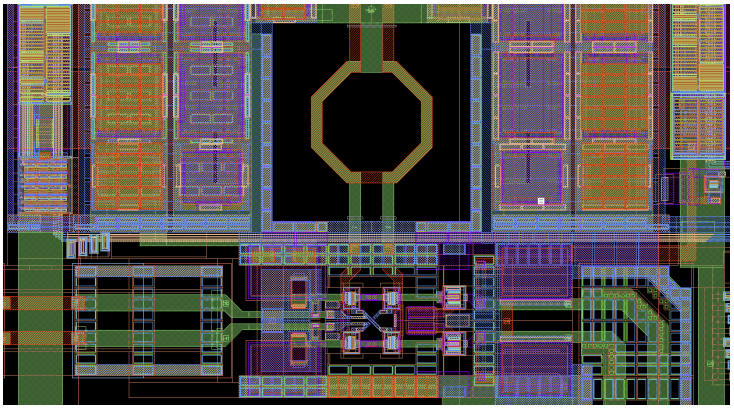


Figure 7.34: *Layout of IF to RF mixer*

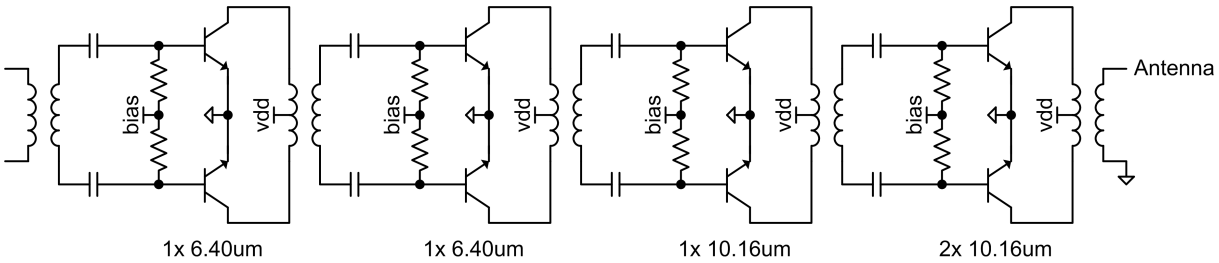


Figure 7.35: *Schematic of Power Amplifier*

bond connection and has a routed out area for the die to sit in that reduces the 60 GHz losses.

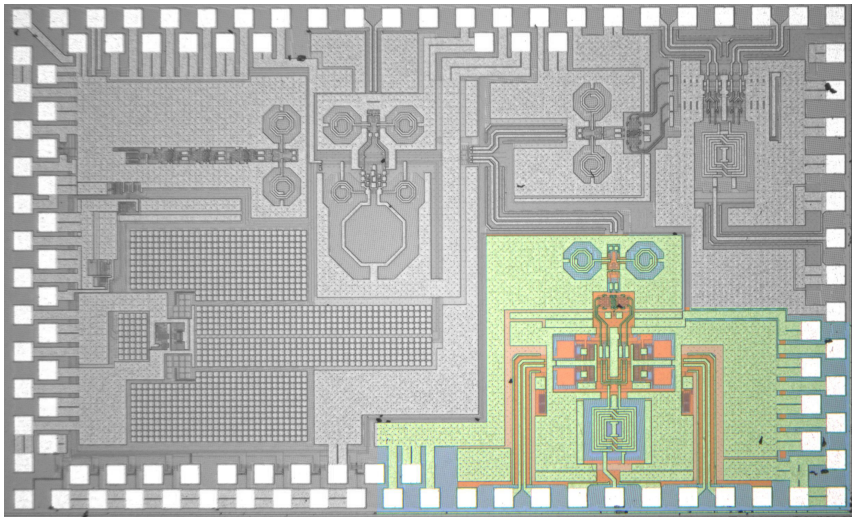


Figure 7.36: *Chip micro-graph for Baseband to IF Chip, the TX is coloured, the rest of the chip is black and white.*

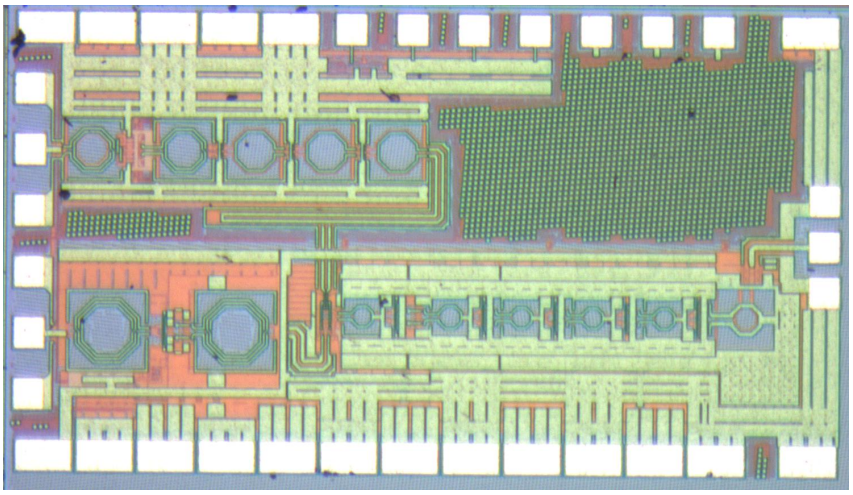


Figure 7.37: *Chip micro-graph for IF to RF chip*

The wire-bond connections are optimised for low loss. A zoomed in photo of the module is shown in Figure 7.39.

The wire-bond connection was simulated and optimised in HFSS. The simulated loss with protective epoxy is between 0.8 and 1.2dB across the 60 GHz band. This also

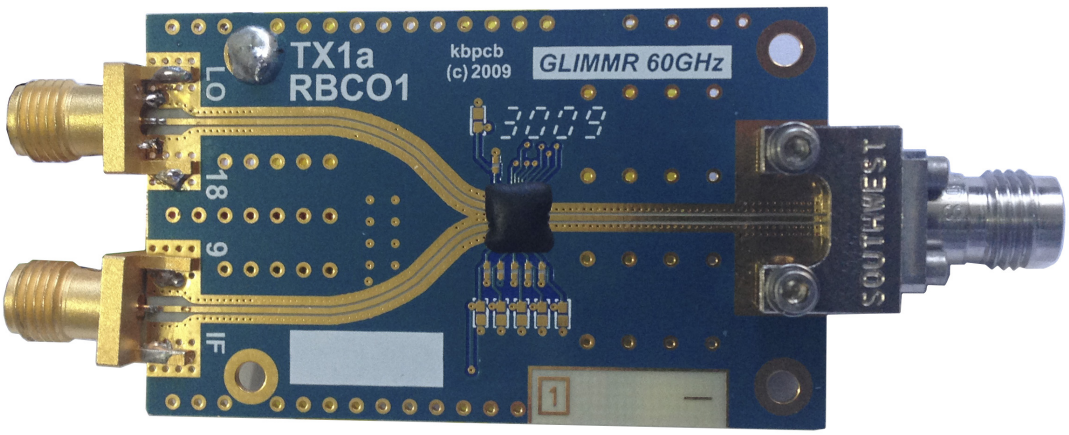


Figure 7.38: *Photo of GTC3 module showing the die with encapsulation and the connectors.*

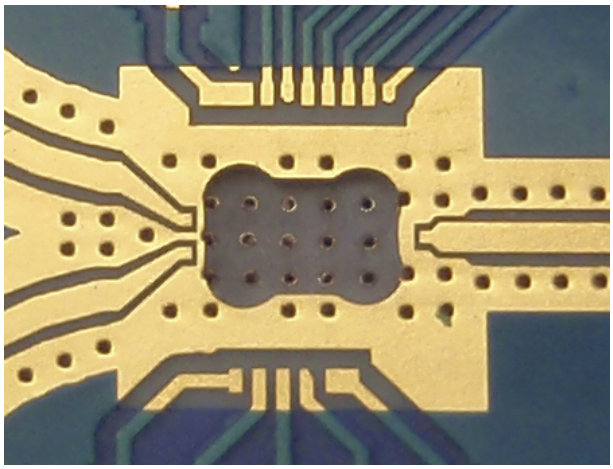


Figure 7.39: *Photo of GTC3 module showing zoom in on the cavity for the chip.*

includes some transmission line routing on the PCB and chip.

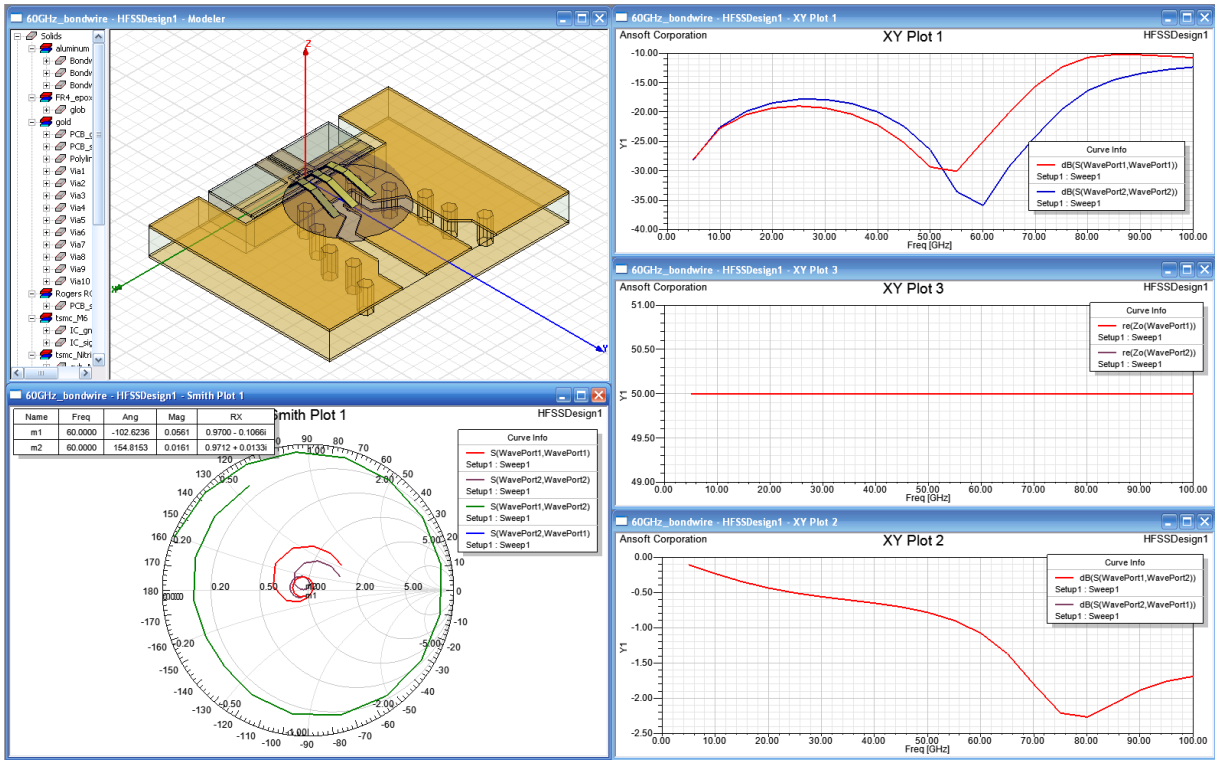


Figure 7.40: *HFSS simulation of the wirebond for GTC3-Tx module*

7.3.6 Measurement Results

The test and measurement setup is shown in Figure 7.41. Agilent E82x7D sources are used for the 9 GHz IF signal and 18 GHz LO signal. A Rohde and Schwarz NRP-Z57 60 GHz power meter is used to measure the cable loss and calibrate the spectrum analyzer. A Rhode and Schwarz FSU 67 GHz spectrum analyser is used to measure different frequency components.

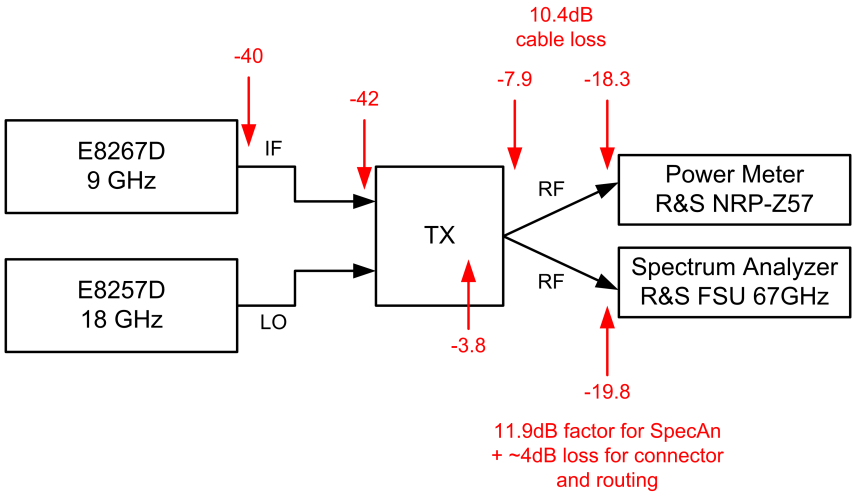


Figure 7.41: *Test and calibration setup for GTC3 measurements.*

The current for different sub-blocks at several bias points is shown in Figure 7.4. It shows the digital controller is working and the block settings can be updated. The last stage of the PA consumes the largest amount of current.

Bias	IF	Mix	PA1	PA2	PA3	PA4	PA5	LO	x3	48G	48G
0	0	0	0	0	0	0	0	0	0	0	0
7	10	6	16	16	15	24	47	10	6	6	6
15	19	9	30	31	30	45	85	19	12	12	12
24	26	12			40	62	112	27	18	17	17
31	34	14	55	53	53	77	131	35	21	22	22

Table 7.4: *GTC3 Tx current consumption in mA from 1.8V.*

The gain of the transmitter from 9GHz IF input to 60 GHz RF output is shown for each 802.11ad channel in Figures 7.42 and 7.43. It can be seen that the transmitter is slightly high tuned. The gain flatness for channels 2,3 and 4 is less than 5 dB which is easily correctable with DAC pre-distortion. Channel 1 flatness is slightly worse and could be corrected with a metal spin.

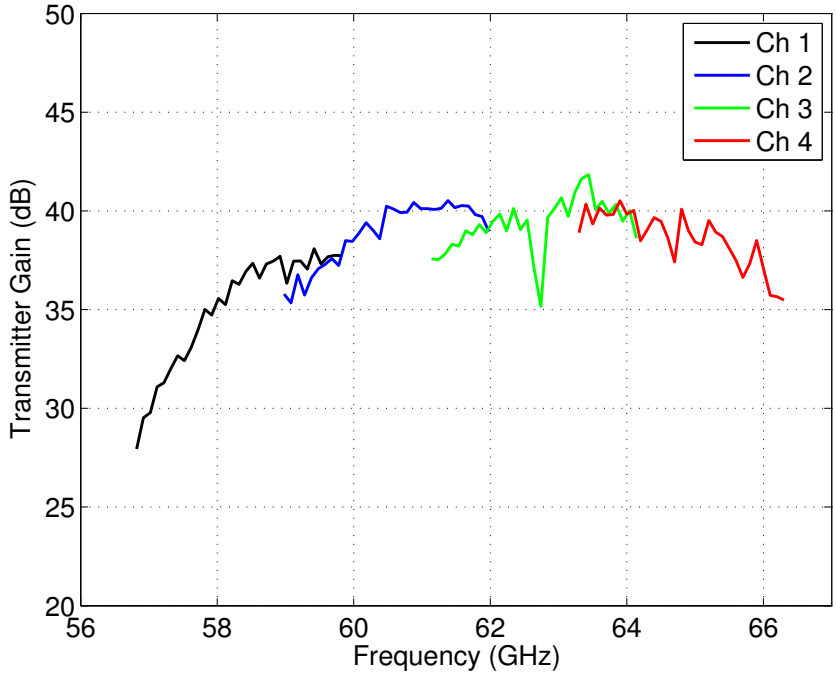


Figure 7.42: *TX gain for each 802.11ad channel.*

The output 1dB compression point of the TX is an important specification. The Op1dB point is shown measured across each channel in Figures 7.44 and 7.45. This measurement is taken with the spectrum analyser and calibrated with the power meter. It shows that the output 1dB compression point varies from 4 to 10 dBm calibrated to the output of the chip. The compression point is dependent on the output match and falls off at the edges of channel 1 and 4. There is also a consistent notch in the measurements at 62.8 GHz which most likely comes from the bond-wire and transmission line interface to the 60 GHz coaxial connector.

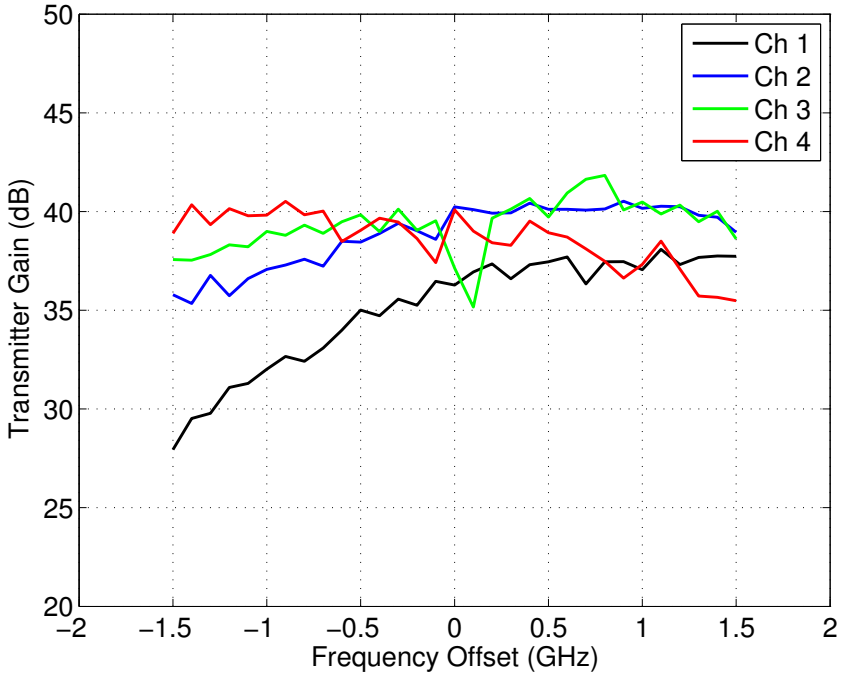


Figure 7.43: *Relative TX gains for each 802.11ad channel.*

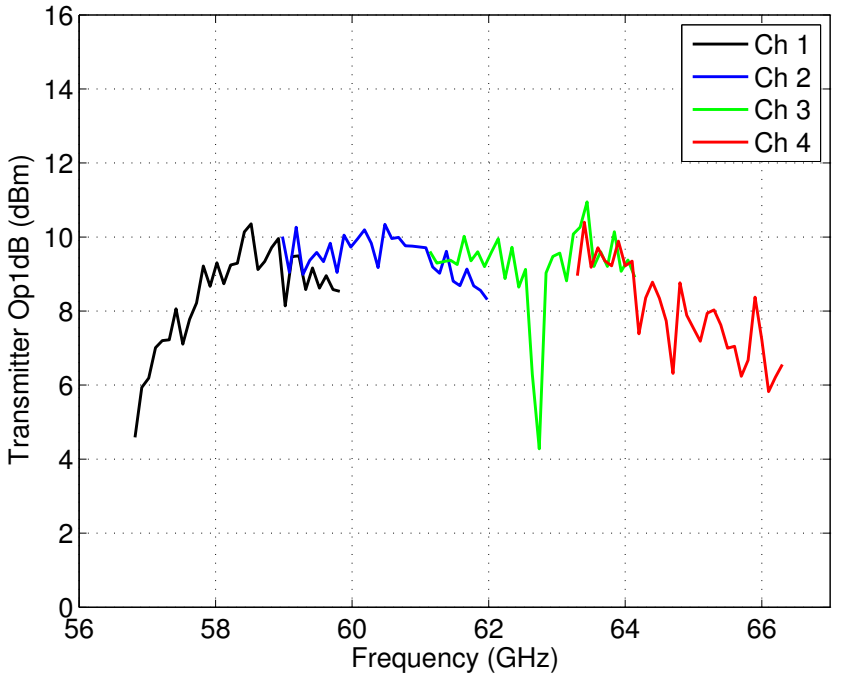


Figure 7.44: *TX output 1dB compression point for each 802.11ad channel.*

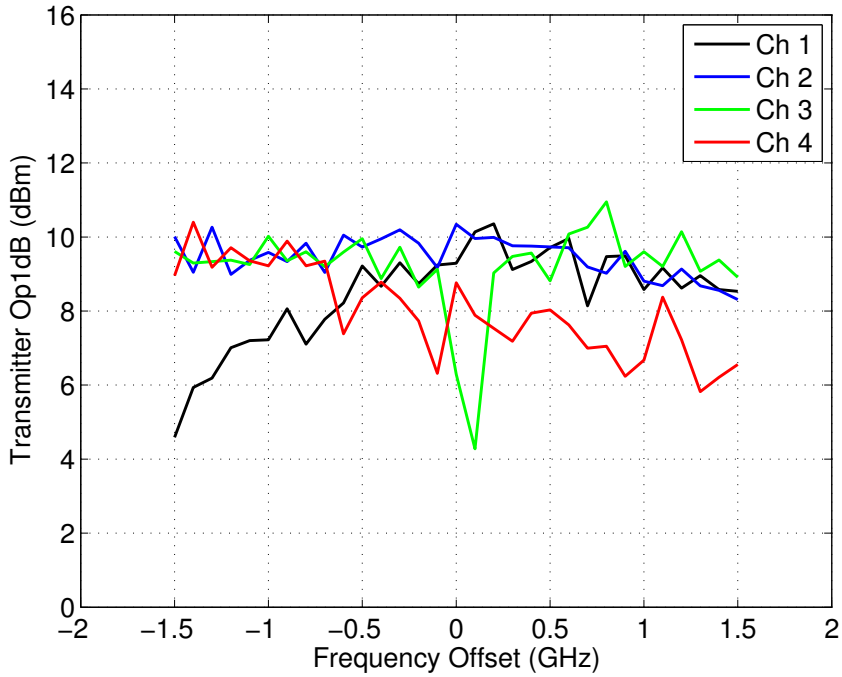


Figure 7.45: *Relative TX output 1dB compression point for each 802.11ad channel.*

A spectrum plot for each channel is shown in Figure 7.46 it shows the lower image, LO feedthrough and the upper image.

Figure 7.47 shows the gain versus IFamp and mixer bias settings. Figure 7.48 shows the transmitter output 1dB compression point versus the IFamp and mixer bias settings.

A plot of the transmitter gain with fixed IF frequency is shown in Figure 7.49. It shows the frequency response of the PA and output matching network. It shows a flat response from 58 to 67 GHz with a steep roll-off beyond that.

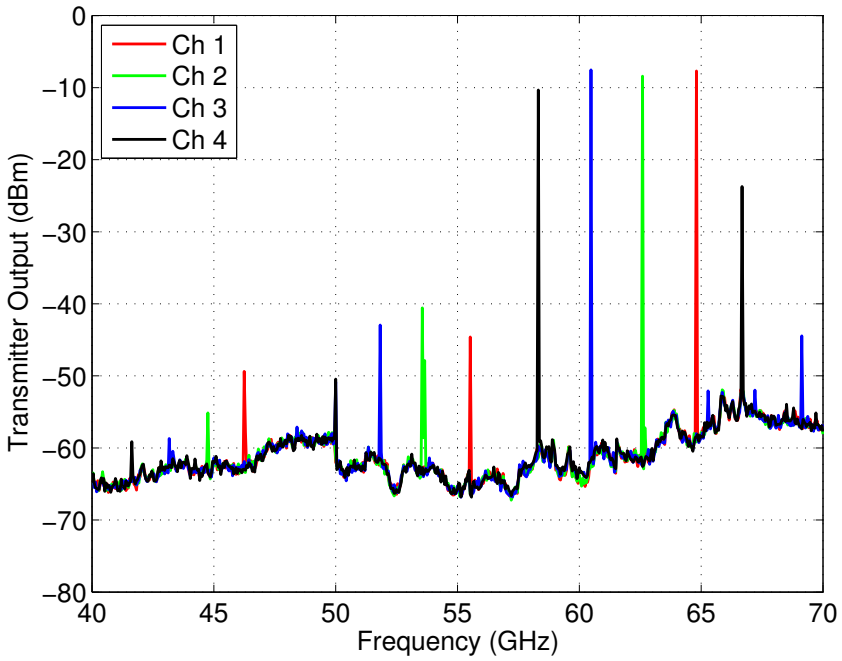


Figure 7.46: *Output spectrum for each channel showing lower image, LO signal and upper image.*

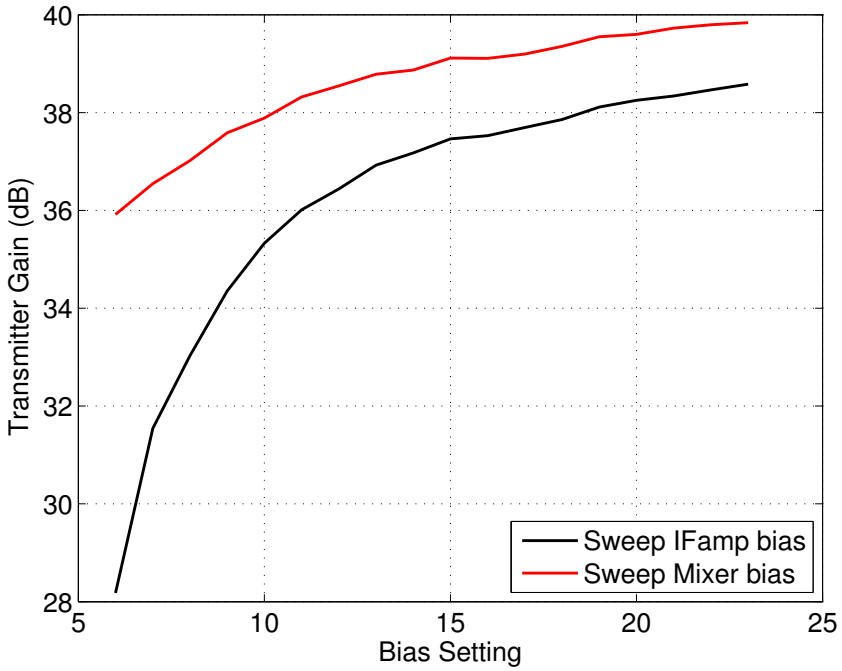


Figure 7.47: *Gain versus IFamp and mixer bias settings.*

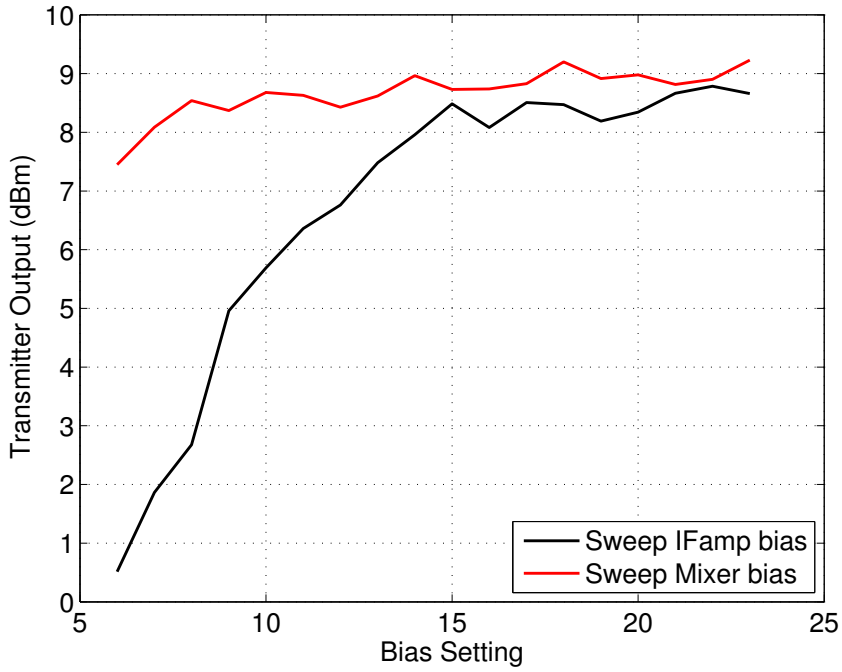


Figure 7.48: *Op1dB compression point versus IFamp and mixer bias settings.*

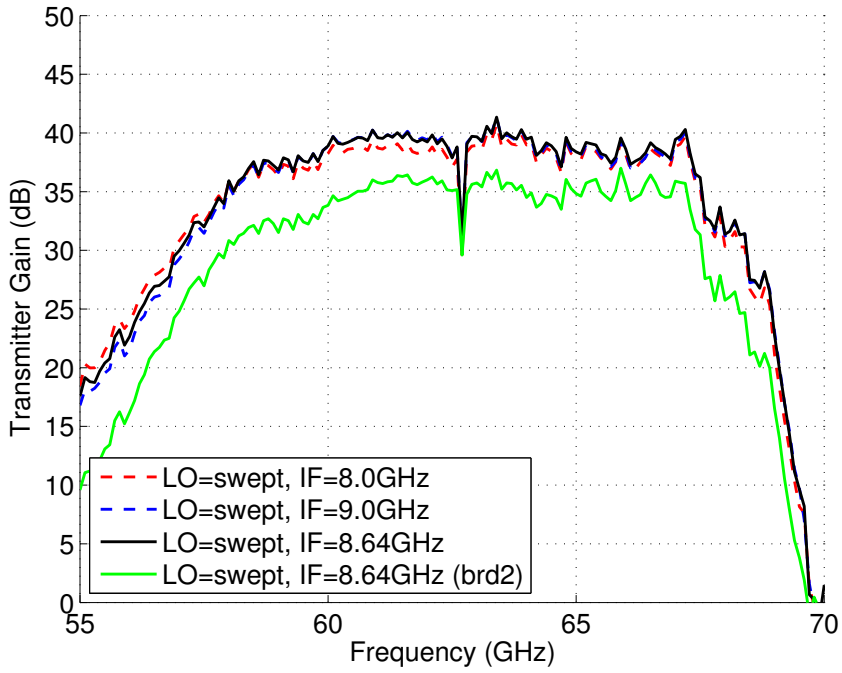


Figure 7.49: *Transmitter gain with swept LO signal, this shows the frequency response of the RF front-end. A second chip is measured which shows the same response, just slightly lower output power likely due to variation in the wire-bonding.*

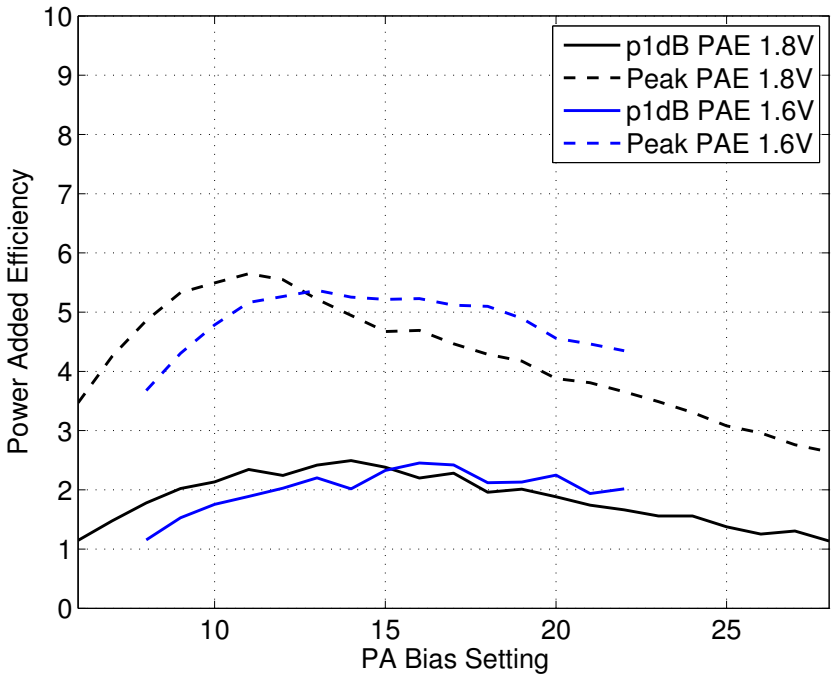


Figure 7.50: *Gain and Saturated Output Power*

7.4 Comparison

Several 60 GHz transmitters have been presented, in [113] a GaAs implentation is shown. It uses a 2.4 GHz IF and has an external LO. The output 1-dB gain compression point is 11dBm and the TX gain is 12dB. [114] shows a 60 GHz transmitter with integrated antenna in 0.18 µm technology. The chip contains a sub-harmonic mixer with 30 GHz LO input and a PA with integrated antenna. [77] presents a 2x2 phased array transmitter in 65nm CMOS. This paper shows some of the benefits of deep submicron nodes. The design achieves 11dBm saturated output power per transmitter and occupies an area of 2.9 x 1.4mm.

In [115] a 60 GHz transmitter is integrated with a baseband signal processor in 90nm CMOS. The PA has a p1dB of 5.1dBm and the full TX consumes 173mW. [82] demonstrates a 16 element phased array transmitter in 0.12 µm SiGe. The 16 elements consume 3.8 W at room temperature and have a peak op1dB of 9.3dBm per element.

Ref	Tech	Interface	Area	p1dB	Power
[113]	GaAs	2.4GHz IF	module	11 dBm	none
[114]	0.18um SiGe	0-2 GHz IF	1.3 x 0.8 mm	11.2 dBm	240 mW
[77]	65nm CMOS	Baseband	2.9 x 1.4 mm	n/a	590 mW
[115]	90nm CMOS	Baseband		5.1	173 mW
[82]	0.12um SiGe	Baseband	6.5 x 6.75	9.3	3.8 W

Table 7.5: *Comparison of 60 GHz transmitters.*

7.5 Summary

This chapter outlined design and measurement results for two 60 GHz transmitters designed in 0.18 µm SiGe.

The first transmitter has a single element and achieves an output compression point of 9dBm. It uses transmission line based design.

The second transmitter uses a novel split sliding IF architecture where the frontend can be placed away from the baseband to IF conversion chip with a single coaxial cable. The single transmitter modules achieve an output compression point of better than 8 dBm and multiple chips can be used in parallel to form a phased array.

8

Conclusions

This research has investigated circuits and architectures for 60 GHz transmitters and proposes a system architecture for high speed applications that is amenable to integration in large consumer electronic devices.

8.1 Contributions

8.1.1 Power Amplifier Design

The power amplifier is a key block in the radio transmitter. A design flow is outlined in Chapter 4 which scales from low frequency to 60 GHz and enabled the first time

right design of four power amplifiers. A high efficiency power amplifier at 1 GHz was designed for the IMS student power amplifier competition and achieved greater than 88% power added efficiency. A transmission line based 60 GHz PA was demonstrated in 0.18 µm SiGe that achieves 30dB gain and 3dB bandwidth of 11.5GHz.

Two transformer coupled power amplifiers were designed for 60 GHz operation. The first, a SiGe 5 stage design achieves a wide bandwidth, high gain but a peak efficiency of only 5%. A second design in 65nm CMOS achieves a high gain and efficiency and shows the advantage of neutralisation. This PA acheived state of the art performance with the highest published efficiency for a 65nm CMOS design.

8.1.2 Transmitter Design and Optimisation

Chapter 4 outlines a link budget for 60 GHz systems and outlines the transmitter specifications for a 60 GHz system. Several 60 GHz specific optimisations are presented such as performance with blocked links, the optimal number of TX antennas given a power budget, whether to use a TX/RX switch or not and the concept of asymmetric links. Two transmitters are designed for 60 GHz operation. The first one is a single chip SiGe design which takes an analog I/Q baseband signal and up-converts to SI60gigahertz. The second uses a novel architecture and is implemented using a dual-chip split-IF architecture.

8.1.3 Split-IF Architecture for 60 GHz Systems

One of the biggest challenges for 60 GHz integration in consumer devices is the requirement for the antennas to be placed near the device perimeter. If using common WLAN architectures this requires the digital to be routed and the entire solution be placed at the edge of the device or the 60 GHz signal to be routed. Routing the 60 GHz signal is challenging due to the high loss. This thesis proposes a new architecture split at an IF frequency which enables an active frontend to be placed anywhere in a device at the end of a coaxial cable.

8.2 Opportunities for Futher Work

The work in this thesis was done in 0.18 µm SiGe and 65nm CMOS, higher performance could be obtained by moving to more advanced nodes.

A high level architecture was proposed for a single coaxial system and the transmitter components were built but we did not study the triplexer or digital controller for such an implementation.

A more optimal split-IF architecture would involve multiple front-ends on a single die, ideally using RF path phase shifting.

8.3 Summary

The work in this thesis focused on the development of transmitters for 60 GHz applications. The first three chapters gave an overview of Silicon technology for mmWave systems and covered theory for transmitters and phased arrays. Several optimisations for mmWave transmitters are shown in Chapter 4.

Chapter 5 presented a design flow for mmWave circuits that is based on careful modeling and the scaling of low frequency design techniques to mmWave. Two power amplifiers are shown. The first, a board level design at 1 GHz and the second a 60 GHz SiGe transmission line based design.

In Chapter 6, two transformer coupled PAs were presented. The first a four stage design in SiGe that reduces the area required significantly compared to the transmission line design. The second uses the same topology in CMOS and shows the benefit of neutralisation for transformer coupled designs.

Finally Chapter 7, presented two transmitters for 60 GHz operation. The first transmitter is a single chip design with single antenna. The second design uses a novel architecture that enables the front-end to be placed at the end of a coaxial cable and allows for a scalable number of antennas. This architecture (co-invented with Leonard Hall) enables the optimal placement of 60 GHz antennas in devices.

A

Acronyms

SSD	Solid-State Drive
TX	Transmitter
PA	Power Amplifier
IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
mmWave	Millimetre Wave
SiGe	Silicon Germanium
GaAs	Gallium Arsenide

InP	Indium Phosphide
PC	Personal Computer
LAN	Local Area Network
WLAN	Wireless LAN
MIMO	Multiple-Input Multiple-Output
USB	Universal Serial Bus
HD	High Definition
PtP	Point-to-Point
SNR	Signal to Noise Ratio
GLIMMR	Gigabit Low-cost Integrated mmWave Radio
GTC1	GLIMMR test chip 1
GTC2	GLIMMR test chip 2
GTC3	GLIMMR test chip 3
FET	Field Effect Transistor
HBT	Heterojunction Bipolar Transistor
MPW	Multi Project Wafer
PLL	Phase Locked Loop
LO	Local Oscillator
LOGEN	LO Generation

GAN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IF	Intermediate Frequency
PCB	Printed Circuit Board
FOM	Figure of Merit
TDDB	Time Dependent Dielectric Breakdown
HCI	Hot Carrier Injection
NBTI	Negative Bias Temperature Instability
VCO	Voltage Controlled Oscillator
DC	Direct Current
AC	Alternating Current
MIM	Metal Insulator Metal
MTM	Metal To Metal
CPW	Coplanar Waveguide
AWGN	Additive White Gaussian Noise
EVM	Error Vector Magnitude
BB	Baseband
MCS	Modulation and Coding Set
RMS	Root Mean Square

SBS	Side Band Supression
DAC	Digtal to Analog Convertor
QAM	Quadrature Amplitude Modulation
AM	Amplitude Modulation
PM	Phase Modulation
EIRP	Effective Isotropic Radiated Power
AGC	Automatic Gain Control
LOS	Line Of Sight

B

Programming Code

B.1 Arduino Code

```
const int reg_width = 5;
const int reg_number = 15;
int data_in[reg_number] = {14,14,14,14,14,14,14,14,14,14,14,14,14,14,14};
int data_out[reg_number];
int incomingByte = 0;

void setup() {
  pinMode(13, OUTPUT);  // this is SCLK
  pinMode(12, INPUT);   // this is MISO  --- chip sdi
  pinMode(11, OUTPUT);  // this is MOSI  --- chip sdo
  pinMode(10, OUTPUT);  // this is EN    --- chip EN
  // init serial port
  Serial.begin(19200);

  digitalWrite(10, LOW);

  for (int i=reg_number-1; i>=0; i--){
    data_out[i] = readWriteReg(0);
```

```
    //Serial.println(data_out[i]);
  }
  for (int i=reg_number-1; i>=0; i--){
    data_out[i] = readWriteReg(0);
    //Serial.println(data_out[i]);
  }
  // clear out registers
  digitalWrite(10, HIGH);
  delay(8);
  digitalWrite(10, LOW);
  delay(8);
}

void loop() {
  // send data only when you receive data:
  if (Serial.available() > 3) {
    // looking for address, value pair 127,222
    int strt=0;
    int gadd=0;
    int addr=0;
    int data=0;
    int gdat=0;
    while (Serial.available() > 0) {
      incomingByte = Serial.read();
      if (incomingByte == 58) {
          strt=1;
        }
      else if (strt == 1 && gadd==0 && gdat==0) {
          addr=incomingByte;
          gadd=1;
      }
      else if (strt == 1 && gadd==1 && gdat==0) {
         data=incomingByte;
         gdat=1;
      }
      else if (incomingByte == 59 && strt == 1 && gadd==1 && gdat==1) {
        if (addr <= 14 && data <= 31) {
          data_in[addr] = data;
          for (int i=reg_number-1; i>=0; i--){
            data_out[i] = readWriteReg(data_in[i]);
          }
          delay(10);
          digitalWrite(10, HIGH);
          delay(8);
          digitalWrite(10, LOW);
          delay(8);
        }
      }
      else if (incomingByte == 60 && strt == 1 && gadd==1 && gdat==1) {
        if (addr <= 14 && data <= 31) {
          data_in[addr] = data;
```

```
        }
      }
      else if (incomingByte == 61 && strt == 1 && gadd==1 && gdat==1) {
        for (int i=reg_number-1; i>=0; i--){
          data_out[i] = readWriteReg(data_in[i]);
        }
        delay(10);
        digitalWrite(10, HIGH);
        delay(8);
        digitalWrite(10, LOW);
        delay(8);
      }
    }
  }
}

unsigned int readWriteReg(int data) {
  int out = 0;
  int in = 0;
  for (int i=reg_width-1; i>=0; i--){
    in = readWriteBit(bitRead(data, i));
    out = out + in*(pow(2,i));
  }
  return out;
}

unsigned int readWriteBit(int data) {
  int val = 0;
  // set data
  digitalWrite(11, data);
  delay(2);
  // raise clock
  digitalWrite(13, HIGH);
  delay(1);
  // read data
  val = digitalRead(12);
  delay(1);
  // set clock low
  digitalWrite(13, LOW);
  // return the read value
  return(val);
}
```

B.2 Python Code

```
import serial
from time import sleep

ser = serial.Serial(
    port='COM61',
    baudrate=19200
)
ser.open()

def ggWrite(addr,data):
    ser.write(':%c%c;' % (chr(addr),chr(data)))
    sleep(2)

def ggLoad(addr,data):
    ser.write(':%c%c%c' % (chr(addr),chr(data),chr(60)))
    sleep(0.5)

def ggTrig():
    ser.write(':%c%c%c' % (chr(0),chr(0),chr(61)))
    sleep(2)

def ggWritePA(bias1,bias2,bias3,bias4,bias5):
    ggLoad(2,bias1)
    ggLoad(3,bias2)
    ggLoad(4,bias3)
    ggLoad(5,bias4)
    ggLoad(6,bias5)
    ggTrig()

def ggWritePS(a,b,c,d):
    ggLoad(7,a)
    ggLoad(8,b)
    ggLoad(9,c)
    ggLoad(10,d)
    ggTrig()
```

C

GLIMMR Test Chips

C.1 GTC1

GTC1 contained several transistor characterisation structures as well as some small circuit designs. The goal was to characterise the process and validate the models. GTC1 was taped out in 2006. The full testchip layout is shown in Figure C.1.

C.2 GTC2

GTC2 contained several circuits including the transmission line PA in Chapter 5 and the single chip transmitter design in Chapter 7. GTC2 was taped out in 2007. The full

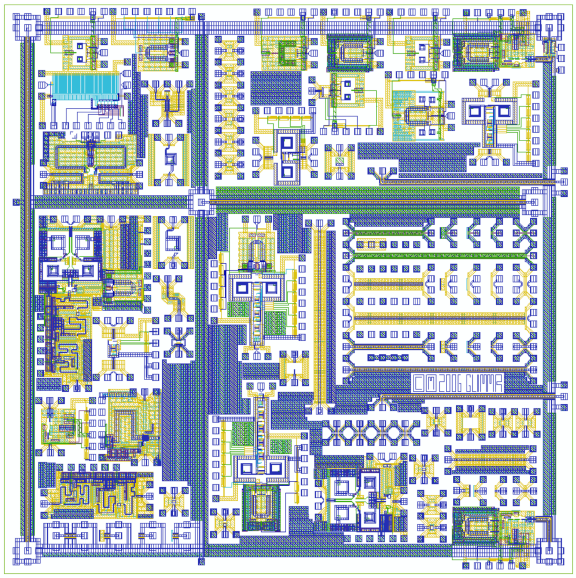


Figure C.1: *GLIMMR test-chip 1 (GTC1).*

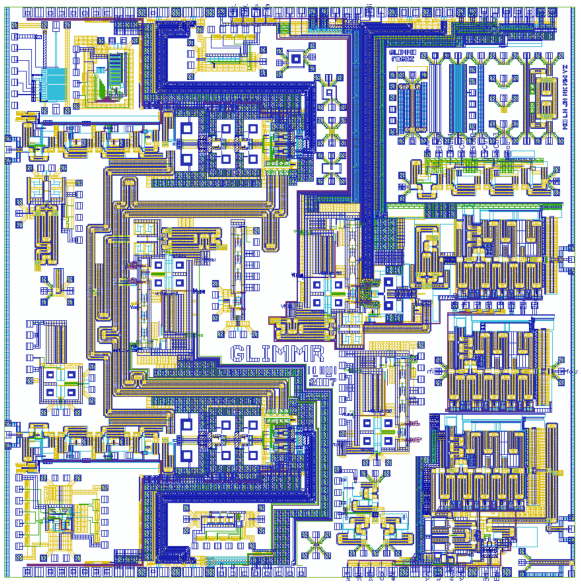


Figure C.2: *GLIMMR test-chip 2 (GTC2).*

testchip layout is shown in Figure C.2.

C.3 GTC3

GTC3 contained several circuits for a split-IF architecture including the transformer based PA in Chapter 6 and the split-IF transmitter presented in Chapter 7. GTC3 was taped out in 2008. The full testchip layout is shown in Figure C.3.

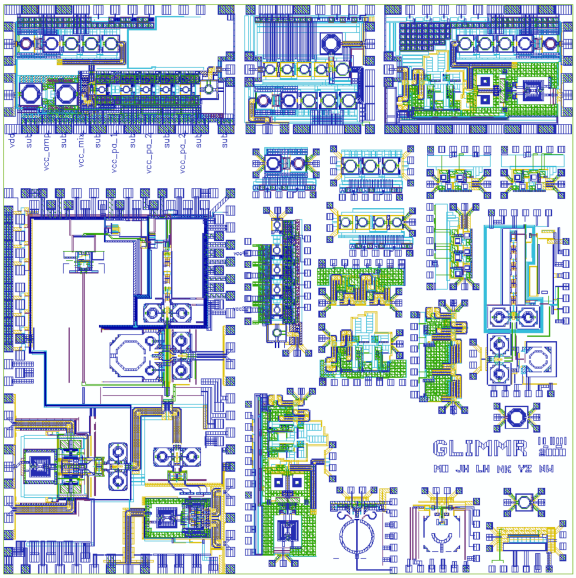


Figure C.3: *GLIMMR test-chip 3 (GTC3).*

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