ANALOGUE RF FRONT-END IC DESIGN FOR ULTRA-WIDEBAND IMPLANTABLE WIRELESS BODY AREA NETWORK RADIO

by

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ABSTRACT

Implantable wireless body area networks (WBAN) are a promising technology for health monitoring and treatment of patients requiring special care, where sensors are placed inside the human body to carry out measurements which may include telemetry or video streaming. Ultra-Wideband technology (UWB) is investigated as a candidate for the proposed implanted wireless body area sensor network due to its wide frequency spectrum and, hence, its low bit energy. UWB is introduced and then explored in terms of system constraints and circuit implementation.

In this work the author has explored the unlicensed frequency spectrum to achieve better communication for implantable medical devices, since the licensed frequency band has been occupied and is overcrowded. The advantages of the unlicensed frequency band technology include a wide bandwidth which allows for Gigabit data rates over short distances. This technology only requires low power consumption due to the low complexity of the Ultra-wideband system and the low transmit power. However, with the growing demand for wireless communications systems, more challenging requirements arise. Since a wide frequency range is required, the design of a transceiver front end in the entire frequency range is challenging. In this work the author has designed a transceiver RF front end, optimised for low power using Silicon on Sapphire (SOS) CMOS technology. The circuit designed has been fabricated and measured.

The author also describes how applicable UWB is used for implantable WBANs and invites future work on designing a radio capable of being installed inside the human body for medical care and monitoring.

STATEMENT OF CANDIDATE

I certify that the work in this thesis entitled **"Analogue RF Front-End IC Design For Ultra Wideband Implantable Wireless Body Area Network Radio"** has not previously been submitted for a degree nor has it been submitted as part of the requirements for a degree to any other university or institution other than Macquarie University.

I also certify that the thesis is an original piece of research and it has been written by me. Any help and assistance that I have received in my research work and the preparation of the thesis itself have been appropriately acknowledged.

In addition, I certify that all information sources and literature used are indicated in the thesis.

. . . . . .

IJI Ayobami Babatunde (Student ID:)

December 12, 2013.

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This thesis would not have been possible without the help, support and patience of my principal supervisor Professor Michael Heimlich in supervising my PhD. He gave me the best in terms of material and knowledge. He encouraged me to work on a variety of projects and thereby provided me with a well-rounded perspective in engineering education. His philosophy of researching fundamental issues that limit the availability of low-cost commercial electronics is both compelling and challenging. I am grateful to him for giving me the freedom to work on things that fitted within the framework of my project. He is an inspiring mentor and a good supervisor; he is always willing to assist.

I would like to express my gratitude to my co-supervisor Professor Anthony Parker for his words of advice as well as giving me books from his library on circuit design when I knocked at his door for assistance. Projects managed by him and Professor Eryk Dutkiewicz funded the circuit design tape-out; without them the tape-out would have been difficult.

This project is also partially funded by the David Skellern Electronics Research Grant.

I should like to thank Dr Xi Zhu (Forest) who now works at Nanyang Technological University, Singapore for his support and contributions to the success of my design. Many thanks are due to Oya Sevimli for sharing with me her experience in circuit design and measurement. Eahteshamul Hoque, Carl Svensson, Aaron Pereira and Sayed Albahrani are my colleagues in the office; they have also contributed in one way or another to the success of my research work. In particular Jabra Terazi provided a lot of support in device modelling; many thanks for

his assistance.

A special thanks to Dr Keith Imrie, an associate to the Department of Engineering, for his professional editorial advice on language and illustrations as well as completeness and consistency, and the program manager Daniel McGill for personally volunteering to provide assistance on professional editorial advice on language and illustration.

I have often greatly benefited from the experience and opinion of other researchers in the field and I should like to thank the following people for their indirect contributions to my thesis: Gengfa Fang and Ana Borba. On a personal note I want to express my regard for all members of staff at the Department of Engineering.

Finally, I acknowledge the encouragement and support given by my parents Chief MWO Olusogo Iji and mrs Sarah Iji; and other members of my family most especially my wife Rachael and our son Abraham; my uncle Comrade Sola Iji and his family; my siblings mrs Bankole Bosede, mrs Abbey Abidemi, mrs Alewi Oluwayemisi, mrs Isowa Abolanle, Pastor Michael Iji, Ayotunde Iji and Elizabeth Oluwakemi Iji.

To The Most High GOD and my father Thomson Olusogo Iji.

Romans 9:16 So then, it is not of him that willeth, nor of him that runneth, but of God that showeth mercy.

STATEMENT OF ORIGINALITY

The designs reported in this thesis were carried out at the Engineering Department, Faculty of Science, Macquarie University between August 2010 and December 2013, under the supervision of Professor Michael Heimlich and co-supervised by Professor Anthony Parker. I Also closely worked with a postdoctoral research fellow in the project, Dr Xi Zhu. The circuits designed in this thesis were fabricated at the Silanna foundry, which is the only silicon laboratory in Australia.

This thesis comprises of eight chapters and three appendix sections. An outline of the main achievements of the work for the thesis is given in Chapter 1. The work of others is acknowledged and referred to in the body of the thesis. The following paragraphs state those portions of the work which are claimed as original contributions of the author.

Chapter 2 and Chapter 3 contain a summary of the work of others. Chapter 2 is mainly background information on the importance of the technology, device process, and characterisation, and citations are been made from different books and publications. The work in Chapter 3 contains some details about the entire UWB system to be designed. Here the author has used existing link budget equations to calculate the required metric for the proposed system architecture.

In Chapter 4, circuit design commences, based on the details of the work in Chapter 2. The first stage of a receiver circuit after the receiving antenna, the low noise amplifier (LNA), requires special consideration and design techniques; some topologies used in the past for LNA circuit design are referred to in various books. In this work the author has proposed a low power LNA, achieved with

the SOS CMOS process technology as a result of it's low threshold operation capability.

The component that follows the LNA in the receiver chain is the mixer; in Chapter 5, the author has reviewed various mixer architectures which include active and passive types of mixer. Both types have been designed for experimental purposes to actually determine the most appropriate type for the receiver circuit. The author has designed both active and passive mixers from existing topologies but with the aim of utilising low power design. The idea of designing a passive mixer was initiated by the author. A passive mixer does not occupy much chip area compared to an active mixer. The circuits in Chapter 4 and Chapter 5 when cascaded make the receiver RF front end.

In UWB transmitter design the major components are the voltage controlled oscillator (VCO) and the pulse generator. In Chapter 6 various VCOs have been reviewed, and the Inductor Capacitor (LC) tank VCO type was proposed due to its low DC power consumption and better phase noise compared to others. The idea of using a MOS varactor was suggested by Dr Xi Zhu.

The pulse generator was designed by the author, who proposed that the pulse generator be driven by a VCO to generate the required UWB pulses.

In Chapter 7, describing the transceiver RF front end, the author has made cascade circuits of mixer and LNA which make up the receiver, and a combination of VCO and pulse generator which make up the transmitter. Chapter 8 concludes the thesis and give suggestions for future work.

Overall, most usage issues associated with the AWR simulation software were solved by Professor Michael Heimlich, and in circuit design layout, similar issues were solved by Dr Xi Zhu.

The material in this thesis has not been submitted towards another degree at

this or any other university.

List of Publications

Some of the work presented in this thesis has appeared as published peer-reviewed journal or conference papers, has been accepted for publication at the time of writing, or has been presented at conferences. I was the main contributor to the publications listed below.

1. Iji Ayobami, Forest Zhu and Michael Heimlich, "Design of Low Power, Wider Tuning Range CMOS Voltage Controlled Oscillator for Ultra Wideband Applications", IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), May, 2012. (cf. Chapter 6)

2. Iji Ayobami, Forest Zhu and Michael Heimlich, "Low Power, High gain, Low Noise Amplifier (LNA) for Ultra Wide-band Applications", Microwave and Optical Technology Letters, Vol. 55, Issue 12, February, 2013. (cf. Chapter 4)

3. Iji Ayobami, Forest Zhu and Michael Heimlich, "A Folded-Switching Mixer in SOI CMOS Technology", 55th Int'l Midwest Symposium on Circuits and Systems (MWSCAS), August, 2012. (cf. Chapter 5)

4. Iji Ayobami, Forest Zhu and Michael Heimlich, "A 3 - 5 GHz LNA in 0.25μm SOI CMOS Process for Implantable WBANs", 55th Int'l Midwest Symposium on Circuits and Systems (MWSCAS), August, 2012. (cf. Chapter 4)

5. Iji Ayobami, Forest Zhu and Michael Heimlich, "Proposed Ultra-Wideband System, and Receiver Circuit for Implantable Wireless Body Area Networks", 12th International Symposium on Communications and Information Technologies (ISCIT), October, 2012. (cf. Chapter 2)

6. Iji Ayobami, Forest Zhu and Michael Heimlich, "A Down Converter Active Mixer, in 0.25μm SOI CMOS process for Ultra Wide-Band Applications", International Symposium on Communications and Information Technologies (ISCIT), October, 2012. (cf. Chapter 5)

7. Iji Ayobami, Forest Zhu and Michael Heimlich, "High Gain/Power Quotient Variable-Gain Wideband LNA for Capsule Endoscopy Application", Microwave and Optical Technology Letters, Vol. 54, Issue 11, November, 2012. (cf. Chapter 4)

8. Iji Ayobami, Forest Zhu and Michael Heimlich, "A 4.5 mW 3 - 5 GHz Low-Noise Amplifier in 0.25μm Silicon-on-Insulator CMOS Process for Power - Constraint Application", Microwave and Optical Technology Letters, Vol. 55, Issue 1, January, 2013. (cf. Chapter 4)

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Chapter 1

Introduction

1.1 Motivation

The emergence of wireless communication has called for new developments and presented increasingly challenging requirements for improvements of the required technology and to foster more convenience to its users and consumers. However, today, challenges include development of a communication device suitable for implant inside the human body for video streaming and telemetry. The technology required to achieve this involves availability of high data access, long battery life, localisation and tracking capabilities, and applications offering un-disrupted service across different networks. As more devices rely on wireless, new technologies are presently facing spectral crowding and the coexistence of wireless devices is a major issue. Considering the limited bandwidth available and accommodating the demand for high data rates is a major task which requires substantive technology that can coexist with devices operating in various frequency bands. Ultra-Wideband technology is a potential candidate for the proposed implantable design; the IEEE TG 802.15.4a group has drafted several proposals for this technology and its implementation such that the carrier of the implantable devices or its user will be free from

other forms of hazards including electromagnetic radiation or electrical burns from the device component sub-assembly such as antenna or electronic components. These new developments in the world of wireless technology have improved medical technology and engineering, enabling the doctor or medical practitioner to have access inside the human body as many times as they want without the need for surgical operations, as technology has led to implantable wireless radios suitable for communication and video streaming inside the human body, using the unlicensed Ultra-Wideband frequency band.

1.2 Overview of Ultra-Wideband Technology

The majority of the initial concepts and patents for Ultra-Wideband (UWB) technology originated in the late 1960s at the Sperry Research Center (Sudbury, MA), then part of the Sperry Rand Corporation, under the direction of Dr Gerald F. Ross. At that time, this technology was alternatively referred to as baseband, carrier-free or impulse. The term "ultra-wideband" was not applied to this technology until 1989 according to [4]. Thus, by the early 1970s the basic designs for UWB signal systems were available and there remained no major impediment to progress in perfecting such systems. After the 1970s, the only innovations in the UWB field would come from improvements in particular instantiations of subsystems, but not in the system concept itself. The basic components were variously known, e.g., pulse-train generators, pulse-train modulators, switching pulse-train generators, detection receivers and wideband antennas. Moreover, particular instantiations of the subcomponents and methodologies were also known, e.g., avalanche-transistor switches, light-responsive switches, use of "sub-carriers" in coding pulse trains, leading-edge detectors, ring demodulators, monostable-multivibrator detectors, integrating and averaging matched filters, template signal-match detectors, correlation detectors, signal integrators, synchronous detectors and antennas driven by a stepped-amplitude input [5].

The pioneering work of Harmuth, Ross, Robbins, van Etten, and Morey [4] defined UWB systems and did so in a very practical manner. Others have contributed to particular instantiations of the subsystems described by these pioneers but, after these pioneering contributions, no one can, or should, lay claim to have invented the field of UWB radio, radar or communications, nor to have invented a particular component or components which made it practical. There never was a time such that a particular subcomponent invention was required for UWB systems to become possible, except, perhaps, the sample-and-hold oscilloscope. In the commercial arena, UWB systems have been utilised and commercialised beginning in the 1970s according to [5].

Today UWB communications has developed such that some of its characteristics have presented great advantages over traditional narrowband systems. The advantages of UWB emanate from Shannon's channel capacity formula which states that the capacity of a channel increases linearly with bandwidth and logarithmically with an increased signal-to-noise ratio (SNR). The Shannon's capacity formula can be stated mathematically as follows:

$$C = B \log_2(1 + \mathrm{SNR}) \tag{1.1}$$

From Shannon's capacity formula, it can be deduced that UWB communications has the capacity to offer both high-data-rate communications over short distances and low-data-rate communications over long distances. Hence, when the bandwidth is extremely large, only a very small signal power is needed to achieve a high data rate. This property offers a UWB system better performance than narrowband systems. UWB signals are also localised in the time domain, which enables precise location and ranging capabilities [6].

1.3 Ultra-Wideband Standards

Ultra-Wideband physical layer systems standards have been defined by the Institute of Electrical and Electronics Engineers (IEEE) for various usages. The IEEE 802.11 Task Group is responsible for Wireless Local Area Network (WLAN) standards and IEEE 802.15 is responsible for Wireless Personal Area Network (WPAN). UWB technology emerged as a potential solution for the IEEE 802.15.3a standard for WPAN, targeting high-data-rate, short-range multimedia applications. The UWB technology for 802.15.3a uses one or more carrier frequencies modulated by a baseband signal, which is essentially an extension of conventional narrowband wireless technology. However, UWB technology has also been adopted at the physical layer by the 802.15.4a low-data-rate task group. The IEEE 802.15.4a low-data-rate physical layer (PHY) Task Group for personal Area Networks (WPAN) was established in March 2004 to develop an alternative PHY to amend 802.15.4. The principal interest is in providing communications and high precision ranging/location capability (1 metre accuracy and better), high aggregate throughput, and ultra-low power, as well as adding scalability to data rates, longer range, and lower power consumption and cost. These additional capabilities over the existing 802.15.4 standard are expected to enable significant new applications and market opportunities [7]. The IEEE 802.15.4a Task Group selected a baseline specification with two optional PHYs consisting of (a) UWB impulse radio and (b) Chirped spread spectrum in the 2.4 ISM band. In contrast to IEEE 802.15.4 (low data rate), it is expected that UWB impulse radio will be able to deliver both communication and precision ranging.

1.3.1 IEEE 802.15.6 Task Group

Today, Task Group 4a has been further modified to IEEE 802.15 Task Group 6 (WBAN), with a standard suitable for real-time health monitoring of a patient and diagnosing many

life threatening diseases. Task Group 6 (WBAN) standard applies in close vicinity to, on, or inside a human body and supports a variety of medical and non-medical applications.

The IEEE 802.15.6 standard for WBAN has been ratified. The purpose of the standard is to define a communication system optimised for low-power in-body/on-body nodes (but not limited to humans) to serve a variety of medical and non-medical applications including consumer electronics/personal entertainment and others [8]. The baseline specification for Task Group 6 (WBAN) impulse radio covers the (3.1 - 4.6) GHz range and offers data rates of up to 10 Mbps.

1.3.2 Impulse Radio-Based UWB System

UWB technology has its origins in impulse radio, which has been studied since the early 1960s. In recent years, impulse based radio experienced a revival due to its promising properties for short range, low power and high speed applications [9]. It was also noted that the first efficient radio transmissions were performed on the basis of impulse transmission.

The major benefit of impulse radio is its low complexity. Compared to conventional receivers, no power-consuming Phase Lock Loop (PLL) synthesizers are required. Due to the large bandwidth available, the demands for frequency accuracy are much more relaxed. Impulse radios are used to generate very short pulses directly from baseband without a carrier, with the corresponding spectrum extending from DC up to microwave frequencies. As a result of its extreme bandwidth, they are capable of reduced interference, resistance against jamming, enhanced encryption and low probability of interception. Potential modulation schemes for UWB impulse radio include On-Off Keying (OOK), Pulse Amplitude Modulation (PAM), Binary Phase Shift Keying (BPSK) and Pulse Position Modulation (PPM).

However the impulse based WBAN UWB radio has the following advantages: low

complexity, low power, relaxed phase noise requirements, lower sensitivity to multipath, lower interference level, position location capability, low probability of interception and lower susceptibility to interference. UWB signals have been demonstrated to propagate through certain obstructions that cannot be penetrated by conventional narrowband systems; this property shows that UWB has very strong penetrating power as demonstrated by through-the-wall imaging systems and ground penetrating radar [10].

It was also noted that UWB impulse radio systems are resistant to multipath fading compared to narrowband systems. In narrowband systems, the received multipath signals of a given symbol can overlap with a subsequent received symbol due to multipath delay; because multipath delays are less than the symbol duration, the received signal from multipath can add either constructively or destructively. Whereas, for pulse based UWB radio the multipath delay is longer than the pulse width, such that the received pulse due to multipath can be resolved. Since the multipath delay is shorter than the time between two consecutive pulses, no overlap will occur between the multipath signals of the two symbols.

An impulse radio transmitter structure consists of a pulse generator, a timing circuit and a clock oscillator [10]. The desired waveform is produced by the pulse generator, while the clock oscillator defines the pulse repetition frequency. Step, Gaussian or Monocycle pulses are suited for UWB communication since they have a broadband frequency spectrum [11]. Hence, with ultra-short time domain pulses, impulse radio based UWB systems transmiting with a very short pulse duration (say nanoseconds) are similar to those used in radar. Impulse radio transmitters are less complex since no sophisticated filters are required. Power consumption is very low since the output power is restricted to avoid for interference with other standards.

1.4 Update on UWB CMOS Transceiver Design

Behzad *et al.* [12] present a UWB CMOS transceiver for multiband OFDM applications. The circuit consumed 105 mW of DC power, with a data rate of 480 Mbps. The circuit architecture in the design is more complex than for impulse radio (IR) and hence it consumes more energy. On the other hand, the CMOS process used in this design is more advanced.

Chi *et al.* [13] present a low power wireless transceiver analogue front end for an endoscopy capsule system. This design is not UWB since it operates at 2.5 GHz, the circuit consumes 29 mW of DC power, and the data rate is 1 Mbps.

A new development came in 2008 when a UWB system for wireless endoscopy emerged; as presented in [14] this work enables real-time diagnosis with high-resolution images. A non-coherent transmitted reference (TR) UWB architecture with differential binary phase shift keying (DBPSK) modulation, it uses the IEEE 802.15.4a channel model. The data rate is 125 Mbps; This work has shed more light on UWB transceiver design for implants. The transmitter in this design is all digital whereas digital circuits at these clock rates are power hungry compared to analogue circuits. Analogue circuits are considered when designing for low power applications.

Another work on CMOS IR-UWB transceiver design is presented in [15]; the proposed architecture in this work composed of a simple and robust design using a Gaussian monocycle impulse generator at the transmitter. The data rate is up to 5 Gbps and consumes 9 mW of power. This design is built on a more advanced 90nm CMOS technology. The transmitter modulation scheme is OOK, which is not as efficient as BPSK.

In 2011, another article on an IR-UWB transceiver was published [16]; this work exploits 6 - 10 GHz of the UWB band to achieve a higher data rate of 2 Gbps. The modulation scheme here is BPSK, due to its simplicity and energy efficiency, as a solution suitable for short-range wireless applications. The circuits are designed on 130nm

CMOS technology. Another publication in 2011 by Solda *et al.* [17] presented an IR-UWB transceiver operating in a similar frequency range as in [16]; the frequency band here is 7.25 - 8.5 GHz and the data rate is 5 Mbps. The circuit is built on 0.13μm CMOS technology.

Following the analysis of previous work on UWB transceiver design and their techniques for low power applications, there are various challenges associated with implementation, which include frequency of operation, modulation scheme, power consumption, circuit architecture etc. The proposed IR-UWB transceiver design in this project has been designed to strike a balance to achieve the design goals with limited resources available. A 3 - 5 GHz IR-UWB transceiver has been proposed using less complex circuitry, hence low power and a better transmit coverage area. The proposed transmitter is based on a BPSK modulator and the circuit is built on 0.25μm SOS process technology.

1.5 Author's Contributions

WBANs require short range, low power and highly reliable wireless communications for use in close proximity to or inside the human body. WBANs are divided into two categories depending on their operating environment: one is a wearable WBAN which mainly operates on the surface or vicinity of the human body and the other is called an implantable WBAN which operates inside the human body. This project has focused on how to make a simple and effective UWB impulse-radio RF front end, comprised of low complexity circuits at low power consumption, suitable for a high data rate. The circuits are designed for an implantable RF front end.

Impulse radio UWB (IR-UWB) promises a significantly higher data rate in low cost, low power wireless applications than conventional narrow-band systems, IR-UWB systems can have much simpler architectures and are more versatile under various channel

conditions. However, there are two important challenges in building an IR-UWB system:

I Ability to achieve large signal bandwidth, or, the ability to generate and process pulses with sub-nanosecond time resolution.

II Ability to accomplish this with low power consumption and low circuit complexity, which translate into low cost.

This work was designed on a 0.25μm CMOS process silicon-on-sapphire (SOS), which is one of the silicon-on-insulator (SOI) semiconductor manufacturing technologies. It is primarily used in aerospace and military applications because of its inherent resistance to radiation. This property makes it suitable for implantable medical electronics which we are explored in this work.

The main advantage for the electronic circuit in this project is the highly insulating sapphire substrate which prevents stray currents caused by EM coupling from spreading to nearby circuit elements. The benefit of the insulating substrate is its very low parasitic capacitance, which provides increased speed, low power consumption, better linearity and more isolation than bulk silicon. SOS has seen relatively little commercial use because of the difficulties in fabrication; they are very small transistors used in modern high-density applications. Because sapphire is a highly insulating substrate there is almost no parasitic capacitance. This provides a wide range of benefits in designs targeting RF, mixed signal/analogue and radiation hard applications.

Following the above devices properties, the author has designed transceiver RF front-end sub-circuits optimised for low power and low complexity.

1.6 Synopsis

This thesis is organised as follows; Chapter 1 introduces the general concept and technology required for the work in this thesis. The design of wireless radio for Ultra-Wideband

applications is discussed. A low power circuit design suitable for implantable radio is identified as a major obstacle. The aim of this thesis is to design low power circuits capable of a high data rate for implantable wireless applications.

Chapter 2 presents a comprehensive discussion on UWB transceiver architecture, analysing how to make a simple transceiver design, with low power consumption. Included in Chapter 2 are the device properties and characteristics.

Chapter 3 presents the link budget of the transceiver RF front-end design constraint as well as the requirements for the proposed transceiver. This helps to point out the requirements of the individual circuits to be designed and to maximise efficiency with low power design. A paper was published as a result of the review work in Chapter 2 and Chapter 3 as:

> Iji Ayobami, Forest Zhu and Michael Heimlich, "Proposed Ultra-Wideband System and Receiver Circuit for Implant Wireless Body Area Networks", *12th International Symposium on Communications and Information Technologies (ISCIT)*, October, 2012.

Chapter 4 presents the building blocks for the receiver sub-circuits RF front end, this includes circuit structure, optimisation techniques for low power without much degradation in the required signal. Fabricated circuits and measured results are also presented. In this Chapter, the following papers have been published:

> Iji Ayobami, Forest Zhu and Michael Heimlich, "Low Power, High gain, Low Noise Amplifier (LNA) for Ultra-Wideband Applications", *Microwave and Optical Technology Letters*, Vol. 55, Issue 12, February, 2013,

> Iji Ayobami, Forest Zhu and Michael Heimlich, "A 3 - 5 GHz LNA in 0.25μm SOI CMOS Process for Implantable WBANs", *55th Int'l Midwest Symposium on Circuits and Systems (MWSCAS)*, August, 2012,

Iji Ayobami, Forest Zhu and Michael Heimlich, "High Gain/Power Quotient Variable-Gain Wideband LNA for Capsule Endoscopy Application", *Microwave and Optical Technology Letters*, Vol. 54, Issue 11, November 2012,

and

Iji Ayobami, Forest Zhu and Michael Heimlich, "A 4.5 mW 3 - 5 GHz Low-Noise Amplifier in 0.25μm Silicon-on-Insulator CMOS Process for Power - Constraint Application", *Microwave and Optical Technology Letters*, Vol. 55, Issue 1, January 2013.

For chapter 5, in the receiver chain the next block to the LNA is the mixer. A down converter mixer, both an active and a passive type, for low power applications has been designed, with much design effort expended to achieve better linearity. The following papers have been published:

Iji Ayobami, Forest Zhu and Michael Heimlich, "A Down Converter Active Mixer, in 0.25μm SOI CMOS process for Ultra-Wideband Applications", *International Symposium on Communications and Information Technologies (ISCIT)*, October, 2012.

and

Iji Ayobami, Forest Zhu and Michael Heimlich, "A Folded-Switching Mixer in SOI CMOS Technology", *55th Int'l Midwest Symposium on Circuits and Systems (MWSCAS)*, August, 2012.

Chapter 6 presents the building blocks for the transmitter RF front end sub-circuits, this includes voltage-controlled oscillator and pulse generator circuit structure, optimisation for low power, design method, fabricated circuits and measured results. A paper has been published on this work as:

Iji Ayobami, Forest Zhu and Michael Heimlich, "Design of Low Power, Wider Tuning Range CMOS Voltage Controlled Oscillator for Ultra-Wideband Applications", *IEEE International Conference on Integrated Circuits Design and Technology (ICICDT)*, May, 2012.

Chapter 7 presents the transceiver front end, divided into receiver and transmitter. The receiver circuit is made up of the LNA and Mixer cascaded while the transmitter is simply the pulse generator and the VCO cascaded to produce UWB pulses. On this work a journal paper has been written and submitted as:

Iji Ayobami, Forest Zhu and Michael Heimlich, "Low Power, Highly Linear, 3.1 - 5 GHz UWB Receiver for Implantable WBAN Applications", *Submitted to IEEE Transactions on Circuit and Systems (TCASII).*

Chapter 8 is the concluding chapter; summaries of the system design are made as well as suggestions for future research. Also details of experience gained during the PhD program are listed. All equations and schematic diagrams relevant to Chapters 2 to 7 can be found in Appendices A and B respectively, while all abbreviations used in this thesis are in Appendix C.

Chapter 2

Background

2.1 Implantable WBAN Transceiver

Ultra-Wideband (UWB) technology is a promising technology for low cost, high data rate, short range, and low power consumption for wireless transmission. This technology was initially developed to solve problems related to short range communications. As technology advances, engineers design smaller and more compact communication devices for easy use and handling. The need for an implantable device is to be very small so that it will be easy for its user to carry without feeling its weight. There are various design issues that should be considered by the circuit design engineer to achieve better properties, as it requires specific design features. Hence, the circuit design topology must be carefully chosen as this determines the size and complexity of the entire design. This work has defined a simple transceiver structure suitable for implantable radio.

An implantable wireless technology has both benefits and challenges which need to be balanced. One of the chief obstacles to implanting wireless devices within the body is the deleterious effects of absorbed radio frequency energy. UWB technology is highly attractive for implantable Wireless Body Area Networks (WBAN) due to its ability to

transmit less energy per Hz within a wide spectrum and at a high data rate. While narrowband communication systems contain their data within a fractional bandwidth of less than 1%, the UWB system uses 20% or more for the same data rate. Secondly, narrowband and other wideband systems use radio frequency carriers to move the signal from baseband to the carrier frequency. Being a carrier-less technology, the implementation of UWB, is somewhat simpler and, therefore, it can be smaller due to its low complexity. However, UWB implementations can still be challenging. To get the several GHz of bandwidth, UWB must directly modulate an impulse, typically with requirements for very sharp rise/fall time. UWB is currently targeted for use between 3 and 10 GHz where significant absorption within the body is found, therefore making receiver signal-to-noise ratios (SNR) a concern.

2.2 Application Requirements

Part of the requirements considered here for the proposed UWB implantable WBAN is to transmit video inside the human body. A typical UWB PHY and MAC layer device should support (640 width 480 height) a resolution of 8 bits per pixel, 3 (Red, Green, Blue) bits for colour (2 frames per second) frame rate, at a data rate of 9.8 Mbps. An additional 50 Kbps is needed for telemetry and 50 Kbps for future use such as controls and actuators. Hence, up to 10 Mbps is sufficient to support no-compression, real-time multimedia applications. The principal requirement, however, of WBANs is low emission due to the fact that it is within the human body (but not limited to humans); hence the emitted power must be as low as possible to avoid damage to organs or tissue. Careful consideration of the regulations are stipulated by the International Commission of Non-ionizing Radiation Protection safety level (ICNIRP). The guideline includes the specific absorption rate (SAR) as the measure of energy absorption, which can be manifested

as heat, and gives a measure of the internal fields which could affect the biological system without heating (non-thermal interactions). The SAR is the rate at which radiation energy is absorbed by tissue per unit weight, and should be referred to as a maximum level. At 3 - 5 GHz, SAR should be $3.23 \times 10^{-6}(W/Kg)$ [18]. The low emission level means that the interference level of WBANs should be reasonably low so that it could be tolerable and tolerant of other wireless systems and serve as a short range communication technology [19]. Other design requirements for WBANs include high security and large scalability. WBANs require short range, low power and highly reliable wireless communications for use in close proximity to or inside the human body. WBANs are divided into two categories depending on their operating environment; one is a wearable WBAN which mainly operates on the surface or in the vicinity of the human body and the other is called an implantable WBAN which operates inside the human body [20].

2.3 UWB Standardisation and Spectrum Regulation

The Federal Communication Commission (FCC) spectral mask was released in February 2002 as 'The First Report and Order' (RO). The RO allowed commercialisation of UWB technology if the UWB design radiation adheres to the spectrum mask. A UWB signal has been defined as a signal whose fractional bandwidth, B_f, is greater than 0.25, where the definition of B_f is as follows:

$$B_f = 2\frac{f_h - f_l}{f_h + f_l} \tag{2.1}$$

where f_h and f_l are the higher and lower -10dB frequencies, respectively [21]. A signal is defined as being UWB if the -10dB signal bandwidth is 500 MHz or larger [22]. The existing FCC radiation limits for different indoor and outdoor UWB applications are presented in Figure 2.1; the Part 15 limit was included as reference, and permits the operation of authorised low-power radio-frequency (RF) devices without a licence from

the Commission or the need for frequency coordination under general emission limits [23]. According to the FCC Indoor Mask Part 15, for indoor emission, the maximum effective isotopic radiated power (EIRP) level in the 3.1 - 10.6 GHz band is set to -41.3 dBm/MHz. All UWB devices must meet this spectral mask for legal operation.

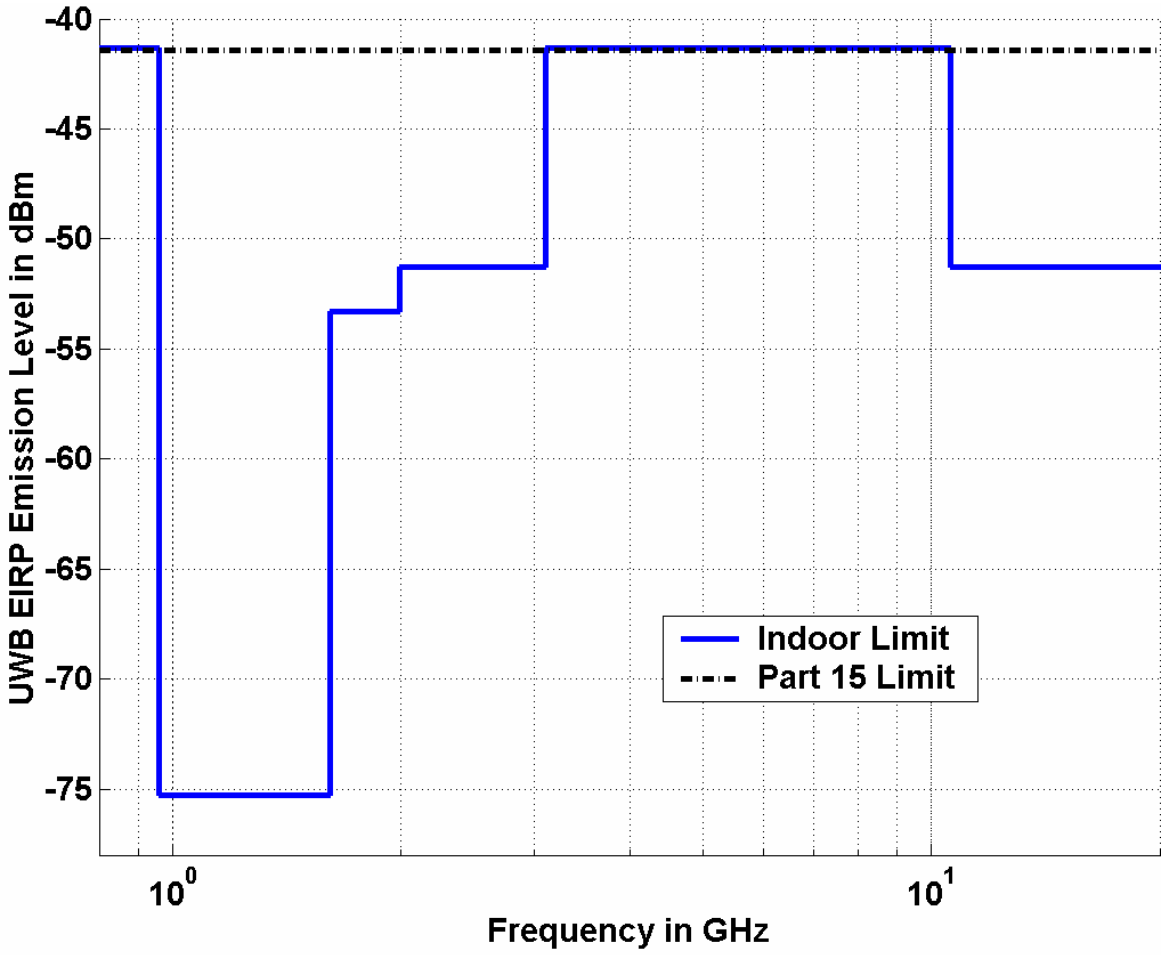

Figure 2.1: Spectrum Mask of UWB for Indoor Environments

The IEEE 802.15.6 Task Group 6 standards for WBAN's physical layer (PHY) operates in two frequency bands: low band and high band. Each band is divided into channels;

both of them are characterised by a bandwidth of 499.2 MHz. The low band consists of 3 channels 1 - 3 only, and it ranges from 3.1 - 4.6 GHz.

2.4 UWB Transceiver Architecture

This project is focused on implantable WBANs, whose basic function is to provide an effective and reliable network for transmission of data such as video through wireless communication links. WBANs can be used to provide assistance for automatic medical treatment, automated dosing and vital signal monitoring. The author considers implantable WBANs for video and other medical monitoring, in a situation where the device will be installed inside the human body to monitor in-situ, dynamic health related issues. As such, key considerations are signal propagation in terms of SAR and spectral mask, circuit implementation in terms of link budget, and overall performance over time as characterised by DC power.

The UWB definition by the FCC gives radio designers the opportunity to employ two different methods to design UWB systems: Impulse-Radio (IR-UWB) and Multi-Carrier based (MC-UWB). IR-UWB has a less complex hardware implementation, less demanding digital processing and greater resiliency to multipath fading effects. Hence, its simple implementation results in low power consumption and simple radio frequency (RF) circuitry. MC-UWB proponents claim greater spectral efficiency and flexibility, more efficient energy capture, but more complicated, bulky circuitry, and more power consumption. Hence, for implantable systems, low power consumption drives the focus of this work to IR-UWB, and then the proposed transceiver architecture is as shown in Figure 2.2. Furthermore, IR-UWB for communications is established by modulating an impulse waveform with sharp rise/fall times over the entire wide bandwidth. The pulse could last for several hundreds of picoseconds and have a bandwidth greater than 0.5

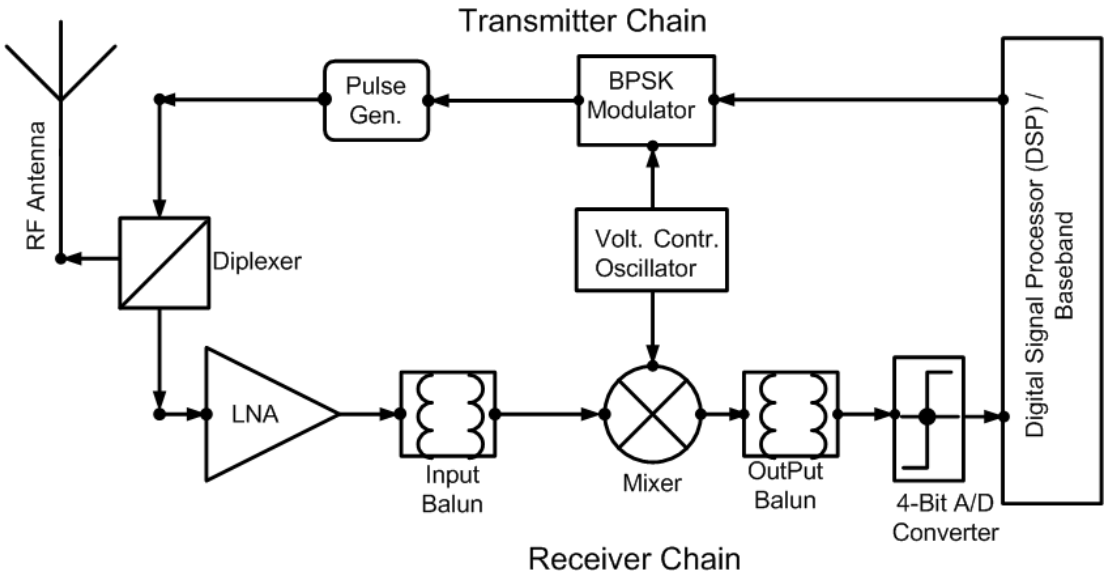

Figure 2.2: The UWB System for Implantable WBANs

GHz for more energy transfer. The Gaussian monocycle has been widely used for UWB design due to its appropriate mathematical properties and its good approximation to actual measurements. The pulse name (e.g. monocycle) simply means the number of zero crossing points in the time domain; for example Gaussian pulses do not cross the x-axis, while the Gaussian monocycle crosses the x-axis once. A train of Gaussian pulses without modulation causes discrete spectral lines with high peak power.

The human body is the medium for electromagnetic wave transfer in this work, hence we have to consider several issues related to the human body. The human body is not an ideal medium for radio frequency transmission. It is partially conductive and consists of materials of different dielectric constant, electrical conductivity, thickness, and characteristic impedance. Therefore, depending on the frequency of operation, the human body can lead to high losses caused by power absorption, centre frequency shift, and radiation

pattern destruction. The absorption affects the magnitude with both frequencies of the applied field and the characteristics of the tissue.

The electromagnetic penetration depth is one of the major issues considered. This is the measure of how deep electromagnetic radiation can penetrate into a material. As investigated, blood has the least penetration depth compared to bone, fat and other organs as well as the relationship between frequency, conductivity and penetration depth of blood as analysed in [24]. Considering the amount of energy absorbed by the human body, it is necessary to recognise that the percentage of incident radiation which is actually absorbed depends on the frequency and the orientation of the subject related to the field. In human tissue, RF radiation may be absorbed, reflected, or may pass through the tissue; it depends on the body structure and the tissue interfaces involved. These interfaces are the interactions from tissue to tissue, or tissue - air - tissue and are clearly complex in the human body. The depth of RF penetration of the human body is also an important factor. Following the FCC standard, the effective isotropic radiated power is limited for this technology at - 41.3 dBm/MHz [19].

2.5 Selected IR-UWB Modulation Schemes

Of the various types of modulation schemes used for IR-UWB modulation, few selected ones including, PPM, PAM, OOK and BPSK modulation scheme will be discussed in this section.

2.5.1 Pulse Position Modulation

Pulse Position Modulation (PPM) is based on the principle of encoding information with two or more positions in time, a pulse modulation technique that uses pulses having uniform height and width but displaced in time from some base position according to the

amplitude of the signal at the instant of sampling. Pulse position modulation has higher noise immunity since the UWB receiver detects the presence of a pulse at the correct time; the duration and amplitude of the pulse are not important [25].

2.5.2 Pulse Amplitude Modulation

Pulse Amplitude Modulation (PAM) is based on the principle of encoding information with the amplitude of the impulses and is the simplest form of pulse modulation that transmits data by varying the voltage or power amplitudes of individual pulses in a timed sequence of electromagnetic pulses. PAM can also be used for generating additional pulse modulations. In general, amplitude modulation is not the preferred way for most short-range communication. Furthermore, more power is required to transmit the higher amplitude pulse [25]

2.5.3 On-Off Keying

OOK is the simplest form of amplitude-shift keying (ASK) modulation that represents digital data as the presence or absence of a carrier wave. In its simplest form, the presence of a carrier for a specific duration represents a binary, one, while its absence for the same duration represents a binary, zero [25].

2.5.4 Binary Phase Shift Keying

Binary Phase Shift Keying (BPSK) is a type of phase modulation using two distinct carrier phases to signal ones and zeros. BPSK is the simplest form of PSK. It uses two phases which are separated by 180° and so can also be termed 2-PSK. It does not particularly matter exactly where the constellation points are positioned, just that they are 180° out of phase. This modulation is the most robust of all the PSKs since it takes serious distortion

to make the demodulator reach an incorrect decision. In bi phase modulation, information is encoded with the polarity of the impulses,

BPSK has an advantage over the other types of modulations due to an inherent 3 dB increase in separation between constellation points [26]. BPSK modulator guarantees superior matching between positive and negative pulses and supports high data rates at low power consumption, since its functional operation is in the digital domain

Implantable WBAN systems are designed for low power in order to achieve long battery life. A simple and efficient modulation scheme will enhance low power design, but there are few modulation schemes that actually support low power architecture; these include On-Off Keying (OOK), Differential Phase Shift Keying (DPSK) and Binary Phase Shift Keying (BPSK). All the above mentioned modulation schemes are well known and have relative advantages in bandwidth efficiency, sidelobe reduction, and ease of implementation [27].

The choice of the modulation scheme affects the amount of smoothing; the author has chosen binary phase shift keying (BPSK) for modulation because its implementation is simpler, it has a better bit error rate, and it accommodates the bandwidth required, compared to QPSK and other modulation schemes. The UWB BPSK transmitter consists of a pulse generator, a voltage controlled oscillator (VCO) and a driving amplifier, as shown in Figure 2.2. The transmitter generates an amplitude modulated signal by translating a digital pulse train into monocycle shaped signals with binary information data emitted by an antenna. The receiver consists of a low noise amplifier (LNA), balun, a Mixer (down converter), and an analogue to digital converter (ADC). Weak pulse sequences on the receiver side are amplified by the LNA, and the output of the LNA is fed to the single ended to differential balun so that fully differential signals are generated. Then the generated differential signals are self-mixed to down convert the received RF signal to baseband. The down converted signal from the mixer is shaped by an ADC whose output is the

recovered data. The pulse shape is sharp and is designed to concentrate energy over the broad range of 3.1 - 4.6 GHz at the -41.3 dBm/MHz power limit of the FCC spectrum mask of UWB. The important feature of the impulse-based transmitter is the absence of a power amplifier. The radio does not require intermediate frequency (IF) processing and this greatly reduces the transceiver complexity and overall power consumption. In an impulse radio receiver, the main function of the LNA is to achieve an input match to the impedance of the antenna for noise optimisation and in order to filter out-of-band interference. Subsequently a flat gain must be achieved over the entire bandwidth, as well as the minimum possible noise figure (NF) and low power consumption. The ADC will transfer signal processing to the digital domain and recover the information data for baseband digital signal processing.

2.6 The Proposed UWB WBAN Transceiver Design Requirements

In a WBAN system data transmission reliability and latency are extremely important. The reliability and latency of a WBAN will depend on the design of the physical and Medium Access Control layers (MAC). This layer determine the power consumption profile of a WBAN which is an important design issue. The MAC layer plays an important role in determining network efficiency and resource utilisation, which ultimately determines a system and the operating cost of a WBAN as mentioned in [28]. Also, a PHY layer could select appropriate modulation and coding techniques to combat transmission channel variability. The performance of a WBAN transceiver can be defined in term of its power efficiency.

Power Efficiency

Power management in a WBAN is a very important operational issue. Power usage can be minimised by optimising the PHY and MAC layer processes. A PHY layer can increase the probability of successful transmissions by selecting appropriate modulation and coding techniques. One attractive method of UWB signalling suitable for low power operation uses short pulses on the order of nanoseconds, to spread energy over at least 500 MHz of bandwidth. The baseband-like nature of this signalling promises a low cost, low power architecture because of the simplified analogue front-end design [29]. The power saving capability of this design is due to the elimination of frequency translation and synthesis, removal of filtering and reduction of external components.

A WBAN should be able to operate in a power constrained environment where power sources such as a battery could last for a longer period of time. Power optimization for the implantable nodes is critical in any design.

2.7 Design Process Technology

In design, the choices of components are really important as they have a great effect on circuit performance and durability, as well as the environment where the circuit is to be used. The life span of circuits can also depend on the materials used for their design, however, careful consideration is required in determining such components. Silicon-on-insulator technology (SOI) is one of the available technologies to fabricate integrated circuits. Traditional circuit manufacturing technologies employ a conductive and doped silicon wafer and, for this reason, are often referred as "bulk complementary metaloxide semiconductor (CMOS) processes". Bulk CMOS devices and circuits are manufactured on the silicon surface. SOI technologies use a silicon-on-insulator substrate in place of bulk substrates. This kind of substrate allows the reducuction of the parasitic capacitances

for each device and therefore provides improvements in performance. In this chapter the author discusses a type of SOI called silicon-on-sapphire (SOS), describing its advantages, the basic devices available and its current-voltage characteristics. SOS complementary metal-oxide-semiconductor (CMOS) technology has been used in radiation-tolerant applications since the 1970s. SOS technologies exhibit several characteristics that make them attractive for use in radiation environments, including an insulating sapphire layer below the active silicon that eliminates the parasitic inter-device bipolar structure associated with latchup in bulk devices. SOS technologies also have been reported to have smaller single event upset cross-sections than equivalent bulk processes [30]. Historically, the SOS process has been utilised and developed for its property of radiation tolerance (or radiation hardness), the ability to withstand environments with high radiation.

2.7.1 Characteristics of Silicon on Sapphire

SOS is one of the silicon-on-insulator semiconductor manufacturing technologies. It is an hetero-epitaxial process for integrated circuit manufacturing that consists of a thin layer of silicon grown on a sapphire (Al_2O_3) wafer at high temperature. SOS is part of the silicon-on-insulator (SOI) family of CMOS technologies. SOS is primarily used in aerospace and military applications because of its inherent resistance to radiation. The major advantage of SOS that makes it suitable for CMOS transistor design is that it is an excellent electrical insulator, preventing stray currents caused by radiation from spreading to nearby circuit elements [31]. SOS analogue circuits benefit from the insulating substrate to provide higher performance at lower power drain. However, the SOS process technology of 0.25μm is more advanced than a similar process technology in silicon-on-insulator or Bulk CMOS.

Some advantages of SOS as listed in [31]:

1. Ability to integrate RF CMOS, High Q passives, mixed signal, digital, memory and

EEPROM on a single die.

2. Very high linearity transistors (+38 dBm IP3 mixers).
3. High Q integrated inductors ($Q_L > 40$ at 2 GHz for 5nH inductor).
4. High isolation (> 50 dB between adjacent devices).
5. High performance RF CMOS: f_{max} typically $3 \times f_t$ (60 GHz at 0.5 μm; and 100 GHz at 0.25μm).
6. Multiple threshold options without additional cost.
7. An extremely low-loss substrate at RF frequencies.
8. Excellent ESD protection with low parasitics.
9. Enables new design options compared to GaAs due to availability of good PMOS transistors.
10. Optically transparent substrate for use in optical applications.
11. Processed in standard CMOS facilities.
12. Lower cost than other RF processes.

A smaller parasitic capacitances reduce the burden on devices and allow transistors to operate faster, as their capacitive load is reduced. Circuit instabilities due to undesired capacitive feedback are also significantly reduced.

2.7.2 Silanna Process Design Kit (PDK): Transistors Description

There are eight types of transistor in the Gx Silanna CMOS process: Five different N-channel transistors, and three different P-channel transistors. The transistor types are

summarised in Table 2.1. The minimum gate length for Peregrine SOS devices is 0.25μm at the time of this work.

Of the transistors described in the table, the most appropriate for RF application and low power is the IN-RF with its very low threshold voltage. For benchmarking of transistors, speed parameters are important; useful measures for the speed of transistors are the transition frequency (f_t) and the maximum frequency of oscillation (f_{max}). The transition frequency is defined as the frequency where the magnitude of the current gain $h_{21}(\omega)$ equals unity. Thus f_t serves as a useful speed measure for current switches.

2.7.3 SOS MOS Characteristics for Analogue Design

Device characteristics are a very important starting point for state-of-the-art analogue design in SOS. Such characteristics can be used to evaluate the best operating region for each transistor in the circuit, and to assess the constant (DC) current levels at each voltage setting. The characteristics also give a visual insight to high-order differential parameters, such as the small signal models and the device gain.

The MOSFET source and drain capacitances, as well as the gate bulk capacitance, were set to zero because the ultra-thin silicon lies on top of the Sapphire insulator substrate in the Silanna CMOS technology. This fact makes it unnecessary to model parasitic effects [2].

The devices were measured across temperatures from 27°C to 125°C but are expected to be extendable above and below these limits and the nominal power supply for this process is 2.5 V [2].

The RF transistor model macros contain the significant capacitive and resistive parasitics in the transistor layout up to the RF model extraction boundary in order to match RF measurements. The RF transistor has a fixed finger width of 8μm with the user being able to change the total width by the varying the number of fingers.

Transistor Type	Transistor Description	Approximate Short-channel Threshold Voltage (V)	Usage
IN	Intrinsic N-Channel	0.08	High performance digital
RN	Regular-V_t N-Channel	0.43	Digital and low-leakage applications
HN	High-V_t	0.70	Digital and low-leakage applications
IP	Intrinsic P-channel	-0.05	High Performance Digital
RP	Regular-V_t P-Channel	-0.41	Digital and low-leakage applications
HP	High-V_t P-Channel	-0.60	Digital and low-leakage applications
IN-RF	**Intrinsic N-Channel; similar core model as RN with a macro model added**	**0.08**	**RF applications**
RN-RF	Regular-Vt N-Channel similar core model as RN with a macro model added	0.43	RF applications

Table 2.1: Transistor Type Descriptions [2].

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2.7.4 Transistor IN-RF DC-IV Characteristics Analysis

Semiconductor manufacturing processes have evolved over time. Device engineers attempt to produce identical transistors with different processes, nevertheless, successive generations of process design (Process Define Kit) can exhibit unintentional, and sometimes unavoidable, performance differences, especially in characteristics not guaranteed on the data sheet. The DC-IV characteristics of the transistor were obtained as shown in Figure 2.3 with the drain-source voltage (V_{DS}) ranging from (0 - 2.5) V at 0.1 V intervals and the gate-source voltage (V_{GS}) ranging from (-0.5 - 1) V at 0.05 V intervals.

Another important performance parameter of the transistor is the Scattering (S)-parameters. At low frequencies most circuits behave in a predictable manner and can be described by a group of replaceable, lumped-equivalent black boxes. But at microwave frequencies, as the circuit element size approaches the wavelengths of the operating frequencies, such a simplified model becomes inaccurate. The physical arrangement of the circuit components can no longer be treated as a black box. We have to use a distributed circuit element model, and S-parameters provide a means of measuring, describing, and characterising circuit elements when traditional lumped-equivalent circuit models cannot predict circuit behaviour to the desired level of accuracy.

S-parameters turn out to be particularly convenient in many network calculations, and this is especially true for power and power gain calculations. The transfer parameters S_{12} and S_{21} are the measure of the complex insertion gain, and the driving point parameters S_{11} and S_{22} are the measure of the input and output mismatch loss. S-parameters are used to characterise RF and microwave components that must operate together, including amplifiers, transmission lines, and antennas (and free space). Because S-parameters allow the interactions between such components to be simply predicted and calculated, they make it possible to maximise performance in areas such as power transfer, directivity, and frequency response.

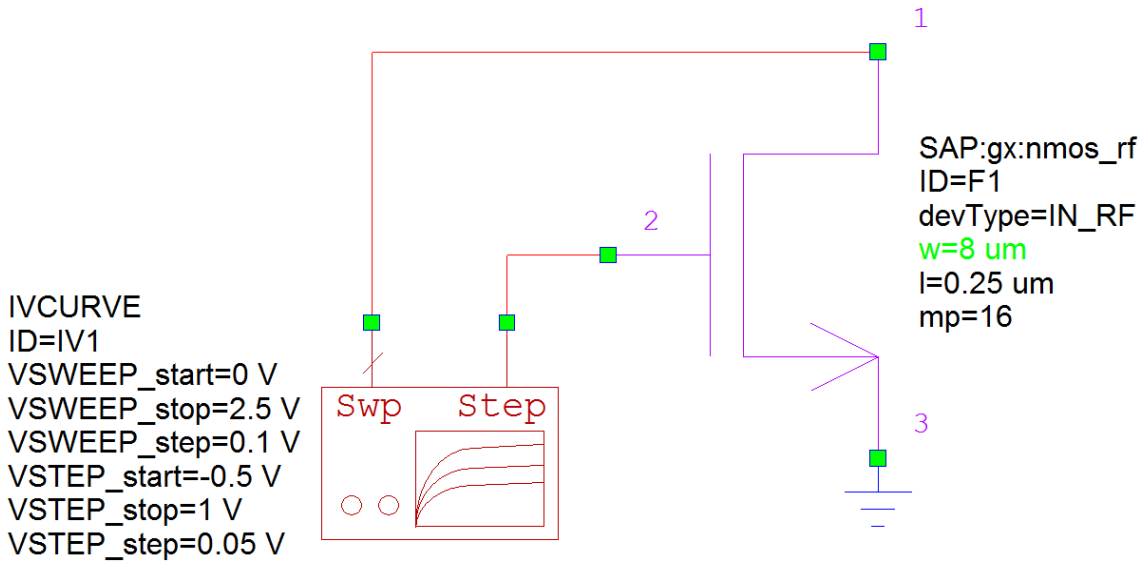

Figure 2.3: DC-IV Characteristics Circuit

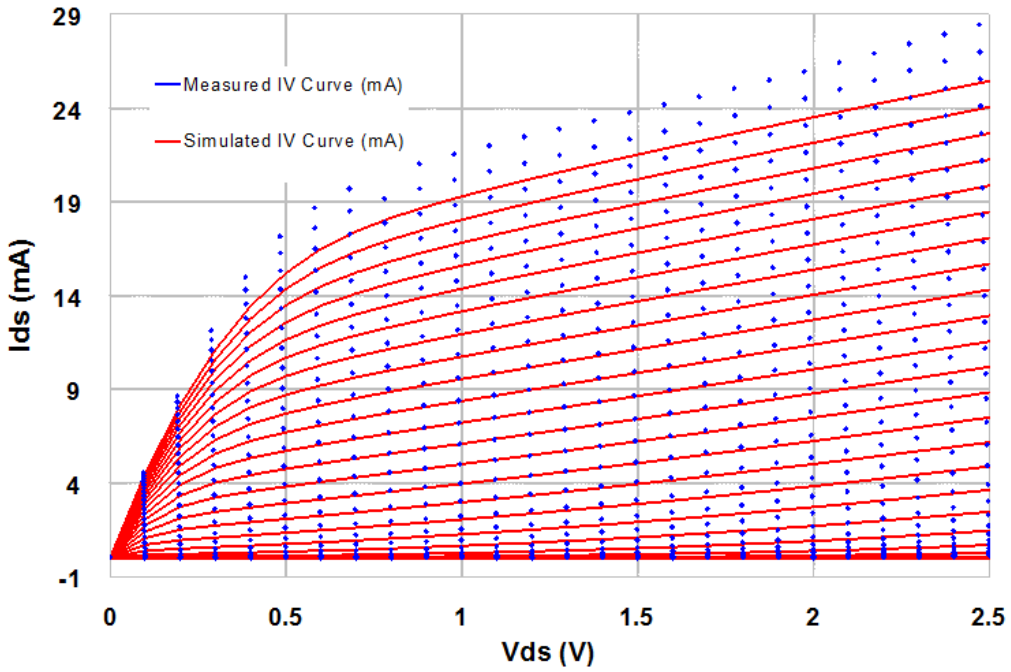

Figure 2.4: DC-IV Characteristics of the Transistor, Measured vs. Simulated

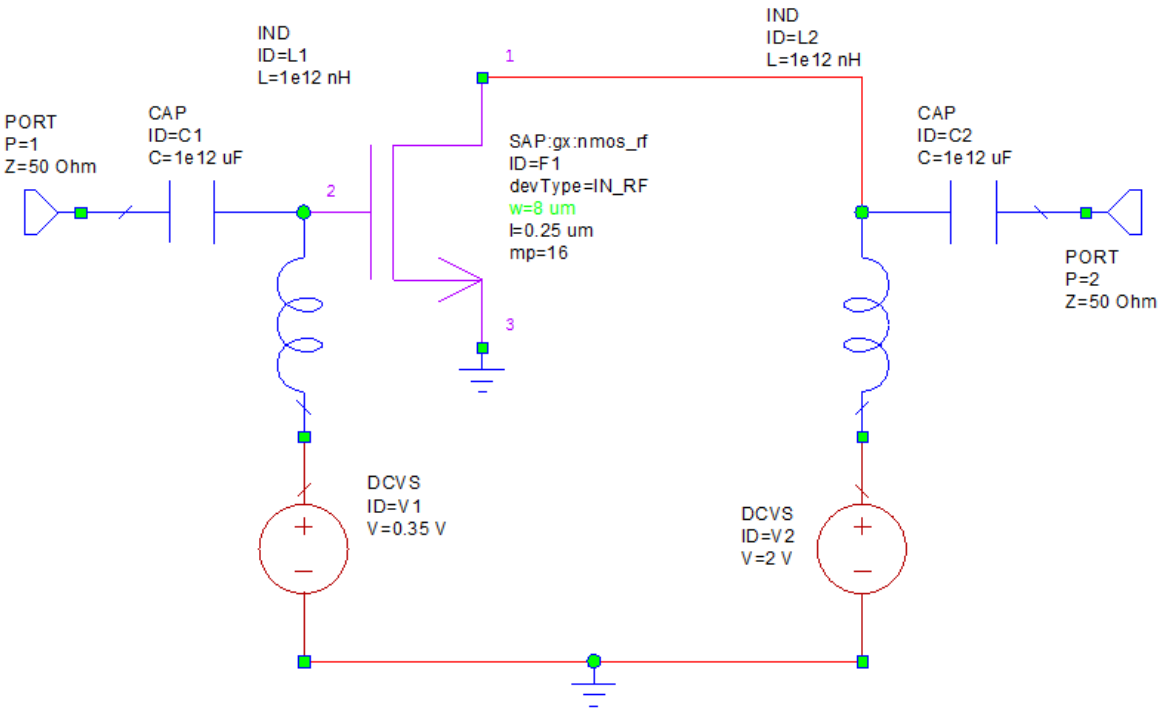

Figure 2.5: Simulation Setup for the Transistor S-Parameter

2.8 Discussion

The transistor IN-RF has the lowest threshold voltage as shown in Table 2.1 and its usage are for RF applications. It is the most suitable for low power design, hence there is need to verify some of its properties such as DC-IV characteristics to study its bias conditions and to compare its model in software with the actual transistor devices. Figure 2.4 presents the DC-IV characteristics of the transistor, measured versus simulated showing that the DC-IV characteristics are close. Another relevant properties is the measure of the Scattering Parameter of the transistor. The simulated S-parameter for the transistor was setup as shown in Figure 2.5 and 2.7. The results here shows how close the transistor model are to the actual transistor devices.

The simulated versus measured data in Figures, 2.5, 2.6 and 2.7 demonstrate that the models are sufficient for the intended designs here below 5 GHz, although they do depart somewhat at higher frequencies and extreme bias conditions perhaps because the Silanna process is optimized for digital design.

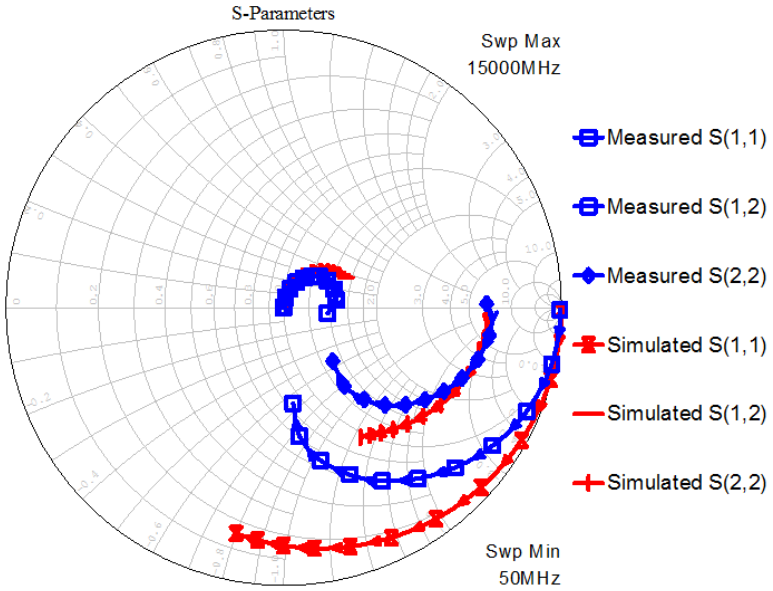

Figure 2.6: Simulated and Measured S-Parameters of the Transistor in Smith Chart

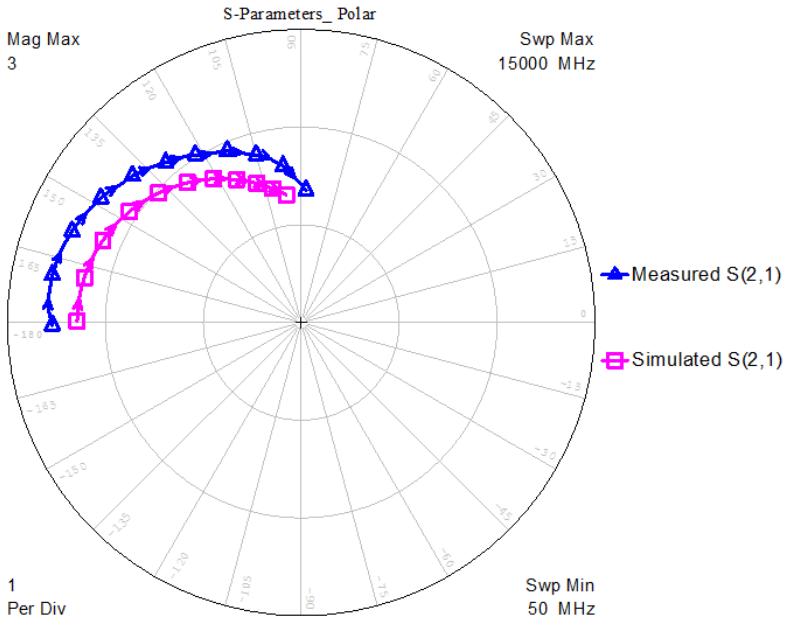

Figure 2.7: Simulated and Measured S-Parameters of the Transistor in Polar plot

2.9 Summary

Ultra-Wideband transmission is well-suited to short-distance applications, such as PC peripherals. Due to the low emission levels permitted by regulatory agencies, UWB systems tend to be short-range indoor applications. Due to the short duration of UWB pulses, it is easier to engineer high data rates; data rate may be exchanged for range by aggregating pulse energy per data bit (with integration or coding techniques). Conventional narrow band may also be used, but is subject to minimum-bandwidth requirements. The advantages of UWB systems are numerous, some of which include: impulse radio without carrier (free from sine-wave carriers), short pulse technique, so the required signal processing can be done in the baseband and no intermediate frequency (IF) processing is needed. This makes impulse radio devices much cheaper than other wireless communication devices, also, the battery life of a UWB device will be longer because of the very low transmitted power as well as the very low power consumption due to the simpler transceiver architecture.

The proposed transceiver has been studied, and details of the FCC regulation for part 15 indoor spectral mask have been considered. All requirements including ICNIRP and SAR were also studied to ensure a proper design measure for the proposed transceiver. Of the various standardisations that have been studied, the IEEE 802.15.6 TG6 standard for WBANs has been chosen for the proposed transceiver architecture. The low band channel of frequency range 3.1 - 4.6 GHz has been selected for this design since transmissions are better at lower frequency; they attenuate at higher frequency. The UWB transceiver architecture proposed here is the IR-UWB because of its simple implementation and low power consumption as compared to MC-UWB. The proposed transceiver is presented in Figure 2.2 showing all the building blocks in the receiver chain and the transmitter chain. Different modulation schemes have been considered and BPSK has been selected for this project.

Also, of various CMOS process technologies, the Silanna Library has been carefully chosen due to its excellent performance in a challenging RF design environment. The 0.25μm SOS process support larger voltages hence good power at lower currents, thereby conserving battery life. SOS is more tolerant of radiation, so for medical applications where the implant may be exposed to different imaging technologies, the electronics would have a longer life.

The transistor was properly measured and shown to agree with the PDK library model. The current-voltage (IV) characteristics and S-parameter measurements of the transistor were analysed and are presented in Figures 2.4 and 2.6 respectively; the results shows that the simulated and measured device characteristics are nearly but not exactly the same. This information is sufficient to analyse the transistor and to predict its performance in high frequency circuits. A smith chart proves to be very useful for the comparison of the S-parameters S_{11}, S_{12} and S_{22} as shown in Figure 2.6. The transmission coefficient S_{21} is plotted in a polar diagram as shown in Figure 2.7. The measured S-parameters represent data of a typical 0.25μm SOS n-channel CMOS device with a gate width of 8μm.

Chapter 3

IR-UWB System Analysis

3.1 Introduction

Ultra-Wideband Transceiver systems exchange data using short duration pulses due to the large signal bandwidth they possess. Thus a significant difference between conventional radio transmissions and UWB is that conventional systems transmit information by varying the power level, frequency, and or phase of a sinusoidal wave. UWB transmissions transmit information by generating radio energy at specific time intervals and occupying a large bandwidth. UWB promises low power implementation with fine time resolution and high throughput at short distances without interfering with other existing wireless communication systems. The wideband nature of the RF front-end architecture leads to a totally different design methodology from traditional narrow-band systems. In narrow band systems, phase response is not critical and the communication link budget can be calculated based on a single value like power level and gain. Additional details of the work reported in this chapter can be found in the author's publication [32].

3.2 Link Budget Analysis

3.2.1 Channel Model

The human body is the medium for electromagnetic wave transfer in this project, hence we have to consider several issues related to the human body. The human body is not an ideal medium for radio frequency transmission. It is partially conductive and consists of materials of different dielectric constants, thicknesses, and characteristic impedances. Therefore, depending on the frequency of operation, the properties of the human body can lead to high losses caused by power absorption, centre frequency shift, and radiation pattern destruction. This absorption affects the magnitude of the applied field and the characteristics of the tissue [3].

The electromagnetic penetration depth is one of the major issues considered. This is the measure of how deep electromagnetic radiation can penetrate into human fluid or tissue. As investigated, blood has the least penetration depth compared to bone, fat or other tissue in the human body. Table 3.1 shows the relationship, at various frequencies, of the conductivity and penetration depth of human intestine.

Frequency (GHz)	**Conductivity (s/m)**	**Relative Permittivity**	**Loss Tangent**	**Penetration Depth (cm)**	**Wavelength (cm)**
3.10	3.7303	53.191	0.4067	1.06	1.30
3.50	4.1103	52.486	0.4022	0.95	1.16
4.00	4.622	51.634	0.4022	0.84	1.02
4.50	5.170	50.801	0.4066	0.75	0.92
4.80	5.517	50.306	0.4106	0.70	0.86
5.00	5.1565	57.89	0.3202	0.79	0.78

Table 3.1: Dielectric Properties of Human Intestine: A Worst-case Scenario [3]

3.2.2 Multipath and Fade Margin

Multipath occurs when waves emitted by the transmitter travel along different paths and interfere destructively with waves travelling on a direct line-of-sight (LOS) path. This is sometimes referred to as signal fading. This phenomenon occurs because waves travelling along different paths may be completely out of phase when they reach the antenna, thereby cancelling each other. The amount of extra RF power radiated to overcome this phenomenon is referred to as fade margin. The exact amount of fade margin required depends on the desired reliability of the link, but a good rule of thumb is 20 dB to 30 dB according to [33]. The Fade Margin is the difference between the Received Signal Strength and the radio Receiver Sensitivity.

The power loss at a distance (d) after travelling through the body is given as:

$$P_L(d) = e^{-\alpha d} \tag{3.1}$$

$$\alpha = \omega \sqrt{\frac{\mu\epsilon}{2}\left[\sqrt{1+\left(\frac{\sigma}{\omega\epsilon}\right)^2}-1\right]} \tag{3.2}$$

where α = Absorption coefficient, d = Distance travelled by wave and, by definition, ω is the angular frequency, μ is the permeability, ϵ is the permittivity, and σ is the conductivity. In the frequency range of (0.1 - 10) GHz, the dielectric constant (ratio of the permittivity in material to that in vacuum) has a value of 5-70 for soft tissues, and the conductivity has a value of 0.02 - 3 $\Omega^{-1}m^{-1}$ [34], [35], [36]. The complex dielectric properties of tissues at various microwave frequencies determine the propagation and absorption distribution of microwaves. Hence, the induced pressure depends on the microwave intensity and complex dielectric constant of the tissue samples [37]. $\alpha \cong 1.179 \times 10^2 m^{-1}$ has been chosen as an average value for tissue, since penetration depths are the inverse of the absorption coefficients according to [37]. At a distance (d) equal to 2 cm, the power loss $P_L(d)$ is calculated to be 10.24 dB. Hence, the total power loss due to absorption and refraction

through the human body is given by

$$P_L(\text{total}) = P_L(d) + P_L(n) \tag{3.3}$$

where $P_L(n)$ = power loss due to refraction of the radio wave through the human body and n = $\sqrt{\mu_r \epsilon_r}$ according to Snell's law, from Table 3.1, ϵ_r is approximately 57.89 (worst case) and μ_r is close to 1 for most materials. Then, $P_L(n)$ = 8.81 dB power loss. The total power loss $P_L(total)$ = 19.05 dB.

3.2.3 Range and Path Loss

As radio waves propagate in free space, power falls off as the square of range. For a doubling of range, the power reaching a receiver antenna is reduced by a factor of four. This effect is due to the spreading of the radio waves as they propagate. Radio wave propagation in the human body can be calculated as follows

$$L_{\text{fs}} = 20 \log_{10}(4\pi D/\lambda) \tag{3.4}$$

where D is the distance between transmitter and receiver which is 2 cm, λ is the wavelength in human body rather than free space. From table 3.1 the average wavelength (λ) = 10 cm. Hence the path loss or propagation loss (L_{fs}) = 8 dB.

3.2.4 Noise Power

All objects which have heat emit RF energy in the form of random (Gaussian) noise. The amount of radiation emitted can be calculated by

$$N = kTB \tag{3.5}$$

where, k is Boltzman's constant ($1.38 \times 10^{-23} J/K$) T is the system temperature, usually assumed to be 290K, and B is the channel bandwidth (1.5 GHz). Hence $N = 1.38 \times 10^{-23} J/K \times 290K \times 1500,000,000 s^{-1} = 6.003 \times 10^{-9}$ mW = -82.22 dBm.

Noise Figure (NF) is a measure of the amount of noise added by the receiver itself. Here, it is assumed to be 12 dB. Receiver Noise Floor = -82.22 dBm + 12 dB = -70.22 dBm.

3.2.5 Receiver Sensitivity

Receiver sensitivity indicates how faint an RF signal can be successfully detected and processed by the receiver. The lower the power level that the receiver can successfully process, the better the receiver sensitivity. Receiver sensitivity is expressed using the version of decibel employed in measurements of radio power, the dBm. Sensitivity in a receiver is normally taken as the minimum input signal S_{min} required to produce a specified output signal having a specified signal-to-noise ratio (SNR) and is defined as the minimum signal-to-noise ratio times the mean noise power (N).

$$S_{min} = \text{SNR} \times N \tag{3.6}$$

$$SNR = (E_b/N_o \times (R/B_T)) \equiv (E_b/N_o)_{dB} + 10\log(R/B_T) \tag{3.7}$$

$$S_{min} = (E_b/N_o \times (R/B_T)) \times kTB \tag{3.8}$$

In theory for BPSK, when Bit Error Rate (BER) = 10^{-6}, then E_b/N_o = 10.5 dB, R is the data rate = 10 Mbps and B_T is the bandwidth.

Then by substituting into 3.7, SNR = 10.5 dB + 10 log(10 Mbps/1500 MHz) = -11.3 dB

$$P_{rx} = \text{Receiver Noise Floor} + \text{SNR} \tag{3.9}$$

$$P_{rx} = \text{-70.22 dBm - 11.3 = -81.52 dBm}$$

NB: tx stands for transmitter and rx stands for receiver.

$$P_{tx} = \text{EIRP} - G_{tx} - G_{rx} + L_{fs} + \text{Fade Margin} \tag{3.10}$$

The Effective Isotropically Radiated Power (EIRP) is -41.3 dBm, antenna gain at transmitter and receiver are both assumed to be 0 dB. Then equation 3.10 can be rewritten as

$$P_{tx} = \text{EIRP} - 0 - 0 + L_{fs} + \text{Fade Margin} \tag{3.11}$$

P_{tx} = -41.3 dBm + 8 dB + 19.05 dB = -14.25 dBm

3.2.6 Link Budget Calculation

The link budgets of the IR-UWB implantable WBAN's analogue front end transceiver are shown in Table 3.2 below. Given that EIRP is -41.3 dBm, antenna gain is assumed to be 0 dB.

Parameter	**Value**
Data Rate (R)	10 Mbps
Propagation Loss (L_{fs})	8 dB
Noise Power (N)	-82.22 dBm
Receiver Power (P_{rx})	-81.52 dBm
Transmitter Power (P_{tx})	-14.25 dBm
Implementation Loss	2 dB
Power (DC)	10 mW

Table 3.2: Link Budget for the Proposed UWB Transceiver

3.3 Prospective Circuit DC Power Consumption

Considering the amount of energy absorbed by the human body it is necessary to recognise that the percentage of incident radiation which is actually absorbed depends on the

frequency and the orientation of the subject related to the field. In human tissue, RF radiation may be absorbed, reflected, or may pass through the tissue. What happens depends on the body structure and the tissue interfaces involved. These interfaces are the interactions from tissue to tissue, or tissue - air - tissue and are clearly complex in the human body. The depth of RF penetration of the human body is also an important factor. Following the FCC standard, the EIRP required for this technology is -41.3 dBm; having considered the required output power, we have chosen to design the required circuit at a very low current. The current consumption was calculated as follows according to [14].

$$I = \frac{1000 \times 10^{-}3Ah}{5\text{days} \times 24h} = 8.3\text{mA}. \tag{3.12}$$

With a very small battery that will produce a voltage source at about 1.2 V DC the entire power consumed by the system could be approximately equal to 10 mW. Therefore, the author intends to drive power as low as possible as well as the radiation, to ensure that the operation is below the regulated standard as stipulated by the ICNIRP. The electromagnetic penetration depth is another issue we have to consider. The MC-UWB wireless transceiver system implemented in CMOS consumes 10.5 mW at 1.5 V DC [14] and the author anticipated lower power consumption for the IR-UWB design. A camera and LED for lighting would add a few mW of additional power drain over and above the transceiver requirements [38]. This gives approximately 15 mW of DC consumption. Pill-based wireless camera systems, the size of a large vitamin pill, for use in the human body have been outfitted with silver-oxide batteries delivering 165 mW-hours at 3 V [38], assuming a DC-DC converter from 3 V to 1.5 V at 90%.

3.4 Discussion

The transceiver RF front end has been analysed. A careful analysis of a channel model for the human body has been properly considered at different frequencies. The author has considered how deep electromagnetic radiation can penetrate into human tissue. Although the human tissue is considered to be lossy, Multipath and Fade margin have been defined for the human body and the power loss calculated.

In this chapter, the link budget for the proposed transceiver has been calculated and the required parameters such as path loss, Noise Power and Sensitivity of the system were calculated. Table 3.2 presented the required link budget for the proposed UWB transceiver RF front-end design, and the required process technology with excellent electrical properties has been chosen.

Chapter 4

Wideband Low Noise Amplifier

4.1 Introduction

The first stage of a receiver is typically, a low noise amplifier (LNA), whose main function is to provide enough gain at a low enough noise figure to overcome the noise of subsequent stages such as the mixer while actually receiving the signal. Aside from providing gain while adding as little noise as possible, an LNA should accommodate large signals without distortion, and frequently must also present a specific impedance, such as 50Ω; to the input source [1]. Low-noise amplifiers are required in receiver systems to increase the amplitude of the very low-level signals from the antenna without adding too much noise. Amplifier applications may require minimum noise, maximum gain, maximum power output, best impedance matching, stability into varying loads, large bandwidth, cascading with other circuits, and other performance features.

A design strategy has to be developed to balance the amplifier gain, input and output impedance, noise figure, and power consumption. The device model has to be properly considered, that is the transistor, which is the most important component and as such should exhibit high gain, low noise figure, stability and offer high linearity performance at

the lowest possible current consumption. The transistor scattering parameters should be examined at different drain-source voltages and levels for frequencies ranging from low to high. Another design consideration is that several LNA topologies need to be examined for proper choice of good design.

In LNA design there are few principles that need to be fulfilled in order to achieve a meaningful design; this includes proper matching networks and stability factors. The input and output matching network are to be matched to 50Ω; the input matching network is an LC arrangement and the output network is made of a buffer amplifier. Stability has to be achieved for the amplifier in the specified frequency range; required stability factors are the K-factor of greater than one and the B-factor of greater than zero. If stability factors are not met, the circuit will oscillate. Additional details of the work reported in this chapter can be found in the author's publication [39], [40], [41] and [42].

4.2 Device Noise Model

The device model has a strong contribution to the integrated circuit (IC) designer's freedom to select what performance is required for the design. The understanding of the device as a model enables the designer to choose lumped elements required to build up the intended circuit that comes in the choice of foundry kit. In principle, one can obtain the minimum noise figure from a given device by using the optimum source impedance defined by four parameters: the correlation conductance (G_c), correlation susceptance (B_c), noise resistance (R_n), and unilateral conductance (G_u) [1]. The MOSFET noise model consists of two sources; the mean-square drain current noise is

$$\overline{i_{nd}^2} = 4KT\gamma g_{do}\Delta f; \tag{4.1}$$

and the gate current noise is

$$\overline{i_{ng}^2} 4KT\delta_{gg}\Delta f, \tag{4.2}$$

where

$$g_g = \frac{\omega^2 c_{gs}^2}{5 g_{do}}$$

Also the gate noise is correlated with the drain noise, with a correlation coefficient defined as:

$$c \equiv \frac{\overline{i_{ng}.i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}.\overline{i_{nd}^2}}}$$

.

According to [1] the long-channel value of c is theoretically j0.395; for simplicity C_{gd} will be neglected since the achievable noise figure in not really affected by C_{gd}.

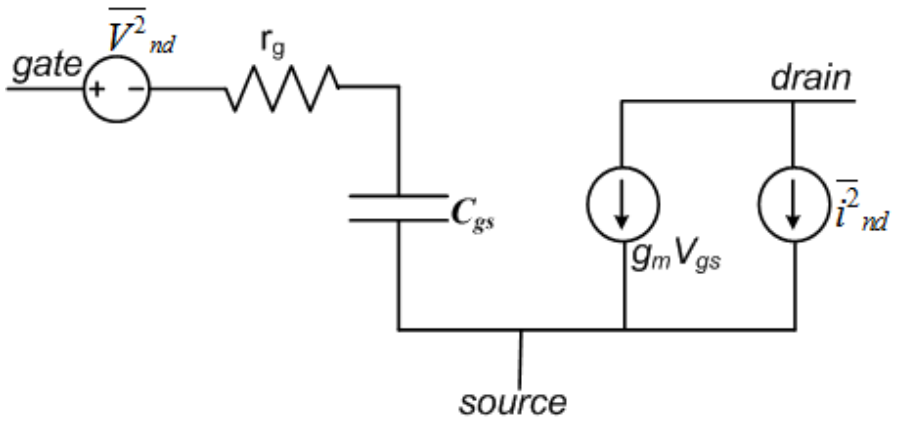

Figure 4.1: MOS Noise Model [1]

The four equivalent two-port noise parameters can be expressed as follows:

$$G_c \sim 0 \tag{4.3}$$

(The correlation admittance is purely imaginary, so that $G_c = 0$.)

$$B_c = \omega C_{gs} \left(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right) \tag{4.4}$$

$$R_n = \frac{\gamma g_{d0}}{g_m^2} = \frac{\gamma}{\alpha}.\frac{1}{g_m} \tag{4.5}$$

$$G_u = \frac{\delta\omega^2 C_{gs}^2(1-|c|^2)}{5g_{d0}} \tag{4.6}$$

The minimum noise figure can be given as

$$F_{min} = 1 + 2Rn[G_{opt} + G_c] \approx 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{4.7}$$

In principle, increasing the correlation between drain and gate current noise would improve the noise figure, although correlation coefficients unrealistically near unity would be required to effect a large reduction in the noise figure. Another important factor is improvements in ω_T that accompany technology scaling, improving the noise figure at any given frequency [1].

4.3 Low Noise Amplifier Topologies

There are four types of LNA topologies as follows: Common-source, Common-gate, Common-emitter, and Common-base LNA. Following these topologies there are several matching networks desired for wideband applications. They can be listed as follows: the Common-source amplifier with shunt input resistor, Shunt-series amplifier ($1/g_m$ termination), the common gate amplifier (Passive feedback termination), and inductively degenerated common-source amplifier.

4.3.1 Common-source amplifier with shunt input resistor

The common-source amplifier with shunt input resistor is a straightforward approach providing a reasonable broadband 50Ω termination. The shortcoming of this method is that resistor R_G adds thermal noise of its own and attenuates the signal by a factor of two ahead of the transistor. Hence a common-source amplifier with shunt input resistor is an unacceptable configuration due to its high noise figure [1].

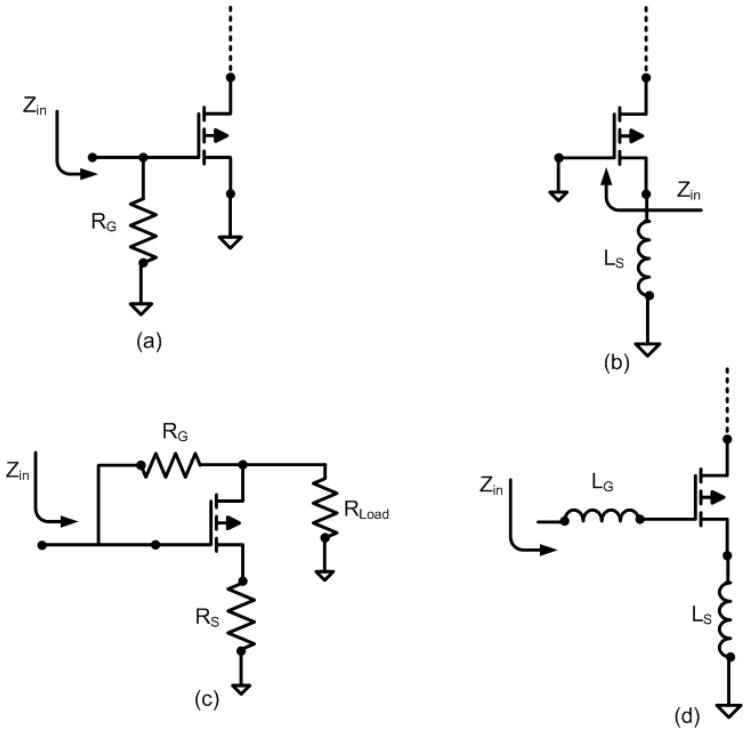

Figure 4.2: (a) Common-source Amplifier with Shunt Input Resistor, (b) Shunt-series Amplifier ($1/g_m$ termination), (c) Common Gate Amplifier (Passive feedback termination), (d) Inductively Degenerated Common-source Amplifier

4.3.2 Shunt-series amplifier ($1/g_m$ termination)

The shunt-series amplifier ($1/g_m$ termination) is another method; the resistance looking into the source terminal is $1/g_m$, and a proper selection of device size provides the desired 50Ω termination. This method is suitable at low frequencies since gate noise can be neglected, but the noise figure will be significantly worse at high frequencies when the gate noise is taken into account [1].

4.3.3 Common gate amplifier (Passive feedback termination)

The common gate amplifier (Passive feedback termination) and Shunt-series amplifier are similar but suffer fewer problems than the previous one; the resistive feedback network continue to generate its own noise and then fails to present to the transistor an equal optimum impedance at all frequencies. As a result the overall noise figure could be better than the previous methods but is generally still larger than the device minimum noise figure F_{min} by a considerable amount.

4.3.4 Inductively degenerated common-source amplifier

A preferable method is to employ an inductive source degenerated amplifier method. With such an inductance, current flow lags behind the applied gate voltage. The advantage of this method is that one has control over the value of the real part of the impedance through choice of inductance [1]. This method will be adopted, and will be discussed through the rest of this chapter.

4.4 Proposed LNA architecture and Topology

The matching networks are essential as they are responsible for impedance transformation of the circuit looking at the circuit such that they are matched to 50Ω, and the output matching network (OMN) can also be matched in the same way. The block diagram in Figure 4.3 shows the arrangements of the input matching Network (IMN) and the OMN, matched to the low noise amplifier.

4.4.1 The Proposed Low Noise Amplifier Circuit

The LNA topology in Figure 4.2(d) has a source inductance L_s chosen to provide the desired input resistance equal to R_s (source resistance). Since the input impedance is

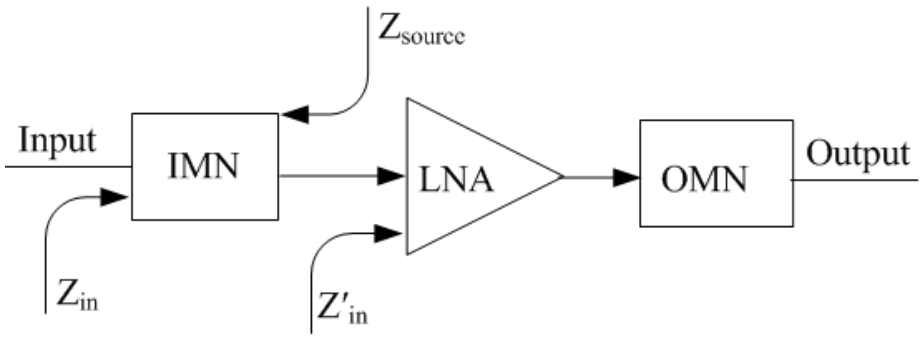

Figure 4.3: LNA Matching Network

purely resistive only at resonance, an additional degree of freedom, provided by the gate inductance L_G, is needed to guarantee a purely resistive input.

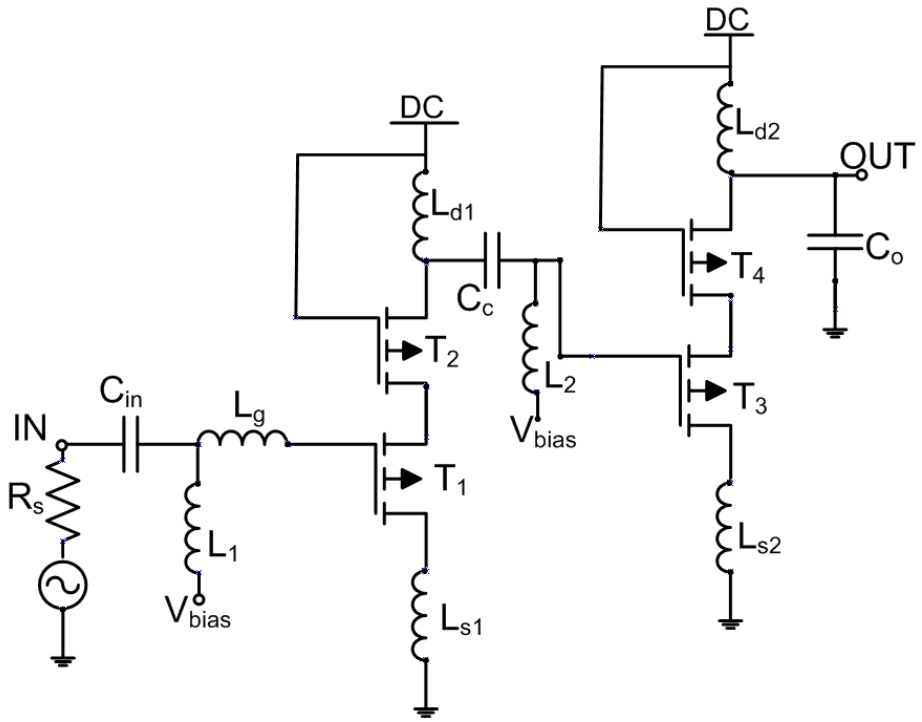

Figure 4.4: Low Noise Amplifier Circuitry

The proposed LNA topology consists of two cascode amplifier circuits; the first stage is optimised for noise performance and the second for linearity as described in [43]. The noise parameters of a cascode amplifier can be given by;

$$R_N = \frac{\gamma}{\alpha}.\frac{1}{g_m} = \frac{\overline{v_i^2}}{4kT\triangle f} \tag{4.8}$$

$$B_{opt.} = -j\omega C_{gs}\left(1 + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{4.9}$$

$$G_{opt.} = \omega C_{gs}\alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{4.10}$$

$$F_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{4.11}$$

where $\alpha = \frac{g_m}{g_{do}}$, g_{do} is the drain-source conductance, ω is the frequency of interest, ω_T is the cut-off frequency, γ is the coefficient of drain noise, δ is the coefficient of gate noise and c is the correlation term [44]. In [44], it was noted that the noise parameter $Z_{opt}^{'}$ is for a cascode amplifier with no degeneration inductor as mentioned in [45], hence it is neglected in this design.

4.4.2 Input Impedance Matching Network

The input matching network is responsible for a low noise figure and for stability of the amplifier. As recorded in [46] a bandpass filter incorporates the input impedance of the cascode amplifier as part of the filter, and shows good performance while dissipating small amounts of DC power. In CMOS technology, the transition frequency is achieved through small C_{gs}, which means that the tuned circuit tends to have a higher Q_s. The inductive high-pass filter is designed as the input matching stage for a wideband characteristic. The input inductive high-pass network will filter out all frequencies lower than 3 GHz, and the author was able to select the required bandwidth of the amplifier. The inductive high-pass network combines the source degeneration inductor L_s and the intrinsic capacitances of

T_1 to achieve a wideband matching characteristic to 50Ω. The equivalent circuit is shown in Figure 4.5 below.

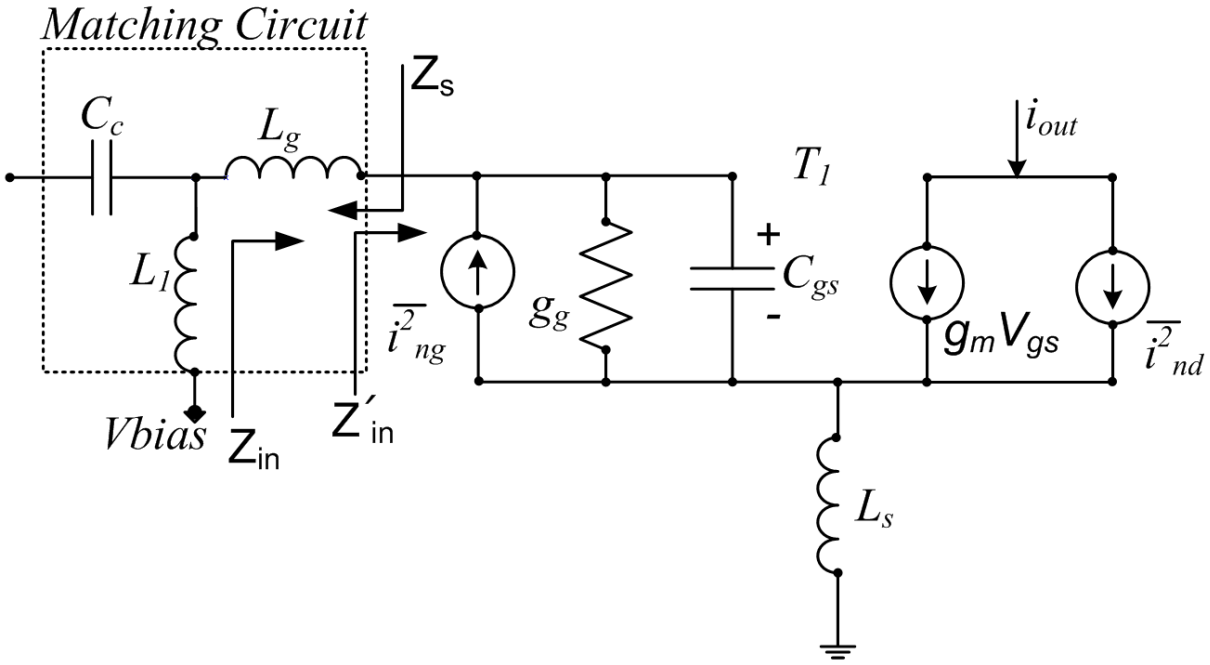

Figure 4.5: LNA Input Matching Network

$$Q_s = \frac{1}{\omega R_s C_{gs}} \tag{4.12}$$

$$Q_{opt} = \frac{G_{opt}}{\omega C_{gs}} = \alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{4.13}$$

For a given Q, higher g_m improves the noise figure, and proper selection of g_m, L_s and C_{gs} ensures that the input impedance can be equal to 50Ω. Hence, the input resistance can be resonated out by a series inductor L_s. From Figure 4.5 Z'_{in} is the impedance to the device. Hence, it follows that

$$Z_{in}(j\omega) = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{4.14}$$

$$= \frac{(j\omega)^2(L_s + L_g)(C_{gs}) + (j\omega)\omega_T L_s C_{gs} + 1}{j\omega(C_{gs})}$$

where $s = j\omega$

$$V_{in} = i_{in}\left[j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}\right] \tag{4.15}$$

For matching $(L_s + L_g)$ are cancelled out by C_{gs} [47]. To achieve the wideband impedance matching, the LNA makes use of the gate and source inductances of the first stage to provide resonance at the frequency of interest.

$$\omega(L_s + L_g) = \frac{1}{\omega C_{gs}} \Rightarrow \omega^2 = \frac{1}{(L_s + L_g)C_{gs}} \tag{4.16}$$

Then

$$R_s = 50\Omega = \frac{g_m}{C_{gs}} L_s$$

The adoption of a double-stage common-source configuration significantly improves the reverse isolation. This is an important performance in UWB LNAs since it presents the signal to flow through the reverse path back to the antenna along several-gigahertz highly crowded frequency spectrum [48].

4.4.3 Linearity Improvement Technique

An LNA must remain linear when strong signals are being received, according to [1]; that is, an LNA must maintain linear operation when receiving a weak signal in the presence of strong interference. The consequences of intermodulation distortion include desensitisation (known as blocking) and cross-modulation. Blocking occurs when the intermodulation products caused by a strong interferer swamp out the desired weak signal, whereas cross-modulation results when a nonlinear interaction transfers the modulation of the carrier to another. Both effects are undesirable as reported in [1]. Hence the circuit designer has to mitigate these problems to the maximum practical extent. The most

commonly used measures of linearity are the third-order intercept point (IP3) and the P_{1dB} compression point. The output of a weakly nonlinear amplifier with input A and output B can be approximated by the first three power series terms;

$$B = g_1 A + g_2 A^2 + g_3 A^3 \tag{4.17}$$

where g_1, g_2 and g_3 are the linear gain and the second- and third-order nonlinearity coefficients of the amplifier respectively. The aim of linearisation is to make g_2 and g_3 small enough to be negligible, keeping only the linear term g_1, hence $B = g_1 A$. An amplifier nonlinearity originates from two major sources:

I Nonlinearity transconductance (g_m), which converts a linear input voltage to nonlinear output drain current

II Nonlinear output conductance (g_{ds}), whose effect becomes apparent with a large output voltage swing and a small drain-source voltage v_{ds} [49].

Let us consider a negative feedback scheme with a nonlinear amplifier A and a linear feedback factor β, as shown in Figure 4.6 where X and X_o are the input and output signals respectively. X_f is the feedback signal and X_i is the difference between X and X_f. Assuming that the nonlinear amplifier can be modelled by

$$X_o = b_1 X + b_2 X^2 + b_3 X^3 \tag{4.18}$$

$$b_1 = \frac{g_1}{1+T_o}, \quad b_2 = \frac{g_2}{(1+T_o)^3}, \quad \text{and} \quad b_3 = \frac{1}{(1+T_o)^4}\left(g_3 - \frac{2g_2^2}{g_1}\frac{T_o}{1+T_o}\right)$$

where $b_{1,2,3}$ are the closed-loop linear gain and second/third-order nonlinearity coefficients respectively, and $T_o = g_1\beta$ is the linear open-loop gain. The IIP2 and IIP3 of the amplifier

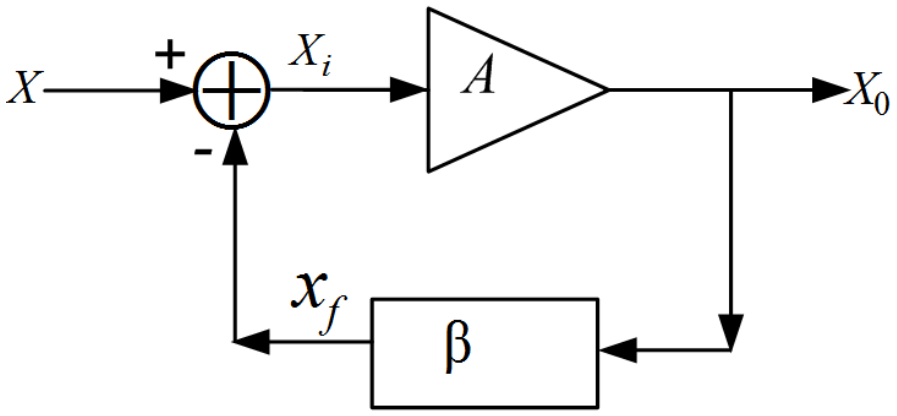

Figure 4.6: Nonlinear Amplifier with Negative Feedback

A and the closed loop system are

$$IIP2, amplifier = \sqrt{\frac{g_1}{g_2}} \tag{4.19}$$

$$IIP2, closed-loop = \sqrt{\left|\frac{b_1}{b_2}\right|} = \sqrt{\frac{g_1}{g_2}(1+T_o)^2} \tag{4.20}$$

$$IIP3, amplifier = \sqrt{\frac{3}{4}\left|\frac{g_1}{g_3}\right|} \tag{4.21}$$

$$IIP3, closed-loop = \sqrt{\frac{3}{4}\left|\frac{b_1}{b_3}\right|} = \sqrt{\frac{3}{4}\frac{g_1}{g_3}\frac{(1+T_o)^3}{(1-\frac{2g_2^2}{g_1 g_3}\frac{T_o}{1+T_o})}} \tag{4.22}$$

The negative feedback improves IIP2 by a factor of $(1+T_o)$ and IIP3 by a factor of $(1+T_o)^{\frac{3}{2}}$ when $g_2 \approx 0$. A nonzero g_2 degrades IIP3 when g_1 and g_3 have opposite sign. Referring to Figure 4.7, the inductor L_s acts as a frequency dependent feedback element with $\beta = \omega L_s$ creating a feedback path between the output current i_d and the gate source voltage V_{in}. Due to the third-order nonlinearity of a transconductance stage, two undesired signals in adjacent channels generate third-order intermodulation (IM3) products at the output of

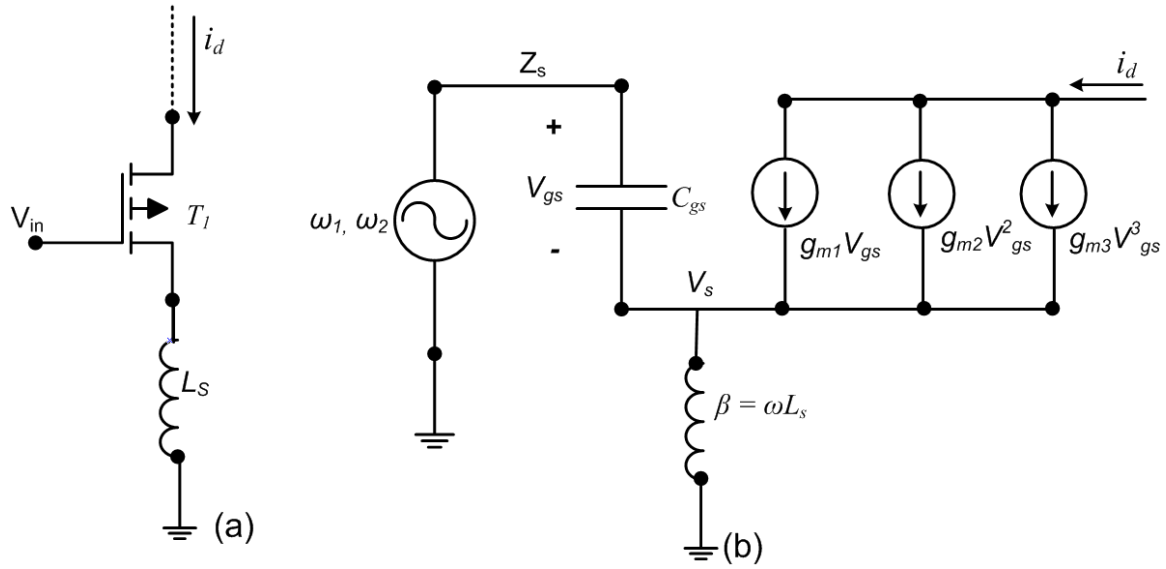

Figure 4.7: (a) Inductive Source-degeneration LNA (b) Small-signal Model

the transconductance stage. The IM3 components corrupt the wanted signal resulting in distortion. The IIP3 is the measure of circuit non-linearity, and from the volterra equation it follows that the transistor drain current i_d [50] is given by

$$i_d = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 + ... \tag{4.23}$$

where g_{mi} is the i^{th}- order coefficient of the transistor T_1 obtained by taking the derivatives of the drain-source dc current I_{ds} with respect to the V_{gs} at the dc bias point.

$$g_{m1} = \frac{\partial I_{ds}}{\partial V_{gs}}, \quad g_{m2} = \frac{1}{2!}\frac{\partial^2 I_{ds}}{V_{gs}^2}, \quad g_{m3} = \frac{1}{3!}\frac{\partial^3 I_{ds}}{\partial V_{gs}^3}.$$

Hence IIP3 can be estimated as follows

$$IIP3 = \sqrt{\frac{3}{4}\left|\frac{g_{m1}}{g_{m3}}\right|} \tag{4.24}$$

as g_{m3} tends to zero it results in a high IIP3.

Two methods are used to improve third-order intercept performance: inductive emitter degeneration, and low-frequency bypassing of the $(f_2 - f_1)$ product at the base-emitter (and collector) junction. Inductive emitter degeneration achieves a linearity improvement at the cost of reduced gain. In the proposed LNA design, much care has to be taken to ensure better linearity as there is a trade-off between amplifier gain, power consumption and linearity. In principle, the amplifier optimal gain impedance does not match the optimal IP3. One way to find IP3 is a measurement in which two sinusoidal input signals of equal amplitude and nearly equal frequencies drive the amplifier. The third-order intermodulation products of the output spectrum are compared with the fundamental term as the input amplitude varies and the intercept is computed. The circuit has been designed at a point where the amplifier gain does not degrade as much and IP3 is still acceptable [40]. In this case, some components and additional stages are added to the circuit to improve the linearity and optimisation of the amplifier gain. In the circuit design a source degeneration inductor (L_s) is added to improve the amplifier linearity thereby reducing the amplifier gain, but subsequent stages were added to compensate for the degraded gain.

4.4.4 Output Impedance Matching Network

The output matching network is made up of a buffer stage. A buffer amplifier simply provides electrical impedance transformation from one circuit to another. There are two major types of buffer circuits; current and voltage buffer amplifiers. A current buffer amplifier is used to transfer a current from a first circuit, having a low output impedance level, to a second circuit with a high input impedance level, while a voltage buffer amplifier is used to transfer a voltage from a first circuit, having a high output impedance level, to a second circuit with a low input impedance level. There are various transistor

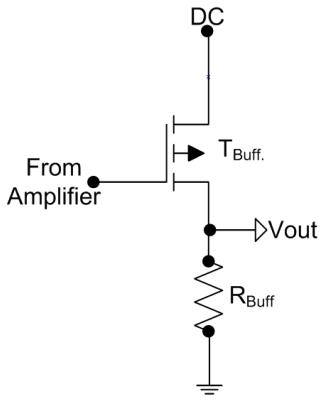

Figure 4.8: Buffer Circuit for LNA Output Impedance Matching

configurations used in the buffer circuits such as common gate, common source and common drain. In this design, the common drain configuration also known as source follower, was considered for the implementation, because it draws very little current without disturbing the original circuit, and gives the same voltage signal as output. As such it acts as an isolation buffer, isolating a circuit so that the power of a circuit is not completely disturbed; for this reason it is called a unity-gain voltage buffer. In this circuit the gate terminal of the transistor serves as the input, the source is the output, and the drain is common to both (input and output).

4.5 LNA Design Simulation and Layout

The LNA circuit design layout was done in AWR. Various types of metal are used to connect components to one another in the layout for proper electrical connection or termination. Here there are various design rules to be fulfilled in order to certify the appropriate layout conditions and to avoid interconnection or communication between metals. Another important stage is the filler generated to fill all space between components; this helps to create effective isolation between components. The layout of the circuit was properly constructed to ensure a smaller chip area and better performance; consideration was also made for on-chip bonding. Bond pads are added to the circuit for proper pinout terminations. The circuit design is properly protected from Electro Static Discharge (ESD); ESD pads were placed on DC and RF points of the circuit. The micrograph of the fabricated LNA is shown in Figure 4.9.

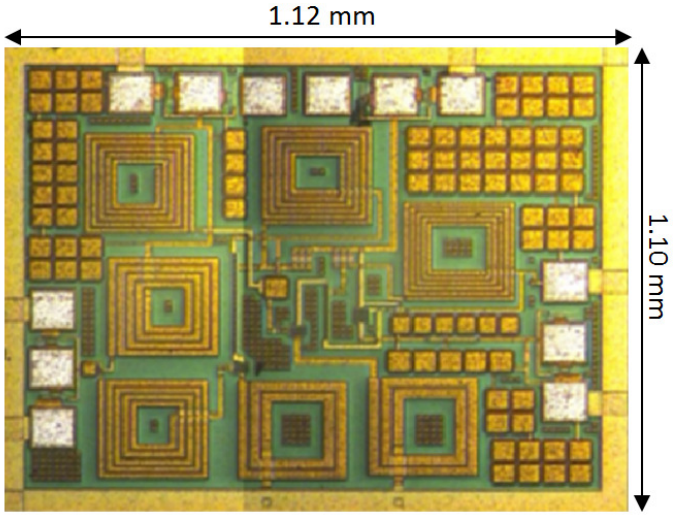

Figure 4.9: Fabricated LNA Micrograph

4.6 Experiment Result

The measurement setup is made up of the following equipments: Rohde & Schwarz signal generator 5 KHz - 6 GHz SMT 06, Rohde & Schwarz FSU spectrum analyser 20 Hz - 67 GHz, Hewlett Packard 8510C vector network analyser (VNA) 45 MHz - 50 GHz S-parameter test set, Agilent 346B 10MHz - 18GHz noise source 28 V DC input, SMA power combiner fairview mirowave MPR18-2 and ECP18-GSG-150 DP signal probe . The scattering-parameter measurement setup is as shown in Figure 4.10(a) and the measurement setup for linearity of the two-port device is shown in Figure 4.10(b). The VNA was properly calibrated for equipment, probe and cable losses. The calibration standard used is a short, open, load, and through (SOLT) connection, purchased as a separate calibration Kit. The device under test (DUT) was properly probed down and the S-parameters were measured with the VNA. The proposed topology for the LNA design was applied to a 3.1

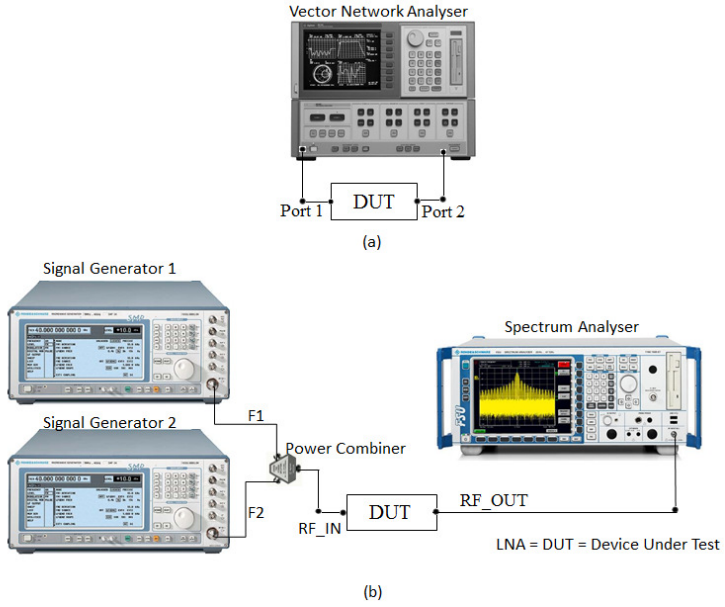

Figure 4.10: (a) VNA Calibration Setup, (b) Measurement Setup for Linearity of a Two-port Device

- 5 GHz wideband amplifier based on Silanna's 0.25μm CMOS process. Proper selection of the matching network was made to optimise the obtained results. The maximum gain achieved with a 50Ω matched load is 18.47 dB as shown in Figure 4.8. An integrated circuit can be damaged by ESD, and the damages ranges from subtle performance degradation to complete device failure. The LNA has a low noise figure of 2.4 dB which is quite low compared to other wideband LNA designs recently published as shown in Table 4.1. This feature places the proposed LNA design as a good candidate for low power IR UWB applications. The excellent agreement between expected and measured results confirms the soundness of the reported design methodology. A comprehensive comparison with state-of-the-art UWB LNAs highlights our claim that the proposed amplifier is able to provide an excellent RF overall performance, at very low power consumption.

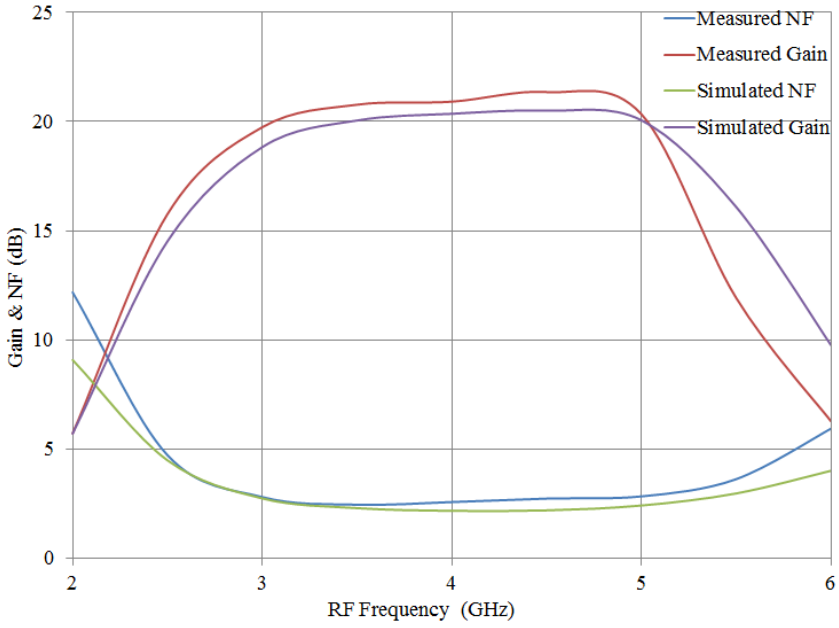

Figure 4.11: Measured LNA Gain vs Noise Figure

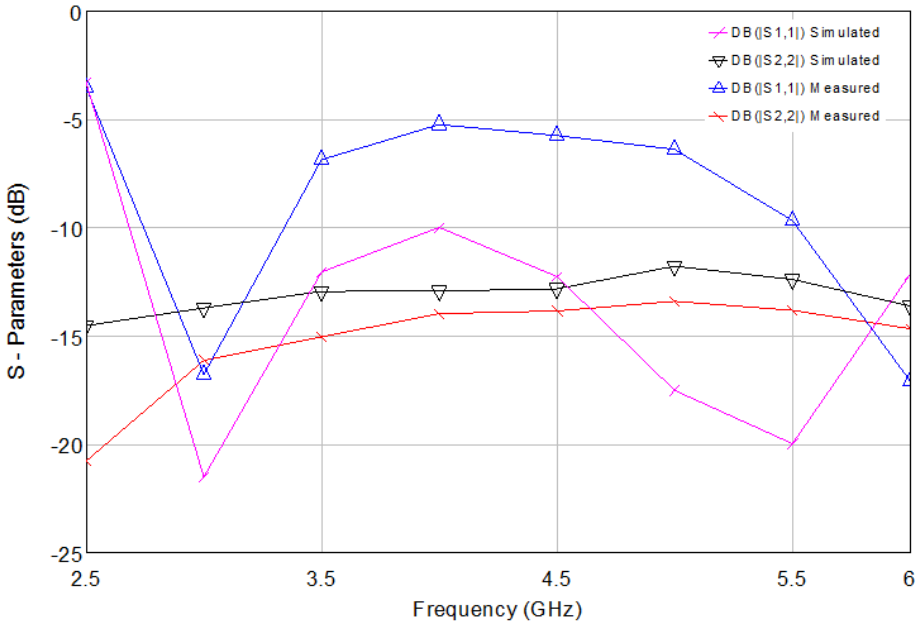

Figure 4.12: Measured Input and Output Return Loss

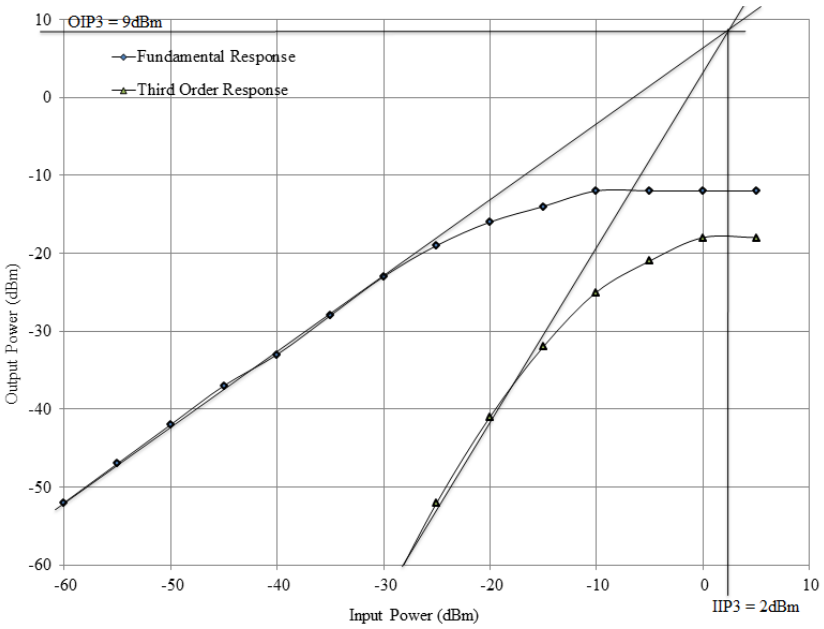

Figure 4.13: Measured IIP3 of the Designed LNA

Ref.	[45]	[46]	[44]	[51]	[52]	[48]	**This Work**
BW (GHz)	3.1 - 10.6	2 - 4.6	2.6 - 9.2	3 - 5	3 - 5	3 - 10	**3.1 - 5**
S11 (dB)	-8	-9	-11.5	-10	<-8	-9	**-17.47**
S22 (dB)	-	-	-	-14	<-14	-	**-25**
S21 (dB)	13.5 - 16	9.8	10.9	11	13	12.5	**18.6 - 21**
NF (dB)	3.1 - 6	2.3	3.5	3.9	3.5	3 - 7	**2.4**
IIP3(dBm)	-7	-7	-5.1	-10	-6.1	-	**2**
PD (mW)	11.9	12.6	7.1	5.6	3.4	7.2	**4.2**
FoM [GHz/mW]	2	1.6	4	1.35	3	3	**7.2**
CMOS Tech.(μm)	0.25	0.18	0.18	0.18	0.13	0.09	**0.25**
Chip Area(mm^2)	1.2	-	-	-	0.4	0.64	**1.2**

Table 4.1: Performance Summary and Comparison with State-Of-The-Art CMOS Wideband LNAs

4.7 Discussion of the Designed LNA

A low noise amplifier has been designed for the proposed receiver structure. A proper circuit topology for the design has been chosen to achieve good gain at very low noise figure and better linearity at low power consumption. The LNA gain and noise figure are presented for this design as shown in Figure 4.11. The linearity is presented in Figure 4.13 with IIP3 measured to be 2 dBm and OIP3 to be 9 dBm. The power compression at 1dB (P_{1dB}) is -20 dBm. The LNA designed was optimised such that the inductors are not too large, to avoid large chip space and inductance coupling, also the circuit layout was properly made to avoid the circuit occupying a large chip area. The area occupied by the LNA is 1.2 mm^2; the micrograph is shown in Figure 4.9. A performance comparison and summary of the LNA state of the art has been made and is presented in Table 4.1, showing that the designed LNA is well designed for the proposed application. To compare

the overall performance of our LNA with previously published ones, a figure of merit (FoM) that takes into account the gain, NF, bandwidth and the dc power consumption of the LNA is defined as

$$FoM[GHz/mW] = \frac{Gain[dB] \times BW[GHz]}{(NF-1)[dB] \times P_{DC}[mW]} \tag{4.25}$$

The FOM is used to characterise the performance of the circuit and to determine the circuit's relative utility for its application. Hence, according to Table 4.1, our amplifier shows a better overall performance than previously published LNAs.

4.8 Summary

In conclusion the difference between the simulated and measured results are expected, the result of the designed LNA shows some variation due to the component's as accuracy as compared to it's model. This includes frequency dependency of the components, modelling inaccuracy and manufacturing variations. Some of these are the important parameters that leads to the variation in the measured and simulated results. The LNA designed in this work is designed for wideband application with specifications which include high gain, low NF and linearity to be met with minimum DC power consumption. Table 4.1 shows that the design in this work achieves better performance.

Chapter 5

Wideband Mixers

5.1 Introduction

Frequency translation in a communication system is performed by a non-linear device known as a mixer. There are various topologies from simple single ended, single balanced mixers to more complicated double and triple balanced mixers that provide better isolation from the Local Oscillator (LO) and fewer spurious signals. The most popular double-balanced mixer used in RFIC design is the Gilbert Cell mixer. Mixers are non-linear devices used in systems to translate by multiplication from one frequency to another. All mixer types work on the principle that a large LO-to-RF drive will cause switching or modulating the incoming Radio Frequency to the Intermediate Frequency (IF). RF mixers are three port active or passive devices. They are designed to yield both a sum and a difference frequency at a single output port when two distinct input frequencies are inserted into the other ports. A mixer can be used as a phase detector or as a demodulator. A mixer that produces a lower frequency when a higher RF frequency is fed into it is called a down-converter, and a mixer that produces a higher frequency when a lower frequency is fed into it is called up-converter. Therefore, a down-conversion mixer

is used in the receiver while an up-conversion mixer is used in the transmitter. This chapter will explore a down-conversion mixer suitable for the proposed UWB receiver design. Following the definition of a mixer, there are some characteristics that should be noted, including conversion gain, noise figure, linearity and isolation. Conversion gain is defined as the ratio of the desired IF output to the value of the RF input. Noise figure is the signal-to-noise ratio (SNR) at the input port divided by the SNR at the output port. Linearity is the figure of merit to give an indication of the mixer's signal handling capability. Isolation is a measure of the leakage, or feedthrough, from one port to another. The more isolation a mixer provides, the lower the amount of feedthrough. Additional details of the work reported in this chapter can be found in the author's publication [53] and [54]. In this chapter the author will explore the advantages of both active and passive mixers.

5.2 Fundamentals of Mixers

Most common type of mixers have a common mode of operation, that is the sum and difference of the two input frequencies are produced at the output as shown in Figure 5.1. In the case of a down conversion, if f_{RF} and f_{LO} are the two input signals, then the f_{IF} signal will have frequency

$$f_{IF} = f_{RF} - f_{LO} \tag{5.1}$$

Alternatively, if the mixer is being used for up-conversion with f_{IF} and f_{LO} inputs the f_{RF} output signal will have frequency

$$f_{RF} = f_{IF} + f_{LO} \tag{5.2}$$

In order to generate a frequency translation, a nonlinear device is required. A straightforward mathematical identity can illustrate how the device produces the mixing operation.

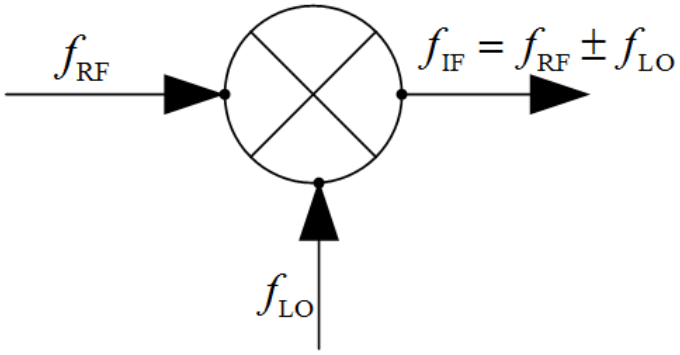

Figure 5.1: Fundamental Mixer Block Diagram

Let us consider two signals, Acos(ω_1t) and Bcos(ω_2t), multiplied together through a non-linear device.

$$A\cos(\omega_1 t)B\cos(\omega_2 t) = \frac{AB}{2}\left[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t\right]. \tag{5.3}$$

5.2.1 Types of Mixers

There are various types of mixer; a mixer can be active or passive. An active mixer is made up of active components, biased for conversion gain at the expense of intercept-point performance, and high power consumption. On the other hand, a passive mixer consists of passive components only, they require higher LO power levels and are characterised by conversion loss, but provide better third-order intercept performance, and power consumption is minimal compared to the active mixer. Mixers can also be divided into several classes:

1. Single Device Mixer
2. Single Balanced Mixer
3. Double Balanced Mixer

A Single Device Mixer uses one nonlinear component, for example diode or transistor, but has the disadvantage of not attenuating the local oscillator amplitude modulated noise and always requires an injector filter. A Single-Balanced Mixer uses two mixing devices, which may be two diodes or two transistors and are usually realised as two single devices connected via a 180-degree or 90-degree hybrid. A Double Balanced Mixer uses more than two mixing devices; there are two common types of double balanced mixer, namely the ring mixer and the star mixer. The ring double balanced mixer can be described by treating its nonlinear components, diode or transistors, as switches which are turned on and off by the LO. The advantage of balanced mixers over single-device mixers includes the rejection of spurious responses and intermodulation products, better LO-to-RF, RF-to-IF, and LO-to-IF isolation and rejection of amplitude modulated noise in the LO. The disadvantage of balanced mixers is their greater LO power requirements. A balanced mixer is used to separate the RF and LO ports when their frequency overlaps and filtering is impossible.

Double-Balanced FET Mixers can be designed for either passive or active modes. The author looks closely at the two major types of double-balanced FET mixers, and explores their advantages for the proposed receiver design.

5.2.2 Gilbert-Cell Mixers

An active FET mixer is based on the Gilbert-cell architecture and is a transconductance mixer, using the LO signal to vary the transconductance of the transistor, with the advantage of providing conversion gain rather than loss. Gilbert-cell mixers have the following advantages: both LO and RF are balanced, providing both LO and RF rejection at the IF output, all ports of the mixer are inherently isolated from each other, there is increased linearity compared to singly balanced, improved suppression of spurious products (all even order products of the LO and/or the RF are suppressed), and high intercept points

compared to singly balanced. However, Gilbert-cell mixers have the following limitations: they require a higher LO drive level, they require two baluns (although the mixer will usually be connected to differential amplifiers) and their ports are highly sensitive to reactive terminations.

5.2.3 Passive FET Mixer

A passive FET mixer is based on FET quads, providing good linearity at the expense of high conversion loss. Passive mixers are attractive for the following reasons: their linearity is quite good compared to that of active mixers, they consume no current compared to that of active mixers. This property makes it suitable for low power design. They have no $1/f$ noise (since no DC current consumption) and they occupy a small chip area because their components are few. However, passive mixers are characterised by loss ranging from $4-6$ dB rather than gain and require large LO drive, almost rail to rail (power consumption).

Active mixers are preferred for RFIC implementation. They are configured for conversion gain, and can use differential amplifiers for active baluns. On the other hand, passive mixers are widely used because of their relative simplicity, wide bandwidth, good intermodulation distortion (IMD) performance and the ultimate of the passive mixer; that is of great importance to this work is low DC power consumption. The transformers or baluns generally limit the bandwidth, and introduce some loss into the signal path, which can be of some concern for the noise figure.

5.3 Wideband FET-Based Gilbert-Cell (Active) Mixer

Mixers are required primarily for multiband systems, such as the MB-OFDM approach, since the system requires down-conversion to baseband or an IF. Therefore, mixer techniques typically used in narrowband wireless receivers can be employed without significant

modification at the IF output. The input transconductor needs to be capable of operating over the entire frequency range. Mixer circuits have been realised using field-effect transistors, the most popular of which is the Gilbert cell. The structure of a Gilbert-cell mixer is as shown in Figure 5.2. The RF signal is fed into the gates of the bottom two transistors, T_5 and T_6, and the LO signal is applied to the upper transistors ($T_1 - T_4$). The upper two pairs of transistors are cross-coupled and act as current switches, changing the polarity of the current flowing through the drain resistors, R_{L1} and R_{L2}. The output signal is taken at the points $+IF$ and $-IF$.

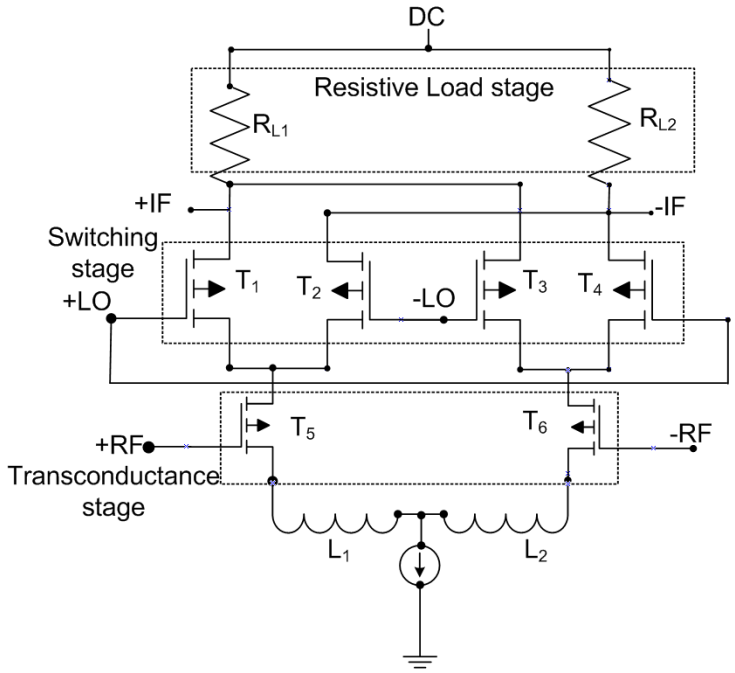

Figure 5.2: Gilbert-Cell Mixer

A traditional Gilbert-cell mixer consists of three different stages: the resistive load stage, the switching stage, and the transconductance stage. Here a degeneration resistor is used in place of the inductors L_1 and L_2 to provide feedback and improve the linearity

of the mixer; the drawback of this is excessive noise and power consumption. In this project, degeneration inductors are used since they do not contribute any noise to the mixer and improve the linearity at minimal power consumption. Although inductors have an associated resistance that generates noise, it cannot be compared to an ordinary resistor. The drawback to using inductors is the chip area they consume, but this has been overcome by the small size and smaller value of the inductor provided by the Sapphicon process kit. The advantage of this topology is that a tail bias current is applied to enable independent settings of the transconductance stage and the LO switches. The Gilbert-cell mixer is preferred due to the fact that its ports are inherently isolated from each other.

5.3.1 Gilbert-Cell Mixer Conversion Gain

Mixer Conversion gain is the ratio of the desired IF output (voltage or power) to the RF input signal value (voltage or power). If the input impedance and the load impedance of the mixer are both equal to the source impedance, then the voltage conversion gain and the power conversion gain of the mixer are the same. When the LO of the mixer is at either peak, one pair of the switching stage transistors is completely off, while the other acts like a cascode device. Hence, the mixer acts like an amplifier with a gain of $\sim R_L/Z_E$ where R_L is the load resistor and Z_E is the degeneration impedance of the input differential pair, which is the transconductance stage.

The LO signal is presented as

$$V_{LO} = \frac{2}{\pi}\cos(\omega_{LO}t) + \frac{1}{\pi}\cos(3\omega_{LO}t) + \frac{1}{6\pi}\cos(5\omega_{LO}t) + \cdots\cdots \tag{5.4}$$

Then, the gain R_L/Z_E will be modulated by the LO signal, since the IF signal is the product of RF and LO. The gain suffers a loss of $2/\pi$ and the Conversion gain (CG) is given as

$$CG_{mix} = \frac{2}{\pi} \cdot \frac{R_L}{Z_E} \tag{5.5}$$

5.3.2 Gilbert-Cell Mixer Noise Figure

The noise in the Gilbert-cell mixer is divided between the input transconductance stage, the switching stage and the mixer load resistors. Each stage will be addressed separately. The noise of the transconductance stage is somewhat compromised by increasing the emitter degeneration in order to increase the mixer IP3. This is because the mixer linearity has more impact on the overall receiver performance than its NF [55]. The noise in the switching stage has two parts. The first part is simply the folding of the image noise coming from the transconductance stage, as well as the input source. This happens even if the mixer switching stage is totally noiseless. The second source of mixer switching stage noise is due to the switching stage noisy devices. It is should be noted that the noise of the switching stage is at its maximum when each of the switching transistors conducts an equal amount of current. This is because, when T_1 and T_2 devices are ON at the same time, they act as a simple differential pair amplifying each other's noise, which is uncorrelated. This noise adds up at the output severely degrading the signal-to-noise ratio [56]. The mixer load also contributes to the overall NF. In low or zero IF receivers, the load is a simple resistor, whose noise contributes to the mixer NF. From Figure 5.2, if $(T_1 - T_2)$ is switched by a square wave then the noise, mainly from T_5 and $2R_L$, can be given as

$$\frac{\overline{i_{nT_5}^2}}{\Delta f} = 4kT\gamma g_{do}\,, \qquad \frac{\overline{e_{nR_L}^2}}{\Delta f} = 2(4kTR_L) \tag{5.6}$$

The noise of T_5 modulated with square wave ± 1

$$e_{nIF}(t) = R_L \cdot i_{nT_5} \cdot S_{LO}(t) \tag{5.7}$$

$$E_{nIF}(\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} R_L \cdot I_{nT5}(\omega - v) \cdot S_{LO}(v)dv = \sum_{k=-\infty}^{\infty} a_k R_L I_{nT_5}(\omega + k\omega_0) \tag{5.8}$$

$$S_{nIF}(\omega) = \sum_{k=-\infty}^{\infty} |a_k|^2 R_L^2 \cdot S_{nT_5}(\omega - k\omega_0) = 4kT\gamma g_{do} R_L^2 \sum_{k=-\infty}^{\infty} |2a_k|^2 \tag{5.9}$$

where S_{nIF} is the power spectral density (PSD) at the IF, and it holds that $\sum |a_k|^2 = 1$, but in practice is less than 1 because of band limitations.

The PSD at the IF output, including the noise of $2R_L$ and R_s, is given as

$$S_{nIF}(\omega) = (4kTR_s g_{m5}^2 R_L^2 + 4kT\gamma g_{do} R_L^2) \sum_k |a_k|^2 + 2(4kTR_L) \tag{5.10}$$

and the power gain for the signal is given as

$$G = (K_c)^2 = \left(\frac{2}{\pi} g_{m5} R_L\right)^2. \tag{5.11}$$

Then mixer noise figure can be given as

$$NF_{balanced} = \frac{S_{nIF}(\omega)}{G \cdot S_{nR_s}(\omega)} = \frac{\pi^2}{4}\left(1 + \frac{\gamma g_{do}}{g_{m5}^2 R_s} + \frac{2}{g_{m5}^2 R_L R_s}\right). \tag{5.12}$$

Then we have

$$NF_{Gilbert} = \frac{\pi^2}{4}\left(1 + \frac{\gamma g_{do}}{g_{m5}^2 R_s} + \frac{2}{g_{m5}^2 R_L R_s}\right). \tag{5.13}$$

5.3.3 Gilbert-Cell Mixer Linearity

The mixer third-order intercept point (IP3) is usually limited by the input Transconductance cell and usually depends on the amount of degeneration used, the type of degeneration (inductive or resistive) and the bias current. Inductive degeneration is widely used for linearity improvement due to its low noise, and mixer linearity is more critical than NF. From Figure 5.2 it follows that inductors L_1 and L_2 provide negative feedback in order to improve IP3 and they also provide optimal noise matching, as earlier discussed in section 4.3.6.

The mixer has to be properly matched, since the input impedance presented by the FET gate is very high and is capacitive. Hence, a good input matching network is required and this can be implemented using on-chip or off-chip components. Off-chip matching networks generally require taking the signal off-chip and then back on which adds noise

to the system, and the losses may result in the need for additional amplification. On-chip components like a transformer or a balun are used to convert differential to single-ended with a disadvantage of occupying larger chip area. The area occupied by a balun is appreciably smaller than that occupied by a transformer.

Active baluns are linear amplifiers having two outputs that have equal amplitudes but differ in phase by 180 degrees, used in providing the phase split necessary for balanced mixers. Baluns are much smaller than their distributed counterparts, therefore they are more useful in integrated circuit applications where space must be minimised. It may be difficult to make a good active balun; the fundamental problem is that FET's low drain-to-source resistance prevents them from making good current sources [57].

5.4 Proposed Ultra Wideband Active Mixer Design

The proposed down converter double balanced active mixer is common in CMOS designs. In this project, the basic Gilbert-cell topology with a couple of additional on-chip baluns is used to convert the differential RF and LO signals to single-ended. At the output a source follower buffer amplifier is used to to drive the 50Ω load of the next stage in the receiver. This choice provides high quality port-to-port isolation due to its fully differential structure, which cancels both LO-RF and IF-RF feedback as reported in [58].

Linearity is a very important issue because nonlinearity brings many problems such as gain compression, cross-modulation and intermodulation, in RF systems. The third-order intermodulation distortion is the most dominant nonlinearity component and thus most popularly used parameter for measurement [59]. In the Gilbert-cell mixer topology, the linearity is mostly dominated by the transconductance stage, therefore it is very important to linearise the transistor transconductance [58], [60]. A technique used in this design to improve gain and linearity is the tail current source at the transconductance of the RF

transistors [53]. The tail current source is represented by a current mirror transistor arrangement controlled by a voltage source, since a current source cannot be provided on-chip.

The core mixer performance is solely dependent on the switching transistors and as such the transistors ($T_1 - T_4$) have to be properly biased in the saturation region close to the triode region. The switching transistors are driven by a LO with -10 dBm power to reach the maximum possible gain and linearity. The load resistors R_{L1} and R_{L2} stacked on top of the LO switch are optimised to obtain a low power dissipation and good conversion gain [53], [54].

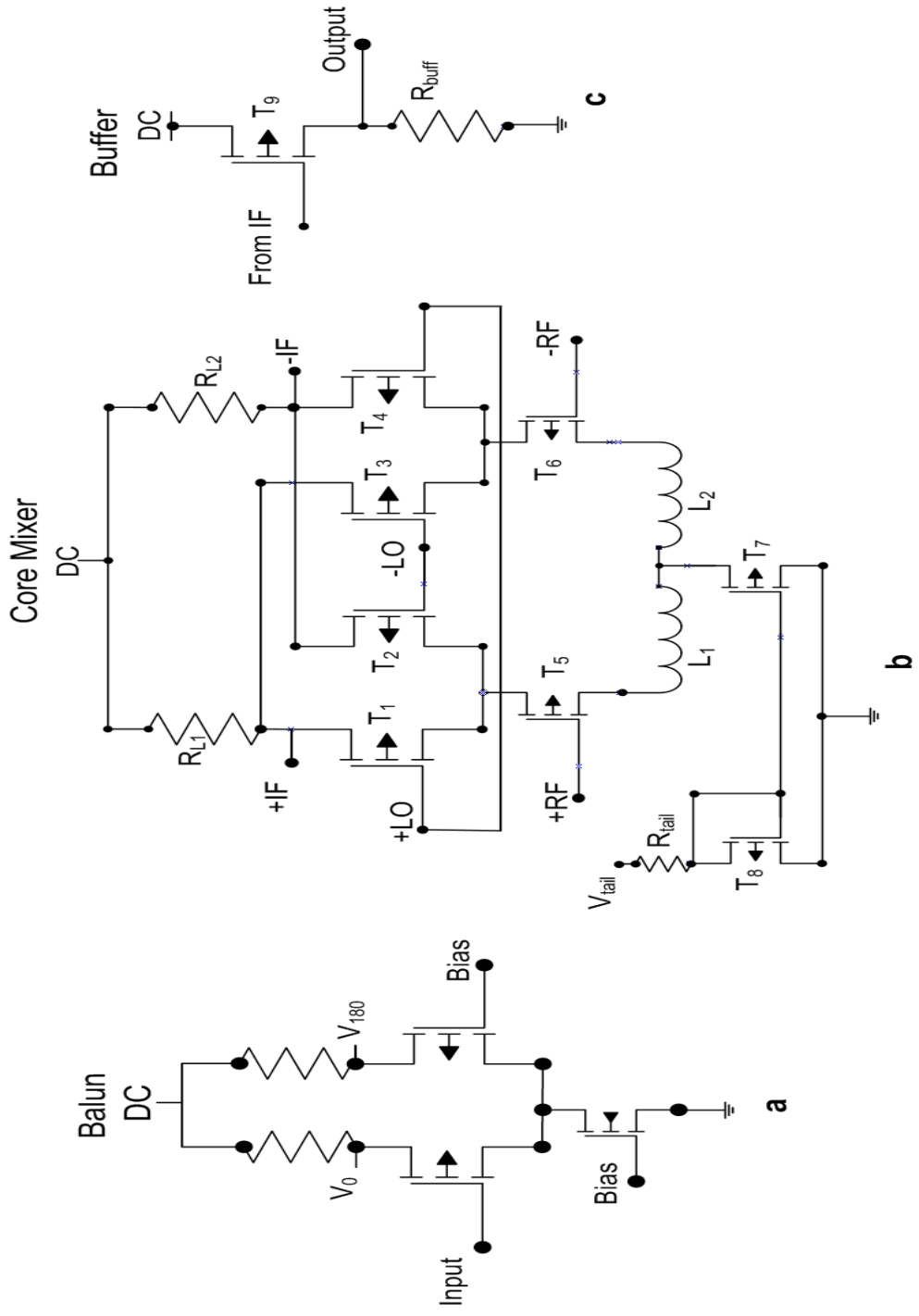

Figure 5.3: Proposed Gilbert-Cell Mixer: (a) Single-End to Differential Balun, (b) Core Mixer, (c) Output Buffer.

5.4.1 Designed Active Mixer Layout

The circuit layout of the mixer was carefully laid out to achieve small chip area, this is one of the design gaol for this work. It is important, during layout to consider the differential pair such that they are made symmetrical for even power flow in the circuit. Figure 5.4 is the fabricated mixer micrograph occupying 1.24 mm^2 chip area.

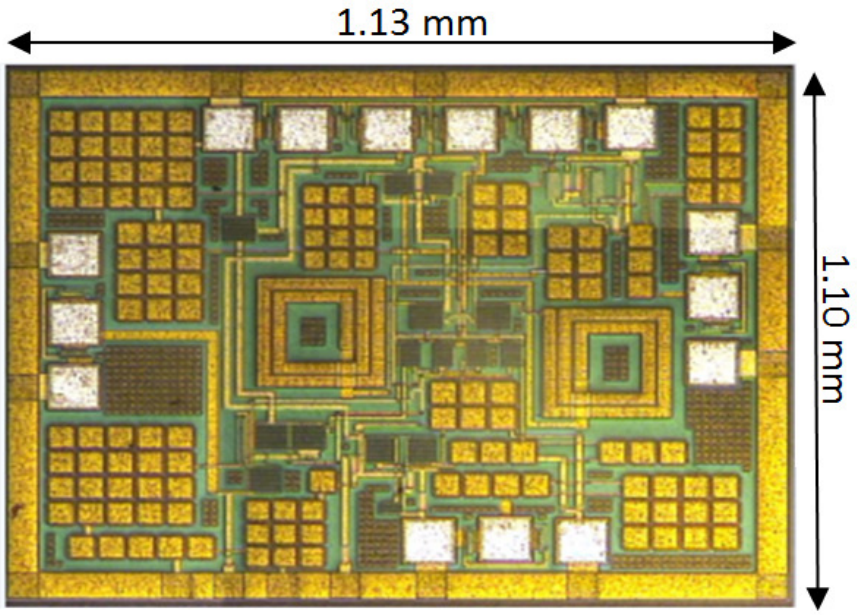

Figure 5.4: Fabricated Active Mixer Micrograph

5.4.2 Designed Active Mixer; Experiment Results

The core Gilbert-cell mixer will down convert the input signal at (3 - 5) GHz through a 4 GHz LO signal to 0.25 GHz. The simulation was performed with an AWR Simulator. The Gilbert-cell mixer designed, including the balun and buffer, is presented in Figure 5.3. There are two types of balun: input balun and output balun. The output balun is responsible for converting differential to single-ended while the input balun converts

single-ended to differential, and both types of balun have been applied in this design. Figure 5.3(a) is the input balun. Figure 5.3(b) is the buffer amplifier, which is responsible for impedance conversion. Figure 5.5 shows mixer conversion gain against the RF swept over various LO input power from -40 dBm to 0 dBm at an interval of 5 dBm. The mixer achieved a measured conversion gain of 19.5 dB and a noise figure of 12.5 dB from (3 - 5) GHz. The Input third-order intercept point at 3.5 GHz was measured to be 10.1 dBm. The power consumed by the core mixer circuit was 4.2 mW and the chip area occupied is 1.7 mm^2. A performance and comparison table of the designed Gilbert-cell mixer with the state of the art is presented in Table 5.1 showing that the proposed mixer has good linearity and low power consumption which make it suitable for implantable radio applications.

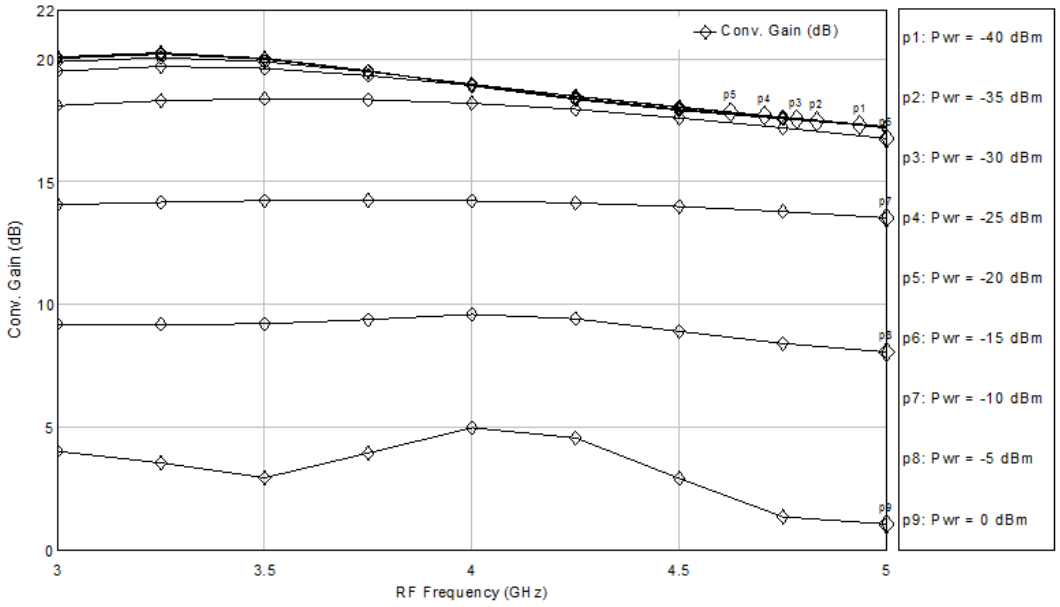

Figure 5.5: Active Mixer Conversion Gain vs Frequency Post-layout Result

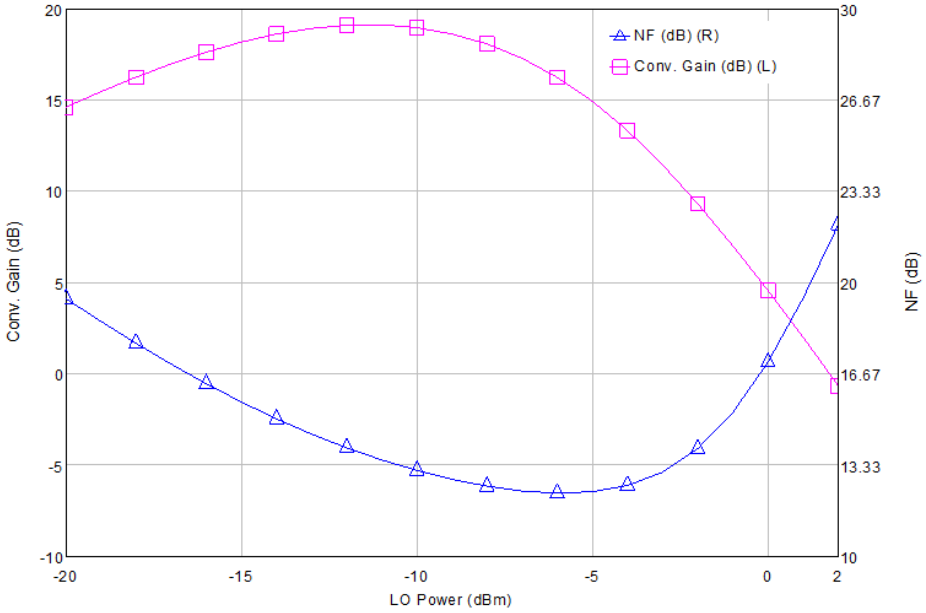

Figure 5.6: Active Mixer Conversion Gain and NF vs LO Power Post-layout Result

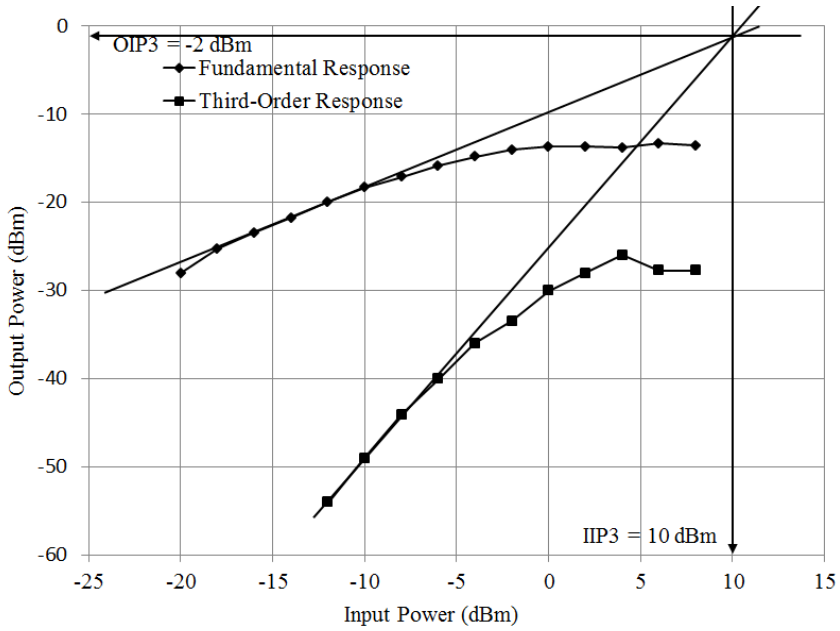

Figure 5.7: Measured Active Mixer Linearity

5.5 Wideband Passive Down Converter

Passive mixers permit a much higher amplitude RF input signal than active mixers before severe distortion products within the output IF become unacceptable. These distortion products are in the form of intermodulation distortion (IMD) and compression distortion. The IMDs may fall in band, or cause other signals to fall in band, possibly swamping out or creating interference with the baseband signal. This causes additional noise, which will degrade system performance and BER. Passive mixers also possess a lower noise figure than active mixers, which is very important for any stage within the front end of a low-noise receiver. In the receiver chain, the mixer is the last block of the radio-frequency (RF) front end and tends to dominate the receiver linearity performance. High linearity is a key performance requirement for the mixer [61]. Passive mixers have been widely adopted for direct conversion (DC) receivers owing to their flicker-noise-free characteristic [62], [63].

The attractive properties of a switching mixer include extremely low power consumption and good linearity. Figure 5.8 shows the schematic of a CMOS switch Mixer. It consists of four CMOS switches and a common source output buffer. Balanced RF signals are applied through the drain of the CMOS switches, and LO signals are applied to its gates. The differential IF output of the mixer is taken from the source of the CMOS switches.

5.5.1 Passive Mixer Switching

This circuit requires good switches that turn on hard (low on-resistance) and turn off well (good isolation). Figure 5.9 represents the switching mode of the transistors as it affects the mixer performance. When the device is “on”, it is in the triode region. Due to a low on-resistance, the coupling through the substrate and LO path is minimal. When the device is “off,” the RF and LO leak into the IF through the overlap and substrate

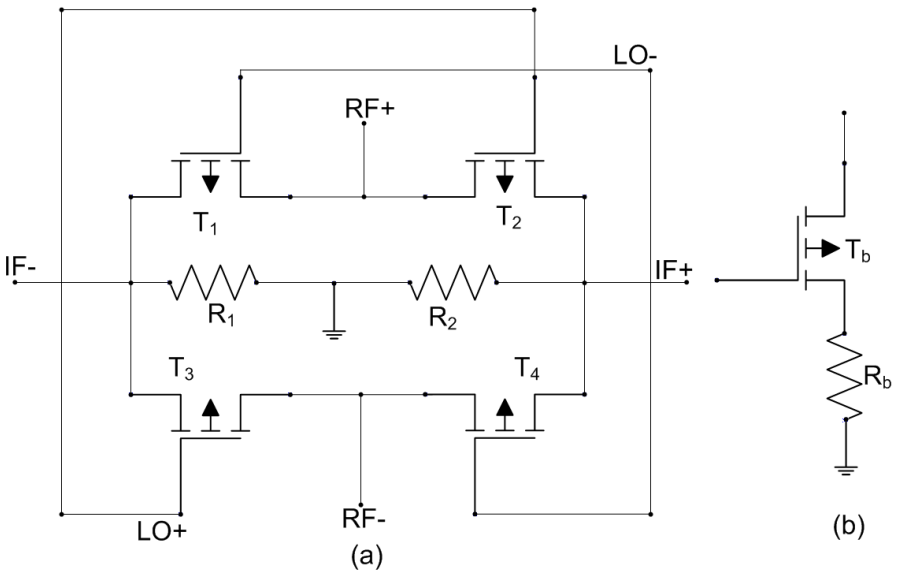

Figure 5.8: (a) Passive Mixer and (b) Output Balun

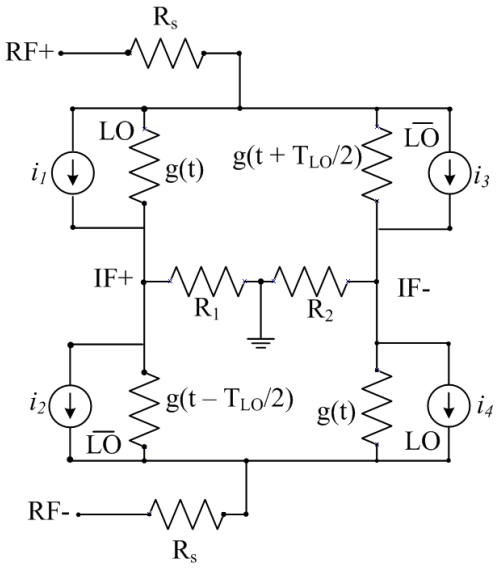

Figure 5.9: Equivalent Core Passive Mixer Circuit

capacitances. A large LO drive is required to turn devices on/off. The RF voltage is then applied to a time-varying conductance, Since the conductance of the LO switches is given by g(t), while the conductance of the $\overline{LO}$ switches is given by g(t - $T_{LO}/2$). The Thevenin equivalent source voltage is given by the open circuit voltage

$$v_T = v_{RF}\left(\frac{g(t)}{g(t) + g(t - T_{LO}/2)} - \frac{g(t - T_{LO}/2)}{g(t) + g(t - T_{LO}/2)}\right) \tag{5.14}$$

$$v_T = v_{RF}\left(\frac{g(t) - g(t - T_{LO}/2}{g(t) + g(t - T_{LO}/2)}\right). \tag{5.15}$$

The channel conductance of the CMOS device is given by

$$g(t) = \mu_o C_{ox} W/L[V_{gs}(t) - V_{ds}(t) - V_{th}(t)]. \tag{5.16}$$

When $V_{ds} = 0$ $g(t)$ is reduced to g_o(t), hence

$$g_o(t) = \mu_o C_{ox} W/L[V_{gs}(t) - V_{th}(t)]. \tag{5.17}$$

The CMOS passive mixer is very linear and the SOS technology enhances this further because of its excellent switching characteristics. Since the device is either "on" or "off," it does not impact the linearity too much. Also, as there is no transconductance stage, the linearity is very good. The drawback is that the passive MOS mixer is lossy and there is no power gain in the device. The overall voltage conversion gain/loss of the mixer due to fundamental tone mixing can thus be approximated as:

$$\frac{v_{out}(f_{out})}{v_{in}(f_{in})} \approx \frac{2}{\pi} g_m\left(\frac{R_f}{1 + j2\pi f_{out} R_f c_f}\right) \tag{5.18}$$

where f_{out} is the output frequency at IF, f_{in} is the input RF frequency, g_m is the total transconductance of the input stage, the factor $\frac{2}{\pi}$ is related to the first harmonic amplitude of the periodically time-varying transfer function and R_f and C_f are the feedback resistor and capacitor of the trans-impedance stage [9], [10]. In this design, the time-domain

output current of the switching stage can be expressed as follows:

$$I_{IF} \approx \frac{2}{\pi} g_m \cos(\omega_{RF} - \omega_{LO})t + \frac{2}{\pi} \cos(\omega_{RF} + \omega_{LO})t + \sum_{n=3,5,7...}^{\infty} \frac{1}{n} \frac{2}{\pi} g_m \cos(\omega_{RF} \pm n\omega_{LO})t \quad (5.19)$$

The linearity performance in the mixer depends on the linearity of the voltage-to-current conversion in the transconductance stage, and on effects from the switching stage and the trans-impedance amplifier stage as stated in [64], [65]. The RF and LO signals are AC coupled into the core mixer through capacitors. AC coupling increases biasing flexibility and suppresses low-frequency distortion interaction between stages. The switches consist of four transistors; the DC bias at the gate of the switches is set where they are operating near the threshold of conduction in order to achieve the lowest on-resistance while preventing overlapping on-periods. Any overlapping on-periods of the switches result in lowered conversion gain and increased flicker noise from the LO port, while an overlapping off-period will result in linearity degradation according to [66] and [67].

5.5.2 Designed Passive Mixer Layout

The passive mixer layout was simple as its components are few compared to the active mixer. The circuit layout was carefully laid to achieve small chip area, Figures 5.10 is the fabricated mixer micrograph occupying 0.70 mm^2 chip area.

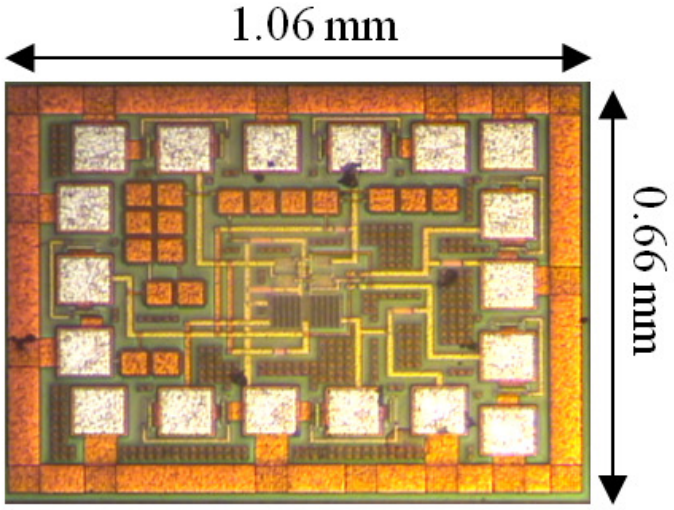

Figure 5.10: Fabricated Passive Mixer Micrograph

5.5.3 Designed Passive Mixer; Experiment Results

The simulated passive mixer result shows excellent performance with good linearity as shown in Figure 5.13, and a considerable gain and NF are presented in Figure 5.12. The designed passive mixer consists of an on-chip balun at LO, RF and IF ports. The passive mixer result in Figure 5.12 achieve some amount of gain from the coupled on-chip balun. Figure 5.11 is the passive mixer conversion loss against the RF port swept over the LO input power from -15 dBm to 10 dBm at an interval of 5 dBm.

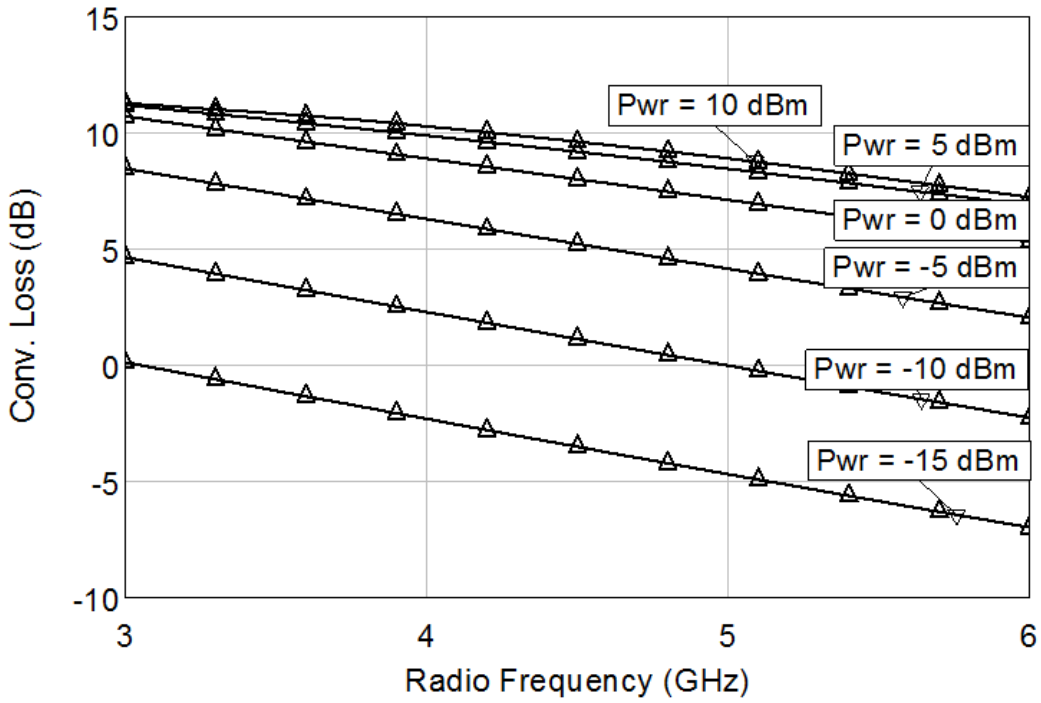

Figure 5.11: Passive Mixer Conversion Loss vs Frequency Post-layout Result

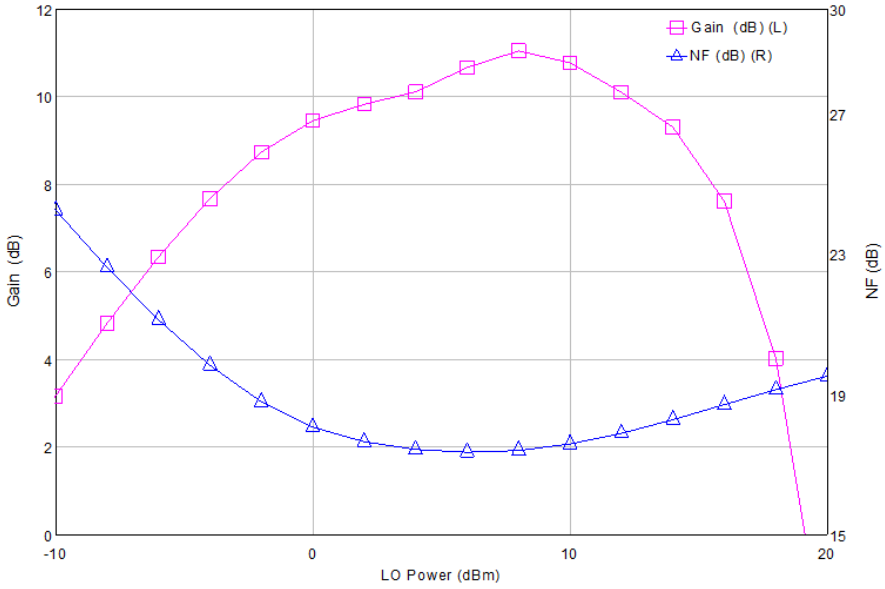

Figure 5.12: Passive Mixer with Active Balun, Gain and Noise Figure vs LO Power Post-layout Result

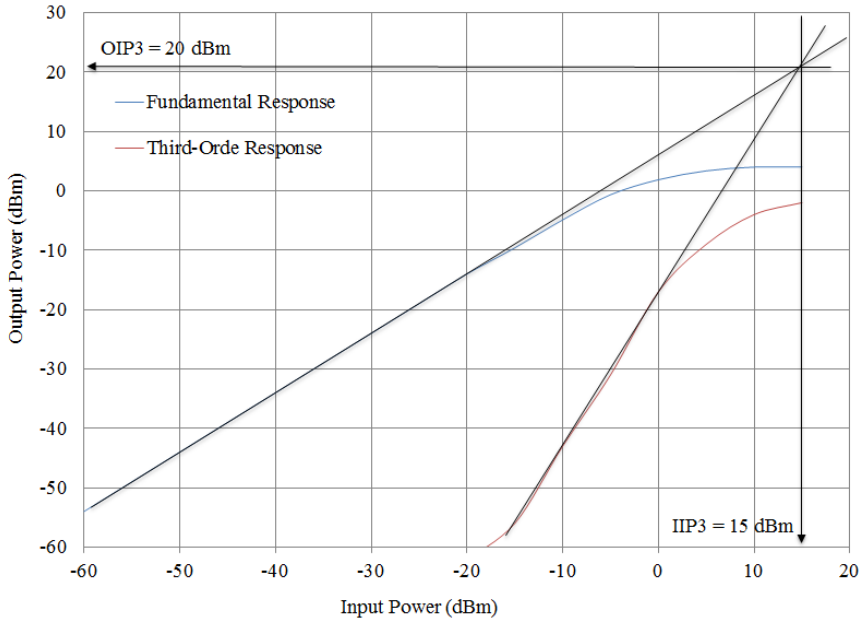

Figure 5.13: Measured Passive Mixer Linearity

Ref.	[68]	[69]	[60]	[54]	∗**1**	†**2**
BW (GHz)	3.1 - 8.1	3.1 - 10.6	2.4	3 - 5	**3.1 - 5**	**3.1 - 5**
CG (dB)	7.5 - 10.8	9.8 - 14	10.1	10	**19.5**	**10.5**
NF (dB)	-12.4 - -15.2	-14.5 - -19.6	12.7	8	**12.5**	**19.8**
IIP3(dBm)	-7	-11	3.8	-	**10**	**15**
P_{DC} (mW)	8	1.85	6	-	**4.2**	**0.8**
CMOS Tech. (μm)	0.18	0.13	0.13	0.25	**0.25**	**0.25**
Chip Area (mm^2)	8.21	0.34	0.53 × 0.6	-	**1.24**	**0.70**

∗1 Active Mixer †2 Passive Mixer

Table 5.1: Performance Summary and Comparison with State-Of-The-Art CMOS Wideband Mixers

5.6 Summary of Mixer Design

An active and a passive mixer have been proposed, designed and fabricated for the proposed receiver architecture. This is so because of the need to experiment and find the most suitable type of mixer, and for research purposes where size and DC power has to be given special consideration. The circuits designed have been optimised for low DC power and better linearity, as this is essential for the the receiver to overcome the effect of cross-talk or intermodulation distortion in the receiver. A Gilbert-cell mixer presents some conversion gain and some amount of linearity good enough to combine with that of the LNA, as compared to a passive mixer which has no conversion gain but conversion loss, although better linearity and very low DC power consumption which is one design focus in this work. In this design conversion gain is as important as linearity. This is why the author has designed both types of mixer to explore their advantages separately. The active mixer has been properly designed for conversion gain while the passive mixer has been designed for low DC power and higher linearity. The conversion gain against RF frequency and LO power for the fabricated active mixer is shown in Figure 5.5 and 5.6. The

simulated noise figure as a function of LO power is presented in Figure 5.6. The measured linearity of the fabricated mixer is shown in Figure 5.7 with IIP3 of 10 dBm, OIP3 of -2 dBm and P_{1dB} of -2 dBm. Simulated results of the passive mixer conversion loss against LO power is presented in Figure 5.12 and the linearity in Figure 5.13. The mixer's design has been compared in Table 5.1 with state-of-the-art Mixer design. The passive mixer proved to be the best option, with small chip area, very low DC power and higher IIP3 of 15 dBm and OIP3 of 20 dBm. The circuit layout was carefully laid to achieve small chip area; Figures 5.4 and 5.10 are the fabricated mixer micrograph occupying 1.24 mm^2 and 0.70 mm^2 chip area respectively.

Chapter 6

Wideband Oscillators and Pulse Generators

6.1 Introduction

Wireless electronics designed with the intent of forming the implanted transceiver of a Medical Body Area Network (MBAN) can be especially challenging. The rigours of regulatory approval create challenges for packaging, and the electromagnetic properties of the various intervening biological materials introduce a high path loss. In almost all cases, implantable medical electronics dictate low-power design techniques to minimise the need for battery replacement or intervals between external recharging.

In transceiver design for low-cost CMOS technology, one of the most important elements is the voltage controlled oscillator (VCO). It is part of the frequency synthesiser to generate the local oscillator signal for up-conversion from and down-conversion to the baseband. VCOs are essential building blocks for frequency conversion, frequency synthesisers, clocks and data recovery loops [70].

Two major types of oscillators are: ring and LC oscillators, each have benefits and

drawbacks. Ring VCOs have inferior noise performance but can generate quadrature signals more readily, while LC VCOs offer better phase noise for a given power dissipation. However, it becomes more difficult to achieve all the desired VCO specifications simultaneously as the frequency of operation approaches the self-resonance frequency of the on-chip inductors and the cutoff frequency of transistors f_T. [70], but it takes up more die area, thereby driving up costs. Additional details of the work reported in this chapter can be found in the author's publication [71].

6.2 Voltage Controlled Oscillator Design

A CMOS VCO can be built in different structures such as a ring, a relaxation circuit or an inductor capacitor (LC) resonator circuit. The various topologies of oscillators have advantages that make them suitable for designers in different applications. VCOs have some characteristics that must be considered for proper functioning and effectiveness. This includes tuning range, operating frequency, power consumption and phase noise. The inductor-capacitance (LC)-tank VCO is preferred compared to relaxation oscillators or ring oscillators to fulfil the required high frequency, noise specification and at low power consumption for UWB application. The LC-tank VCO is made up of high quality passive devices such as inductors and varactors in an inherently lossy CMOS technology. In LC-tank VCOs, phase noise and power consumption depend primarily on the quality factor of the tank [72]. Integrated LC voltage-controlled oscillators (VCOs) are common functional blocks in modern radio frequency communication systems. Due to the ever-increasing demand for bandwidth, very stringent requirements are placed on the spectral purity of local oscillators [73].

6.3 Properties of Oscillator

The most critical performance specification of an oscillator is its spectral purity, usually characterised by phase noise. Phase noise is the term used to describe the aggregate noise power of unwanted modulation products close to a signal at a specified offset from the actual carrier frequency. In the frequency domain, an ideal signal appears as a single frequency spectral line, while the phase fluctuations due to phase noise appear as sidebands around the centre frequency. Intuitively, phase noise can be thought of as an infinite number of phase modulation sidebands, each one arising from a low frequency modulating signal [74].

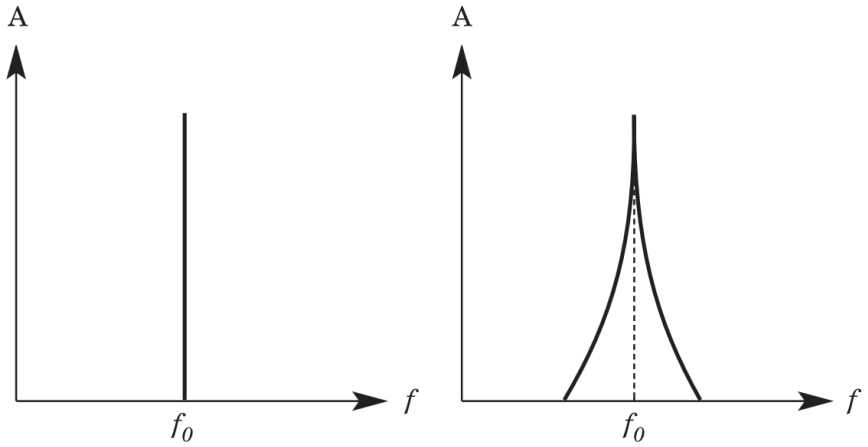

Figure 6.1: An Ideal, Noiseless Signal has a Single Spectral Line (left); The Addition of Phase Noise Results in a Signal with Modulation Sidebands Extending above and below the Nominal Centre Frequency (right).

As noise power is higher near the carrier, it can extend far into the sidebands; the actual offsets are multiples of ten to allow logarithmic scale plots of the power levels. The noise power contribution may be to due to several varied mechanisms and each will affect the carrier at different offsets. In a receiver, the phase noise of the local oscillator

(LO) degrades the received signal-to-noise ratio (SNR) of the desired signal at the IF by a process often referred to as reciprocal mixing. This limits the ability to detect a weak signal in the presence of a strong signal in an adjacent channel [75]. Phase noise also corrupts the information present in phase modulated signals by effectively rotating the symbol constellation, degrading the bit error rate (BER) of communication systems. In a transmitter, LO phase noise is modulated onto the desired signal and results in energy being transmitted outside of the desired band [76]. Since many wireless transceivers are battery powered, it is a requirement to minimise the power consumed by the oscillator circuit. Thus, there is a tradeoff between phase noise and power consumption until the voltage swing is maximised [77]. In UWB transmitter design phase noise is not as critical and so power consumption could be minimised to the barest minimum [71].

6.3.1 Oscillator Design Theory

A microwave resonator is the component in a microwave circuit that determines the frequency of oscillation. It can be implemented in various ways depending on the following factors: operational frequency, required performance, cost and chip size. An oscillator can be either a series or a parallel LC network. The resonance frequency of a series or parallel resonant circuit is given by:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{6.1}$$

The quality factor, or Q-factor, is a characterisation of the loss of a resonant structure, as higher Q-factor implies lower loss. The Q-factor is defined as:

$$Q = \omega \frac{\text{Average energy stored}}{\text{Energy loss per second}} \tag{6.2}$$

Hence, for a series RLC circuit,

$$Q = \frac{\omega_0 L}{R} \tag{6.3}$$

LC resonators are easy to implement on-chip at relatively low microwave frequencies. The Q-factor of the resonator circuit may be very low, as the Q-factor of the inductor leads to poor phase noise performance in VCOs. However, the phase noise of an oscillator is proportional to $1/Q^2$, so improving the Q-factor of the inductor will vastly improve the oscillator performance.

An oscillator can be viewed as a single two-port feedback circuit or as double one-port circuit. The linear feedback model for an oscillator can be represented as shown below, The closed-loop transfer function of Figure 6.2, can be given as

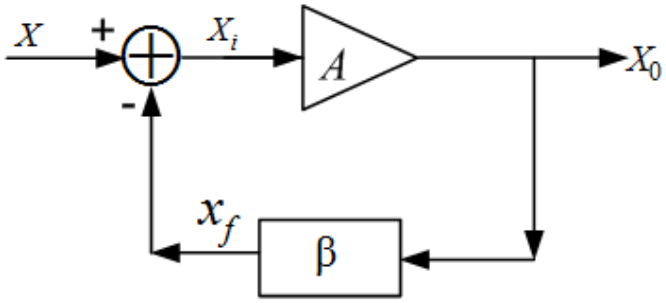

Figure 6.2: Basic Oscillator Feedback Model

$$A_f(s) = \frac{A(s)}{1 - A(s) \cdot \beta(s)}. \tag{6.4}$$

The Barkhausen criterion for oscillation is given as follows;

$$A(s) \cdot \beta(s) = 1 \tag{6.5}$$

where $s = j\omega$.

The Barkhausen's criterion for oscillation is necessary but not sufficient. If the phase shift is equal to 360^0 at zero frequency and the loop gain is sufficient, the circuit latches up rather than oscillates. To stabilise the frequency, a frequency selective circuit network is added and is named as the resonator [78]. If A has zero phase shift, β can be implemented

as a resonator realised with an LC tank having zero phase shift at the desired oscillation frequency. Another way to view an oscillator is as shown in Figure 6.3 which consists of an active network and a resonator circuit; when the equivalent parallel resistance R_T of the resonator is exactly balanced by a negative resistance $-R_a$ of the active circuit, the negative resistance compensates for the losses in the resonator and a steady-state oscillation is achieved.

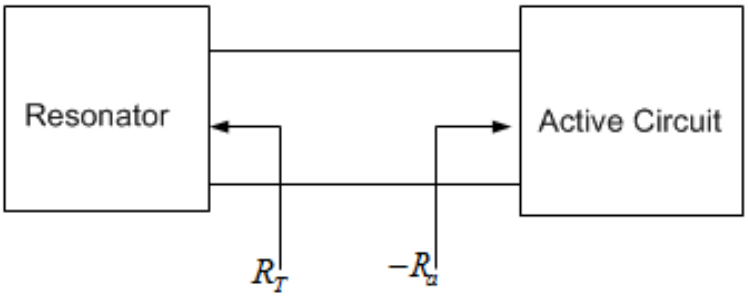

Figure 6.3: One-port Network View of an Oscillator

Oscillators can be classified into various categories depending on the components; that is, single transistor oscillator and differential oscillator. The single transistor oscillator topologies are the Colpitts and Hartley oscillators, among others, while the differential oscillator topologies are the single switched VCO (SS-VCO) and the double switched VCO (DS-VCO). The differential topologies are popular in the design of integrated oscillators [78].

The differential LC cross-coupled transistor SS-VCO, consumes less power compared to the DS-VCO which requires a large supply voltage due to additional stacking of the PMOS. The parasitic capacitances associated with the transconductance cell are large in the DS-VCO, hence this reduces the tuning range and the maximum oscillation frequency but gives better phase noise performance compared to the SS-VCO at the expense of high power consumption and larger chip area.

There is a fundamental start up constraint: The LC VCO equivalent parallel tank impedance at resonance R_T is a strong function of the oscillation frequency and inductance:

$$R_T\omega_0 = Q_T\omega_0 \cdot L = \frac{(\omega_0 L)^2}{r_s} \tag{6.6}$$

where Q_T is the resonator quality factor and is assumed to be dominated by the inductor losses represented here by a physical series resistance r_s of the coil, which eventually becomes a function of frequency due to proximity effects and substrate eddy current induced losses. In any oscillator, the most important design criterion is satisfying the startup conditions, and in tuneable LC oscillators these conditions are a function of frequency.

In this thesis we focus on the SS-VCO, which consists of two integrated inductors, a varactor, and two transistors cross-coupled. The transconductance in this circuit is set by the bias condition and the dimensions of the cross-coupled paired transistors, which provides a negative resistance to compensate for the losses in the resonator circuit. In order to control the negative resistance, and hence set the oscillation amplitude, a tail current source is employed.

6.3.2 Phase noise of an ideal oscillator

The Norton form of current source across an LC tank can be represented by a mean-square spectral density of [79]

$$\frac{\overline{i_n^2}}{\Delta f} = 4kTG \tag{6.7}$$

where G is the reciprocal of the tank resistance. The net effective impedance seen by the shunt noise current source is simply that of a perfectly lossless LC resonator, for a small displacement $\Delta\omega$ from the the centre frequency ω_0 the impedance of an LC tank may be approximated by [79]

$$Z(\omega_0 + \Delta\omega) \approx j\frac{\omega_0 L}{2\Delta\frac{\omega}{\omega_0}}. \tag{6.8}$$

when

$$Q = \frac{R}{\omega_0 L} = \frac{1}{\omega_0 G L}.$$

Hence,

$$|Z(\omega_0 + \Delta\omega)| \approx \frac{1}{G}\frac{\omega_0}{2Q\Delta\omega}. \tag{6.9}$$

Multiplying the spectral density of the mean-square noise current by the square of the magnitude of the tank impedance, to obtain the spectral density of the mean-square noise voltage, gives

$$\frac{\overline{V_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f}|Z|^2 = 4kTG\left(\frac{1}{G}\frac{\omega_0}{2Q\Delta\omega}\right)^2 = 4kTR\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2. \tag{6.10}$$

Note that an increase in tank Q reduces the noise when all other parameters are held constant, also thermal noise causes fluctuations in both amplitude variations in real oscillators are attenuated and phase fluctuations dominate. The equipartition theorem of thermodynamics allows us to assert that, in the absence of amplitude limiting, noise energy splits evenly between amplitude and phase fluctuations so that suppression of amplitude variations leaves us with half the noise given by equation 6.10 [79]. Moreover, we are interested in how large this noise is relative to the carrier rather than its absolute, value so it is traditional to normalise the mean-square noise voltage density to the mean-square carrier voltage, and report the ratio in decibels. This results into a phase noise given by

$$L(\Delta\omega) = 10\log\left[\frac{\overline{V_n^2}/\Delta f}{\overline{V_{sig}^2}}\right] = 10\log\left[\frac{2kT}{P_{sig}}(\frac{\omega_0}{2Q\Delta\omega})^2\right]. \tag{6.11}$$

The units of equation 6.11 are commonly expressed as decibels below carrier per hertz (dBc/Hz) at some offset frequency $\Delta\omega$ from the carrier frequency ω_0.

Leeson [79] further modifies equation 6.11 to

$$L(\Delta\omega) = 10\log\left\{\frac{2FkT}{P_{sig}}\left[1 + (\frac{\omega_0}{2Q\Delta\omega})^2\right]\left(1 + \frac{\Delta\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right)\right\} \tag{6.12}$$

In the early work of Lee and Hajimiri [79] on oscillators, it is further shown that

$$P_{SBC}(\Delta\omega) = 10\log\left[\frac{I_m C_m}{4q_{max}^2\Delta\omega^2}\right]^2. \tag{6.13}$$

where P_{SBC} is the sideband power disposed symmetrically about the carrier

$$P_{SBC}(\Delta\omega) = 10\log\left[\frac{\frac{\overline{i_n^2}}{\Delta f}\sum C_m^2}{4q_{max}^2\Delta\omega^2}\right]. \tag{6.14}$$

From Parseval's theorem

$$\sum C_m^2 = \frac{1}{\pi}\int_0^{2\pi}|\Gamma(x)|^2dx = 2\Gamma_{rms}^2. \tag{6.15}$$

Phase noise can then be expressed as

$$L(\Delta\omega) = 10\log\left[\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{max}^2\Delta\omega^2}\right]. \tag{6.16}$$

Another important design feature is a low phase noise for LC oscillators with high quality resonator or LC-tank. This can be demonstrated by the equations for phase noise and power consumption.

$$dV_{out}^2\Delta\omega = KT\cdot r_s\cdot[1+F]\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\left(\frac{2}{A^2}\right). \tag{6.17}$$

$$g_m = \frac{1}{R_T} = \frac{r_s}{(\omega_0 L)^2}. \tag{6.18}$$

where $dV_{out}^2\Delta\omega$ is the single-side-band spectral noise density at an offset $\Delta\omega$ from the oscillation frequency ω_0, g_m is the transconductance calculated from the Barkhausen criterion, F is the term that include the excess noise of the oscillators negative resistance, A is the differential output amplitude and r_s is the LC-tank effective resistance, and is generally determined by the inductor. From equations (6.17) and (6.18) the inductor series resistance should be kept as low as possible, since this lowers the phase noise as well as the power consumption.

The phase noise of a cross-coupled oscillator is given by [79]

$$L(\Delta\omega) = 10 \cdot \log \cdot \left(\frac{\overline{i_n^2}/\Delta f}{2(\Delta\omega)^2} \cdot \frac{\Gamma_{rms}^2}{q_{max}^2} \right). \tag{6.19}$$

where $\Delta\omega$ is the offset frequency from the carrier, q_{max} is the maximum signal charge swing, i_n^2/Δf is the power spectral density of the parallel current noise, and Γ_{rms} is the rms value of the effective impulse sensitivity function (ISF) [80], [79]. ISF is defined as

$$\Gamma_{eff}(\omega t) = \Gamma(\omega t) \cdot \alpha(\omega t) \tag{6.20}$$

where Γ is the impulse sensitivity function (ISF) representing the time-varying sensitivity of the oscillator phase to perturbations and α is the noise modulating function (NMF), a deterministic periodic function representing the modulation of the noise [80]. The noise density is given by

$$i_n^2/\Delta f = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS} - V_T) \tag{6.21}$$

where γ is the mobility of the carriers in the channel, C_{ox} is the oxide capacitance per unit area, W and L are the width and length of the MOS transistor respectively, V_{GS} is the gate source voltage, and V_T is the threshold voltage. Equation (6.21) is valid for both short- and long-channel regimes of operation. As reported in [81] the noise generated from the pMOS and nMOS transistors reaches its maximum when the oscillator is sensitive to perturbation and hence results in a lower phase noise for a given resonator Q and bias current.

6.3.3 Tuning Frequency of VCO

A wide tuning range in a VCO is a major aim and can be achieved by a parallel combination of switched binary-weighted capacitors or a MOS varactor. The loop gain of a VCO varies considerably over the wide tuning range. The sensitivity of the quality factor of inductors to operational frequency, varactor nonlinearities and its quality factor

variations causes significant deterioration in phase noise and some amplitude variations. These issues make UWB VCO design more complicated. In general VCOs are mostly tuned using variable capacitors. The amount of variable capacitance that can be added to the LC-tank is limited by the fixed parasitic capacitance from the inductor and the transistors. High-Q inductors are obtained by a combination of high inductance with low parasitic resistance. But these result in a coil occupying a large area, and also in high parasitic capacitance which degrades PN. In a VCO with a variable capacitor the tuning range is non-linear and the resulting gains are large, which makes the VCO more susceptible to voltage noise induced phase noise. In this work we have implemented two different methods of tuning, using a PN diode varactor and a MOS varactor. In a MOS varactor, the MOS transistor drain and source are connected together. Both methods are used to achieve a wide tuning range VCO with very low phase noise and low power supply. The major advantage of a MOS varactor is that it can be easily integrated in CMOS. Although Q is relatively low in the transition region of a MOS transistor, a low-Q MOS varactor can be used to obtain fine tuning as described in [55]. High speed VCO design is challenging for many reasons, one of the major difficulties is the resonator design. It is desirable for the resonator to have a large inductor for better L/R ratio to achieve better phase noise and a large varactor with high C_{max}/C_{min} ratio for a wider frequency tuning range, because

$$Tuning = \frac{C_{v,max} + C_{fix}}{C_{v,min} + C_{fix}} \tag{6.22}$$

where C_v is the varactor capacitance and C_{fix} is the fixed parasitic capacitance. The frequency of oscillation f_o is determined by

$$f_o = \frac{1}{2\pi\sqrt{L(C + \Delta C)}} \tag{6.23}$$

where ΔC is the change in capacitance due to the varactor. This imposes a trade-off between the tuning frequency and phase noise [55].

There are three device properties employed to improve the tuning range:

1. Large MOS varactor with good C_{max}/C_{min} ratio and Q
2. SOI transistor to reduce transistor fixed capacitance by 30% compared to bulk CMOS
3. Small single-turn top level-only inductor; that is, the use of a smaller inductor allows larger varactors, hence better tuning range.

6.3.4 VCO Designed with MOS Varactor

A more promising approach to tuning is with the voltage controlled gate capacitance of the MOS structure [82]. The quality factors and absolute capacitance over the tuning range are generally high. A strong capacitance variation within a few hundreds of millivolts makes MOS varactor devices useful at low supply voltages [80]. This work have equally demonstrated a high tuning range MOS varactor suitable for UWB transmitters.

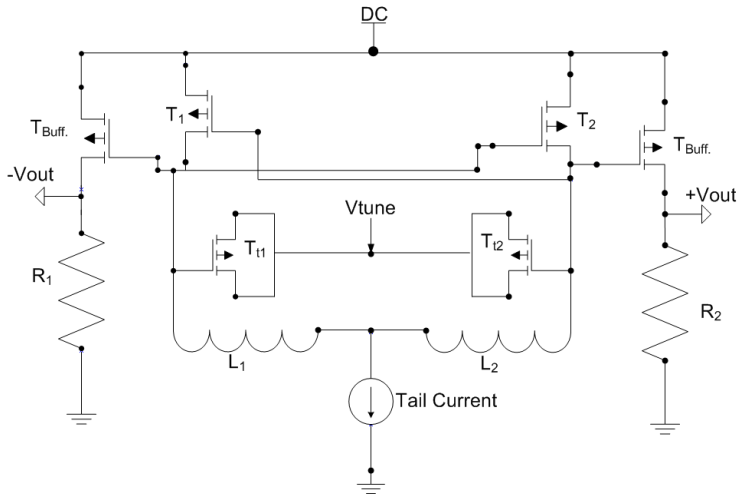

Figure 6.4: MOS Varactor VCO

6.3.5 VCO Layout

The VCO layout structure was made symmetrical since it is differential with a balanced output. All necessary design rules were carefully observed in AWR. An automated circuit verification and performance run such as the design rule check (DRC) and layout versus schematic (LVS) was performed. To achieve greater accuracy and critical interconnects to better understand electromagnetic (EM) couplings between metals in the design, an EM analysis is used before the design goes to the manufacturer. The last stage in the design flow is the generation of the filler cells, used to fill any spaces between regular library cells to avoid planarity problems. They are needed when the density of the required metal or layer has not met the foundry requirement. Thus, it must be added either for low or high frequency.

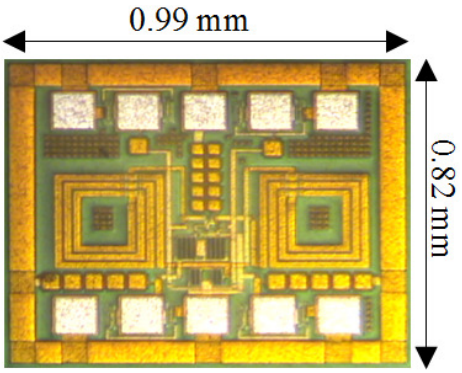

Figure 6.5: Fabricated MOS Varactor VCO Micrograph

6.3.6 Designed VCO Experiment Results

A wide tuning range MOS varactor VCO has been designed and measured. The oscillation frequency as measured ranges from 3.1 - 3.6 GHz when a tuning voltage of 0 - 1.8 V is applied at the varactor, and the amplitude of oscillation (that is the power spectrum) is

below -14 dB across the entire frequency range. The phase noise has been measured at various offset frequencies of 1 MHz, 2 MHz, and 3 MHz resulting in phase noise of -108 dBc/Hz, -115.44 dBc/Hz and -121 dBc/Hz respectively. The total power consumed by the designed VCO including the output buffer is 4 mW from a 1.5 V voltage source.

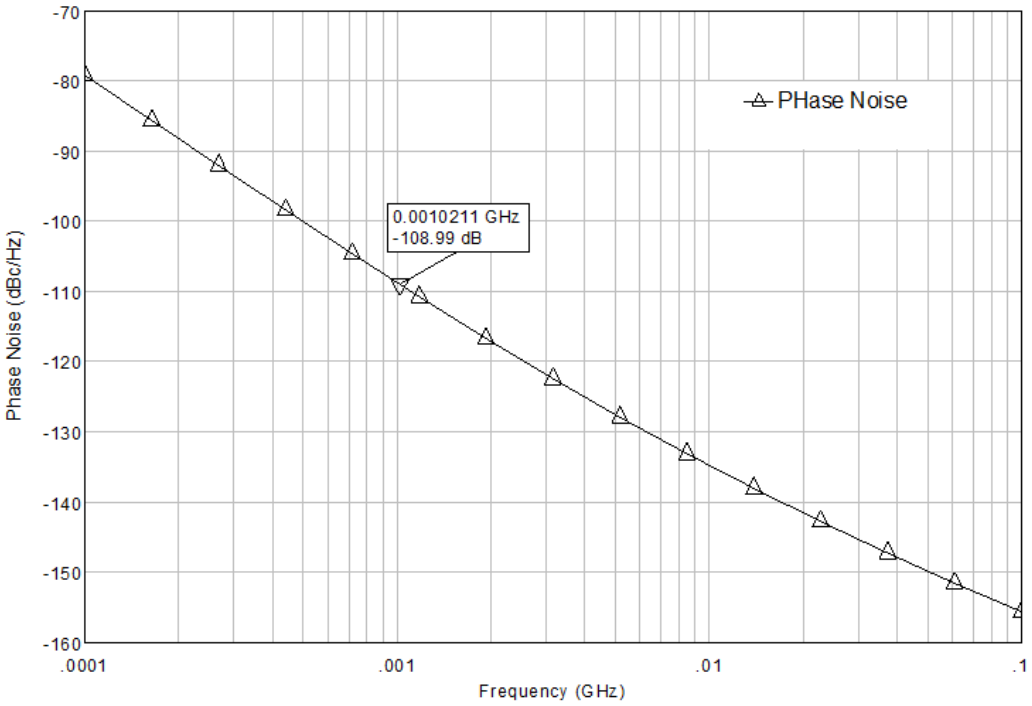

Figure 6.6: Simulated MOS Varactor VCO Phase Noise

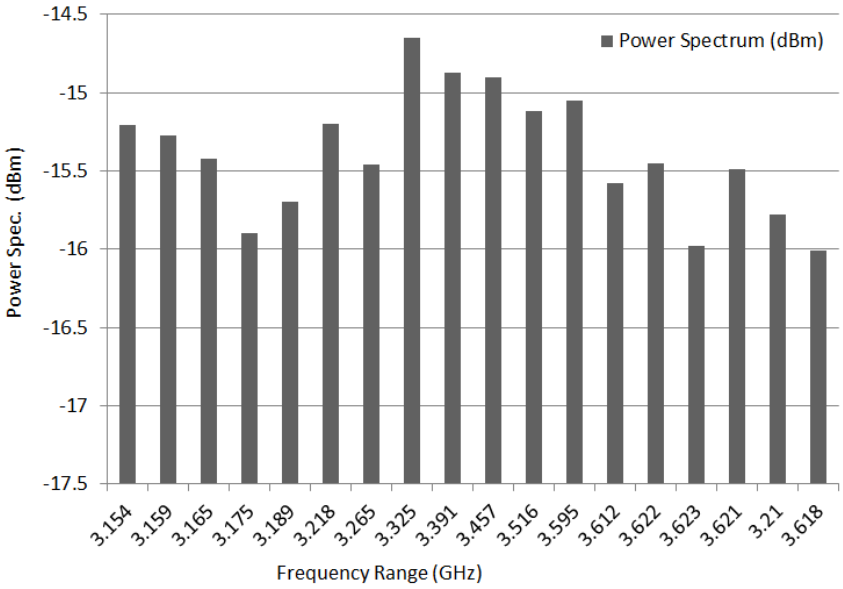

Figure 6.7: Measured Power Spectrum of the MOS Varactor VCO

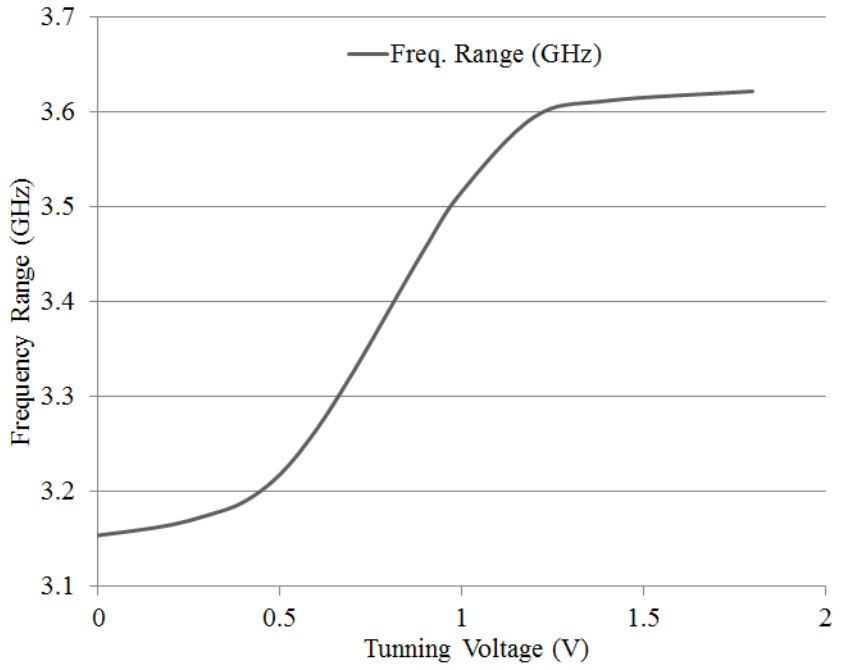

Figure 6.8: Measured Frequency Tuning Range of the MOS Varactor VCO

6.3.7 Phase Noise Calculation

Phase Noise Measurement with spectrum analyser can be calculated as follows: Ps (Carrier level): -13.73 dBm, Pssb (Single Side Band Noise Level at offset): -68.76 dBm. The Pssb has to be converted to a value in 1Hz bandwidth:

L(Noise/1Hz/SSB) = Pssb - 10 log(RBW), where RBW is the resolution bandwidth.

Hence, from the data in Figure 6.9,

L(Noise/1Hz/SSB) = -68.76 - 10 log(200,000) = -121.27 dBm.

Phase Noise at 1MHz offset is: PN(1MHz offset) = L(Noise/1Hz/SSB) - Ps

= -121.27 dBm - (-13.73 dBm)

= -108.87 dBc/Hz

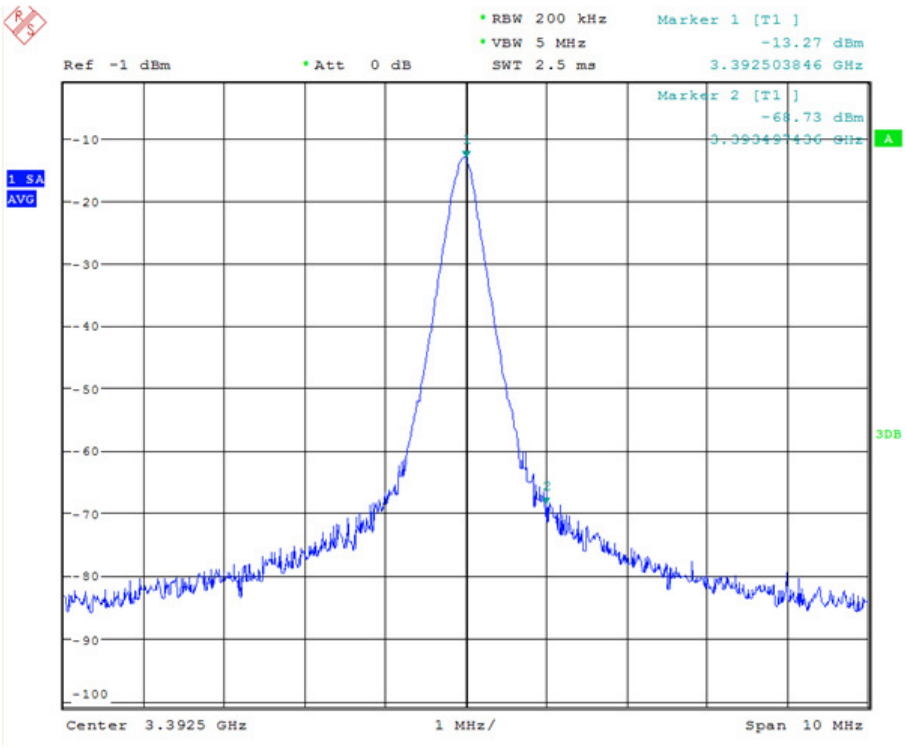

Figure 6.9: Measured Phase Noise of the MOS Varactor VCO is -109 dBc/Hz at 1MHz Offset

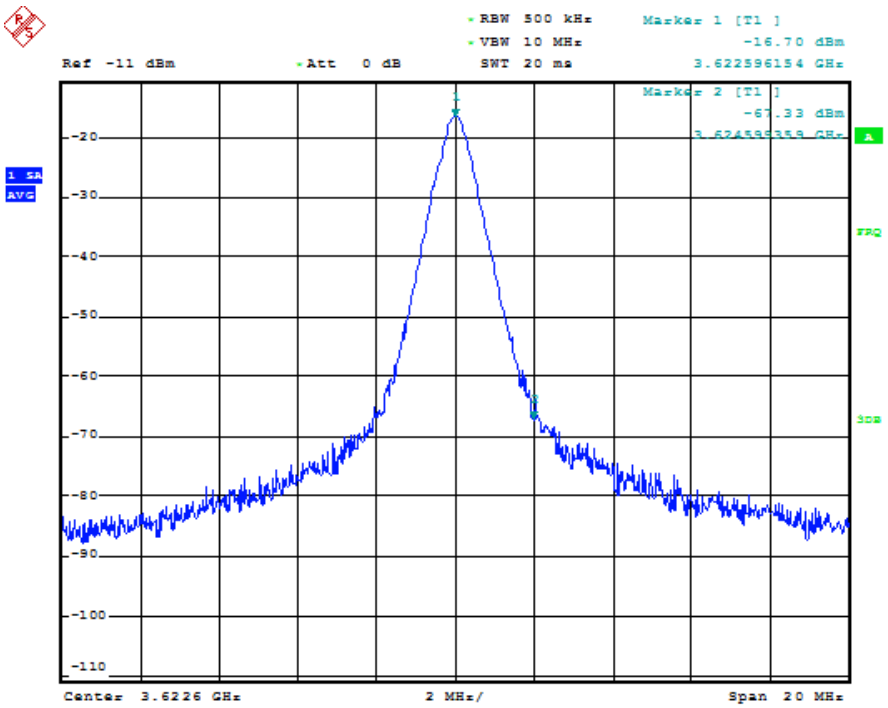

Figure 6.10: Measured Phase Noise of the MOS Varactor VCO is -118 dBc/Hz at 2MHz Offset

6.3.8 Automated Phase Noise Measurement

The automated phase noise was measured using the Rohde & Schwarz FSU spectrum analyser 20 Hz - 67 GHz with the application for Phase noise measurement software FS-K40. The automated measurements are presented in Figure 6.11 and 6.12 at different frequencies. The result obtained from the calculated phase noise are quite close to the automated measured phase noise.

6.3.9 VCO Figure of Merit (FoM) Calculation

A figure of merit is a quantity used to characterised the performance of a VCO relative to other VCOs of the same characteristics. The power, phase noise, frequency of oscillation,

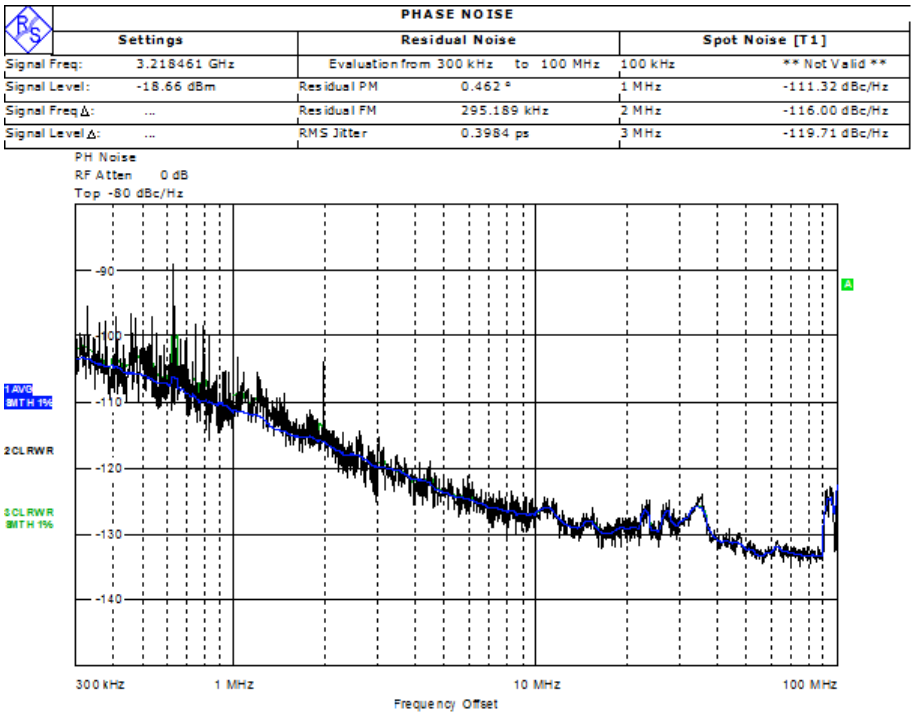

Figure 6.11: Automated Measured Phase Noise of the MOS Varactor VCO at Different Offset

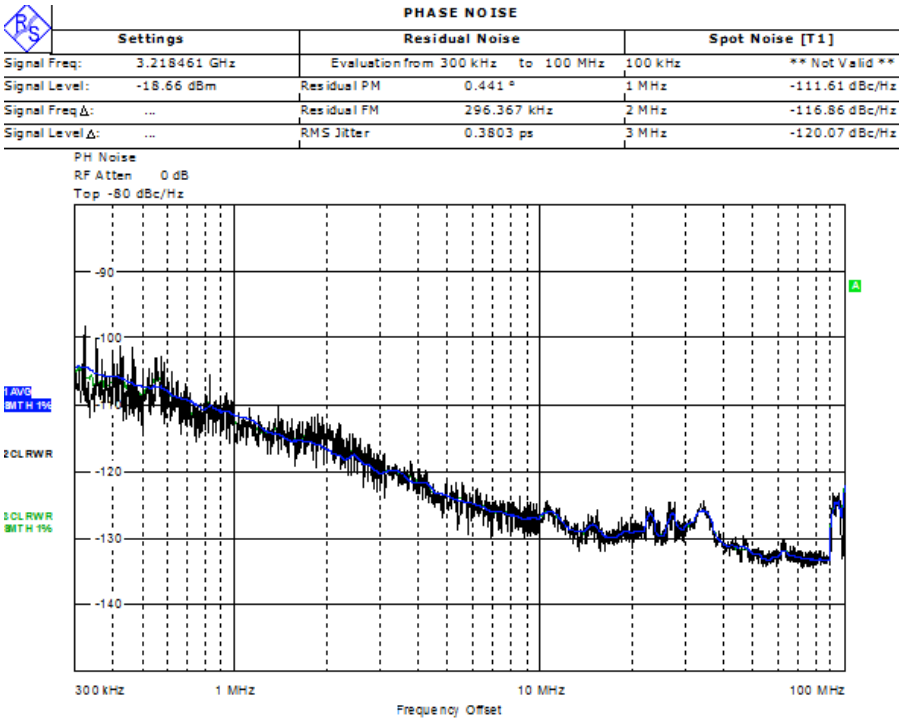

Figure 6.12: Automated Measured Phase Noise of the MOS Varactor VCO at Different Offset

offset from carrier trade offs are included in the FoM value:

$$FoM = L_{\Delta\omega} - 20\log\left(\frac{\omega_o}{\Delta\omega}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right). \tag{6.24}$$

FoM_T is also used to factor the tuning range and is given by

$$FoM_T = L_{\Delta\omega} - 20\log\left[\frac{\omega_o}{\Delta\omega}\cdot\frac{FTR}{10}\right] + 10\log\left(\frac{P_{DC}}{1mW}\right). \tag{6.25}$$

where FTR is the frequency tuning range of the VCO as a percentage, ω_o is the oscillation frequency, $\Delta\omega$ is the offset from the carrier, $L_{\Delta\omega}$ is the phase noise at the specified offset and P_{DC} is the DC power consumed by the VCO core.

6.4 Discussion of the Designed VCO

Various VCOs ware examined for this work, but the MOS varactor VCO was chosen as the best due to its wide tuning range and excellent phase noise performance. A wideband MOS VCO varactor has been designed, fabricated and measured.

Some oscillators have been designed in the past for different needs and applications, and they are associated with one design problem or another. As earlier mentioned, oscillators are designed for a large tuning range and low phase noise irrespective of the operating frequency. In [83] a highly tunable low phase noise VCO was presented; the technique is based on a diode varactor LC tank, and the performance is excellent in both tuning range and phase noise but at the expense of high DC power consumption. A 5 GHz transformer-coupled VCO was reported in [84]; for this design the phase noise and tuning range were also excellent but the DC power consumption was high. In [85], a VCO MB-OFDM frequency synthesiser has been reported for UWB. This design has a wide tuning range and low phase noise at the expense of DC power consumption, but design has not been fabricated. In a recent work, a VCO design for UWB low power applications was reported in [86], designed in 90nm CMOS. This design has a wide tuning range at the expense of phase noise and DC power consumption and the presented results are post layout. The various VCO designs discussed above, have fairly good phase noise as well as a wide tuning range with a major drawback of high DC power consumption which may not be acceptable for low power or implantable radio applications, however in this work a VCO with a low phase noise and wide tuning range at low power is essential. Hence this design is superior to those in [83] - [86]. A comparison and state-of-the-art VCO performance is presented in Table 6.1.

The VCO designed operates in a frequency range of (3 - 4) GHz. The phase noise is measured using a spectrum analyser and calculated to be -108 dBc/Hz at a 1 MHz offset frequency; the simulated and measured phase noise are presented in Figures 6.6

Ref.	[83]	[84]	[85]	[86]	**This Work**
Frequency (GHz)	1.8	5	4.224	2 - 5	**3.1 - 5**
Offset Frequency (MHz)	0.6	1	1	1	**1**
Phase Noise (dBc/Hz)	-127.5	-116.67	-120	-75.2	**-111**
FoM (dBc/Hz)	-	-184	-	-137	**-184**
FoM_T (dBc/Hz)	-	-202	-	-	**-187**
V_{DD} (V)	1.8	1.5	1.8	1	**1.2**
P_{DC} (mW)	32.4	5.85	3.42	8.26	**0.6**
CMOS Tech. (μm)	0.25	-	0.18	0.09	**0.25**
Chip Area (mm^2)	-	0.56 × 0.7	-	0.43× 0.5	**0.85×0.95**

Table 6.1: Performance Summary and Comparison with State-Of-The-Art CMOS Wideband VCO

and 6.9 respectively. The VCO frequency range as a function of power spectrum and tuning voltage are presented in Figures 6.7 and 6.8 respectively. The VCO micrograph is presented in Figure 6.5 with 1.2 mm^2 chip area. The DC power drawn from a 1.2 V voltage source is 0.6 mW.

6.5 Pulse Generator

Pulsed UWB technology is based on the transmission of pulses that have a very short time duration, on the order of a nanosecond or sub-nanosecond, thereby spreading the radio signal power over a wide bandwidth. It potentially offers high time and range resolution, reduced multipath fading, low power and complexity, high data rates and a low probability of undesired detection and interception. Energy-efficient and low-cost pulsed UWB transceivers are attractive for wireless communication and biomedical applications.

6.5.1 Motivation

Modulation is another important function for an IR-UWB system. The information data will be modulated into a special impulse train by the modulation circuit block for wireless transmission. The BPSK scheme in this design has the advantages of simple architecture, low complexity and easy implementation. The differential BPSK modulation circuit, receives one of its inputs from the baseband signal, and the other, the frequency control signal, from the oscillator; the two signals are up-converted and generated into Gaussian pulses for transmission. In this work the design of a UWB pulse generator has been tailored for a low hardware complexity and power consumption.

6.5.2 Pulse Generator Design

There are two categories of pulse generators: the analogue pulse generator and digital pulse generator. A digital pulse generator combines the edges of a digital signal and its inverted signal to form a very short duration pulse and then a differential circuit is used to up-convert the signal. The disadvantage of any digital circuit is its high power consumption. An analogue pulse generator is designed employing the square and exponential functions of transistors biased in the saturation and the weak inversion region respectively.

Since low power design has been our major interest, an analogue pulse generator is the best choice. The only disadvantage of this method is that the amplitude of the output pulse is small, but a wideband amplifier can be applied to improve the amplitude.

The pulse generator is the essential component in an impulse-based UWB transceiver since the design of the pulse will not only affect the transmission and reception of impulse signals but also have an impact on how the interface UWB affects to other frequencies [87]. Existing pulse generators for UWB transmission are not an option for low power applications due to their size and power consumption. Traditional Gaussian UWB pulse generators using Schottky or step-recovery diodes (SRD) are difficult to achieve with standard CMOS according to [88]. Much work on CMOS pulse generators has been carried out for UWB at (3.1 - 10.6) GHz. Some pulse generator designs consists of a rectangular pulse generator and an expensive band-pass filter. These band-pass filters are expensive due to the large size of their inductor which is not desirable in integrated circuit design.

This design is based on a CMOS Gaussian-pulse generator. In generating an ultra-short pulse the desired wave shape must be determined for the system. The most popular pulse shape for UWB communication systems is the Gaussian pulse since it has a condensed power spectral density (PSD) property and its a lower sidelobe compared to a rectangular or sinusoidal pulse; that is most energy is contained in the spectrum of the Gaussian pulse. Gaussian pulses are preferred to simple pulses since they have no DC component, which could represent a limit for the spectral mask compliance and the radiation frequency of the antenna.

The Gaussian pulse and its derivatives are the most common UWB pulse shapes; this is because they feature a sharper frequency roll-off and a higher out-of-band sidelobe rejection compared to other pulse shapes. The standard Gaussian pulse waveform is given

by

$$X(t) = \frac{A}{\sqrt{2\pi\sigma}} \exp -\frac{t^2}{2\sigma^2} \tag{6.26}$$

where A is a constant amplitude, and σ is the original Gaussian standard deviation.a Gaussian pulse is transmitted, due to the derivative characteristics of the antenna, the output at the transmitter antenna can be modeled by the first derivative of the Gaussian pulse. Therefore, if a general Gaussian pulse is given by equation 6.26 [89].

$$X^{(1)}(t) = -\frac{At}{\sqrt{2\pi\sigma^3}} \exp -\frac{t^2}{2\sigma^2} \tag{6.27}$$

then the output at the transmitter antenna will be

$$X^{(2)}(t) = -\frac{A}{\sqrt{2\pi\sigma^3}}(1 - \frac{t^2}{\sigma^2}) \exp -\frac{t^2}{2\sigma^2} \tag{6.28}$$

Equations 6.26, 6.27 and 6.28 represent the Gaussian, monocycle and doublet pulse respectively.

In general, the fourier transform (X(f)) and PSD (P(f)) of the nth-order derivative of the Gaussian waveform can be written as

$$X(f) = A(j2\pi f)^n \exp -\frac{(2\pi f\sigma)^2}{2} \tag{6.29}$$

$$P(f) = A^2(j2\pi f)^{2n} \exp -(2\pi f\sigma)^2 \tag{6.30}$$

This PSD depends strongly on the values of n and σ, shifting to higher frequencies for larger n and smaller σ. This is clearly observed in equation 6.30 and in the peak emission (centre) frequency f_m [89] and [90].

$$f_m = \frac{\sqrt{n}}{2\pi\sigma} \tag{6.31}$$

The low and high frequency components also scale differently with n and σ [90].

The proposed pulse generator consists of three stages of inverter and a NAND gate. A square waveform generator produces a square pulse with sharp rising and falling edges,

which feeds into the delay stage. The delay stage generates three inverted and delayed square waveforms successively. The delay time can be adjusted properly by sizing the PMOS and NMOS transistors of the inverters. The pulses are then combined and inverted by the NAND gate to produce the required Gaussian pulse. During operation, the inverter stages operate as push-pull to reduce the total power consumption because, at any time, only one transistor will be in conduction during pulse generation.

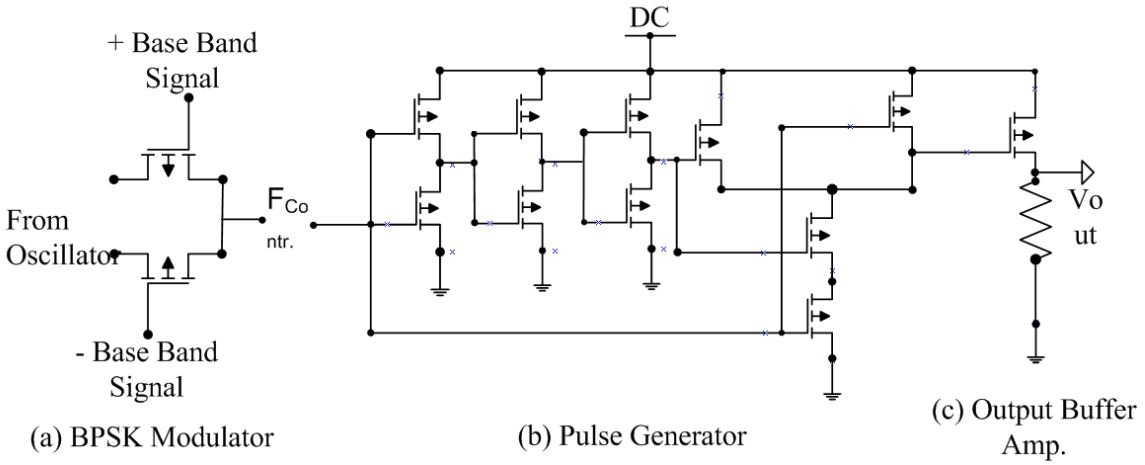

Figure 6.13: Pulse Generator Circuit

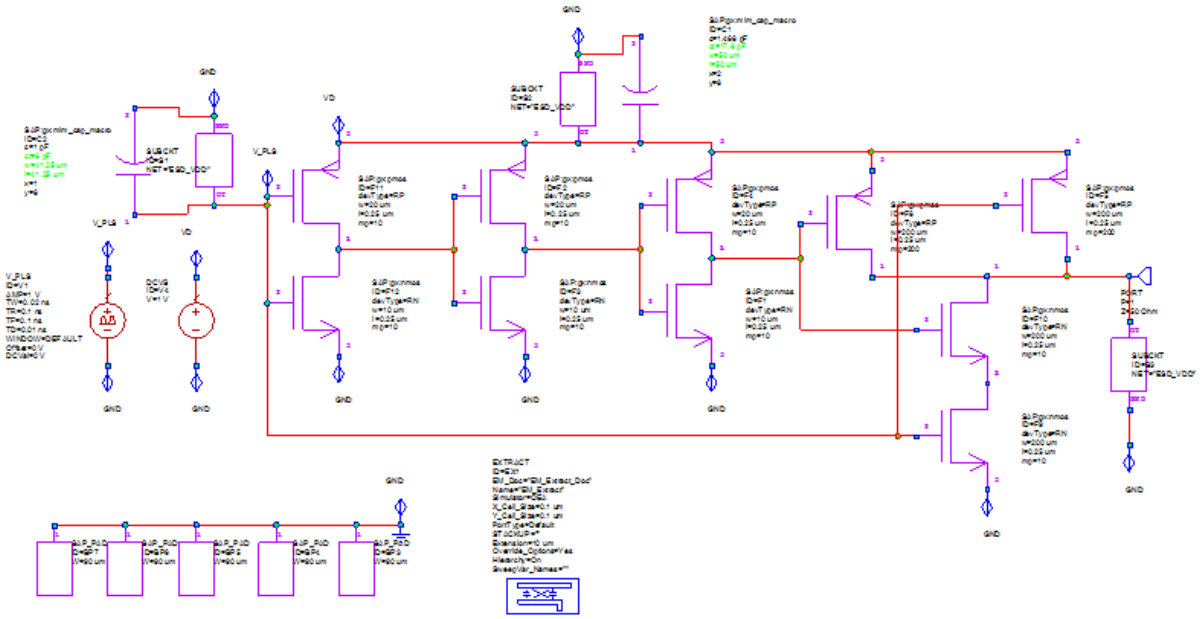

Figure 6.14: Schematic of Designed Pulse Generator Circuit in AWR

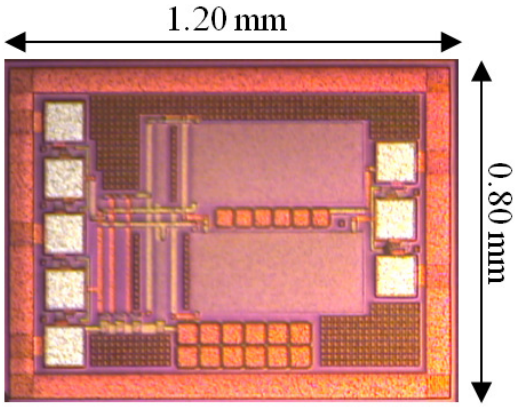

Figure 6.15: Pulse Generator Micrograph

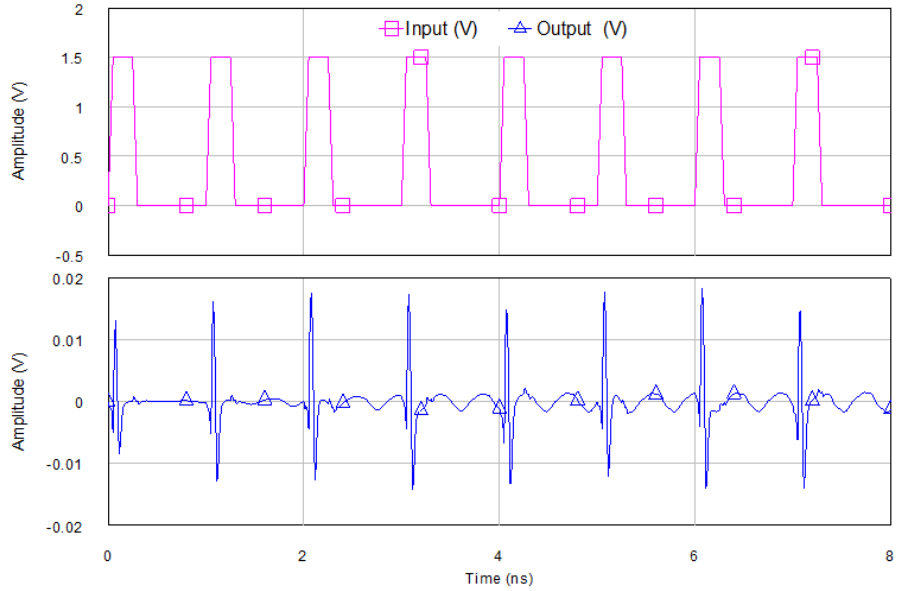

Figure 6.16: Simulated Gaussian Monocycle Pulse of the Pulse Generator

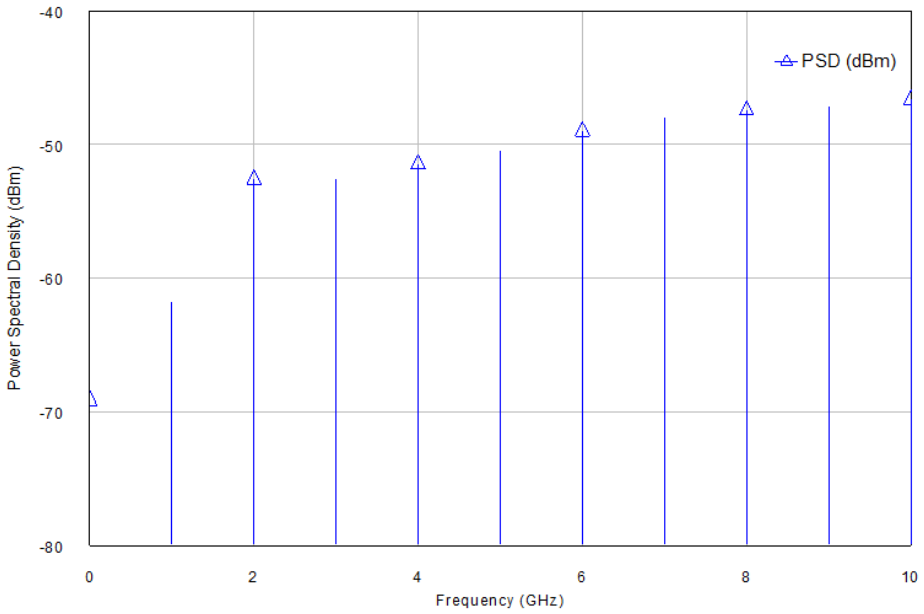

Figure 6.17: Simulated Power Spectral Density of the Pulse Generator

6.6 Pulse Generator Discussion

A pulse generator has been designed and fabricated. The spectral power density is presented in Figure 6.17. The simulated pulse generator output is presented in Figure 6.16. The pulse generator power spectral density is very much below -41.3 dBm which fulfils the spectral mask indoor limit. The amplitude of the output is 20 mm^2, it is important to improve the output pulse amplitude of the pulse generator without exceeding the PSD limit since a power amplifier is not a component of a UWB transmitter. This can be achieved by driving the pulse generator with a free running voltage controlled oscillator; details of this will be discussed in the next Chapter. The micrograph of the pulse generator is presented in Figure 6.15 covering a chip area of 1.0 mm^2.

Chapter 7

UWB Transceiver RF Front End

7.1 Introduction to receiver design

The first stage of receiver front end has the dominant effect on the noise figure, gain and linearity performance of the overall system. The noise figure of the LNA in the receiver chain determines the noise figure of the receiver provided the gain is high enough. Nonlinearity in an RF front end causes many problems such as harmonic generation, gain compression, intermodulation, and desensitisation. The rapid evolution of wireless communications has led to high performance RF circuits in silicon, due to its low cost and high level of integration, but this circuit must still provide high linearity to suppress intermodulation due to increased coexistence of adjacent blockers [91]. This work presents a high performance CMOS front end for applications at UWB frequencies. The purpose here is to develop an analogue receiver front end (LNA + mixer) operating at 3 - 5 GHz for implantable radio applications.

7.2 UWB Receiver Design Consideration

The use generated short pulses requires the use of multi-pulse symbol structures to avoid producing strong spectral lines at multiples of the pulse repetition frequency. Randomisation of the generated pulse train produces a flatter spectrum which helps an IR-UWB system to minimise the use of the available spectral power [92]. There are two methods of data demodulation in UWB communication systems. One is coherent demodulation, which needs precision timing synchronisation between transmitter and receiver which greatly increases the system complexity. The other is non-coherent demodulation, which needs special devices such as a step recovery diode (SRD) to generate or to detect the pulses [93]. A non-coherent receiver is able to recover the energy spread in the multipath channel without requiring channel estimation, with the drawback of noise and interference enhancement. Hence, a non-coherent receiver architecture has been proposed in this design. A fully integrated receiver based on this technique has been fabricated in 0.25μm CMOS SOS technology.

7.3 IR-UWB Receiver Architecture

The IR-UWB receiver architecture implemented in this design is as shown in Figure 7.1. It consists of a low noise amplifier, the down-conversion mixer or the demodulator, and the pulse generator. The signal received from the antenna is multiplied in the demodulator by the signal generated by the pulse generator. The mixer in the receiver chain down converts the RF signal to the required IF signal. The design specifications of the RF front-end low noise amplifier include high gain, low noise figure, input and output matching network, measures of linearity such as the 1dB compression point and intermodulation intercept points across the required frequency range of (3.1 - 5) GHz.

The noise figure of a cascaded system such as the receiver shown in Figure 7.1 can be

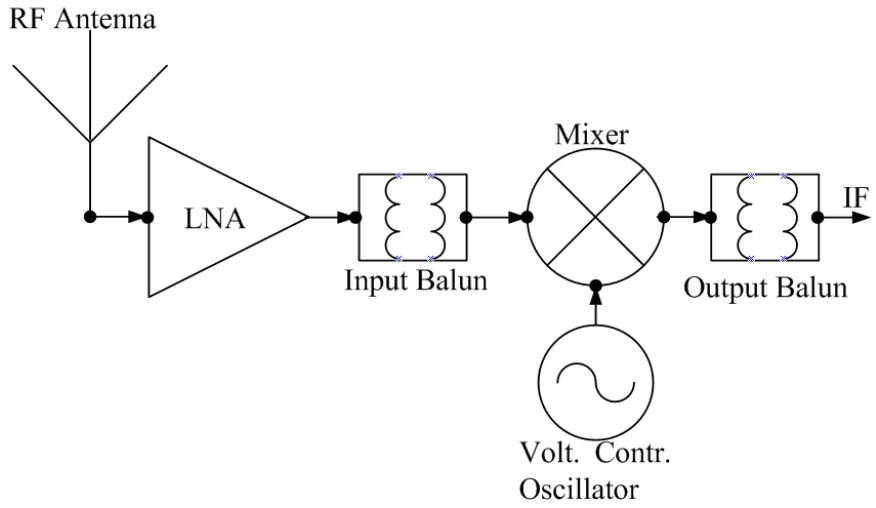

Figure 7.1: The Receiver Architecture

calculated using Friis formula for noise factor. It can be shown that the noise of the first stage is dominant if its gain is high. Thus the noise figure of a receiver is particularly determined by the noise figure of the LNA located at the front of the receiver. Hence, if the gain of the LNA is high enough, the output noise contribution of the next stages will be small.

$$F_{Total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 ... G_{n-1}} \tag{7.1}$$

7.4 Proposed UWB Receiver Design

Various topologies of receiver RF front end have been designed for UWB application in the last few years. In [94] an MB-OFDM UWB receiver has been designed using 0.25μm SiGe BiCMOS technology. This design covers the entire UWB frequency range with high gain and very low noise figure, which makes this design a challenge to others. However, the shortcoming of this design is poor IIP3 and large DC power consumption which limit its application for low power. Another design of UWB receiver by B. Shi et al. [95] using

0.13μm CMOS technology also covers the entire UWB band. It has better gain and noise figure at the the expense of high DC power consumption and poor IIP3.

[96] describes another receiver designed for UWB applications, covering the entire UWB band; the average gain in the design is 73.5 dB and noise figure is 8.4 dB which makes this design outstanding. The shortcoming of this design is poor IIP3 and excessive DC power consumption and as such it may not be suitable for low power applications. Recently, in [97], a paper on a two-stage down-conversion architecture for a 3.1 - 8 GHz UWB receiver front end, using 0.18μm CMOS technology, was presented. This design was able to achieve a better IIP3 compared to previous designs in [94], [95] and [96]. Unfortunately, its total DC power consumption, including buffer, is tremendously high. Another recent development in receiver design according to [98] is a UWB RF receiver design front end. This design is good enough in terms of gain and noise figure but has poor IIP3, and the DC power consumption was not reported. In this work, the author has proposed two types of receiver following the two types of mixer proposed in chapter 5; the goal is to further investigate the best combination of circuits that will support the aims of this project. The receiver's design was optimised for high gain, low noise figure and better IIP3 at low DC power consumption. Table 5.1 shows a summary of the design's receivers and a comparison with the state of the art.

The receiver, as earlier stated, consists of the low noise amplifier that receives weak signal at 3 - 5 GHz from the antenna, amplifies the signal at a minimal noise figure then sends it signal to a mixer whose LO is driven at 3.5 GHz; here the mixing process takes place and the frequency is down-converted to 0.25 GHz. The receiver front end has been designed, fabricated and measured; the signal output is suitable to provide the required analogue signal to the ADC stage, and then to the digital back end of the proposed implantable WBAN. Figure 7.1 illustrates the receiver block diagram; each stage has been carefully designed and coupled for proper matching from one stage to the next to

achieve the expected results.

7.4.1 Receiver Circuit Layout

The circuit layout of the receiver was carefully made to achieve an accurate match between schematic and the post-layout simulation. All necessary design rule checks and a layout versus schematic check were performed without error, and the GDSII file was extracted to prepare the design for manufacture. The design has been manufactured and the micrographs are presented in Figures 7.2 and 7.3.

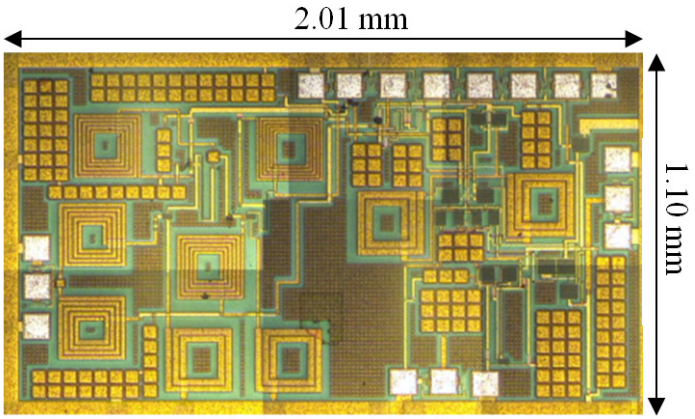

Figure 7.2: Micrograph of Receiver with Active Mixer

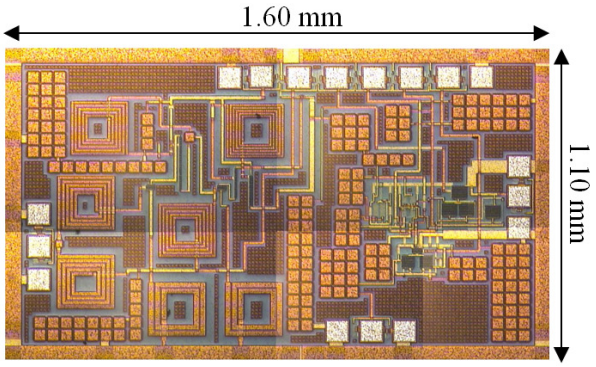

Figure 7.3: Micrograph of Receiver with Passive Mixer

7.4.2 Receiver Design with Active Mixer

The receiver front-end gain and noise factor can be calculated as follows

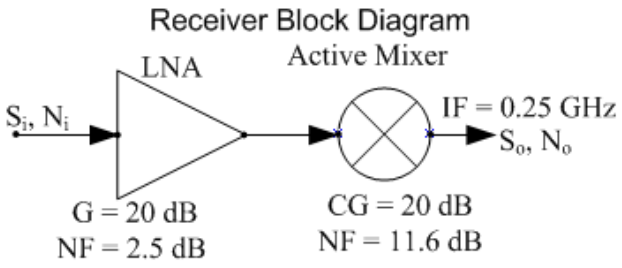

Figure 7.4: Receiver with Active Mixer Chain

The overall gain can be calculated by direct addition since they are in dB

$G_T = G_{LNA} + CG_M$

G_T = 20 dB + 20 dB = 40 dB.

The overall noise factor can be calculated from equation 7.1:

$$F_{Total} = F_{LNA} + \frac{F_M - 1}{G_{LNA}} \tag{7.2}$$

Converting all dB to magnitude:

F_{LNA} = 2.5 dB ≡ 1.778, G_{LNA} = 20 dB ≡ 100, F_M = 11.6 dB ≡ 14.454

Hence,

$$F_{Total} = 1.778 + \frac{14.454 - 1}{100} \tag{7.3}$$

F_{Total} = 1.913 then 10 log(1.913) = 2.817 dB.

Figure 7.5 presents the overall conversion gain as a function of LO power and the overall noise figure as a function of LO power of the receiver designed with an active mixer; for an LO power of -10 dB they are 40 dBm and 2.8 dB respectively. The linearity has been measured with with IIP3 of -30.5 dBm and an OIP3 of 9 dBm as presented in Figure 7.6. The P_{1dB} compression point for the receiver is 5 dBm. The receiver circuit

micrograph is presented in Figure 7.2 with 2.2 mm^2 chip area. A Performance Summary and Comparison with a state of the art CMOS Wideband receiver is presented in Table 7.1.

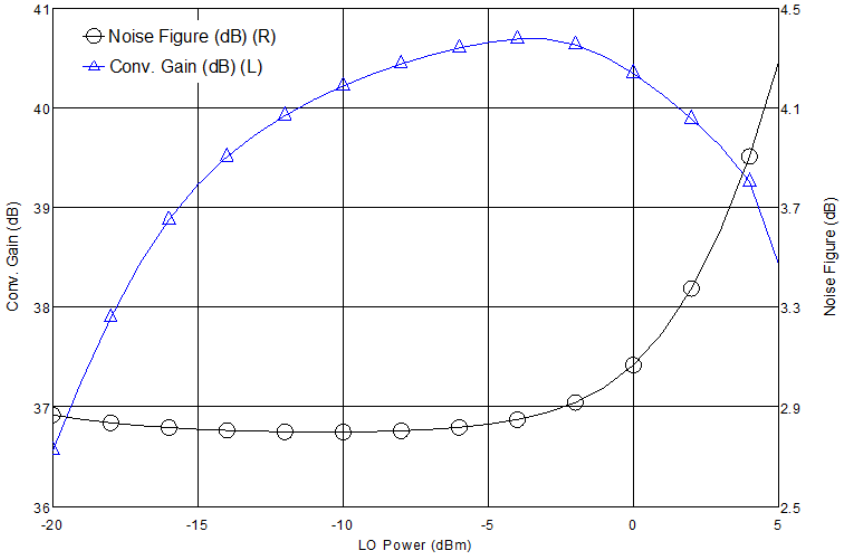

Figure 7.5: Receiver with Active Mixer: Conversion Gain vs LO Power and Noise Figure vs Lo Power Post-layout Result

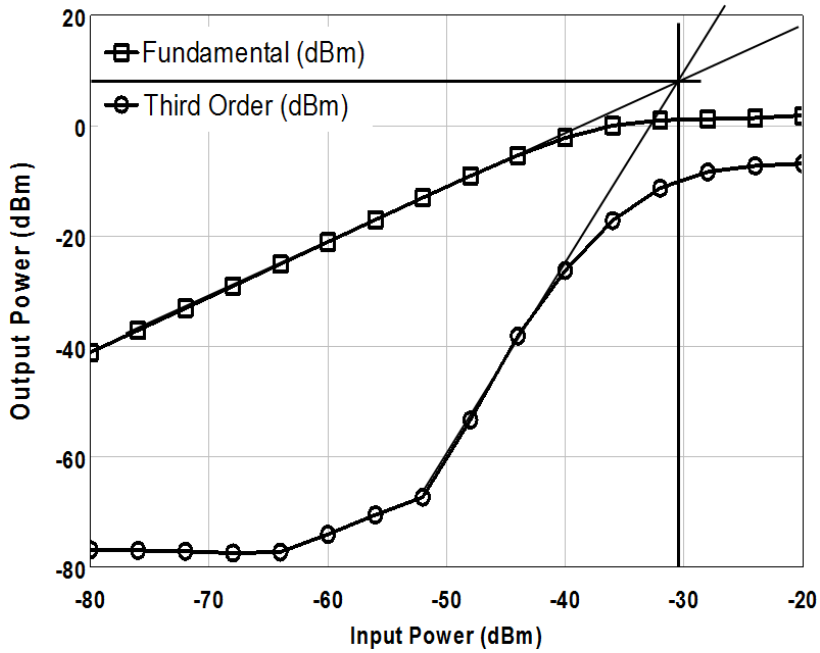

Figure 7.6: Receiver with Active Mixer: Measured Linearity

7.4.3 Receiver Design with Passive Mixer

The receiver gain and noise factor can be calculated as follows

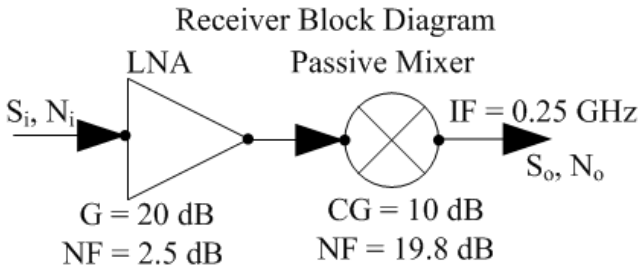

Figure 7.7: Receiver Chain with Passive Mixer

The overall gain can be calculated by direct addition since they are in dB:

$G_T = G_{LNA} + CG_M$

G_T = 20 dB + 10.51 dB = 30.51 dB.

From equation 7.2, converting all dB to magnitude: F_{LNA} = 2.5 dB $\equiv$ 1.778, $G_{LNA} \equiv$ 20 dB = 100, F_M = 19.8 dB $\equiv$ 95.499

Hence,

$$F_{Total} = 1.778 + \frac{95.499 - 1}{100} \tag{7.4}$$

F_{Total} = 2.723 then in dB, 10 log(2.723) = 4.350 dB.

Figure 7.8 presents the overall conversion gain as a function of LO power and the overall noise figure as a function of LO power of the receiver designed with the passive mixer to be 30.5 dBm and 4.5 dB respectively.

The linearity has been measured with an IIP3 of -8 dBm and an OIP3 of 2 dBm as presented in Figure 7.9. The P_{1dB} compression point for the receiver is -9 dBm. The receiver circuit micrograph is presented in Figure 7.3 with a 1.76 mm^2 chip area. A Performance Summary and Comparison with a state-of-the-art CMOS Wideband receiver is presented in Table 7.1.

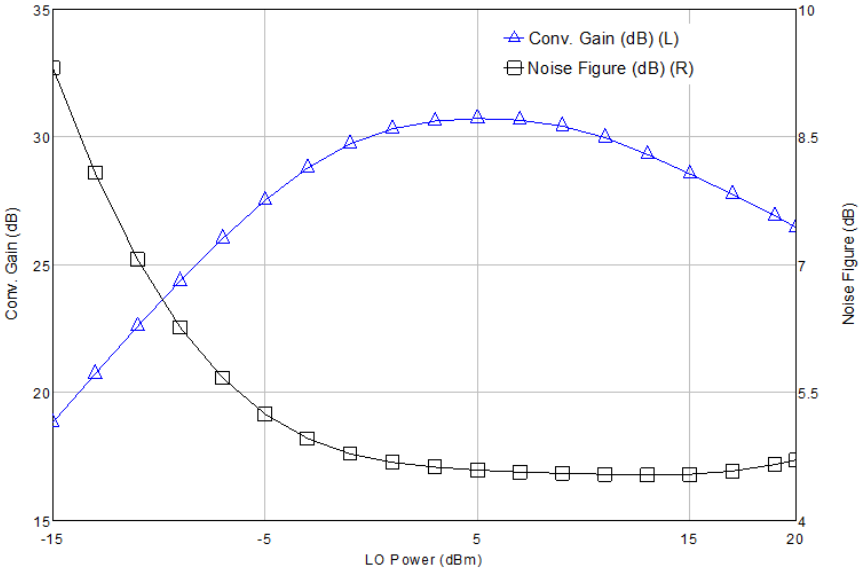

Figure 7.8: Receiver with Passive Mixer: Conversion Gain vs LO Power and Noise Figure vs LO Power Post-layout Result

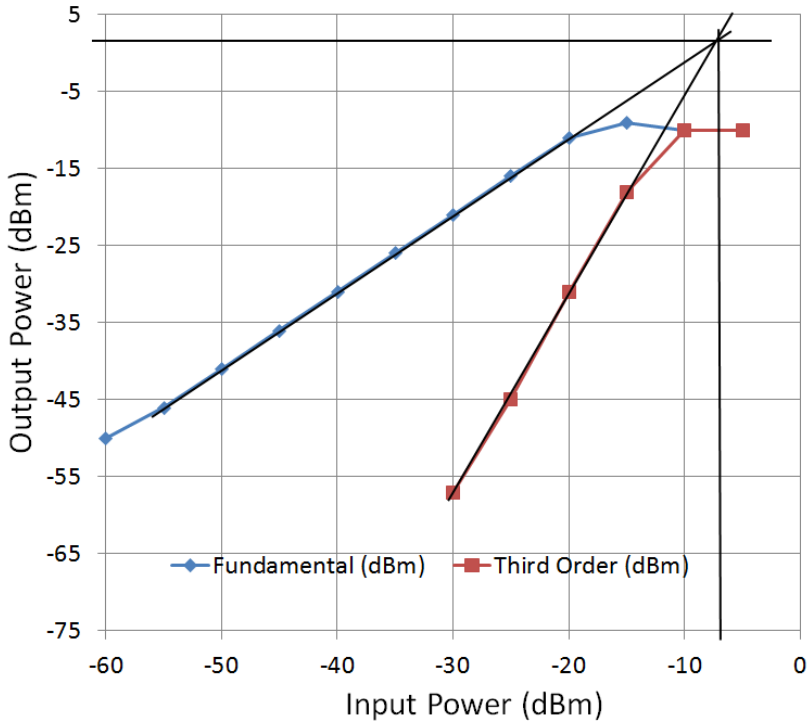

Figure 7.9: Receiver with Passive Mixer: Measured Linearity

7.5 Receiver Design Summary

The high gain LNA designed in chapter 5 and both types of Mixer designed in chapter 6 have been properly matched together separately, which makes up a receiver with active mixer and a receiver with passive mixer. The mixer has an input balun which converts the single ended signal from the LNA to differential for the mixer. The balun also contributes some gain to the receiver circuit. So both single-ended to differential and differential to single-ended balun are engaged in this design for mixer input at RF and output at IF.

Two receiver front ends have been designed, fabricated and measured. Baluns are used to convert from single-ended to differential at the RF input to the mixer from the antenna and differential to single-ended at the IF output of the receiver. The receiver designed with an active mixer achieves high gain while the receiver designed with a passive mixer is employed due to its simplicity and good intermodulation distortion performance. For the purpose of comparison, the advantages of both receivers may be explored separately to determine the best fit for the proposed RF front end. Table 7.1 is the summary and comparison with several state-of-the-art CMOS Wideband receivers; the design described in this work shows better performance in terms of gain, noise figure, linearity and power consumption.

Measurement setup for gain: The mixer and receiver circuits are three-port devices and as such they are measured in the same way. Their gain can be measured using two signal generators and a spectrum analyser. The measurement setup is as shown in Figure 7.10. The gain of the DUT is computed and processed.

Measurement setup for linearity: The linearity of the mixer and receiver circuits are measured using the same set of equipment as above but with an additional signal generator and a power combiner to produce a two-tone signal into the RF port to the DUT. The measurement setup is as shown in Figure 7.11.

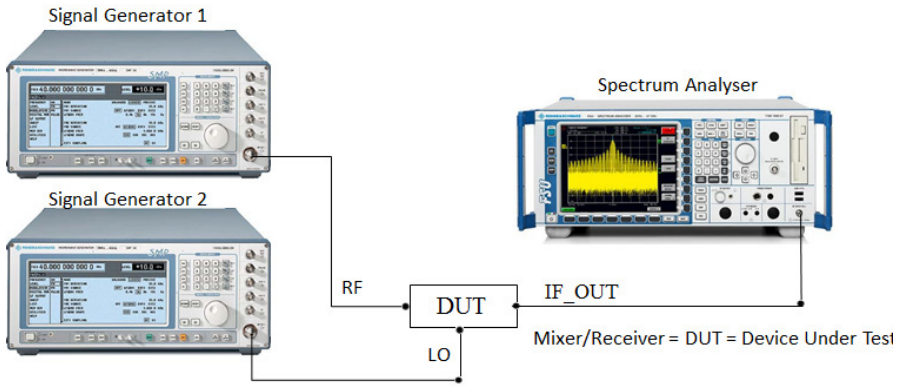

Figure 7.10: Measurement Setup for Mixer/Receiver Gain

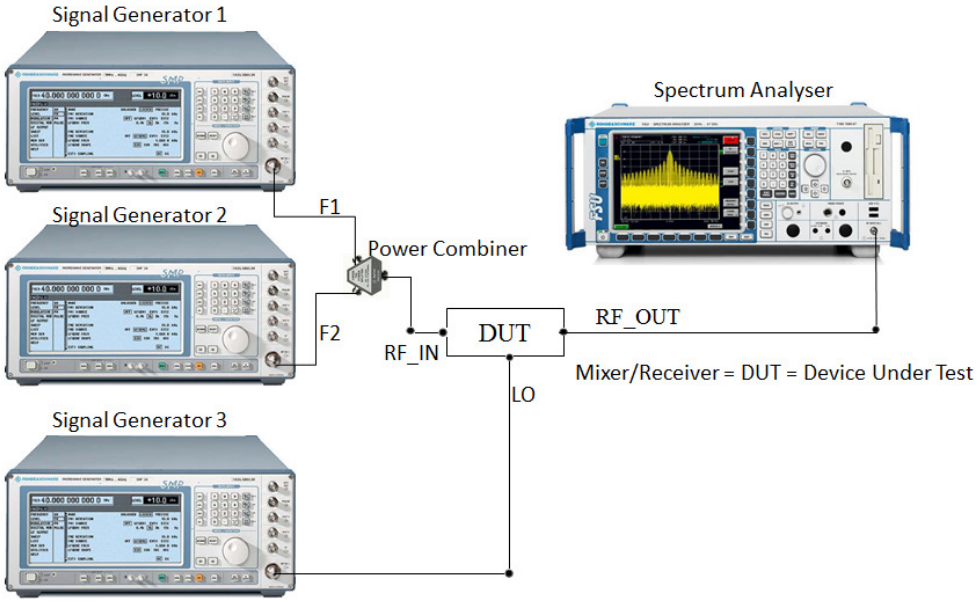

Figure 7.11: Measurement Setup for Mixer/Receiver Linearity

Ref.	[94]	[95]	[96]	[97]	[98]	**1**	**2**
BW (GHz)	3.1 - 10.6	3.1 - 10.6	3.1 - 10.6	3.1 - 8	3 - 5	**3.1 - 5**	**3.1 - 5**
CG (dB)	21.8	26.4	73.5	36.1	18	**40**	**30.5**
NF (dB)	4.1 - 6.2	4.8 - 7.7	8.4	5.4 - 8.3	6.1	**2.8**	**4.5**
IIP3(dBm)	-12.7	-11.5	-	-2.5	-13.2	**-30.5**	**-8**
P_{DC} (mW)	83.7	48	88.74	50.4	-	**22**	**6**
CMOS Tech. (μm)	0.25*	0.13	0.13	0.18	0.18	**0.25**	**0.25**
Chip Area (mm^2)	1.1	1	0.98 × 3.3	0.84 × 1.06	-	**2.2**	**1.76**

∗ SiGe BiCMOS, † 1 Receiver with active mixer, ‡ 2 Receiver with passive mixer

Table 7.1: Summary and Comparison with State-Of-The-Art CMOS Wideband Receivers

7.6 Introduction to UWB Transmitter

UWB technology has great potential for low-power, low-cost radio as it transmits information through short baseband pulses without employing a carrier. Impulse-based UWB provides a low probability of detection, strong multi-path fading resistance and accurate location awareness, which make it a promising radio technique [87].

UWB communication by means of short carrier-free pulses was first conceived in the time-domain electromagnetic spectrum in the 1960s [99]. At this time, the low interceptability and fine ranging resolution of UWB pulses made this type of signalling attractive for military and radar applications; but today the potential for high data rates has ignited commercial interest in UWB systems. Both direct-sequence (DS) impulse communication and multiband orthogonal frequency division multiplexing (OFDM) are presently being considered for UWB standards [12].

DS-UWB and IR-UWB are impulse-based systems. They need no fast fourier transform (FFTs), no digital to analogue converters (DACs) and no fast hopping synthesisers, and since the signal of the impulse-based UWB is duty-cycled, the circuits can be shot down between impulse intervals. Therefore, the impulse-based system leads to low complexity and a low power design well suited for high data rate communication applications [100], [101].

The wideband nature of UWB signals inevitably causes interference with existing narrow-band services, and can be hazardous to some sensitive wireless systems like the Geographical Positioning System (GPS) and Federal Aviation Systems; the FCC has set a limit on the transmitted PSD of the UWB systems to be -41.3 dBm/MHz. The specified spectral mask poses interesting design challenges to system and circuit designers.

There are several pulses applied to UWB systems these include step, Gaussian and Gaussian monocycle pulses. These pulses have similar characteristic of ultra wideband spectrum, since the spectrum of Gaussian monocycle pulse does not includes the DC

portion and low-frequency part, it is available for UWB applications [102].

7.7 UWB Transmitter Design Consideration

Carrier-free and single-carrier transmitters are used in impulse radio. The carrier-free systems directly transmit extremely short pulses on the order of a nanosecond or less, which occupy a bandwidth of up to several GHz [103]. The Gaussian pulse and its derivatives are often utilised as the transmitted pulse since they provide smaller sidelobes and a sharper roll-off in the frequency domain as compared to other pulse types. Hence the fifth derivative of the Gaussian pulse complies with the FCC spectral mask for indoor UWB applications [104]. Therefore, a low-order Gaussian pulse is produced and a filter is commonly employed to shape the pulses in the transmitter.

In single-carrier UWB systems, there are generally two methods to generate FCC compliant pulses: the switch-based method and the up-conversion method. In the former, a narrow pulse is produced first and then the pulse is used to control the switching on and off of the oscillator [103], [105]. It is power efficient since the oscillator is not working and consuming power most of the time due to the low duty cycle of the pulse. However it is only suitable for on-off keying (OOK) or pulse-position modulation (PPM) and energy-detected receivers [105]. In the latter method, a baseband pulse with a low pass spectrum is up-converted in frequency using the LO by a modulator. The centre frequency and the bandwidth can be regulated flexibly by the LO and the baseband pulse separately. Hence it is convenient to make the power spectrum density of the pulse comply with the FCC mask.

7.7.1 Gaussian Pulses Waveform

The most common type of pulses applied UWB are the Gaussian pulse and Gaussian monocycle pulse.

A Gaussian pulse is characterised mathematically as follows:

$$V(t, f_c, A) = A \times e^{-\left(\frac{t-T_c}{T_{au}}\right)^2} \tag{7.5}$$

where A determines the amplitude of the pulse, t is time, T_c is time delay (determine the pulse position) and T_{au} is time decay constant (determine the pulse duration). The resulting shape of the Gaussian pulse from equation 7.5 can exhibits the dc voltage portion in time domain and the low-pass spectrum in frequency domain. The relationship between the pulse duration and center frequency f_c of the pulse is:

$$T_{au} = \frac{1}{(\pi \times f_c)} \tag{7.6}$$

A Gaussian monocycle pulse is the first derivative of the Gaussian pulse in time domain, can be written as:

$$V(t, f_c, A) = 2A\pi f_c \sqrt{e}(t - T_c)e^{-2[\pi f_c(t-T_c)]^2} \tag{7.7}$$

and in frequencey domain a Gaussian monopulse can be written as:

$$V(f, f_c, A) = \frac{1}{2}\sqrt{\frac{2e}{\pi}}\frac{A}{f_c^2}e^{-\frac{1}{2}\left(\frac{f}{f_c}\right)^2} \tag{7.8}$$

The design of ultra-short Gaussian monocycle pulses with controlled pulse to pulse interval of between one hundred and one thousand nanoseconds, with pulse widths of one or lesser than one nanoseconds are referred to as wideband.

7.8 UWB Transmitter Architecture

Pulse based transmitter designs for UWB systems, OFDM and DS-UWB systems require very different types of transmitter. The topologies used for OFDM UWB modulation

are similar to those of existing narrowband systems. Hence, we will focus on the implementation of pulse-based transmitters. A typical pulse-based transmitter consists of a data modulator, which activates the UWB pulse generator in different ways depending on the modulation type such as OOK, PPM or BPSK. The UWB pulse generator then produces modulated pulses with precise frequency characteristics that satisfy the FCC UWB spectrum mask. These circuits are generally categorised into analogue and digital implementations [106], [107], [108]. The transmitter in this report is based on an analogue approach, and generates UWB pulses using a BPSK modulator circuit. A model block diagram of the transmitter can be seen in Figure 5.1. The performance of UWB systems is strongly dependent on the multi-access and modulation scheme. The modulation schemes employed in IR-UWB systems are OOK, PPM and BPSK. In this transmitter design a BPSK scheme is utilised because of its better performance in multi-path environments. The increase of power spectral density levels in BPSK due to the multi-path is less than PPM or OOK, also the bit error rate (BER) of a system with the same E_b/N_o using BPSK is lower than others according to [109].

Most electronic signal processing systems require frequency or time reference signals. To use the full capacity of communication channels, such as wireless, wired and optical channels, transmitters modulate the baseband signal into different parts of the spectrum to exploit better propagation characteristics or to frequency multiplex several messages, and the receivers down-convert them for demodulation. There are two basic types of controlled oscillators that exist: voltage controlled oscillators (VCO) with a voltage control signal and current controlled oscillators (ICO) with a current control signal. In some instances like data communications, the data rate is very accurately standardised. Since a local clock signal is derived from the incoming data signal with a clock recovery circuit to track small variations in the sender's clock rate and to align the phase of the local clock for optimal data recovery, it requires an oscillator whose frequency is controllable [110]. Another

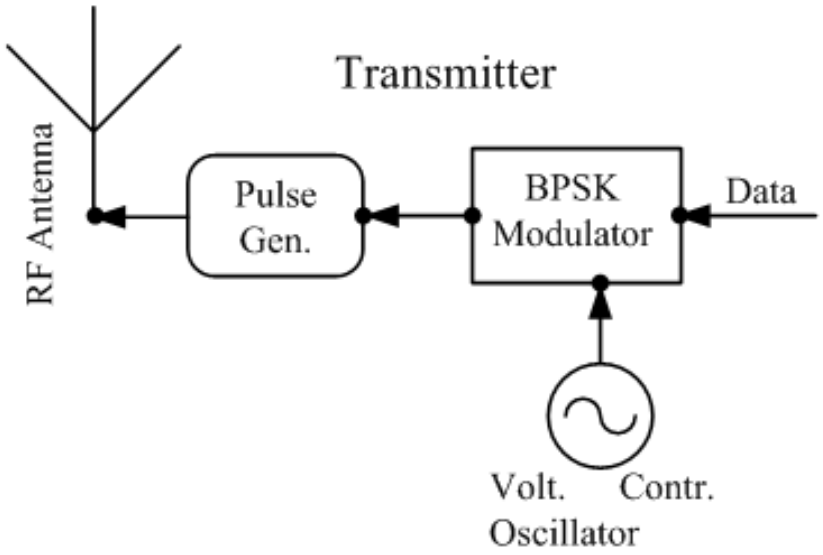

Figure 7.12: Proposed IR-UWB Transmitter Block Diagram

important application of VCOs is for the modulation or demodulation of frequency, or angle modulated carriers.

In [111] a low-powered pulse generator using digital delay elements was presented. The average power consumption at a 100 MHz pulse repetition rate is less than 0.4 mW for the supply voltage of 1.8 V. Also a low powered tunable transmitter for UWB radio based on a ring oscillator VCO was presented in [112]. The drawback in the transmitter design is the disadvantage of a ring oscillator over an LC oscillator, that is high power consumption. Recently, a transmitter IC with BPSK modulator was presented in [100] and [105]. In a similar way this thesis has adopted the same design but with a better LC VCO to achieve a larger bandwidth and lower phase noise at a low power consumption.

7.9 Experiment Result

The proposed transmitter in this work has been designed and simulated results are presented. The transmitter has been designed according to the UWB regulated standard of transmit power less than -41.3 dBm and pulse width between hundreds and thousands of picoseconds. The simulated pulse generated and power spectral density are presented in Figure 7.13 and 7.14 respectively. A pulse width of 200 picoseconds is applied, with a peak to peak pulse of 100 picoseconds and the amplitude of the input signal is 1 Volt. The output pulse generated has an amplitude of 125 mV and the transmitter power is -42 dBm.

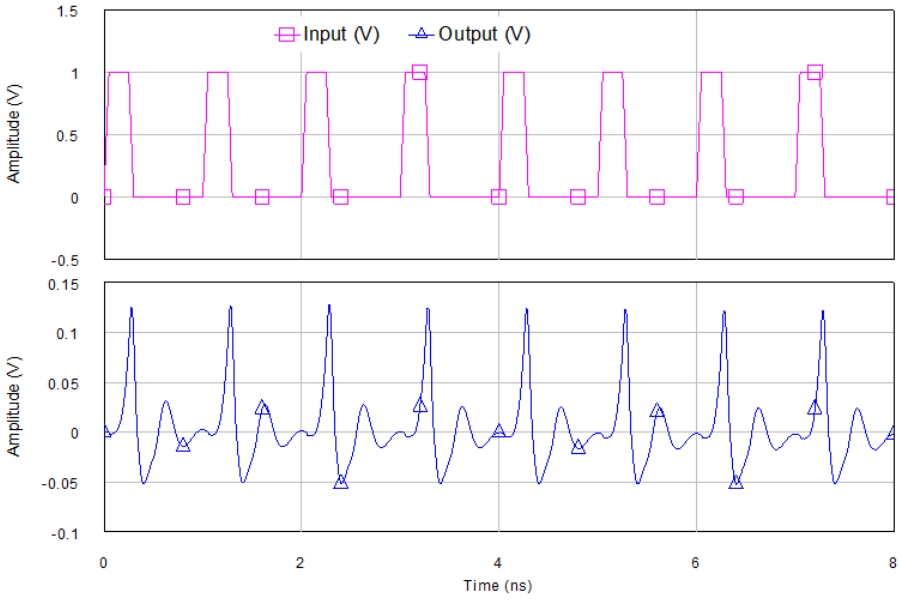

Figure 7.13: Simulated Gaussian Monocycle Pulses

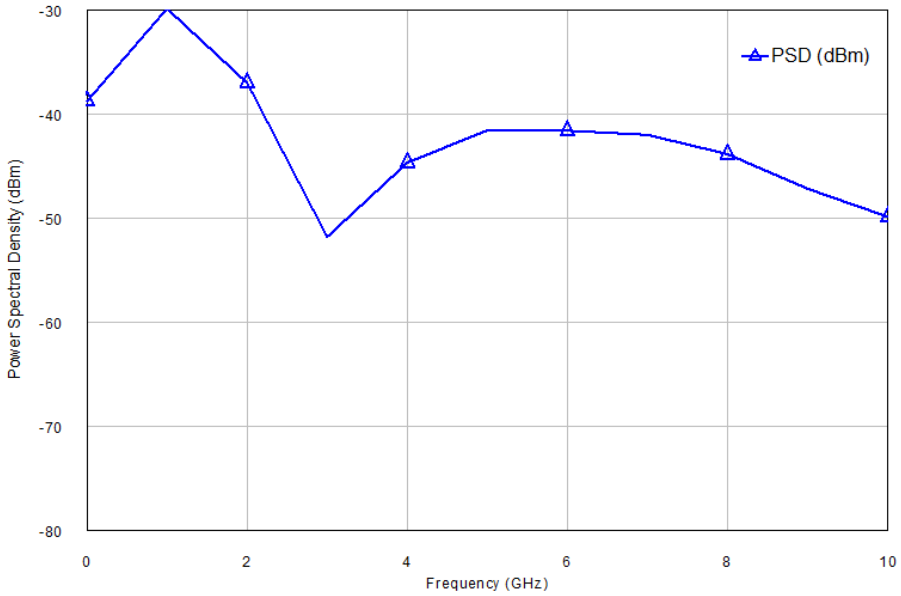

Figure 7.14: Simulated Power Spectral Density of the Transmitter

7.10 Transmitter Design Summary

In UWB transmitter design, a pulse generator is the principal circuit while the VCO provides the necessary frequency and controls the delay or pulse duration. This simple circuitry is used to produce extremely narrow pulses at a very high repetition rate. The generated pulses are then modified to meet the FCC spectral requirements. In this work, a pulse duration time of 200 ps, a peak to peak amplitude of 39 mV and a power consumption of 3.1 mW drawn from a 2 V supply was achieved. The PSD is lower than -41.3 dBm\MHz as defined by the UWB standard.

Chapter 8

Conclusion and Future Work

8.1 Summary of Completed Work

In Chapter 1, the project has been introduced, the motivation and the standardisation of impulse radio was discussed, referring to history and regulation requirements in UWB radio design and updates analysing what has been done and what needs to be added to meet the current technological challenges. In Chapter 2, implantable transceiver design for UWB was analysed, with various regulations and application requirements in this direction such as the ICNIRP and SAR. Also discussed is the transceiver architecture suitable for implantable radio and low power applications at low cost. In Chapter 3, UWB RF front-end design was further analysed, with the link budget system design calculations detailing the path loss and sensitivity of the system. The DC power consumption was also analysed and calculated for low power and long battery life. In Chapter 4 and 5, the circuit design commenced, starting from the receiver chain which consists of the LNA, the Mixer and VCO. A careful design was made of each circuit to exceed the current state of the art. The circuit schematic was properly laid out in AWR and a proper cascade of the circuit was made at minimal coupling losses. The receiver has been discussed from block diagram to circuit schematic and to measurement level. Excellent individual circuit designs were put together to achieve the required receiver. A performance table was made

for each circuit designed, presenting the state of the art.

In Chapter 6, analysis of the transmitter has been made featuring the VCO and pulse generator from block diagram to circuit schematic level. This has been designed to meet the FCC stipulated PSD. Previous work on transmitter design was carefully studied and a new design technique was introduced to achieve large bandwidth and less complex circuitry. Of various types of modulation scheme the best for this design has been considered to achieve excellent transmitter design.

Chapter 8 is the UWB transceiver front end; here, individual circuit designed has been cascaded to form the receiver and the transmitter. In this work the author have designed a low power, less complex analogue RF integrated circuit architecture for implantable wireless body area networks; each circuit has been carefully designed to achieve the state of the art. Despite the 0.25μm CMOS technology used, the designed circuits have been measured up to the current technology. Proper design measures have been put in place to achieve good results. The simulated results are a good fit with the measured results.

Adequate electrostatic discharge (ESD) protection is required for all IC chips, as they are susceptible to ESD damage. However, an ESD protection structure will induce extra parasitics into the circuits such as parasitic capacitance, resistance, substrate noise coupling and self-generated noise, etc., which may significantly affect the core IC performance. Since many RFICs are hand-held devices, they need more ESD protection to avoid damage during and after testing. It is challenging to design an effective ESD circuit; a comprehensive simulation has been carried out using AWR CAD tool. This work has explored good circuit design techniques to overcome the insurgence of ESD protection. The circuit designed for the receiver covers 2mm^2 chip area, while the transmitter covers 0.8mm^2. Therefore the total circuit covers less than 3mm^2 chip area which is small enough for the proposed implant requirement.

8.1.1 Future Work

An analogue RF front end has been proposed for implantable wireless body area networks, to capture images and for video streaming and telemetry, with a transmit distance of 2 cm from one sensor to another. In the future, there should be provision for a longer distance of, say, 5 - 10 cm between nodes; this could be achieved by increasing the transmit power and the receiver gain. A better devices technology will yield better results. Further developments include the ability to move the implant in the body from one location to another through an external control unit or computer.

Appendix A

Derivation

A.1 MOSFET Two-Port Noise Parameters [1]

Recall that the MOSFET noise model consists of two current sources. The mean-square drain current noise is

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f; \tag{A.1}$$

the gate noise is

$$\overline{i_{ng}^2} = 4kT\delta g_g\Delta f, \tag{A.2}$$

where

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{do}}. \tag{A.3}$$

Also recall that the gate noise correlates with the drain noise, with correlation coefficient given as

$$c \equiv \frac{\overline{i_{ng}.i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}.\overline{i_{nd}^2}}}. \tag{A.4}$$

To derive the four equivalent two-port noise parameters:

$$R_n \equiv \frac{\overline{e_n^2}}{4kT\Delta f} \tag{A.5}$$

$$G_u \equiv \frac{\overline{i_u^2}}{4kT\Delta f} \tag{A.6}$$

$$Y_c \equiv \frac{i_c}{e_n} = G_c + jB_c \tag{A.7}$$

A.2 Third-Order Non Linearity [1]

For the specific case of a transconductance,

$$i(V_{DC} + v) \approx c_o + c_1 v + c_2 v^2 + c_3 v^3. \tag{A.8}$$

Consider two sinusoidal input signals of equal amplitude but slightly different frequencies:

$$v = A[cos(\omega_1 t) + cos(\omega_2 t)]. \tag{A.9}$$

Substitute this into the above equations to identify the components of the output spectrum. The DC and fundamental components are as follows:

$$[c_o + c_2 A^2] + \left[c_1 A + \frac{9}{4} c_3 A^3\right] [cos(\omega_1 t) + cos(\omega_2 t)]. \tag{A.10}$$

In general, the nth harmonics come from nth-order factors. Harmonic distortion products, being of much higher frequencies than the fundamental, are usually attenuated enough in tuned amplifiers so that other nonlinear products dominate. The quadratic term also contributes a second-order intermodulation (IM) product as in a mixer:

$$[c_2 A^2][cos(\omega_1 + \omega_2)t + cos(\omega_1 - \omega_2)t]. \tag{A.11}$$

The cubic term gives rise to third-order intermodulation products:

$$(\frac{3}{4} c_3 A^3)[cos(\omega_1 + 2\omega_2)t + cos(\omega_1 - 2\omega_2)t + cos(2\omega_1 + \omega_2)t + cos(2\omega_1 - \omega_2)t]. \tag{A.12}$$

It is straightforward from the sequence of equations to compute the input-referred third-order intercept point (IIP3) by setting the amplitude of the IM3 products equal to the amplitude of the fundamental:

$$|c1A| = \left|\frac{3}{4}c_3A^3\right| \Longrightarrow A^2 = \frac{4}{3}\left|\frac{c_1}{c_2}\right| \tag{A.13}$$

$$IIP3 = \frac{2}{3}\left|\frac{c_1}{c_3}\right|\frac{1}{R_s} \tag{A.14}$$

A.3 VCO Design Constraint [1]

The maximum power constraint is imposed in the form of the maximum bias current I_{max} drawn from a given supply voltage V_{supply}:

$$I_{bias} \leq I_{max}. \tag{A.15}$$

The tank amplitude is required to be larger than a certain value, $V_{tank,min}$, to provide a large enough voltage swing for the next stage:

$$V_{tank} = \frac{I_{bias}}{g_{tank,max}}. \tag{A.16}$$

The tuning range of the oscillation frequency is required to be in excess of a certain percentage of the centre frequency ω:

$$L_{tank}C_{tank,min} \leq \frac{1}{\omega_{max}^2} \leq L_{tank}C_{tank,min} \tag{A.17}$$

where $\frac{(\omega_{max}-\omega_{min})}{\omega}$ = minimum fractional tuning range and $\frac{(\omega_{max}-\omega_{min})}{2} = \omega$. The startup condition with a small loop gain of at least α_{max} can be expressed as:

$$g_{active} \geq \alpha_{min}g_{tank,max} \tag{A.18}$$

where the worst-case condition is imposed by $g_{tank,max}$.

Phase noise in the cross-coupled topology

$$L(\Delta\omega) = \frac{1}{8\pi^2\Delta\omega^2} \cdot \frac{1}{q_{max}^2} \cdot \sum \left(\frac{\overline{i_n^2}}{\Delta f} \cdot \Gamma_{rms,n}^2 \right) \tag{A.19}$$

where $\Delta\omega$ is the offset frequency from the carrier and q_{max} is the total charge swing of the tank. The impulse sensitivity function (ISF) Γ represents the time-varying sensitivity of the oscillator's phase to perturbations. The $\frac{\overline{i_n^2}}{\Delta f}$ term represents the equivalent differential noise power spectral density due to drain current noise, inductor noise, and varactor noise given as follows:

$$\frac{\overline{i_{M,d}^2}}{\Delta f} = 2KT\gamma(g_{do,n} + g_{do,p}) \tag{A.20}$$

$$\frac{\overline{i_{ind}^2}}{\Delta f} = 2kTg_L \tag{A.21}$$

$$\frac{\overline{i_{var}^2}}{\Delta f} = 2kTg_{v,max} \tag{A.22}$$

Appendix B

Circuit Schematics in AWR

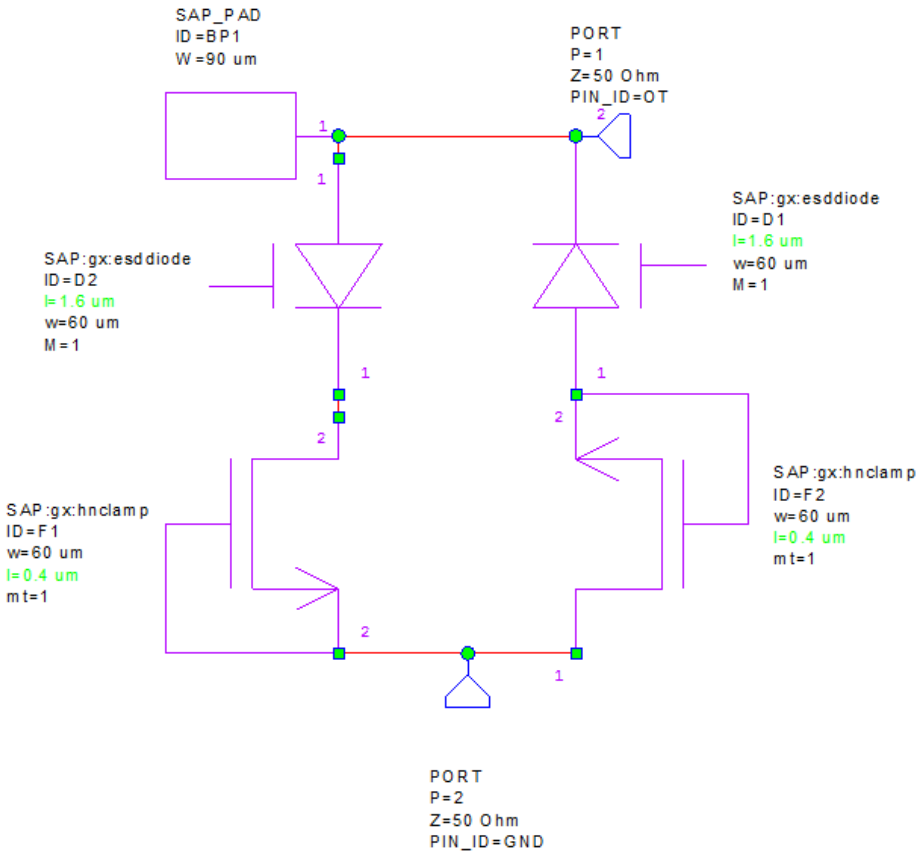

Figure B.1: ESD Circuit Schematic

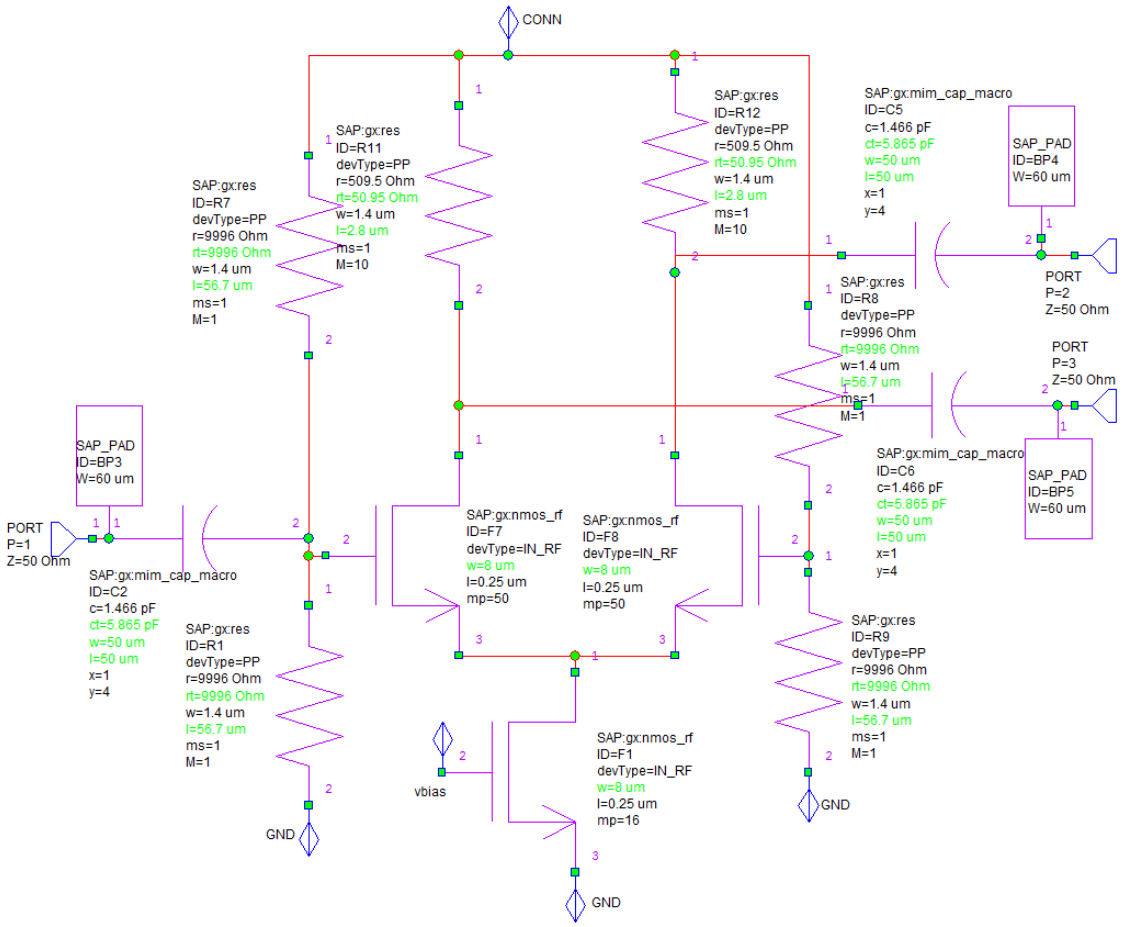

Figure B.2: LO and RF Balun Circuit Schematic

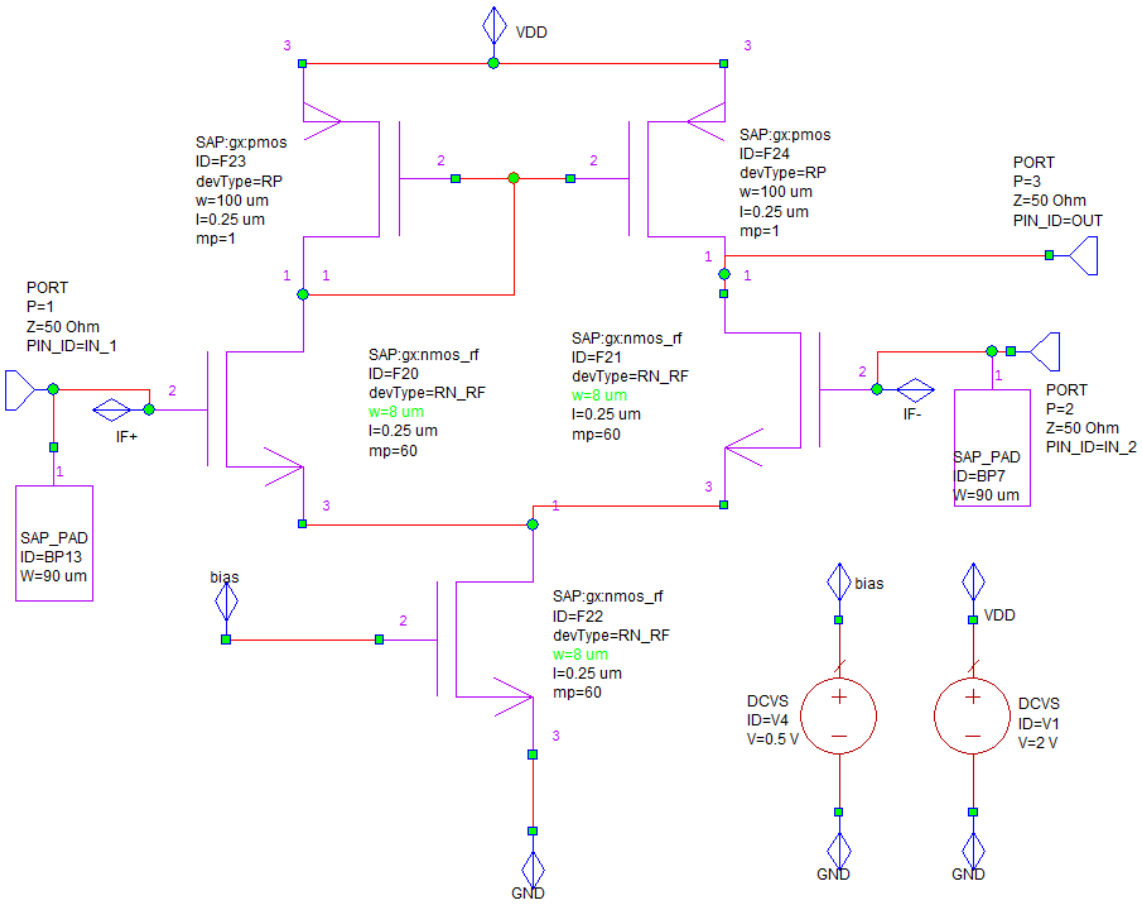

Figure B.3: IF Balun Circuit Schematic

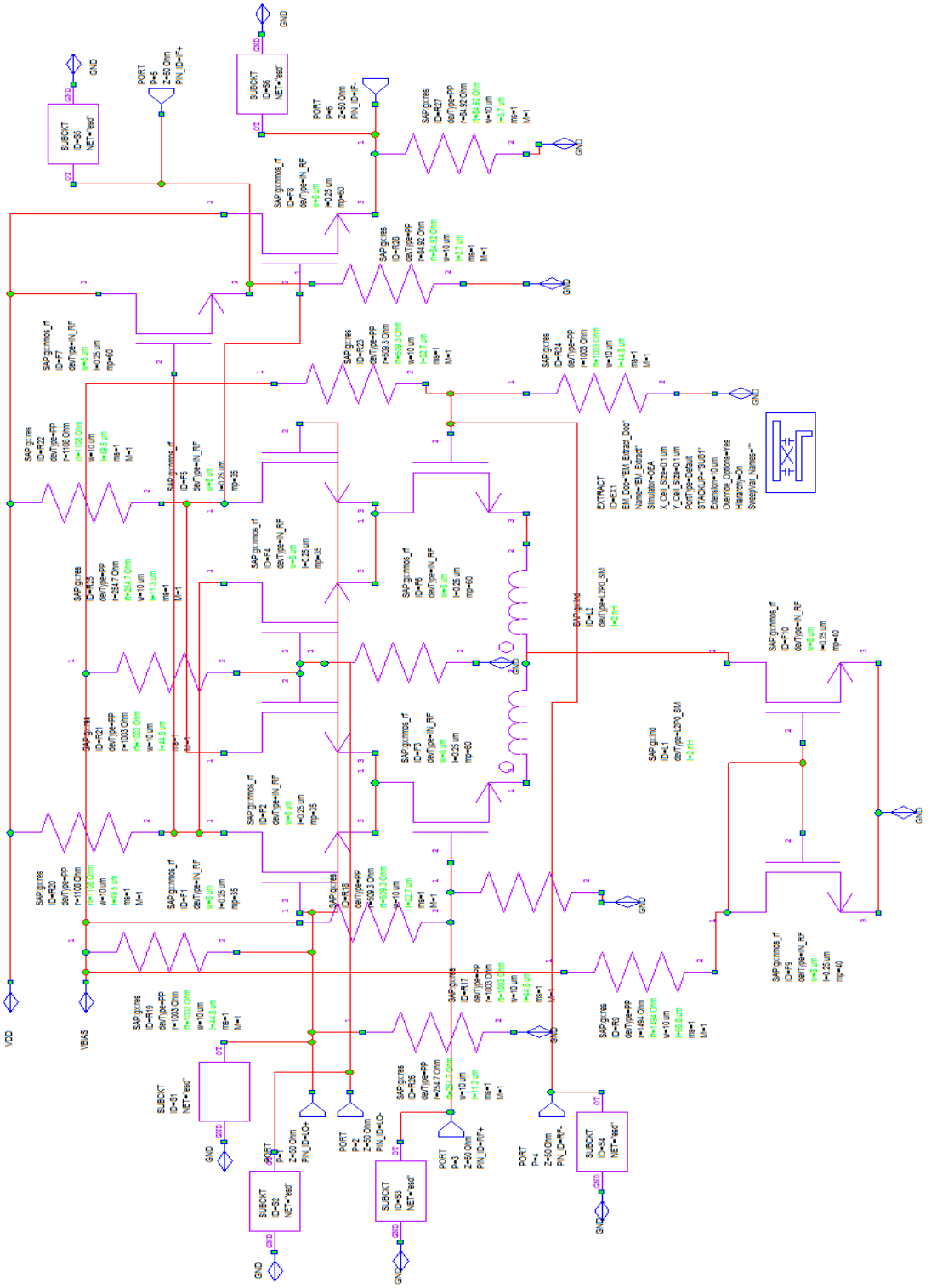

Figure B.4: Core Gilbert Cell Mixer Circuit Schematic

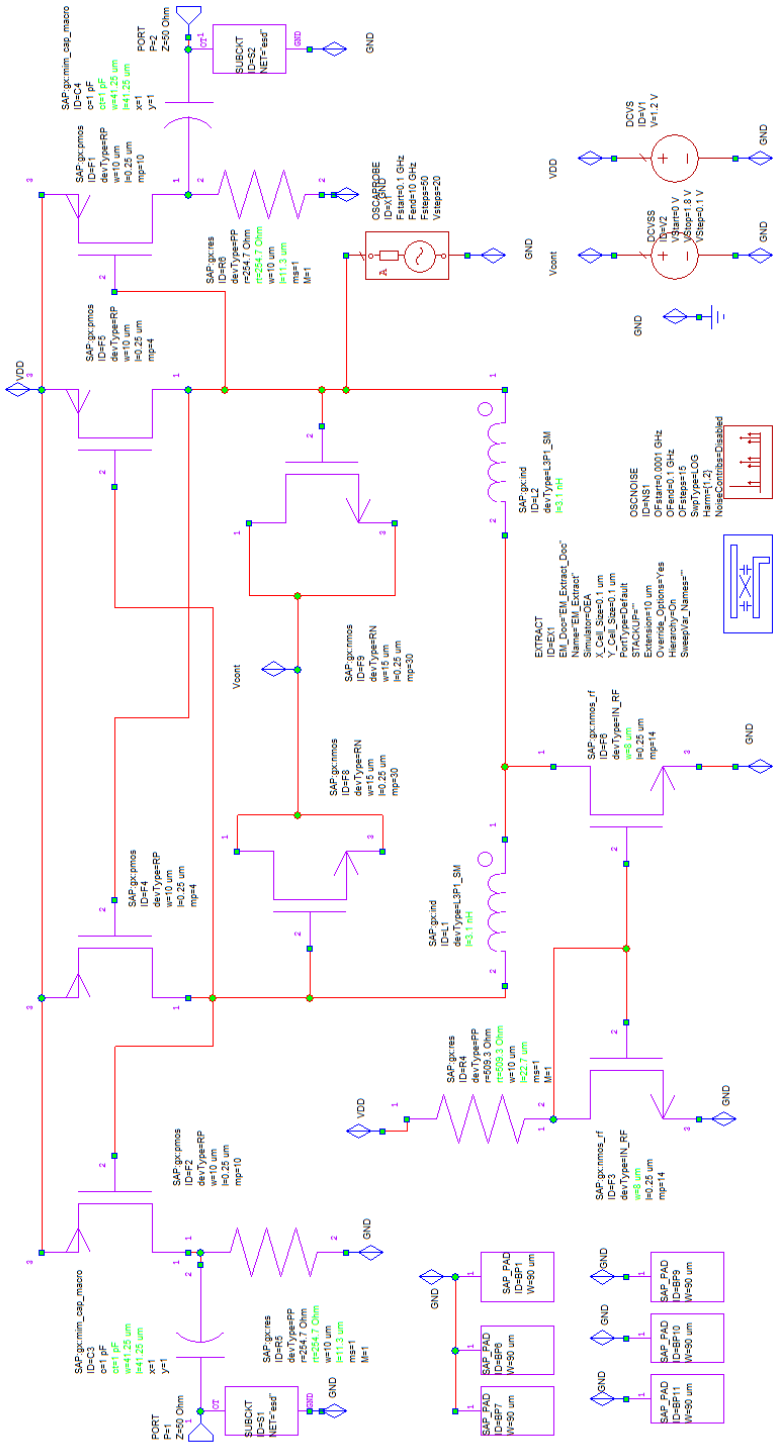

Figure B.5: VCO Circuit Schematic

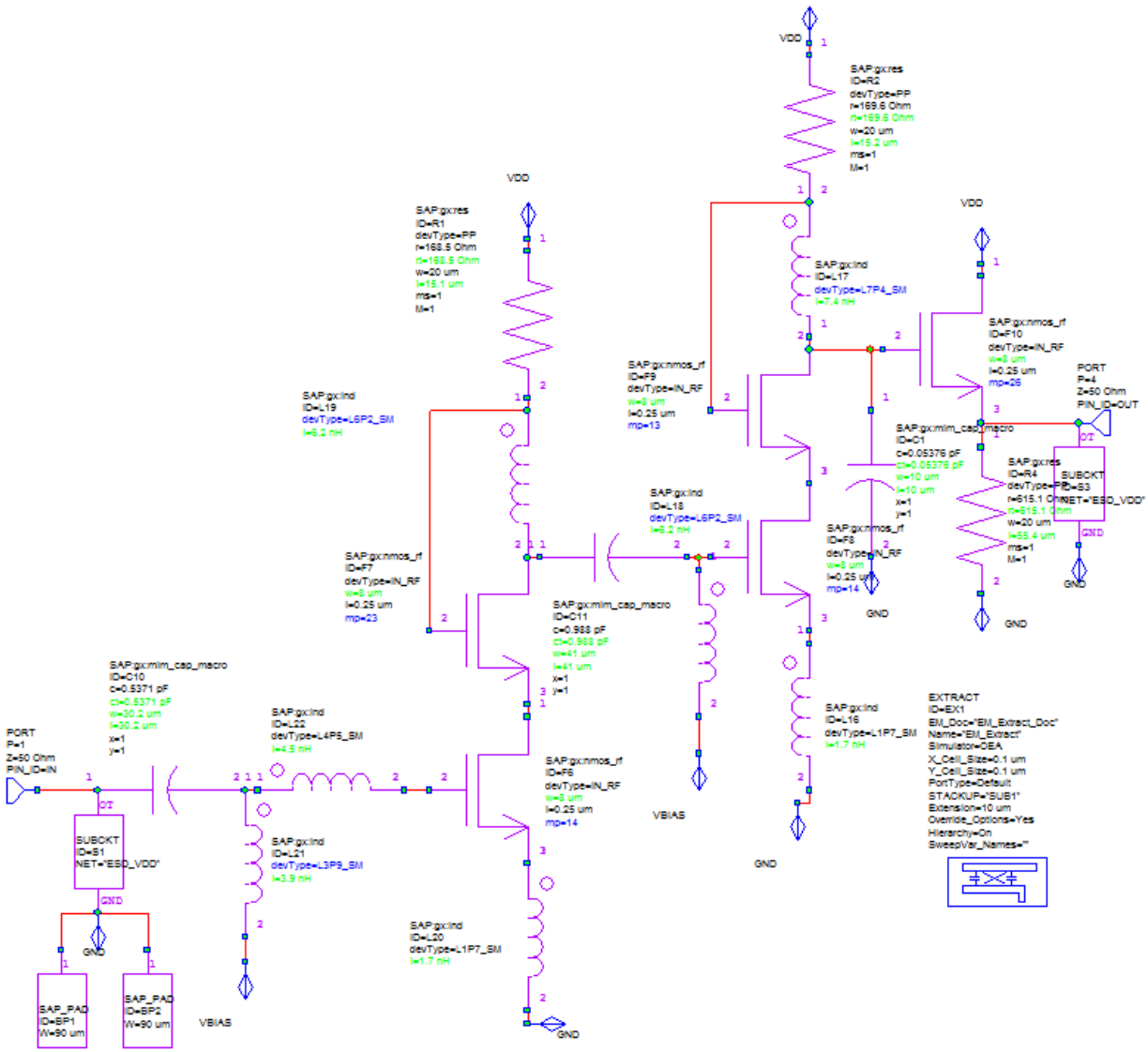

Figure B.6: LNA Circuit Schematic

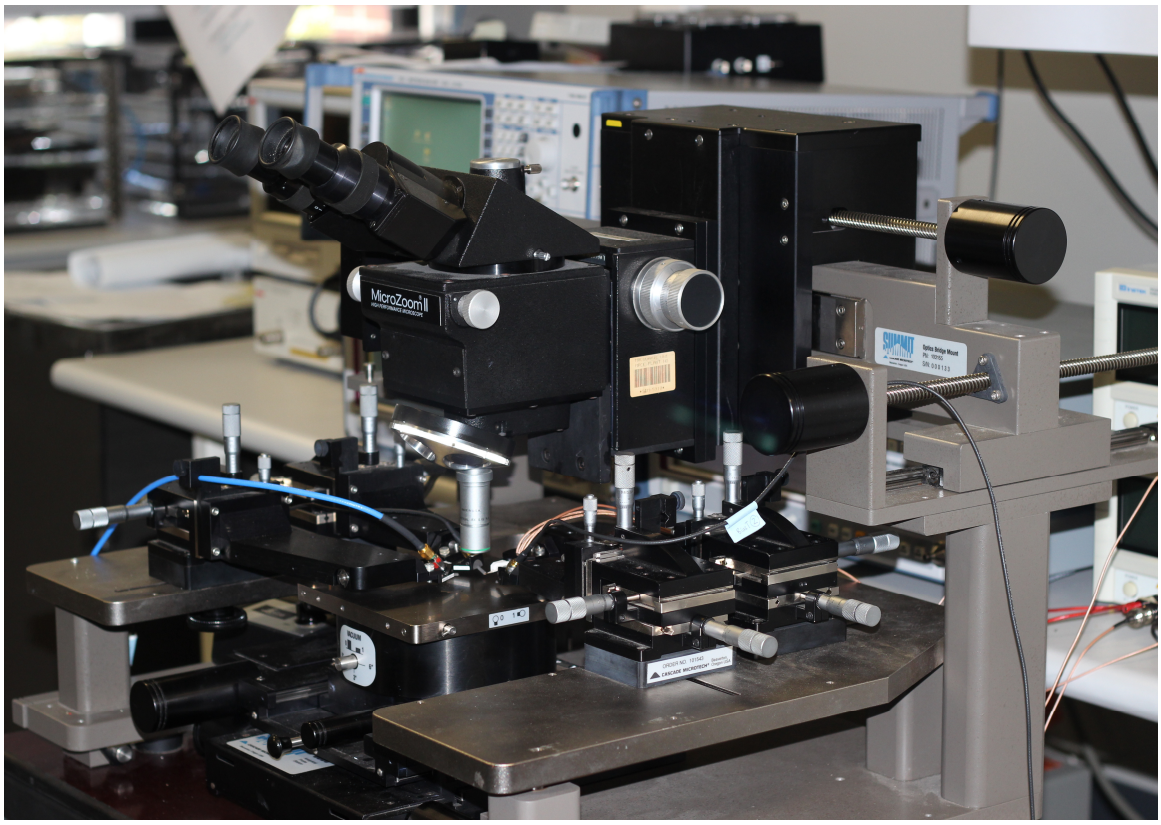

Figure B.7: Probe Station and Equipment

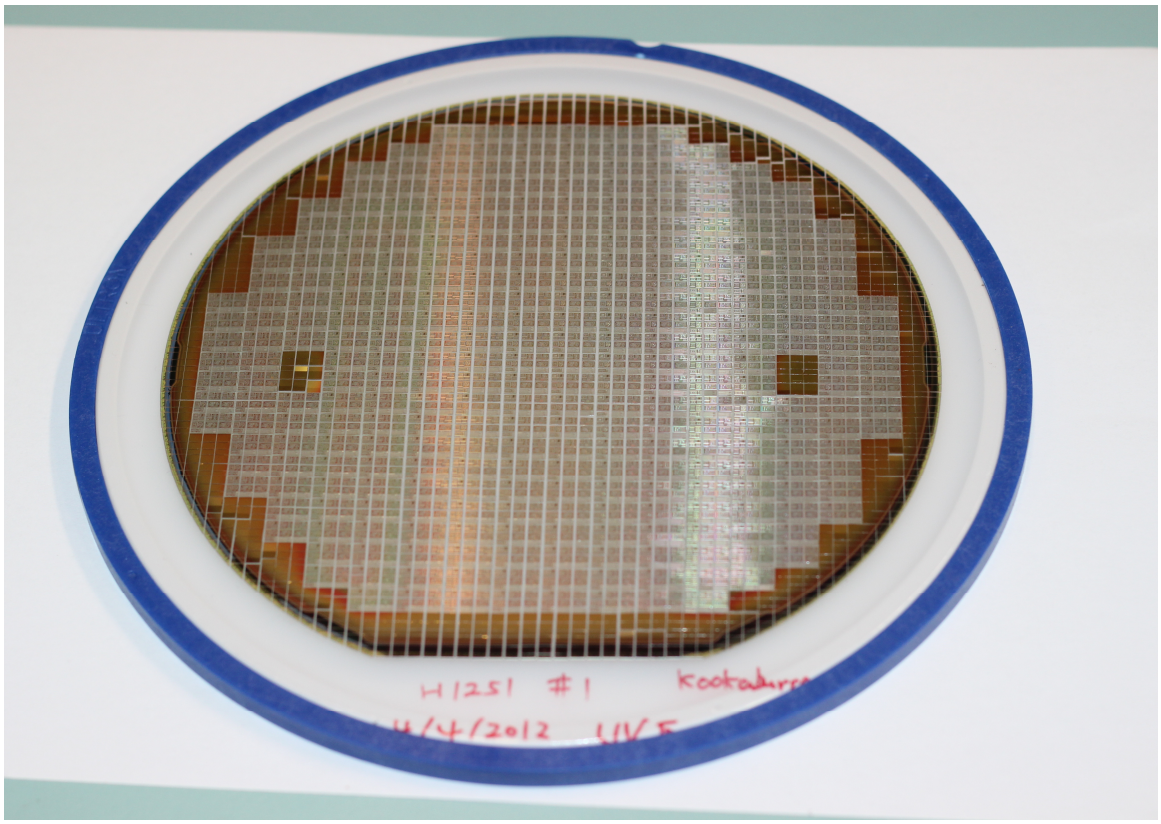

Figure B.8: Wafer Micrograph

Appendix C

Abbreviations

ADC	Analogue-to-Digital Converter
BER	Bit Error Rate
BiCMOS	Bi-polar Complementary Metal Oxide Semiconductor
BPSK	Binary Phase-Shift Keying
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analogue Converter
dB	Decibels
dBm	Decibels referrd to 1 milliwatt
DBPSK	Differential Binary Phase-Shift Keying
DPSK	Differential Phase-Shift Keying
DS	Direct Sequence
DS-VCO	Double Switched Voltage Controlled Oscillator
DUT	Device Under Test
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIRP	Effective Isotropic Radiated Power
ESD	Electro-Static Discharge

FFT	Fast Fourier Transform
FCC	Federal Communication Commission
FoM	Figure of Merit
FTR	Frequency Tuning Range
GaAs	Gallium Arsenide
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GPS	Geographical Positioning System
ICNIRP	International Commission of Non-ionizing Radiation Protection Safety Level
ICO	Current-Controlled Oscillator
IEEE	Institute of Electrical and Electronics Engineering
IF	Intermediate Frequency
IIP3	Third-Order Intercept Point
IMD	Intermodulation Distortion
IMN	Input Matching Network
IM3	Third-Order Intermodulation
ISF	Impulse Sensitivity Function
IR	Impulse Response
LC	Inductor Capacitor
LNA	Low Noise Amplifier
LO	Local Oscillator
LOS	Line Of Sight
MAC	Medium Access Control
MOS	Metal Oxide Semiconductor
mA	Milli-Ampere
mV	Milli-Volts

mW	MilliWatt
MWO	Microwave Office
NMF	Noise Modulating Function
NMOS	N-type Metal Oxide Semiconductor
OFDM	Orthogonal Frequency Division Multiplex
OMN	Output Matching Network
OOK	On-Off Keying
OQPSK	Quadrature Phase Shift Keying
PAM	Pulse Amplitude Modulation
PDK	Process Design Kit
PHY	Physical Layer
PMOS	P-type Metal Oxide Semiconductor
PN	Phase Noise
PPM	Pulse Position Modulation
PSD	Power Spectral Density
Pssb	Power Single Side Band
RBW	Resolution Bandwidth
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
rms	Root Mean Square
Rx	Receiver
SAR	Specific Absorption Rate
SiGe	Silicon Germanium
SNR	Signal-to-Noise Ratio
SOI	Silicon on Insulator
SOLT	Short, Open, Load, Through

SOS	Silicon on Sapphire
SRD	Step Recovery Diodes
SS-VCO	Single Switched Voltage Controlled Oscilator
TG	Task Group
TR	Transmitted Reference
Tx	Transceiver
UWB	Ultra Wideband
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VNA	Vector Network Analyser
WBAN	Wireless Body Area Network

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