Nonlinear Modelling of GaAs and GaN High Electron Mobility Transistors

By

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Statement of Candidate

I certify that the work in this thesis entitled "**Nonlinear Modelling of GaAs and GaN High Electron Mobility Transistors**" has not previously been submitted for a degree, nor has it been submitted as part of requirements for a degree to any other university or institution other than Macquarie University.

Except where acknowledged in the customary manner, the material presented in this thesis is, to the best of my knowledge, original and written by me.

In addition, I certify that all information sources and literature used are indicated in the thesis.

Jabra Tarazi
November 2020

Synopsis

This dissertation reports the work carried out by the author in a collaborative research projects between the author employers and Macquarie University. Professor Anthony Parker and Professor Michael Heimlich are the academic supervisors from Macquarie University. Dr. Simon Mahon and Mr. Anthony Fattorini are the industrial managers from Macom and Altum RF. This dissertation contains eight chapters.

This dissertation presents a new approach to scalable, large-signal modelling of GaAs and GaN microwave HEMT devices. The model can be used to accurately synthesise arbitrary device geometries and is consistent with the small-signal model.

In Chapter 3, a formulation of an intrinsic small-signal model that is consistent with the associated large-signal model is presented. The extracted small-signal parameters of the equivalent model linearly scaled with device width and are independent of frequency in the non-dispersive operating regions. Memory effects, i.e. thermal and trap states, are embedded in the steady-state small-signal intrinsic parameters, and for the large-signal model to scale accurately, these effects need to be separated from the extracted small-signal intrinsic data.

In Chapter 4, a lumped-element thermal model is formulated that can accurately model the local temperature rise, i.e. at the individual gate finger, and that scales correctly with number of fingers. The lumped-element thermal model is fitted to SPICE thermal model data, whose results are verified using Gate Resistance Thermometry (GRT) measurements. A newly-developed trap-state characterisation technique that is used to fit an adequate trap circuit model over a wide bias range is presented in

Chapter 5.

The thermal and trap circuit models form part of the complete large-signal model which is fitted to the extracted multi-bias small-signal intrinsic parameters in Chapter 6. In Chapter 7, a case study power amplifier design is presented using GaN HEMT technology that is based on the complete large-signal modelling techniques and procedures developed in this dissertation.

Chapter 1 presents today's device modelling challenges for MMIC designs, discusses the aim and the scope of the work and outlines the thesis structure.

Chapter 2 presents a background and literature review of GaAs and GaN FET devices. Basic GaAs and GaN HEMT device physics is discussed. Nonlinear dynamic effects are introduced, and the difference between small-signal and large-signal HEMT device modelling is outlined. Approaches to nonlinear modelling of HEMT devices are presented, including physics-based models, measurement-based models and more accurate nonlinear models. The information in this chapter is the work of other researchers.

In **Chapter 3** a formulation of an intrinsic small-signal model that is consistent with the associated large-signal model is presented. Initially the intrinsic active region in HEMT devices is introduced, and a fully reactive intrinsic FET equivalent circuit model is presented. A description of the small-signal S-parameter measurements required for the extraction process is provided. Different electromagnetic simulators are introduced as possible tools to analyse the extrinsic access metalisation of HEMT devices. An algorithm for the extraction of the intrinsic small-signal parameters is provided and applied to commercial GaAs and GaN technologies. Results indicate that the intrinsic linear model parameters are invariant with frequency and scale linearly with the gate-finger width of the device.

In Chapter 3 the intrinsic small-signal model formulation, extraction technique and verification by linear scalability and frequency-independence, were developed by Jabra Tarazi, building on suggestions from Professor Anthony Parker. All measurement and simulations were performed by Jabra Tarazi. The extraction work done on GaN devices

is recent and was performed by Jabra Tarazi, but has not been published yet. A large portion of this work is published as a conference paper:

- J. Tarazi, S. J. Mahon, A. P. Fattorini, M. C. Heimlich, and A. E. Parker, "A scalable linear model for FETs," in *2011 IEEE MTT-S International Microwave Symposium*, June 2011, pp. 1–4.

The role of all other authors in this paper was supervisory.

In **Chapter 4** a thermal FEM SPICE model is developed to model the local temperature rise in multifinger devices taking into account self-heating, mutual heating and end effects. A lumped-element thermal model is formulated that can accurately model the local temperature rise, i.e. at the individual gate finger, and scales correctly with number of fingers. The lumped-element thermal model is fitted to SPICE thermal model data, whose results are verified using GRT measurements.

Jabra Tarazi implemented the FEM thermal model for a multifinger device in SPICE using an AWK script which is coded by him. All simulations in Chapter 4 were performed by Jabra Tarazi. The GRT measurements used to verify the SPICE thermal model were supplied by the semiconductor foundry. A significant part of this work have been published in the following conference paper:

- J. Tarazi, A. E. Parker, B. Schwitter, and S. J. Mahon, "Thermal modelling of multifinger GaAs/GaN FETs using SPICE," in *2014 1st Australian Microwave Symposium (AMS)*, June 2014, pp. 7–8.

The role of all other authors in this paper was supervisory.

The formulation and the fitting of the scalable lumped-element thermal model is a work of Jabra Tarazi which has not been published yet.

In **Chapter 5** a newly-developed trap-state characterisation technique is presented. The trap state probe is introduced and implemented to observe the full gate-lag transient. The trap state extraction procedure is presented, and the trap rate is extracted. An extracted large-signal HEMT device, that includes a fitted trap circuit model,

is then used to simulate and verify the measured gate-lag transients. The model also demonstrates the capability to predict the low-frequency dispersion of the Y-parameters.

The trap model extraction technique is developed by Jabra Tarazi building on suggestions from Dr. James Rathmell and Professor Anthony Parker. All measurements and characterisation work in Chapter 5 is performed by Jabra Tarazi. The formulation of the instantaneous drain current is the work of Jabra Tarazi. The extraction of the trap state, fitting of the trap model to extracted trap state data, and fitting of the large-signal model is the work of Jabra Tarazi. This work have been published in the following conference paper:

- J. Tarazi, J. G. Rathmell, A. E. Parker, and S. J. Mahon, "Extraction of a trapping model over an extended bias range for GaN and GaAs HEMTs," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 2017, pp. 244–247.

The role of all other authors in this paper was supervisory.

In **Chapter 6** the complete model was fitted to the extracted multi-bias small-signal intrinsic parameters, which were shown to scale linearly with the device size. The "MQFET" large-signal model is introduced. The drain current and its derivatives, and the channel capacitances of the model are fitted to the multi-bias small-signal measured data. The model is shown to predict the small-signal and large-signal performance of arbitrary synthesised device geometries.

Jabra Tarazi developed the procedure for the large-signal model extraction with guidance from Professor Parker. Most measurements and characterising work in Chapter 6 is performed by Jabra Tarazi. Dr. Bryan Schwitter assisted with some of the measurements and the thermal data. The Verilog-A code of the MQFET model is a Macquarie University proprietary intellectual property that developed by Professor Parker. A part of this work has been published in the following conference paper:

- J. Tarazi, B. K. Schwitter, A. E. Parker, and S. J. Mahon, "AlGaN/GaN HEMT

nonlinear model fitting including a trap model," in *2015 IEEE MTT-S International Microwave Symposium*, May 2015, pp. 1–4.

The role of all other authors in this paper was supervisory.

In **Chapter 7** a 10 Watt, 10 to 40 GHz GaN power amplifier is designed based on the complete large-signal model developed in the previous chapters. An introduction to non-uniform distributed amplifiers is provided. The de-embedding of the measured load-pull target to the intrinsic terminals of the device is discussed. Scaling the intrinsic load-pull target is discussed and cross-checked with Cripps' load-line theory. The design benefited from the scalable model in optimising the transistor unit cell layout. The design also benefited from the built-in electrothermal simulation capability. A state of the art 4-to-1, 10 to 40 GHz impedance transformer is designed, fabricated and used in the design.

The distributed amplifier and the broadband transformer are designed by Jabra Tarazi. Dr. Schwitter performed device measurements and characterisation and he also provided an updated extracted model utilising the extraction techniques developed by Jabra Tarazi. The design work in this chapter has not been published yet.

Finally, **Chapter 8** concludes the dissertation by summarising the major outcomes. Areas for future research are suggested.

Abstract

Accurate modelling of transistors is considered to be an invaluable foundation for successful circuits. This dissertation presents a new approach to scalable, large-signal modelling of GaAs and GaN microwave HEMT devices, that can be used to accurately synthesise arbitrary device geometries. The modelling technique involves an extraction of frequency-independent small-signal intrinsic model parameters that linearly scale with zero offset in proportion to device width. These parameters are extracted from multi-bias steady-state small-signal measurements, i.e. thermal and trap states, are embedded in the extracted small-signal model parameters. Local temperature rise and trap-state of the measured device are separately characterised. A lumped-element thermal model is formulated that can accurately model the local temperature rise, i.e. at the individual gate finger, and scales correctly with number of fingers. A newly-developed trap-state characterisation technique that is used to fit an adequate trap circuit model over a wide bias range is presented. The thermal and trap circuit models form part of the complete large-signal model, in which the interaction of the thermal and trap models are critical to the model completeness, scalability and accuracy, as well as the consistency with the small-signal model.

The complete model is fitted to the extracted multi-bias small-signal intrinsic parameters. The model is shown to accurately predict the small-signal and large-signal performance of arbitrary synthesised device geometries. The model is then used to design a GaN PA which benefited from the scalability and built-in electrothermal simulation capability of the model to achieve best electrical and thermal performance.

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Many thanks go to Dr. James Rathmell, who provided a detailed edit of this thesis

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I must not forget to thank Peter Vun who I am grateful to have worked with at Macquarie University during the period of 2007 to 2009. Peter introduced me to the transistor modelling world and provided invaluable support in the early stages of my career.

To mum and dad, thank you for your ongoing love and support. You have always encouraged me to pursue my goals and for that I am forever grateful.

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1

Introduction

Recent trends in wireless technology require microwave monolithic integrated circuits (MMIC) to deliver unprecedented data rates with increasing levels of integration [3] [4]. This means active components of the circuits are running at higher power densities due to the use of higher-order modulation schemes, and are also placed in close proximity to each other which leads to increased levels of electromagnetic coupling and mutual heating.

Due to the tough design requirements, MMIC design engineers are faced with two major challenges in designing these circuits; Firstly, MMIC designers need to accurately capture the electromagnetic coupling and feedback loops between different parts of the integrated circuits. Secondly, to accurately predict the RF performance of the circuit while ensuring the operating temperature of a device is known in order to successfully predict the onset of potential failure mechanism and whether the predicted temperature

gives the required device lifetime needed for operation.

Considering a simple millimeter-wave front-end module design, three main components are integrated to form this circuit; a low noise amplifier (LNA), a power amplifier (PA) and a switch. Different device sizes and layouts are required in the different components for optimum performance, and hence, several models are needed by circuit design engineers in order to design and predict the performance of each of those components. Moreover, different operating bias regions for an active device are required in each component which results in the need to extract/fit several models for the same process targeting different operating regions and conditions. In addition to the electrical modelling capability requirements, MMIC design engineers are increasingly required to consider the impact of heat on their circuits due smaller chip size, high power levels and high data rates requirements.

1.1 HEMT Modelling Challenges

Accurate high-electron-mobility transistor (HEMT) device modelling is an invaluable basis for successful circuit design. It enables design engineers to deliver the required performance of their circuits in less time and less effort. Current standard millimeter-wave circuit design workflow requires design engineers to continuously switch between different small-signal and large-signal device models when simulating different parts of an integrated circuit or when exploring different dc operating points. It is often the case that the small-signal characteristic of the large-signal model used to establish bias points is different to that of the small-signal model. Also due to the dispersive nature of the traditional model formulation, the model parameters do not scale linearly with device size.

Models provided by the foundries usually work well at some typical bias condition only and lack accuracy at other biases, they also have convergence issues, limited control device and layout scalability and frequency extrapolation. Small-signal models in process design kits (PDKs) are most likely nonequivalent to their large-signal counterparts under small-signal drive conditions around a dc operating point.

Scaling becomes an issue when scaling to a very large device, and such a limitation arises from inadequate thermal modelling. Although, many sophisticated thermal modelling tools are available [2] for MMIC designers, the integration of such thermal tools in the circuit design flow in order to perform electrothermal analysis is time consuming, complicated to use and not price competitive.

1.2 Motivation

Modern GaN and GaAs MMIC designers require device models that can be highly integrated or embedded into the circuit designs to accurately capture the electromagnetic coupling between these devices and the different components in a circuit. The models also need to scale correctly with device sizes, work accurately over a wide range of biases, i.e. different regions of operation, and extrapolate in frequency. Electrothermal modelling is also required to complement the scaling of the large-signal model and accurately predict the RF performance of the circuit. It is also necessary to ensure the operating temperature of a circuit satisfies the lifetime requirement. In addition, performing electrothermal simulations are essential in predicting the transient behaviour in application such as high power pulsed-radar. Nonlinear memory effects, such as time-dependent trapping and thermal self-heating need to be captured by the large-signal model in order to provide ideal scalable and non-dispersive model parameters.

The ability to accurately model and scale the temperature rise in a device is desired to complement the scaling of the large-signal model. This can be done by performing electrothermal analysis at the device level or design level, in which the integration of the electrical simulation and the thermal analysis needs to be simple but adequate. Improving the device model accuracy, scalability and integration in MMIC designs while dramatically simplifying the model extraction process for a wide range of device sizes and geometries was the driver behind this project.

1.2.1 Aims

The aim of this dissertation is to develop a new approach to scalable, large-signal modelling of GaAs and GaN microwave HEMT devices. The model needs to accurately synthesise arbitrary device geometries and needs to be consistent with the small-signal model. For the large-signal model to scale accurately, memory effects, i.e. thermal and trap states need to be separated from the extracted small-signal intrinsic data.

To achieve the aim of this dissertation, firstly, the extracted small-signal parameters of the equivalent model need to scale linearly with device width and they should be independent of frequency in the non-dispersive operating regions. Secondly, a lumped-element thermal model is required that can accurately model the local temperature rise, i.e. at the individual gate finger, and scales correctly with number of fingers. This enables a built-in electrothermal simulation capability ensuring accurate device scaling and allowing local temperature rise to be monitored under small-signal as well as large-signal excitation and under a range of bias, temperature and mounting conditions. Finally, an adequate trap circuit model that works over a wide bias range is needed.

The thermal and trap circuit models form part of the complete large-signal model, in which the interaction of the thermal and trap dynamics are critical to the model completeness, scalability and accuracy, as well as the consistency with the small-signal model.

The aims of the project are summarised in the following points:

- Identify the extrinsic parameters the HEMT device and separate them from the intrinsic device to ensure the intrinsic parameters scale linearly with device width.
- Formulate a lumped-element thermal model that can accurately model the temperature of an individual gate finger, and scales correctly with number of fingers.
- Develop a trap-state characterisation technique that works over an extended range of biases.
- Develop a scalable, large-signal modelling approach for GaAs and GaN microwave HEMT devices to accurately synthesise arbitrary device geometries.

1.2.2 Scope

This dissertation concerns characterisation and modelling of microwave and millimetre-wave GaAs and GaN MMIC HEMT devices. It is assumed that the channel is quasi-static, that is, the gate width is relatively short compared to the wavelength and the gate is not divided into segments. The scope of this thesis is bound by the intrinsic scaling, which refers to the active region of the HEMT device. The geometry scaling is taken care of by EM tools, i.e., the metalisation is left to be analysed by EM tools, accepting the results and leaving issues of access network to the EM tool. The issue of how to deal with access resistances that are in part of a diode-nature was not aim of this thesis.

The development of thermal simulation software was not an aim of this thesis. However, the developed finite-element model (FEM) is used to model the temperature rise at the gate junction (gate metal and device epilayers). Thermal models developed in this thesis are based on 2D simulations, and the aim was not to do 3D heat-flow study, but rather to provide adequate details for the circuit model. 3D thermal modelling is only implemented to verify the assumptions in the 2D thermal modelling. The dissertation is not overly concerned with the detailed physics of the trapping mechanism and channel heat source. Rather, their effects are characterised and adequately modelled. This dissertation is not concerned with thermal transient modelling, rather, the results of the transient simulations obtained from the SPICE FEM model are used to fit the lumped-element local thermal model.

Developing a code for large-signal model equations was not an aim of this thesis. However, an available large-signal model (MQFET) is used to fit the extracted data developed in the thesis. Microstrip HEMT devices are used in the modelling and verifications and coplanar devices were not considered, however, the modelling technique reported in this thesis can be used to generate models for coplanar devices.

Verification of models developed in this thesis is done at typical power amplifier biases and all verification was performed at ambient temperature. Gate current modelling or impact ionisation effects were not aims in this dissertation because a major portion of this project is applied to a commercial GaN technology that does not exhibit

significant impact ionisation.

The model developed in this dissertation concerns the mainstream amplifier design application and verification is needed for exotic classes. Switch-mode modelling was also outside the scope of this work.

The design of the power amplifier was not the aim of this thesis, however, the design is used as a vehicle to assess the developed model and show its usefulness in such a design. The stability in power amplifiers is also beyond the scope of this thesis.

2

Background

A summary of the relevant portions of the literature is presented as a technical background for the work presented in this dissertation. It starts with a brief overview of GaAs and GaN HEMT technologies. The intrinsic device model topology is discussed and its effect on the overall model characteristic is presented. Various large-signal modelling methods are introduced as possible approaches to large-signal modelling. An overview of thermal and trap states is presented.

2.1 High Electron Mobility Transistor

GaAs HEMTs have superior electron transport characteristic ensuring high speed and high power applications. GaAs HEMT devices have been used commercially since the late 1980's, and they have been replacing traditional field-effect transistors (FETs) due

to their ability to operate at higher frequencies, improved power densities, low noise and high gain. GaN HEMT is another excellent technology that has dramatically evolved in recent years, and it is gaining a lot of traction in microwave engineering applications. Compared to GaAs, GaN features low operating resistance and high breakdown voltage, which makes it an ideal candidate in high power high efficiency applications.

This section provides an overview of GaAs and GaN HEMTs. Only depletion model devices are studied in this thesis where increasingly negative gate bias is applied to reduce the concentration of the electrons in the channel. Positive bias is applied to the drain terminal to accelerate electrons in the channel from source to drain.

2.1.1 GaAs pHEMT

The first GaAs HEMT device was developed in 1979 by Takashi Mimura of Japan as lattice-matched AlGaAs/GaAs configuration [5]. Fig. 2.1 illustrates a typical GaAs-based HEMT structure. An abrupt hetero-structure is created between a wide bandgap material, AlGaAs, and lower bandgap material, undoped GaAs. The wide bandgap material is doped, which results in a very high concentration of charge that is formed at the interface of the AlGaAs/GaAs hetero-junction and confined to two dimensions, which is therefore known as 2-DEG.

Development of the GaAs pseudomorphic HEMT (pHEMT) saw improvements to the bandgap discontinuity problem by introducing a lower bandgap channel layer material (InGaAs). The InGaAs layer is lattice mismatched to the GaAs buffer layer; however, since it is very thin (0.2 nm) the strain is acceptable.

More advanced HEMT structures that are commercially available contain an additional thin layer of undoped AlGaAs that is used as spacer layer in order to reduce the coulombic scattering and improve isolation of the charge carrying region. Charge density can be increased in the 2-DEG by using double hetero-junction structures [6].

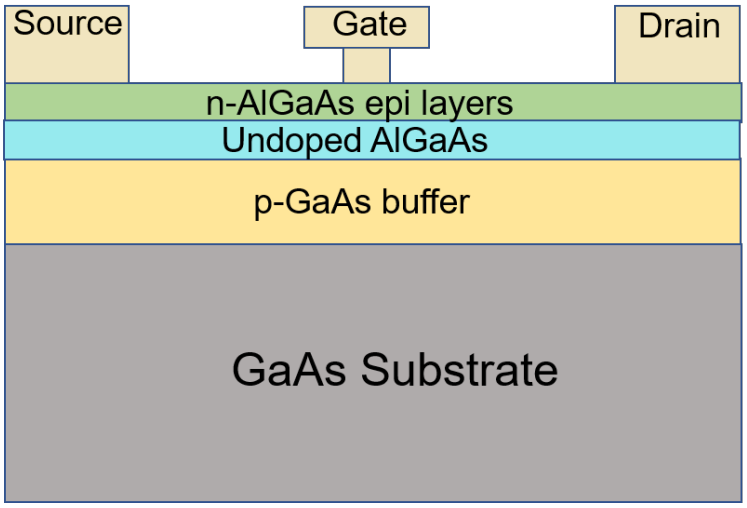


Figure 2.1: A basic example of GaAs HEMT structure.

2.1.2 AlGaN/GaN HEMT

GaN-based HEMTs have similar structures to conventional GaAs-based HEMTs as shown in Fig. 2.2, however, no intentional doping is required in AlGaN/GaN HEMTs. The electrons forming the 2-DEG in a GaN-based HEMT arise from the epitaxial growth process as explained by Trew *et al* [7] [8]. The AlGaN semiconductor exhibits both spontaneous and piezoelectric polarisation. Spontaneous polarisation is the polarisation that occurs in the material when the lattice is at equilibrium, while piezoelectric polarisation is strain induced. Due to the intense electric field formed due to the polarisation, weakly bonded surface electrons get ionised, which then drift toward the AlGaN/GaN hetero-junction, where they become confined in the 2-DEG. The equilibrium in the AlGaN/GaN system will be reached when the electric field is reduced to the extent that no more electrons are transferred.

2.2 Intrinsic Model Topology

The topology of a core intrinsic model is crucial in getting the large-signal response correct [9]. Having a non-physical model representation of the device, where adjustments are required to compensate for the simplicity in the model topology, limits the

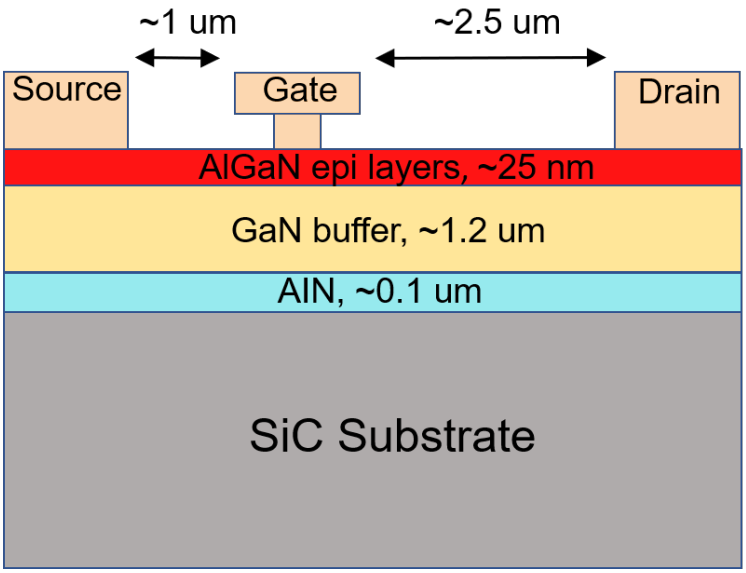


FIGURE 2.2: A basic example of GaN HEMT structure.

model accuracy and prevents the scalability of device in geometry and frequency. The addition of a frequency-dispersive element, such as a time delay, will introduce a non-conservative and a nonphysical reactive component [10]. This results in dispersive small-signal capacitance and conductance terms.

This type of dispersion may be avoided by having a correct representation of the intrinsic equivalent model parameters which does not include nonphysical dispersive elements [10].

Rate-dependent physical phenomena in HEMT devices such as self-heating and trapping are referred to as memory effects or dynamic effects. These effects cause dispersion in the small-signal model parameters and are usually slowly varying in relation to high frequency stimuli, and therefore their response is generally only influenced by the quiescent condition. Fig. 2.3 presents a simple block diagram illustrating how the heating and trapping effects can be included in the nonlinear model where the response of the nonlinear model becomes a function of four state variables; gate-source potential, v_{gs}, drain-source potential, v_{ds}, temperature-state, T and trap-state, v_t.

The frequency dispersion of the reactive currents depend on heating and trapping time which defines the state of the device. This state is defined by the state variables,

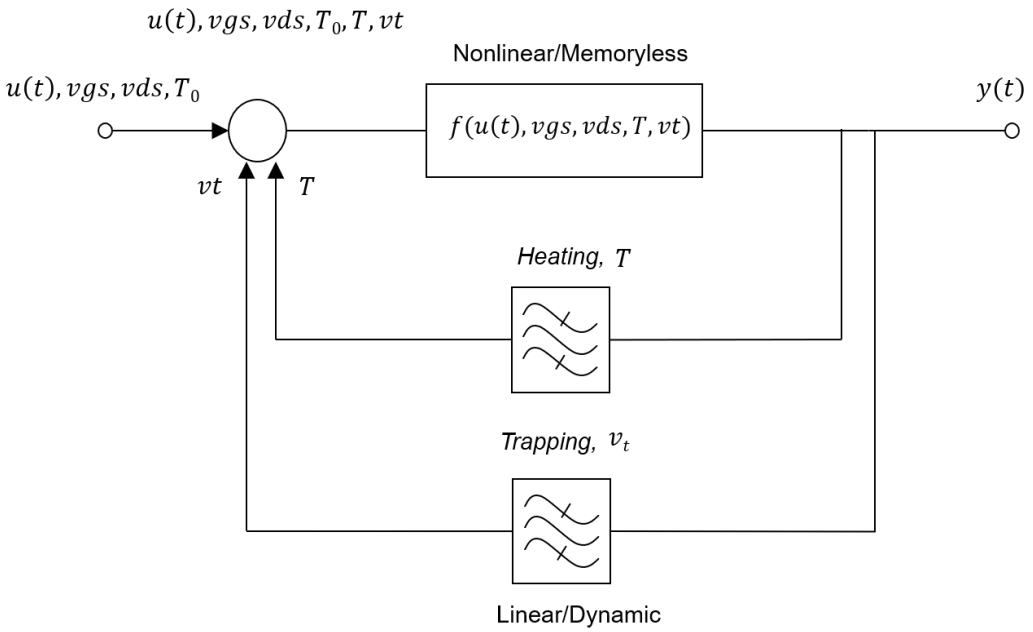


Figure 2.3: A simple block diagram model of a nonlinear device illustrating how the memory effects can be included.

which are the potential values of temperature and trap.

Slow-state variables do not respond to rapid changes so the device remains in a constant state while being driven by a large-signal at a microwave frequency. Thus, small-signal steady-state characteristics are problematic in predicting the large-signal response when used alone. Instead, constant states are required to predict large-signal data.

In theory, performing a quick step is needed to measure the characteristics without disturbing the state of the device. These characteristics are termed *isodynamic*, which give the drain-current the characteristics for constant temperature and trapping states. A sophisticated arbitrary pulse pattern and arbitrary control of initial bias and pulse timing is used in Chapter 5 to measure the trapping states over an extended bias range.

2.3 Large-signal Models Review

Good large-signal models are essential for the design of nonlinear microwave circuits. Due to increasing commercial demand for high performance circuits and the emerging of new technologies such as GaN HEMTs, device models need to keep up with the increasingly complicated requirements on the accuracy and generality. Available nonlinear device modelling techniques are presented in this section.

2.3.1 Measurement-based Models

Measurement-based models eliminate the use of equation and expression development and the parameter extraction from device modelling flow. Table-based models and Artificial Neural Network (ANN) models are discussed here.

Table-based Models

Table-based models [11] take measured, mathematically transformed data and store the resulting discrete values of the current-voltage (I-V) and charge-voltage (Q-V) relations in a multidimensional table. During simulations, simulator finds the solution through interpolation between points in the tables. Thus, the equation development and the parameters extraction process for the device modelling flow is completely eliminated. The calculation of Q-V functions from bias-dependent small-signal measured data is considered to be independent of process technology and generic for many device types.

One major limitation of table-based models is that the I-V and Q-V relations are defined by the interpolation algorithms used by the simulator. These algorithms need to smoothly interpolate between the measured discrete data points in order to define the I-V and Q-V relationships. More complex algorithms are required to be implemented to guarantee smooth and reliable results, where the use of mathematical expression describing the device is eliminated at the expense of additional complexity [12].

Inaccuracy in predicting high-order distortion products under small-signal drive, is another limitation to some of the table-based models, this is attributed to the input signal magnitude being significantly smaller than the distance between two neighboring

discrete measured data points. The results of limited accuracy of the model is mainly determined by the interpolation algorithm used by the model during simulation rather than the acquired measured data [13].

Table-based models may be combined with empirical models to form effective hybrid models in cases where additional accuracies are required to fit the measured data. An example of this hybrid approach is found [14]. For good large-signal simulation results, it is essential to cover a very wide range of device operating bias conditions.

Artificial Neural Network Models

The main limitation found in table-based models is the use of spline functions as they exhibit poor extrapolation properties and possibility of oscillation when interpolating between data points. These limitations can be eliminated by replacing the table-based interpolation algorithms by ANNs [15] [16].

ANNs are mathematical functions that are defined in terms of simple universal nonlinear processing elements (neurons) that are joint together. ANN method is a powerful mathematical functional approximation technique that provides smooth functions and nonvanishing derivatives of infinite order while guaranteeing the capability to fit any nonlinear function in any number of independent variables. This is considered a key enabler for accurately predicting high-order distortion in nonlinear devices at low signal levels. ANN models can be used and trained on scattered intrinsic voltage data, which eliminates the need of re-gridding or referencing during simulation and I-V and Q-V relations are trained directly using the intrinsic voltage grid.

Compared to table-based models, ANN-based nonlinear transistor models provide more uniformly accurate, smoother results. In addition, ANN models can accommodate discrete symmetry constraints which make them ideal candidates for designing resistive-FET mixers, where the instantaneous drain-source RF voltage crosses zero during operation.

ANN measurement-based models do not converge as rapidly as polynomials and their extrapolation properties are also poor. However, computational geometrical algorithms, which are also refereed to as *guided extrapolation* methods, are used to ensure

robustness of DC convergence, transient and large-signal harmonic balance analysis outside the region where data is acquired [17] [18] [19].

2.3.2 Behavioural Models

Behavioral models are simplified models of the essential nonlinear behavior of the complex sub-circuits, which means that these models will run more quickly, and use less memory than if an entire complex subsystem was simulated at the transistor level. Behavioral models are a black-box approach, as opposed to the traditional modelling approach, where detailed knowledge of the device physics or circuit configuration and operation is used to minimise the number of equations that describe the essential properties of the circuit or device. The dynamical behavior of the circuit that is observed at its accessible terminals is described in this approach. Hence, the model of a complex circuit or system can be derived, without prior knowledge of its internal circuitry or topology.

Cardiff and Keysight X-parameter models are considered the two main implementations of behavioural models used in the industry.

The Cardiff model [20] was first developed by Qi *et al* [21]. The formulation of the model is based on the polyharmonic distortion (PHD) modelling approach [22]. The extraction of the Cardiff model utilises the nonlinear current and waveform lookup data used in the direct waveform lookup (DWLU) approach in order to maintain the advantages of the measurement-based approach. The cardiff model is capable of capturing the responses due to the fundamental and harmonic load-pull at both input and output.

X-parameters can be measured using a Nonlinear Vector Network Analyser (NVNA), and these measurements are used to generate behavioural models of a device or a circuit. The models are considered rigorous supersets of small-signal and load-pull data that are applicable at to both linear and nonlinear conditions and applications [23]. X-parameter models include harmonic and intermodulation generation by the nonlinear device-under-test (DUT) in response to large-signal stimuli [24].

The X-parameters enable predictive nonlinear simulation under small to moderate

mismatch, allowing prediction of component behaviour in complicated nonlinear circuits. They are specifically useful for modelling transistors for new device technology where a suitable compact model may not be available. X-parameter models are more convenient to share with customers, for example, when system-level simulations or circuit debugging are required, rather than sharing the device model where the intellectual property of the model needs to be protected.

X-parameter behavioural models simulate high-frequency devices very accurately, however, they do not support conventional transient analysis simulations. Bandwidth is limited by the measurement system and large file size for comprehensive models are some of the main limitation of the X-parameters models.

Cardiff model is shown to be scaled in terms of devices' geometry and frequency [25]. Similarly, X-parameter models can also scale with device geometry [26] [27] and frequency [28].

2.3.3 Compact Models

In general, compact large-signal models are defined by closed-form expressions with parameter values which are fully specified by physics [29] or inspired by physics where these model parameters are determined to provide the best fit to measured data [9] [30] [31] [32]. The most common approach is to extract the model parameter values from simple dc measured data, which provides information about current sources, and small-signal parameter measurement, which gives information about the nonlinear capacitances. A good parameter extraction procedure is required in order to get accurate and repeatable results.

Detailed compact models, or *empirical* models, can take many years of development and refinement in order to be adopted by design engineers and successfully implemented in their circuit design flow. The parameter extraction process can take several days and even weeks by expert modelling engineers. This process usually takes longer time than anticipated for many reasons including; poorly-chosen parameters values that cause poor convergence of the model, getting stuck in local minima or simply, the I-V and Q-V nonlinear functions are too simple to fit the measured data or they are not suitable

for a certain device technology.

The scope of this thesis is to develop a large-signal modelling approach for HEMTs, that can work in all simulation modes and any computer-aided design (CAD) tool. The model should include self-heating and trapping dynamic effects, consistent with small-signal model. It should scale both electrically and thermally with device size and extrapolate in frequency. It is preferable that noise sources are included in the model.

As shown in the previous sections, measurement-based models and behavioural models can be used to develop very accurate large-signal models, however, the accuracy of these models are bound to their measurement range and cannot be used beyond their characterisation range including, bias, temperature, frequency, input signal magnitude. The compact model that is formulated in [9] is used in Chapter 6 of this thesis to develop a complete large-signal intrinsic model that scales with device width and enable the synthesis of arbitrary device geometries.

The large-signal model must have a topology that correctly accounts for dispersion due to dynamic effects, and also the core nonlinearity of the model is mathematically conservative, where a network of nonlinear lumped-element is represented with non-dispersive conductance/transconductance and capacitance/transcapacitance. Such a model eliminates the dispersion artifacts generated by the model itself and enables the extraction of a model that represents the true intrinsic behaviour of the transistor device. Therefore, consistency with small-signal equivalent model parameters device is achieved, device scaling becomes possible and the extra effort that is required to extract large number of models for the same device technology can be eliminated [10] [9].

In principle, nonlinear large-signal characteristics can be derived by integrating the small-signal data. This can be done by taking two-port vector network measurements using a Vector Network Analyser (VNA) over broad range of frequencies, and repeated over wide dense range of bias points. The small-signal intrinsic parameters become a function of accessible terminal potentials which are needed to be viewed as surfaces above gate-drain potential plane. Line integrals over the surfaces of these parameters give the current and charge functions that are the basis for large-signal model [33].

2.3.4 MQFET

The MQFET nonlinear model that is formulated based on [9] is used to fit the data. The large-signal model formulation in [9] is a parallel I-V and Q-V state function formulation. MQFET is a Macquarie University proprietary that developed by Professor Anthony E. Parker. MQFET is a charge-based model and is written in Verilog-A. MQFET has six nodes; gate, drain, source, impact ionization, thermal and trap. External trap and thermal networks connect to the relevant nodes of the MQFET, which feedback into the bias-dependent behavior of the model. The gate, drain and source nodes take the intrinsic biasing condition of the FET. The circuit model of the thermal is developed and discussed in details in Chapter 4 of this thesis in which this thermal circuit model consist of a reduced lumped-element RC network that is obtained via detailed finite-element SPICE modelling. The charge trap network is presented in Chapter 5, in which the trap charge is modelled as a capacitor potential that is added to the gate potential via the MQFET's trap node. The impact ionization node has not been used in the model fitting and is not considered in the scope of this thesis.

Fig. 2.4 shows the MQFET subcircuit in a schematic. The gate, drain and source terminals of the MQFET model are connected to the corresponding access resistances, R_g, R_s and R_d which link the intrinsic model to device's access metalisation . The trap circuit model is connected to the trap node of the MQFET with the intrinsic voltages fed to the model in addition to the temperature of the device, in order to predict trap state accurately. The use of terminal pins enables a hierarchical implementation of the model.

The parameters of the MQFET model can be divided into four groups; gate-drain diode, drain current, charge model and impact ionisation parameters. The gate-drain diode parameters control the forward and reverse diode junction currents and the breakdown voltage. The drain current and the charge model parameters are responsible for modelling the nonlinear drain current and capacitance terms respectively, based on bias conditions, temperature and trap state variables. The last group of parameters is for responsible for modelling the impact ionisation, however these parameters are not

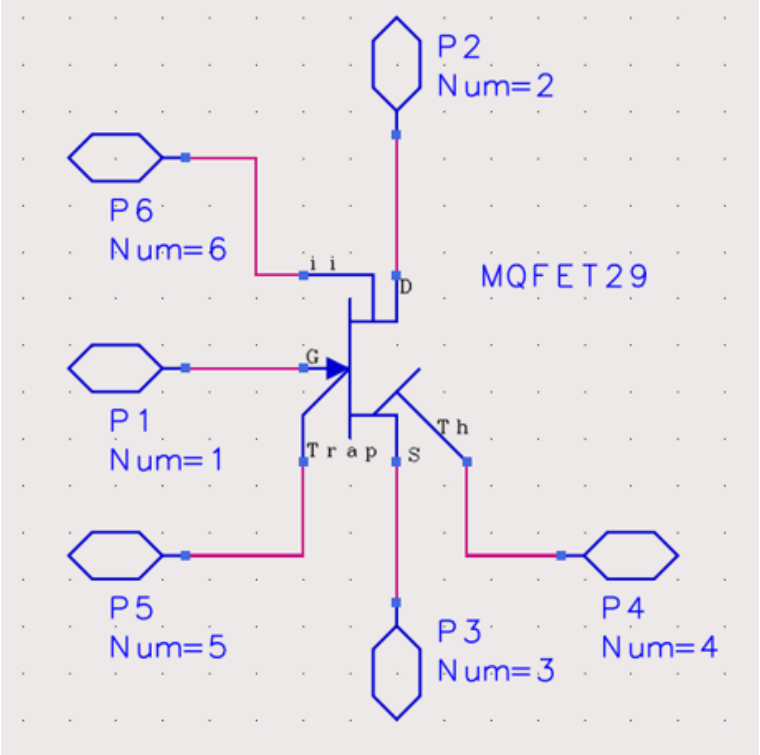


FIGURE 2.4: MQFET model symbol showing the accessible nodes including the dynamic feedback nodes; thermal, trap and impact ionisation. The model is used in Chapter 5 as part of a complete large-signal intrinsic model with Chapters 3, 4 and 5 preparing for this integration.

used or fitted in this thesis and the impact ionisation is set to zero in the model.

2.4 Thermal State

FET thermal modelling is one of the major topics of this dissertation and is the focus of Chapter 4. The thermal-state is an independent state variable that refers to the junction temperature of a device, and has time-dependent response which is relatively slow compared to a microwave input-signal response. The temperature has a significant impact on all aspects of transistor operation and must be accounted for when modelling transistors. For instance, increasing temperature reduces drain current, increases the rate of trapping and reduces the speed of impact ionisation response [34] [35] [36] [37].

Traditionally, the modelling of temperature is limited to scaling the drain current

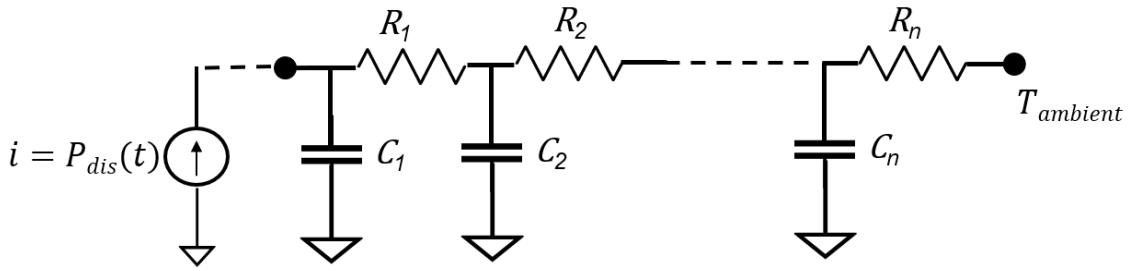


Figure 2.5: RC ladder network used in dynamic electrothermal transistor models.

by a thermal coefficient accounting for the power dissipation in the device. The presented thermal state of the device is not known, and hence, any interaction between the different state variables during the transition from the isodynamic current at the beginning of a transient to the final steady-state value is not captured in the transistor model. An accurate model needs to have a junction temperature terminal at which the thermal state of the transistor is presented.

A single-pole or *first-order* thermal equivalent circuit is incorporated in many dynamic electrothermal transistor models to estimate the thermal-state at the gate junction. However, in real transistor devices, the thermal response changes over several decades of time due to materials with different thermal properties used in the device stack-up. A RC ladder network (equivalent thermal network of capacitance and resistance) can be used to model a more realistic transient thermal response of a transistor device in order to capture the sub-first order response of the device [35]. Examples of electrothermal modelling methods can be found in [38] [39]. An example of RC ladder network used in dynamic electrothermal transistor models is shown in Fig. 2.5.

2.4.1 FETs Thermal Modelling Overview

Thermal modelling methods that are specifically suited to device thermal analysis are presented in this section. These methods can be divided into three categories; closed-form models, finite-element method and physical models.

Closed-form Models

Several closed-form models have been proposed for estimating the channel temperature of FETs. The 45-degree heat spreading model [40] which assumes that all heat flows in a 45-degree wedge from channel to backside is a compromise between the two extremes of columnar flow and pure spreading. This results in a very simple model that can be extended to multiple gate fingers [41]. The Cooke model [42] makes use of the analogy between heat flow and electric field, taking closed-form equations for the capacitance of parallel lines and applying them to the thermal problem of a multifinger FET. An improved closed-form model for multifinger devices based on ellipsoidal and elliptic cylinder isotherms was developed by Darwish *et al* [43].

Generally closed-form models do not account for temperature-dependent substrate thermal conductivity, however, this can be accounted for accurately using the Kirchoff transformation [44]. All of the closed-form models ignore details such as surface metallisation, passivation, substrate vias, and epi layers near the heat source.

Finite-element Models

As already noted, closed-form models are only useful for solving simple geometries or performing quick trade-off studies. Finite element and finite difference simulation offer the capability to solve more complex heat-flow problems which makes them very popular for analysing FET thermal behaviour. However, the accuracy of the solution depends on a detailed and accurate description of the physical structure and adequate mesh density in regions of high temperature gradient. Considering devices from an outsourced wafer fab, the epi details may be unknown to the modelling engineer. Even if the detailed epi structure is known, the sub-micron features of the heat source and surrounding epilayers present modelling difficulties when their dimensions are comparable to the phonon mean free path. At such small scales heat flow does not conform to Laplace equation and a full description requires Boltzmann transport equations which dramatically increases the computation effort required. Usually these effects are ignored and the heat source is approximated by a larger volume or Laplace equation is

applied for sub-micron features. In this way the simulated temperature is a proxy for device stress but may be physically inaccurate.

Finite-element model tools are particularly useful when they are combined with experimental data. Such a combination can be used to improve device temperature estimations, where the spatial resolution provided by the FEM tools are beyond practical limitations [45].

Performing transient simulation could be time-consuming and usually simplifications of the structure are needed in order to make it possible. Usually, it is impractical and inefficient to couple FEM tools with electrical simulation in order to perform electrothermal simulations.

Some CAD circuit design tools, like Keysight ADS [46] offer a built-in thermal tool including the option to perform electrothermal simulation on a design level. However, such an option can be expensive and needs to be supported by foundry PDKs. Performing electrotheraml simulations using FEM tools can be inefficient and may be restricted to steady-state due to long computational time needed. The accuracy of the FEM analysis is usually a trade-off between accuracy, i.e. mesh density and calculation time.

Physical Models

The channel heat-source distribution can be modelled more accurately using physical models. They take into consideration the Fourier heat equation to model thermal effects and also drift/difussion equations to model electronic transport. In [47], the correlation between the geometry of the channel heat-source and the channel electric field distribution was taken into account when performing thermal analysis. Also, 2D drift/difussion equations were used, along with Fermi-Dirac statistics, to simulate electronic transport in the channel.

A detailed information about the electrical characteristics of the device under analysis are required, such as dopant levels and carrier concentrations. The channel power dissipation profiles were then exported to a pure thermal 3D simulator.

More detail of a similar study was presented by Benbakhti *et al* [48] which concluded

that both bias and topology play significant roles in defining the heat-source geometry

Limitations of physical models arise when the analysed heat flow occurs on the scale of the phonon mean free path, and the behaviour diverges from that of the classic heat flow equation. This limitation is addressed by switching to a more appropriate model that treats the heat flow as a quantum-mechanical system. While this is an interesting area of research it is beyond the scope of this thesis. A detailed description of such models is presented in [49].

2.5 Trap State

Trapping characterisation is one of the major topics of this dissertation and more details are given in Chapter 5. Electron trapping is an inherent attribute within the channel and surface layers of HEMTs [50], [51], [52]. HEMTs are biased to control the flow of charge through their channels. Some of this charge may become 'trapped' in energy states presented by material imperfections and defect centres in the substrate region, at material interfaces or the surface of the device. The polarity, location and amount of traps depends on the semiconductor fabrication process. The trapped charge contributes a potential that influences the channel conduction. Changes to the terminal bias will control the trap state and also the rates of trapping [1]. Trap states can also be affected by wideband signals that have long time constants similar to their own [53].

Pulsed-I/V characteristics, shown in Fig. 2.6 for the device used here, routinely demonstrate the trap induced gate-lag phenomena. A well-known issue for HEMT charactisation is the extent and rate of trapping because it has a high degree of bias- and temperature-dependence [54], [55], [56], [57]. HEMT circuit models need to account for trapping and self heating dynamics to predict intermodulation and large-signal operation accurately [58], [59].

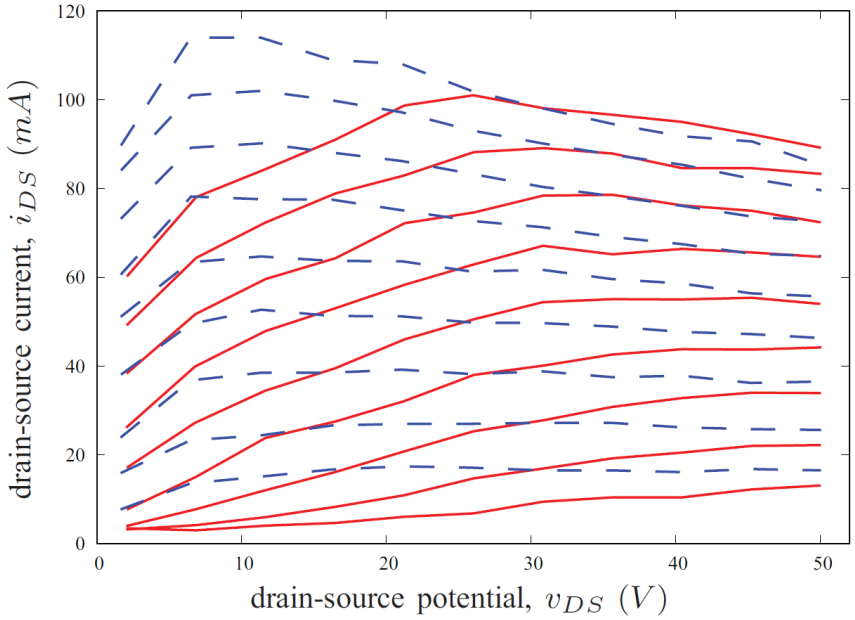


Figure 2.6: Pulsed-I/V of a GaN device, measured at two different times. Duty cycle 10%, pulse time: blue dash 50 μs, red solid 1s.

2.5.1 Modelling of Trapping

characterizing trap states over bias and temperature has been a major challenge in large-signal modeling of HEMTs. Drain-conductance dispersion in small-signal S parameter measurements has been fitted to dynamic models [60], [61]. Pulsed-I/V studies are effective for characterising trapping rates, while a transient measurement, from an initial trap state to a destination state [62], reveals the extent of trapping. These studies are restricted to bias conditions with observable drain current and to time frames that can be too slow at high potential bias conditions. This restriction limits observation to only a small portion of possible trap states even though memory of other states can be a significant contributor.

The initial approaches use time constant networks to add dynamic characteristics to a steady state model [63], [64]. One or two diodes have been added to the time-constant networks to model the different trap capture and emission rates [65], [66]. The trap potential is scaled to account for bias and temperature-dependence and the trapping dynamic is implemented by adding the trap-state potential to the pinch-off

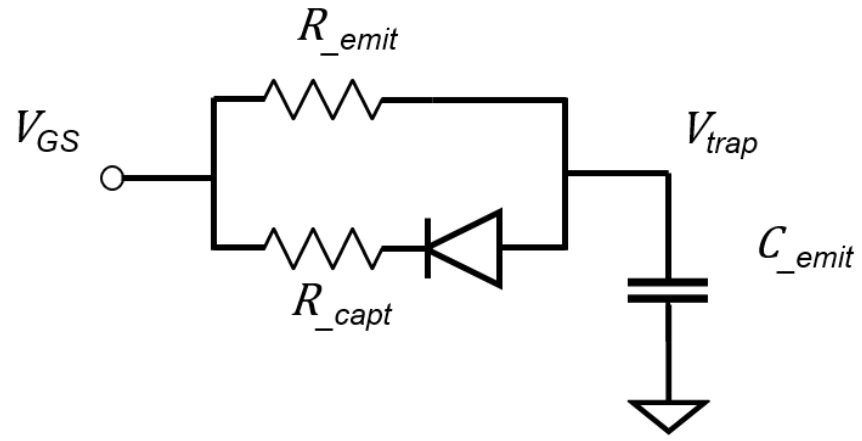


FIGURE 2.7: Traditional circuit model of a trap centre with a single diode.

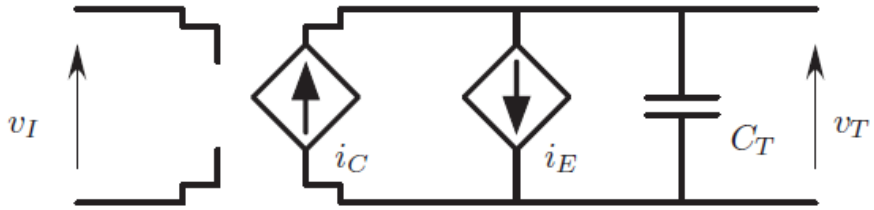


FIGURE 2.8: Circuit model of a trap centre [1].

potential. These models do not account for dependency on the trap state itself. A trap model that includes a diode is shown in Fig. 2.7.

The trap-state depends on the position of the Fermi level, E_I, relative to the energy level in the bandgap. It is influenced by the terminal potentials of the FET and in most cases, a simple linear combination of terminal potential provide an adequate model. A trap model can be implemented in a circuit simulator with a capacitor and single dependent current source. Depending on the bias and temperature conditions, this trap model accounts for the variation of the response rates from nanoseconds to minutes.

The generic trap-centre model depicted in Fig. 2.8 includes temperature and trap-state dependence to elegantly predict trapping rates in any state [1]. The trap state is modeled as a trap potential, v_T , across a charge storage capacitor, C_T , that is driven by charge capture, i_C, and emission, i_E, currents. The latter are controlled by the trap

state and a bias-dependent control potential (analogous to the trap energy), v_I .

3

Extraction and Verification of Intrinsic Small-signal Model Parameters

The scalable linear equivalent circuit model serves many purposes in the successful design of complex microwave and millimeter-wave circuits. It allows the designer to interpolate continuously among bias conditions and device sizes from a finite set of measured S-parameters. Scaling accuracy is paramount for correct device size selection during the early stages of MMIC design, especially if the optimal device width is not available as a test structure. Design also benefits from linear models that are exactly equivalent to their large-signal counterparts under small-signal drive conditions around a dc operating point. This helps MMIC design engineers to tune or optimise their circuits much faster than using large-signal models, due to the lower computational

complexity of linear solvers. The ability to switch between small-signal and large-signal models becomes a seamless process.

This chapter begins with a discussion of established equivalent circuit models, a candidate formulation is discussed relative to the requirements needed for large-signal equivalence, scalability and frequency-invariant parameters with the extraction of the intrinsic small-signal model that is consistent with a large-signal model and that linearly scales with zero offset in proportion to device width. In section 3.2, the small-signal S-parameters measurement required for accurate model extraction is provided. The access network is analysed using several EM tools and de-embedded from the measured data in section 3.3 Section 3.4 presents the extraction of small-signal parameters exhibiting the desired characteristics over a range of device sizes useful for microwave and millimtre-wave design for commercial GaAs and GaN processes.

3.1 Scalability of Intrinsic Model Parameters

The intrinsic device is the active part of the HEMT where non-linearity and memory effects occur which is distinct from the other sections of the HEMTs where the response to input stimulus is linear. A true intrinsic model can be defined as a model whose parameters scales linearly with the device width, i.e. at zero device width, the parameters of this intrinsic model should go to zero. Such behaviour demonstrates that all parasitic passive elements have been excluded from the modelled element. However, such a scalable intrinsic model has not been discussed in the literature and certainly cannot be found in any process design kit (PDK) supplied by semiconductor foundries, which usually provide macromodels for discrete device sizes or models with inaccurate scaling properties.

Modern MMIC are designed using sophisticated EM tools which can analyse large and complex passive structures to assist circuit designers in modelling their circuits more accurately. EM tools also can be used to analyse an arbitrary device layout capturing the extrinsic access network. Theoretically, an EM model of the extrinsic access network can be combined with an accurate scalable intrinsic model to synthesise

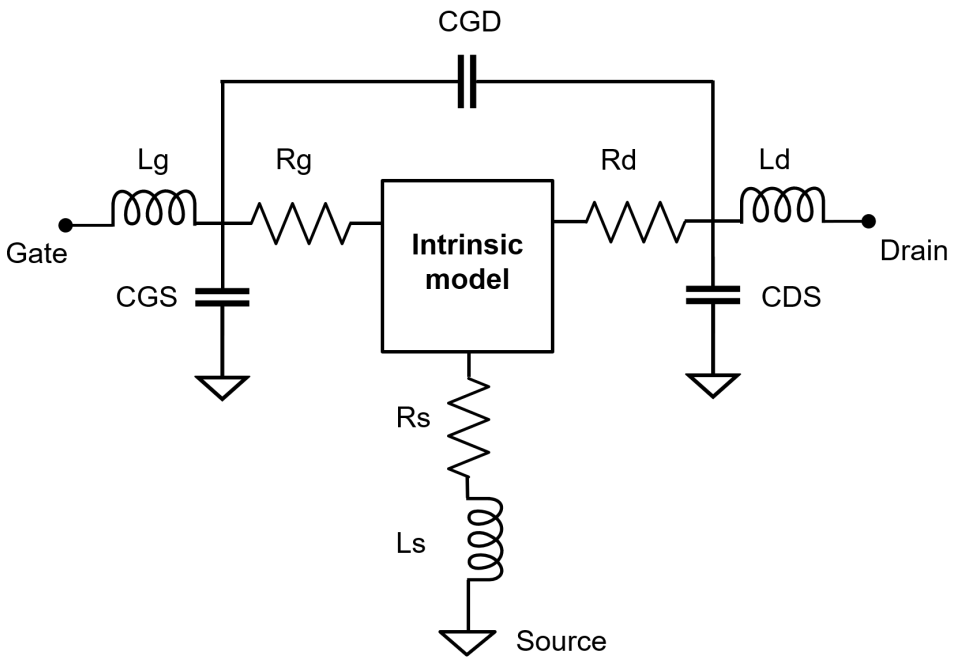


Figure 3.1: HEMT device Model representation showing the extrinsic equivalent circuit.

any arbitrary transistor device model accurately. A generic and simplified lumped element representation of a HEMT is shown in Fig. 3.1, This network is divided into two parts; the extrinsic part and the intrinsic part. The extrinsic network describes the electrical passive network needed to make necessary connections to the transistor active region. Given the physical nature of the access network, it is linear and bias independent allowing it to be described by a frequency-dependent complex impedance network. Furthermore, a network of resistance, capacitance and inductance elements can be used to describe some aspects of the metal structure.

Since the purpose of the access network is to provide electrical contacts to the intrinsic device, measurements carried out to characterise the intrinsic device always incorporate the access network and are affected by it. So an accurate representation of the access network is needed in order to remove or de-embed its effect from the measured data. Inaccuracies in the access network representation introduces errors to the de-embedded intrinsic device data. These inaccuracies are then manifested as erroneous dispersion of the intrinsic model elements in the iso-dynamic region of the device. The

extrinsic parameters of this network are constant and fixed once extracted. These extrinsic parameters do not necessarily scale linearly with the size of the transistor and must therefore be measured or modelled for each new device size or geometry. These extrinsic parameters can be extracted using cold FET techniques such as in [67] or pure EM technique, or a mixture of both.

The electromagnetic method is used in this thesis. On the other hand, the parameters of the intrinsic network vary with bias and with excitation frequency. Ideally, the intrinsic parameters ought to scale linearly with the size of the device, i.e. the gate width of the transistor but more effort is needed to extract these parameters over a wide range of biases and frequencies.

Fig. 3.2 shows the per-finger measured Y-parameters of a 2×75 μm low-noise, 0.15 μm pHEMT, biased at 3.5 V and 100 mA/mm. The effect of the transistor metallisation has been removed using the algorithm in [68] where an EM model of the access network is subtracted from the measured S-parameter data. The resulting intrinsic device data exhibits a small amount of residual dispersion due to impact ionisation.

A traditional standard [69] [70] and a full-reactive formulation of the equivalent circuit model for the purely intrinsic part of microwave FETs and pHEMTs are shown in Fig. 3.3 (a) and Fig. 3.3 (b), respectively. The standard model is sufficient to fit the real parts of the two dominant Y-parameters but not the imaginary parts. To see this by inspection, note that in Fig. 3.2 the values of the four imaginary Y-parameters are quite different and yet the model only has three capacitors (and no inductors) to model the four reactive terms. The standard model circumvents this by introducing two dispersive elements, R_i and τ, whereas the full-reactive model includes a transcapacitance, X_{ds}, as the fourth reactive element.

The circuit analysis of the standard model, Fig. 3.3 (a), yields four equations, two of which are dispersive in the general case, i.e. y_{11} and y_{21}.

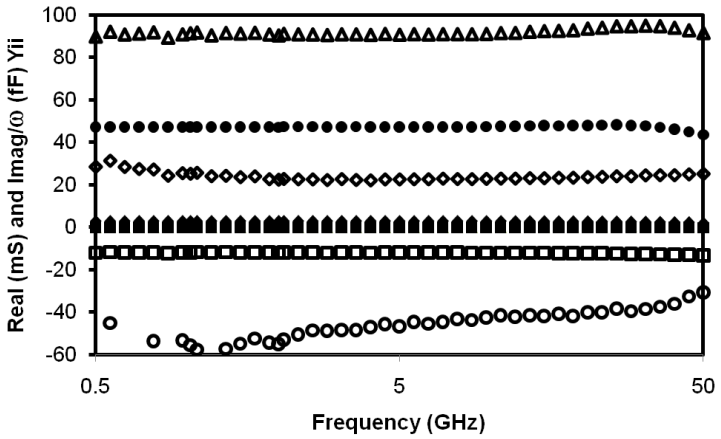
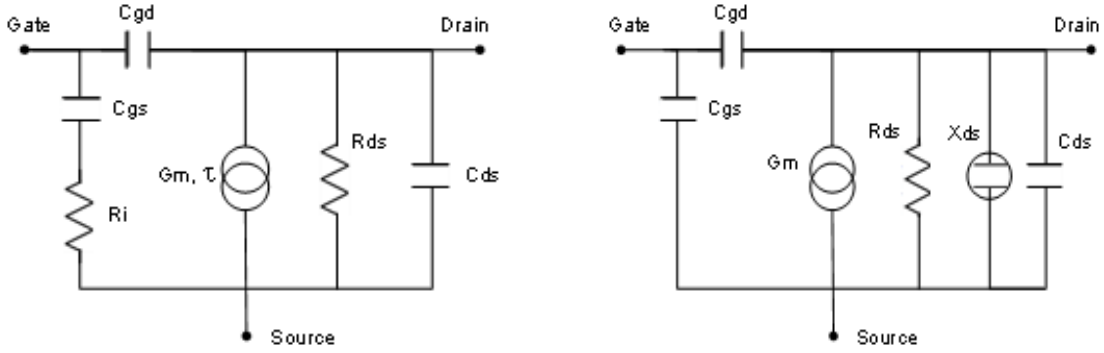


Figure 3.2: Intrinsic Y-parameters of each finger of a 2×75 μm HEMT at 3.5 V and 100 mA/mm: y_{11} (triangles), y_{12} (squares), y_{21} (circles) and y_{22} (diamonds). Real parts shown with filled shapes, imaginary hollow.



(a) Standard model.

(b) Full-reactive model.

Figure 3.3: Intrinsic FET equivalent circuit models.

$$y_{11} = \frac{\omega^2 R_i {C_{gs}}^2}{1 + \omega^2 R_i^2 {C_{gs}}^2} + j\,\omega \left(\frac{C_{gs}}{1 + \omega^2 R_i^2 {C_{gs}}^2} + C_{gd} \right) \tag{3.1}$$

$$y_{12} = -j\,\omega\, C_{gd} \tag{3.2}$$

$$\Re\{y_{21}\} = g_m \frac{(\cos(\omega\tau) + \omega R_i C_{gs} \sin(\omega\tau))}{1 + \omega^2 R_i^2 {C_{gs}}^2} \tag{3.3}$$

$$\Im\{y_{21}\} = g_m \frac{\sin(\omega\tau) + \omega^2 R_i C_{gs} \cos(\omega\tau)}{1 + \omega^2 Ri^2 {C_{gs}}^2} - \omega\, C_{gd} \tag{3.4}$$

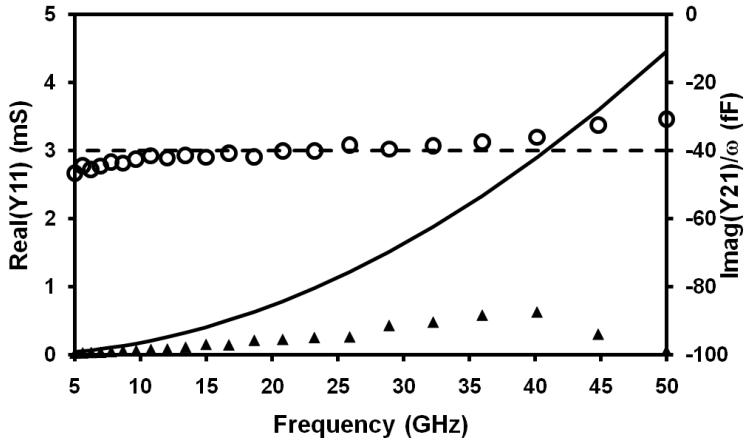


FIGURE 3.4: Intrinsic Y-parameters vs model with $R_i = 7\ \Omega$: Real part of y_{11} (data shown as triangles, model as solid line), Imaginary part of y_{12} (data shown as hollow circles, model as dashed line).

$$y_{22} = g_{ds} + j\,\omega\,(C_{ds} + C_{gd}) \tag{3.5}$$

Fig. 3.4 shows that with $\tau = 0$ ps and $R_i = 7\ \Omega$, the fit to $Im\{y_{21}\}$ is good but at the expense of the fit to $Re\{y_{11}\}$. Not only has the fit deteriorated but it has become highly dispersive whereas the measured data is not.

Although the element R_i is used in some noise models [71], forcing it to zero removes a source of non-physical dispersion from the equivalent circuit model. With $R_i = 0$, (3.1)-(3.5) become:

$$y_{11} = j\,\omega\,(C_{gs} + C_{gd}) \tag{3.6}$$

$$y_{12} = -j\,\omega\,C_{gd} \tag{3.7}$$

$$\Re\{y_{21}\} = g_m\,cos\,(\omega\tau) \tag{3.8}$$

$$\Im\{y_{21}\} = \omega\left(g_m\,\frac{sin\,(\omega\tau)}{\omega} - C_{gd}\right) \tag{3.9}$$

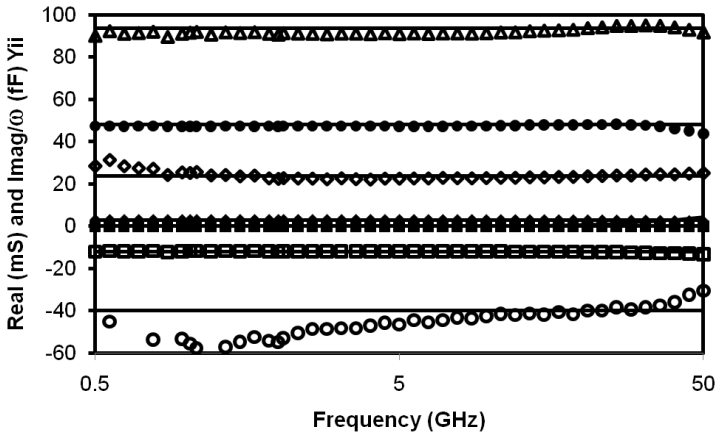


Figure 3.5: Fit to intrinsic data with the non-dispersive model y_{11} (triangles), y_{12} (squares), y_{21} (circles) and y_{22} (diamonds). Real parts shown with filled shapes, imaginary hollow.

$$y_{22} = g_{ds} + j\,\omega\,(C_{ds} + C_{gd}) \tag{3.10}$$

For millimetre-wave frequencies and low drain voltages, $\omega\tau \ll 1$, hence, (3.8) and (3.9) can be further simplified, so that the remaining dispersive terms are removed to give:

$$y_{21} = g_m + j\,\omega\,(X_{ds} - C_{gd}) \tag{3.11}$$

and

$$X_{ds} = g_m\,\tau \tag{3.12}$$

The transcapacitance, X_{ds}, appears between the intrinsic drain and source nodes in the equivelent circuit model but is controlled by the potential between the gate and the source nodes. This is the imaginary counterpart to the transconductance, g_m. The intrinsic equivalent circuit model becomes Fig. 3.3 (b) [67] and the fit to data is very good in the mm-wave region as shown in Fig. 3.5.

3.2 Small-signal Measurement

When making measurements for model extraction, the reference planes should be located at the device input and output planes used by the MMIC design engineer. This may seem like an obvious requirement, but the use of common standards such as GGB Incs CS-5, or Cascade Microtech's ISS calibration structures cause the measurements reference planes and the device input and output planes to be offset.

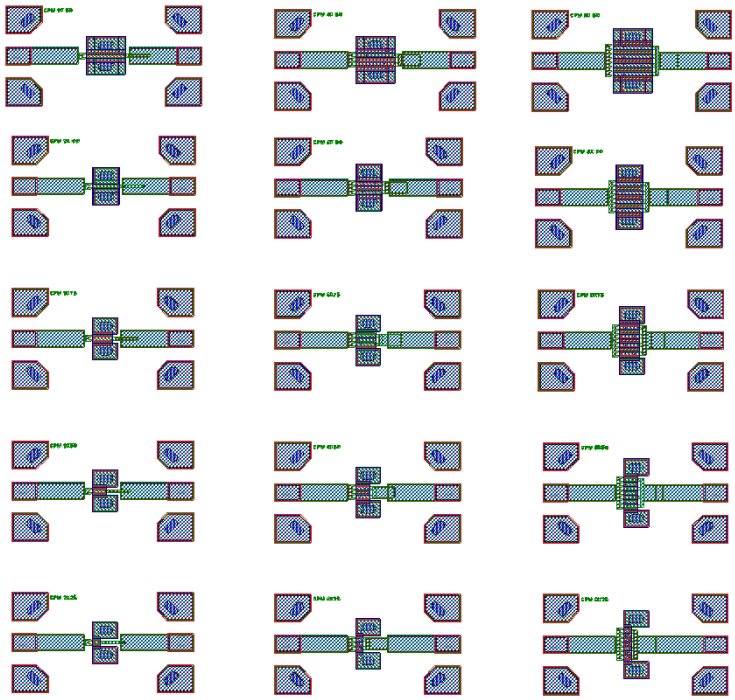


Figure 3.6: Test structures of various HEMT devices used for single-finger model extraction and verification.

3.2.1 HEMT Test Structures

An array of 2-finger, 4-finger and 8-finger GaAs 0.15 μm pHEMT microstrip with two backvias are layed out as shown in Fig. 3.6. The 2-finger array including, 2×25, 2×50, 2×75 and 2×100 μm is used for the extraction and the reason for that is device electrical and thermal symmetry for the two gate fingers (active region). The rest of devices are used for verification of scalability of the model.

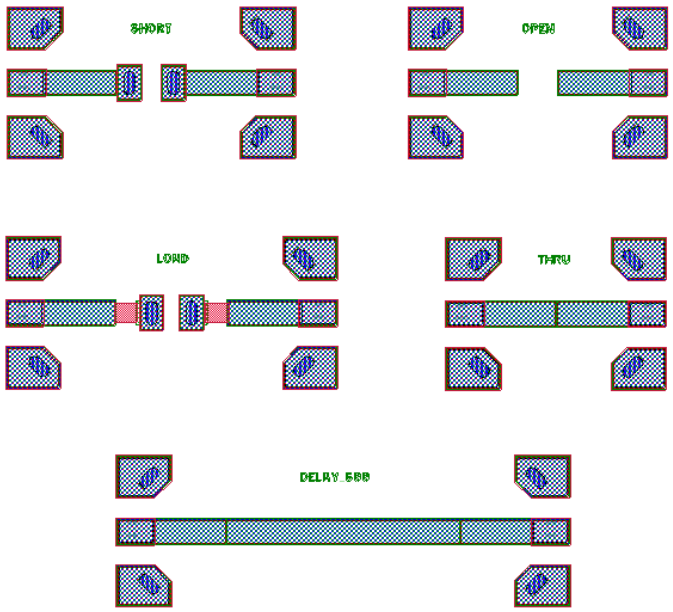


Figure 3.7: SOLT calibration structures used with the Vector Network Analyser to deembedd the small-signal measurements to the DUT.

In order to characterise the intrinsic small-signal RF response of the HEMT, test devices shown in Fig. 3.6 are mounted on copper block using solder for better thermal performance. Then on-wafer measurement were done using ground-signal-ground RF probe that had 100 μm pitch.

3.2.2 Calibration Structures

An accurate instrument calibration to well-defined reference planes is achieved using one of the Vector Network Analyser (VNA) on-Wafer calibration methods such as Thru, Reflect, Line (TRL) or Short, Open, Load, Thru (SOLT). In this case, the SOLT calibration method is used. Fig. 3.7 shows the on-wafer SOLT calibration standards which are used to set the reference plane at the wanted extrinsic terminals of the test devices. A further advantage of this approach is that the probe-to-microstrip transition falls inside the calibrated measurement path, eliminating the need to separately deembed this discontinuity. The effect of cables, bias tees, probes and probe pads are also taken care of through the SOLT calibration and the reference plane of the measurement

is extended to the extrinsic terminals of device under test (DUT) as shown in Fig. 3.8.

3.2.3 Measurement Plan

Two-port small-signal S-parameters measurements are made over a wide range of gate and drain biases. The SOLT on-wafer calibration standard is used to calibrate the VNA over the frequency range of 50 MHz to 50 GHz with 64 frequency points in a logarithmic scale. S-parameters data is used to derive the small-signal Y-parameters at the bias points which are to be used in the extraction process of the intrinsic finger.

Test devices that are used in this measurement are carefully selected from a wafer that displays typical performance characteristics and falls within the accepted limits of the foundry. Several devices of the same design are measured in order to ensure that a typical device is selected for the extraction.

3.3 Extraction of Intrinsic Parameters

Several methods exist that are used to extract an equivalent lumped-element extrinsic network or to analyse the access network of a device using an EM tool. A Lumped-element equivalent network representation is reasonably accurate at low frequencies, i.e. below 6 GHz, but its accuracy starts to degrade at higher frequencies due to distributed effects of the access metalisation and increased coupling between ports, which the lumped models typically ignore. In addition, the parameters of the lumped-element network do not always scale linearly with the width of the device. These limitations of the lumped-element network detract from the aforementioned advantages of the scalable intrinsic model, and severely limit the ability of the model to extrapolate in frequency.

In this thesis EM modelling of the extrinsic access network is used, combined with the cold-FET extraction technique that is used for initial estimates of the access resistance values.

3.3.1 Electromagnetic Analysis For Device Metalisation

EM tools have advanced in recent years due to the performance increases in the computing capabilities and improvements to the underlying solvers. This has enabled MMIC designers to produce more complex and compact successful designs with more confidence and fewer design iterations. Microwave and millimetre-wave design engineers rely heavily on EM analysis to analyse passive components and interconnects. However the advantages of EM tools can also be extended to analyse the metallisation of HEMT devices. This can be crucial in modelling exercises, to accurately separate/extract the intrinsic active device from the access network surrounding it.

From a design perspective, EM models of the HEMT access networks and other passive components and interconnect can be consolidated to simulate large portions of circuits, or even entire layouts, to capture coupling and feedback between active and passive elements. Many EM simulators are available for MMIC designers as standalone tools such as Sonnet [72], or these tools can be embedded in design suites like AXIEM [73] and Momentum [74].

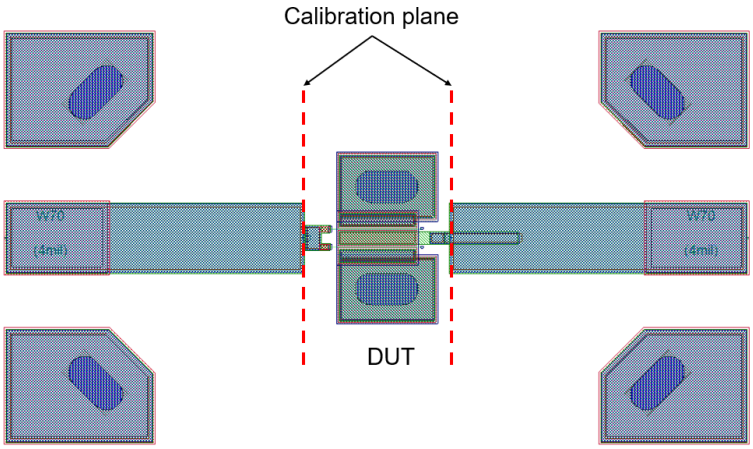


Figure 3.8: A 2 ×75 μm microstrip HEMT device layout showing the SOLT calibration reference planes.

Fig. 3.8 shows a 2×75 μm common-source microstrip HEMT device layout. The sources are grounded by two vias that extend to the metal on the backside of the substrate. These vias are termed *backvias*. The device has input and output RF

feeds; the input is connected to the gate terminal and the output feed on the right hand side is connected to the drain terminal. A 2-finger device is selected for the extraction process of the single-finger intrinsic model because of the layout symmetry which means that the two active fingers of the device are assumed electrically and thermally identical and always excited in phase. Measuring small 2-finger devices also simplifies the measurement requirements, e.g. power supply current limits.

The active region around the gate finger defines the channel of the HEMT and its behavior is guided by the semiconductor epitaxial layers and doping profile which cannot be accurately analysed without first accounting for the access metalisation.

Fig. 3.9 shows how an EM analysed metalisation is connected to the intrinsic single-finger model.

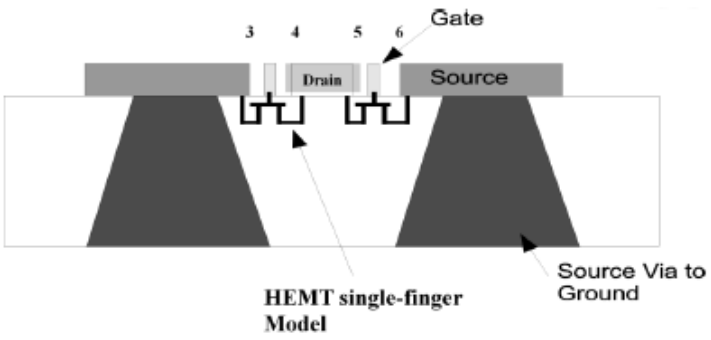


Figure 3.9: Connecting the intrinsic single-finger model to an EM-analysed access network structure that uses internal ports.

Configuring the EM geometry is non-trivial, especially when it comes to defining the EM ports and the way these ports interact with the geometry being simulated. Three EM tools are considered for analysing the metalisation of HEMT devices; AXIEM, Sonnet and Momentum. The results of the analysis are then separated from the 2-port measured S-parameter data, through the a de-embedding algorithm which is explained in details in section 3.3.2.

AXIEM EM Structure Setup

AXIEM is a planar 3D simulator that uses the Method of Moments to solve for the currents on conductors that can be embedded in a stack-up of planar dielectric layers.

The dielectric layers are infinite in the x-y plane. AXIEM uses a mesh defined on the surface of the conductors as the basis for the solution. The effects of the dielectric layers are taken into account mathematically through Green's functions.

An AXIEM EM structure setup is illustrated in Fig. 3.10. The materials and stack-up definitions for this EM structure match what is supplied by the foundries. The ports are also shown in the same figure. There are two common types of ports that are used in planar EM tools; edge ports and internal ports. The edge ports are used to connect the accessible external device terminals, i.e. the gate and drain, to dc bias and RF signals. However, internal ports are generally used to access nodes that are not accessible for direct for probing or analysing, i.e. the active region or *intrinsic gate-finger* of a HEMT. In Fig. 3.10, ports (1) and (2) connect the gate and the drain terminals respectively. Each gate-finger is accessed by two internal ports, i.e. ports (3) and (4) for the top gate-finger and (5) and (6) for bottom gate-finger.

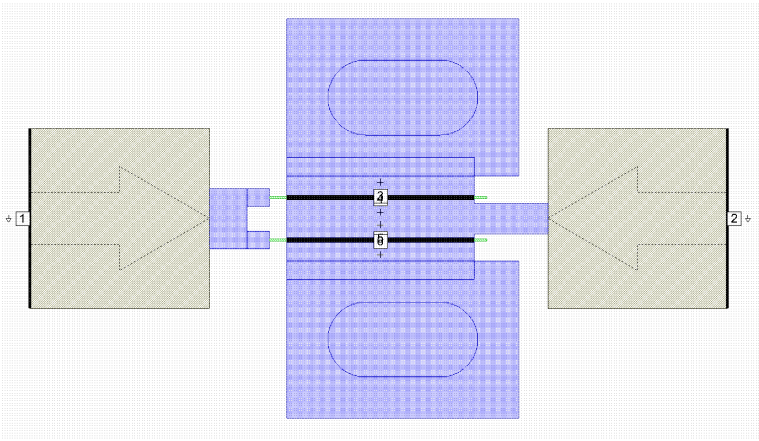


Figure 3.10: AXIEM EM structure setup for 2×75 μm microstrip device.

The internal ports extend along the gate width of the HEMT, separating the gate metal on one side form the drain or source metal on the other. The negative terminal of the intrinsic port becomes a local ground, i.e. the negative terminal of the port. A simple example of how to connect the internal port of Fig. 3.12, in a schematic, is shown in Fig. 3.13.

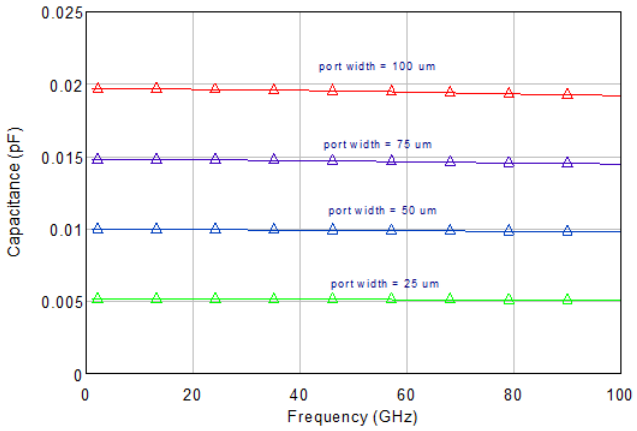


Figure 3.11: AXIEM's internal port capacitance versus frequency with port width swept from 25 μm to 100 μm.

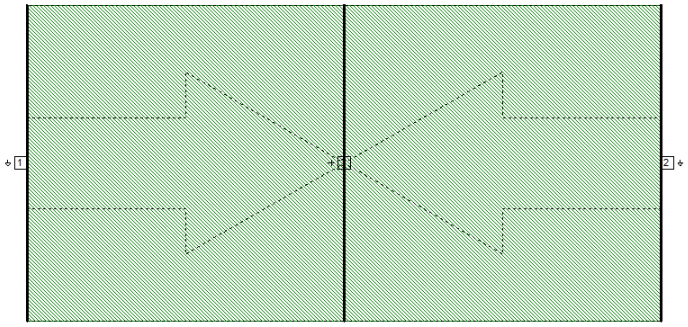


Figure 3.12: AXIEM EM structure used to calculate the capacitance associated with its internal port.

The internal ports in AXIEM are un-calibrated and there is some residual capacitance associated with these ports. To determine the value of the port capacitance, a separate EM structure is analysed in which an internal port is set across two touching microstrip lines. Both of the microstrip lines are de-embedded back to the internal port, i.e. zero length, in order to calculate the capacitance associated with the internal port alone. A parametrised EM simulation is setup to sweep the width of the two microstrip lines together from 25 to 100 μm in 25 μm steps to assess the relationship between the port width and the internal port's capacitance. Fig. 3.11 show the capacitance value of the internal port simulated for different widths, and the results confirm

that the associated port capacitance scales linearly with the width of the internal port.

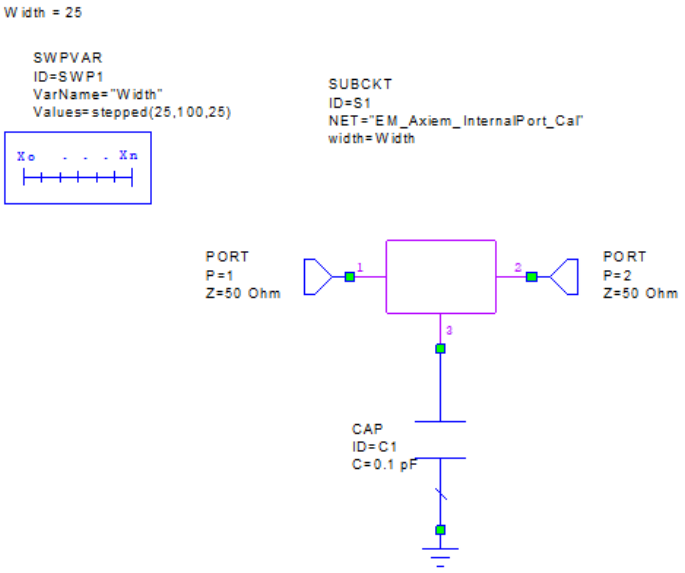


Figure 3.13: AXIEM internal port connected in a schematic.

As the internal port capacitance scales linearly with port width, it can be accounted for easily during the extraction of the intrinsic model. Therefore the port capacitance will not introduce any artifacts that limit the scalability or accuracy of the model.

MOMENTUM EM Structure Setup

Momentum is another 3D planar EM simulator that is also based on the Method of Moments technology. Similar to other EM tools, such as AXIEM and Sonnet, Momentum is able to evaluate multilayer planar geometries.

Differential gap-ports in Momentum are similar to the internal ports in AXIEM, however their implementation in the layout is quite different. Momentum requires the two ports to be placed on the edges of physically separated metal polygons. During the port calibration process, which happens in the background while simulating the structure, Momentum extends the edges of the two polygons and sets a very small gap between the two ports which are differentially excited. Another similar differential port are also avaialable in Momentum called the SMD-port. The extra extended metal

is de-embedded in the case of the SMD-port and not de-embedded in the gap-port case. The differential gap-ports exhibit better behaviour in terms of the capacitance value associated with the port. Transmission line ports (TML) are used to excite the extrinisc gate and drain terminals to apply the DC bias.

Fig. 3.14 demonstrates how the metalisation of a HEMT and the associated ports are setup in Momentum. Similar to AXIEM, these differential gap-ports are uncalibrated and there is a capacitance associated with them. Fig. 3.15 demonstrates the associated capacitance of the differential gap-port scales linearly with the width the port.

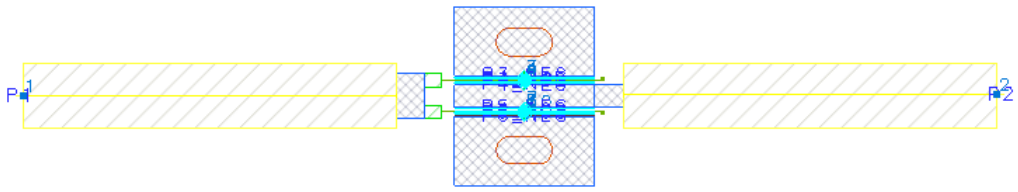
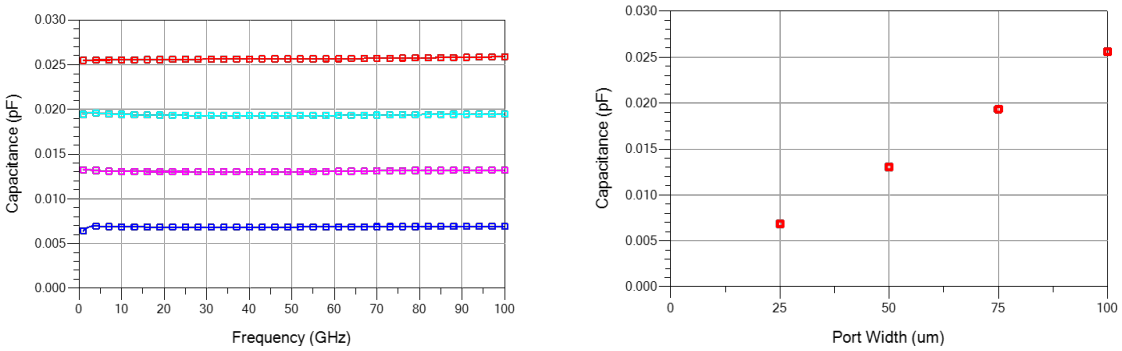


FIGURE 3.14: Momentum layout setup for a 2 $\times$75 μm.



(a) (b)

FIGURE 3.15: Momentum's internal port capacitance with differential gap-port width swept from 25 μm to 100 μm versus (a) frequency and (b) port width at 10 GHz.

Sonnet EM Structure Setup

Sonnet employs the Method of Moments applied directly to Maxwell's equations to solve the planar 3D problems. In Sonnet, the simulation is contained within a finite

boundary in which the lossless, conducting sidewalls form a perfect ground reference for any edge port.

It's worth mentioning that Sonnet is the only tools amongst the other tools mentioned that utilities the Fast Fourier Transform (FFT) due to the use of perfectly conducting sidewalls which allows Sonnet to reach a precise solution to full numerical precision. This results in extremely high dynamic range, permitting accurate modelling of very weak coupling effect, for example.

Sonnet is the only tool available that supports the co-calibrated ports, in addition to the conventional internal ports as offered in AXIEM and Momentum. When using co-calibrated ports, the intrinsic region is defined by three terminals; the gate, drain and source.

The co-calibrated internal ports are accurately de-embedded in Sonnet. Certain ports are added to certain groups based on their proximity so that they can be simultaneously de-embedded using the high accuracy de-embedding technique [75].

In addition to the co-calibrated ports feature, Sonnet has another useful capability which is the "box symmetry" option. This option can only be used if the structure to be analysed is symmetrical in one axis. If this option is enabled for a suitable candidate, the simulator will implement a perfect magnetic wall along the line of symmetry and solve only half of the structure. This results in a 50 to 70% reduction in simulation time.

Fig. 3.16 shows a 2 $\times$ 75 μm Sonnet EM layout structure. The symmetry option is selected in this case and the top half of the structure is only configured with the co-calibrated internal ports 3A, 4A, 4B and 5B as shown in Fig. 3.17 . Ports 3A and 4A are de-embedded simultaneously because of their proximity and the same applies to ports 4B and 5B.

An example of a Sonnet stackup is shown in Fig. 3.18, which includes two microstrip metal layers; "MET" and "PC" representing the top-side metal and the perfect conductor respectively. The metal layers sit on a 100 μm thick SiC substrate and a backvia

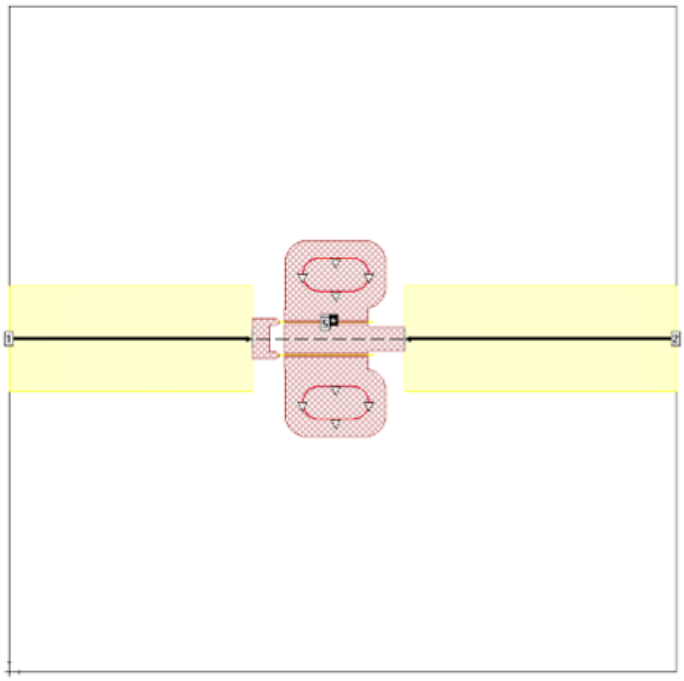


Figure 3.16: Sonnet layout setup for a 2×75 μm microstrip device.

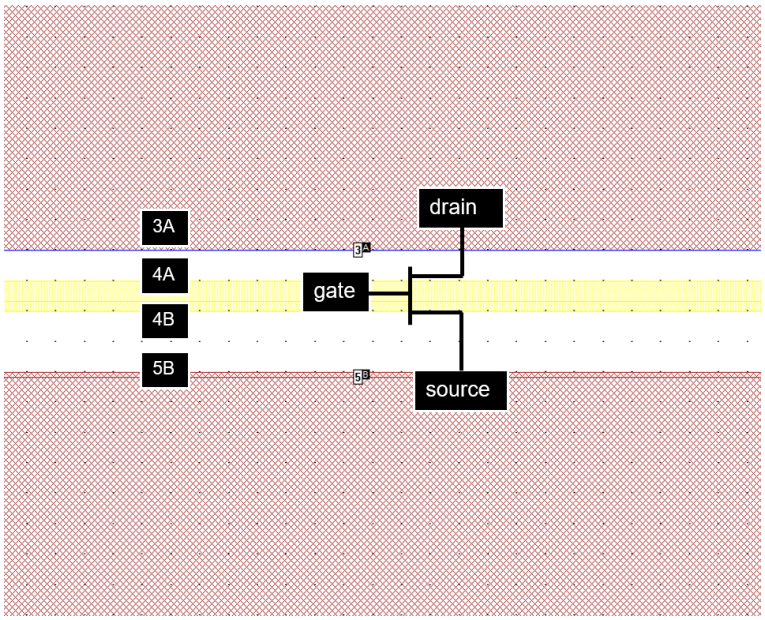


Figure 3.17: Sonnet co-calibrated ports setup, illustrating how the intrinsic model is connected to the EM in the schematic.

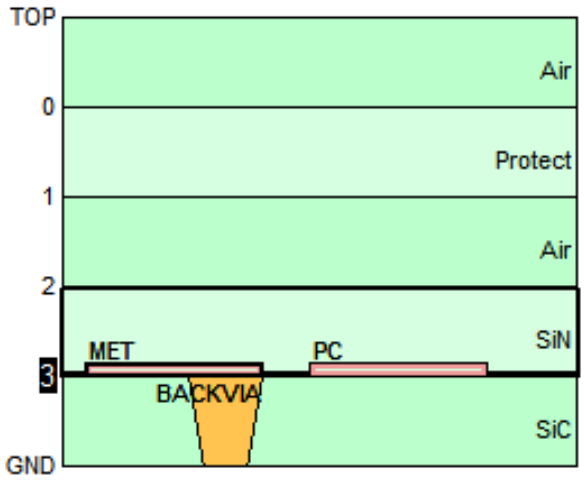


Figure 3.18: Sonnet stack-up example.

extends from the top of the SiC substrate to the backside ground.

3.3.2 De-embedding the Extrinsic Network from Small-signal Measured Data

As demonstrated in the previous section, the implementation of internal ports in the three EM tools (Sonnet, AXIEM and Momentum) are not identical. The excitation and calibration of these internal ports are also different across the different tools. Consequently the EM results obtained from each software tool are not absolutely equivalent and are generally not interchangeable. Therefore, EM structures, including transistor metalisation, that contain internal ports, are not universally calibrated to the intrinsic device (i.e. the gate-finger).

Sonnet is the only tool has the perfectly co-calibrated port option which results in accurate port de-embedding with no residual port capacitance. The symmetry plane option is also found only in Sonnet, which helps to reduce the problem size and speed up the simulation time significantly. On the other hand, Sonnet is a standalone EM tool, which adds a significant additional cost on design teams. Moreover, Sonnet is not fully integrated into design suites, unlike AXIEM and Momentum which form part of the AWR and ADS design suites respectively. Using Sonnet as a standalone EM solver

disturbs the design workflow and increases the possibility of human error.

In this section, Sonnet is used used to calibrate the AXIEM and Momentum EM structures that will be used in the extraction process.

For each gate finger, and when co-calibrated ports are used, the EM analysis results in three internal nodes connected to the intrinsic active region of the device; gate, drain and source. However, when uncalibrated internal ports are used in AXIEM or Momentum, only two internal nodes result from the EM analysis; the drain and the source, while the gate is locally grounded.

Consider the block diagram of the HEMT shown in Fig. 3.19, it illustrates the segregation of the external parasitics from the intrinsic device of a HEMT [76] [77] [68]. The 4×4 parasitic admittance matrix $\boldsymbol{Y_P}$ is partitioned into four 2×2 submatrices, $\boldsymbol{Y_{ee}}$, $\boldsymbol{Y_{ei}}$, $\boldsymbol{Y_{ie}}$ and $\boldsymbol{Y_{ii}}$. Thus, the port currents become

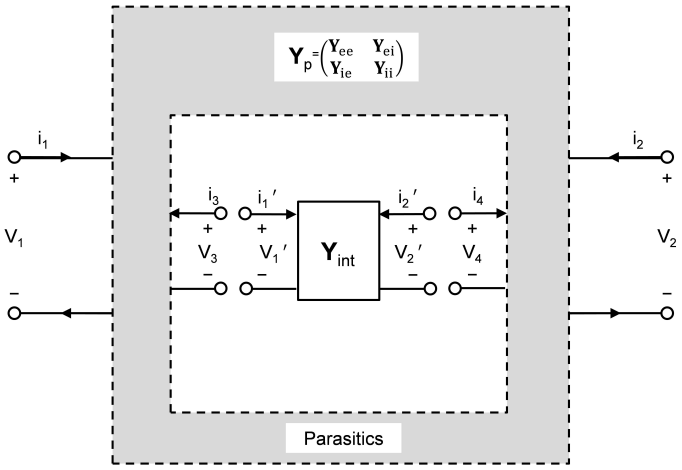


FIGURE 3.19: Extrinsic one-finger HEMT in admittance form with gate, drain and source metal, $\boldsymbol{Y_p}$ segregated from the intrinsic device $\boldsymbol{Y_{int}}$.

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \boldsymbol{Y_{ee}} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} + \boldsymbol{Y_{ei}} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} \tag{3.13}$$

$$\begin{bmatrix} i_3 \\ i_4 \end{bmatrix} = \boldsymbol{Y_{ie}} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} + \boldsymbol{Y_{ii}} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} \tag{3.14}$$

The 2-port Y-parameters measurement of the device, which can be obtained from the small-signal S-parameters measurements, is given by

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \boldsymbol{Y_{meas}} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{3.15}$$

The intrinsic device Y-parameters which represents the intrinsic gate-finger active region, can be described from Fig. 3.19 as

$$\begin{bmatrix} i_1\prime \\ i_2\prime \end{bmatrix} = \boldsymbol{Y_{int}} \begin{bmatrix} v_1\prime \\ v_2\prime \end{bmatrix} \tag{3.16}$$

By applying the boundary conditions where $v_3 = v_1\prime$, $v_4 = v_2\prime$, $i_3 = i_1\prime$, and $i_4 = i_2\prime$ to above equation we have

$$\begin{bmatrix} i_3 \\ i_4 \end{bmatrix} = -\boldsymbol{Y_{int}} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} \tag{3.17}$$

with substituting (3.15) into (3.13)

$$\boldsymbol{Y_{meas}} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \boldsymbol{Y_{ee}} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} + \boldsymbol{Y_{ei}} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} \tag{3.18}$$

which can be rewritten as

$$(\boldsymbol{Y_{meas}} - \boldsymbol{Y_{ee}}) \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \boldsymbol{Y_{ei}} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} \tag{3.19}$$

and with substituting (3.17) into (3.15)

$$-\boldsymbol{Y_{int}} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} = \boldsymbol{Y_{ie}} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} + \boldsymbol{Y_{ii}} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} \tag{3.20}$$

which can be rewritten as

$$(\boldsymbol{Y_{int}} + \boldsymbol{Y_{ii}}) \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} = -\boldsymbol{Y_{ie}} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{3.21}$$

and by substituting (3.21) into (3.19) with a simple matrix manipulation, we get the following equation

$$\boldsymbol{Y_{int}} = -\boldsymbol{Y_{ie}} \left(\boldsymbol{Y_{meas}} - \boldsymbol{Y_{ee}}\right)^{-1} \boldsymbol{Y_{ei}} - \boldsymbol{Y_{ii}} \tag{3.22}$$

The equations above are implemented in Cadence AWR Microwave Office where the de-embedding is taken care of. The de-embedded 2×2 Y-parameters matrix that describes the active region of the HEMT, is then converted from common-gate to common-source configuration. A complete channel charge model with a total of four frequency independent capacitance terms are obtained from and the four complex Y-parameters terms are used the verify the dispersion and scalability in order to validate the extraction of the intrinsic device.

The conversion to common-source can be done as shown in [78]

$$YCS_{11} = YCG_{11} + YCG_{12} + YCG_{21} + YCG_{22} \tag{3.23}$$

$$YCS_{12} = -(YCG_{12} + YCG_{22}) \tag{3.24}$$

$$YCS_{21} = -(YCG_{21} + YCG_{22}) \tag{3.25}$$

$$YCS_{22} = YCG_{22} \tag{3.26}$$

and the common-source intrinsic model parameters are calculated as

$$g_{gs} = Re(Y_{11}) \tag{3.27}$$

$$g_{gd} = Re(Y_{12}) \tag{3.28}$$

$$g_m = Re(Y_{21}) \tag{3.29}$$

$$g_{ds} = Re(Y_{22}) \tag{3.30}$$

$$C_{gd} = -Im(Y_{12}) \tag{3.31}$$

$$C_{gs} = Im(Y_{11}) - C_{gd} \tag{3.32}$$

$$X_{ds} = -Im(Y_{21}) - C_{gd} \tag{3.33}$$

$$C_{ds} = Im(Y_{22}) - C_{gd} \tag{3.34}$$

3.3.3 Noise

In a section of the channel with gate width w, noise may be modelled by two correlated noise currents sources at the intrinsic model level, i_{gw} from gate to source and i_{dw} from drain to source [79] [80] [81].

$$\overline{i_{dw}^2} = 4\,k\,T_{cw}\,\Delta f\,g_{mw}\,P \tag{3.35}$$

$$\overline{i_{gw}^2} = 4\,k\,T_{gw}\,\Delta f\,{C_{gs}}^2\,\omega^2\,/\,g_{mw}\,R \tag{3.36}$$

where P and R are constants and T_{gw} and T_{cw} are the gate and channel temperatures at w. Cappy's analysis [81] suggests that P should be ≈ 1 and $R \approx 0.2$.

The total drain and gate noise currents are obtained by integrating (3.35) and (3.36)

$$\overline{i_{dw}^2} = \int_0^W 4\,k\,T(w)\,\Delta f\,g_m\,P\,dw \tag{3.37}$$

$$\overline{i_{gw}^2} = \int_0^W \frac{4\,k\,T(w)\,\Delta f\,{C_{gs}}^2\,\omega^2\,R}{g_{mw}}\,dw \tag{3.38}$$

Equations (3.37) and (3.38) may be simplified by assuming g_m and C_{gs} are constant with frequency

$$\overline{i_{dw}^2} = 4\,k\,\Delta f\,g_m\,P\int_0^W T_c(w)\,dw \tag{3.39}$$

$$\overline{i_{gw}^2} = \frac{4\,k\,\Delta f\,\omega^2\,R\,{C_{gs}}^2}{g_m}\int_0^W T_g(w)\,dw \tag{3.40}$$

Clearly from (3.39) and (3.40), the noise current models depends on the intrinsic model equivalent parameters, g_m and C_{gs}.

Thus, noise parameters belongs to the intrinsic part of the device and noise measurements must be de-embedded in the same way as the small-signal measurements, in order for noise model parameters to scale linearly with device width.

3.4 Practical Application and Verification

3.4.1 Application to GaAs Process Technology

Process Technology

The devices that are measured and modeled in this section were fabricated on a commercial 0.15 μm low noise pHEMT technology grown on 100 μm GaAs substrate. For typical DC device characteristics, the peak transconductance is 370 mS/mm at V_{DS} = 4 V with maximum output current density of 500 mA/mm. Typical the threshold voltage is -0.45 V and typical gate-drain junction breakdown voltage is greater than 9 V. For typical RF performance, the transition frequency, f_T is 110 GHz with power density of 540 mW/mm at 29 GHz.

Small-Signal Measurement Details

An Agilent 8510C VNA is used to perform small-signal S-parameters measurements. The VNA is calibrated from 50 MHz to 50 GHz with 64 frequency points covering the frequency range in logarithmic steps. A 2-channel source measure unit (SMU), is used to bias to the gate/drain of the DUT through Agilent 0.45 MHz to 50 GHz bias tees. A fine bias list file is created to control the SMU, with V_{DS} and V_{GS} swept from 0 to 4 V and -1 to +0.6 V respectively. On-wafer SOLT calibration is used to accurately set the measurement reference plane at the DUT's input and output terminals. In-house measurement software is used to automate the measurement.

Four 2-finger devices; 2×25, 2×50, 2×75 and 2×100 μm, are mounted on copper blocks, using solder paste, and measured for the single-finger model extraction. Two-finger devices are favoured for the extraction because they are ideally electrically symmetrical. Furthermore, and assuming no fabrication defects, the symmetrical 2-finger device also guarantee that the two fingers are thermally symmetrical and running at the same temperature.

Extraction of Access Resistance Values

The parasitic access resistances; R_g, R_s and R_d are initially estimated through the cold-FET extraction technique described in [67]. These values are used as a starting point for the extraction, they are adjusted and tuned in a fitting process until minimal dispersion in intrinsic model parameters is achieved. This process of fitting the access resistance may take several iterations.

EM Device Layout Structure Setup

The full metalisation, i.e. gate, drain and source metal structures including the source backvia, of each device of the four 2-finger devices is analysed using the Sonnet EM tool co-calibrated ports. Fig. 3.16 shows the Sonnet EM structure with the full metalisation of a 2×75 μm microstrip device, in which all non-metallic features of the standard device layout are removed, including the epitaxial layers in the vicinity of each gate finger.

The external gate and drain feeds in the EM structure are de-embedded to the DUT's extrinsic terminals in order to exactly match the calibration reference planes of the device test structure. Configuration of the EM structure is a crucial step in the extraction process, in which it is essential for the EM model layout to replicate the real physical device structure as accurately as possible.

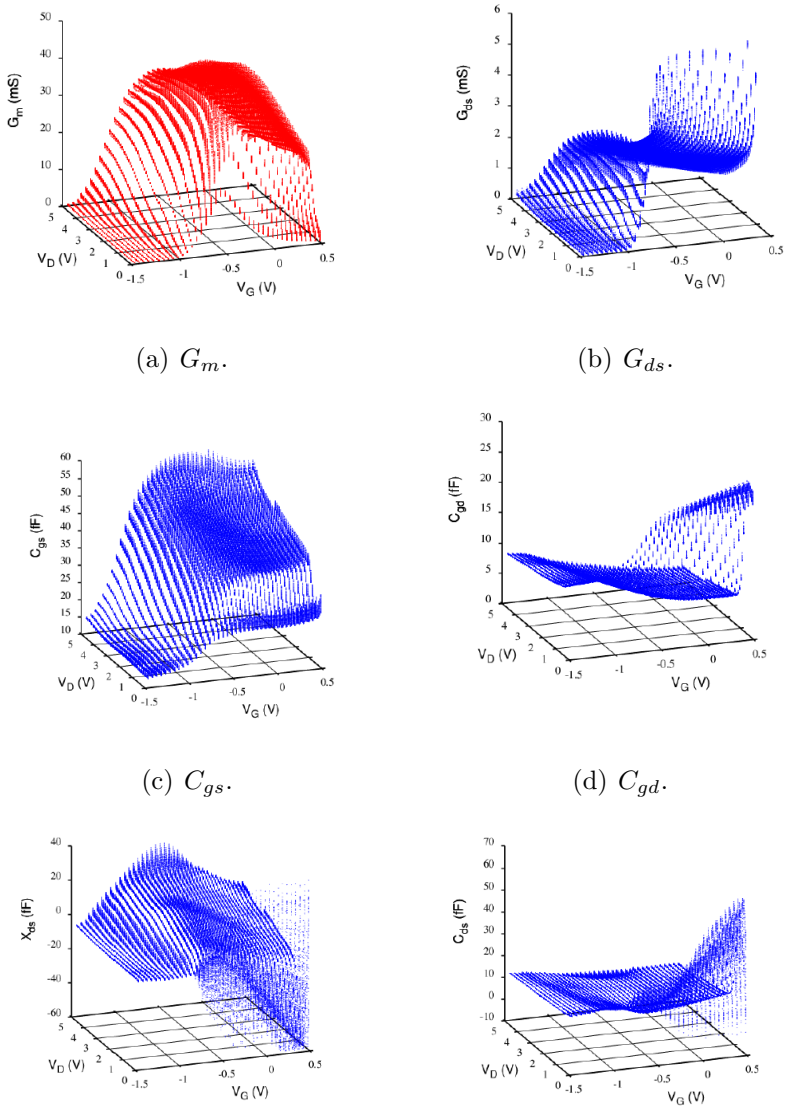
Extraction Verification

The extracted intrinsic small-signal model parameters should exhibit minmal dispersion and scale linearly with device width. These two characteristics of the intrinsic data will be used to verify the extraction.

Dispersion-less Intrinsic Data

The model was extracted from de-embedded intrinsic measurement data for transistors at 3.5 V and 100 mA/mm with nominal widths of 25, 50, 75 and 100 μm. The extracted intrinsic data exhibits some evidence of dispersion due to impact ionisation above V_{DS} = 3 V and where V_{GS} is high enough to promote significant drain current

but low enough to allow tunneling current to the gate as presented in Fig. 3.20.



(a) G_m. (b) G_{ds}.

(c) C_{gs}. (d) C_{gd}.

(e) X_{ds}. (f) C_{ds}.

Figure 3.20: Intrinsic model parameters extracted for a wide range of gate and drain biases. Measurements taken from 50 MHz to 50 GHz with 64 points covering the frequency range in logarithmic steps.

Scaling the Intrinsic Data

Fig. 3.21 shows the excellent linear scaling of the transconductance and output conductance for the range of device widths measured. The capacitances C_{gs}, C_{gd}, C_{ds} and the transcapacitance, X_{ds} also scale linearly from 25 μm to 100 μm as shown in

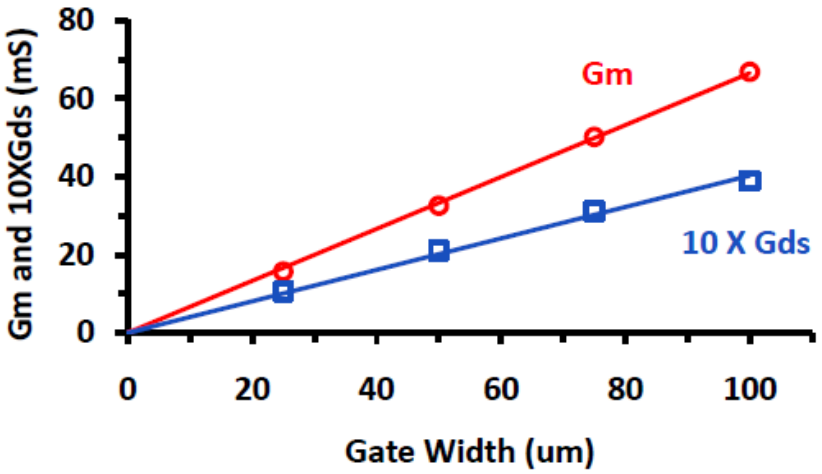


FIGURE 3.21: Extracted transconductance, g_m, (circles) and output conductance, $10 \times G_{ds}$, (squares) per finger for four HEMT widths. Solid lines show scaling fit.

Fig. 3.22.

3.4.2 Application to GaN Process Technology

Process Technology

The devices that are measured and modeled in this section were fabricated on a commercial 0.15 μm GaN HEMT technology. The process includes two metal interconnect layers tantalum nitride, thin film resistors, epitaxial resistors, metal-insulator-metal capacitors and through substrate vias to the backside ground. The epitaxial layers are grown on a 100 μm SiC substrate. For typical DC device characteristics, the transconductance is 370 mS/mm at V_{DS} = 20 V with maximum output current density of 860 mA/mm. Typical the threshold voltage is -2 V and gate-drain junction breakdown voltage is 120 V. the transition frequency, f_T is 34.5 GHz and maximum stable gain at 10 GHz is 18 dB. The power density for this process is typically 3 W/mm at 29 GHz.

Small-Signal Measurement Details

A Keysight N5290A, 900 Hz to 110 GHz PNA mm-wave system is used to perform small-signal S-parameters measurements. The VNA is calibrated from 50 MHz to

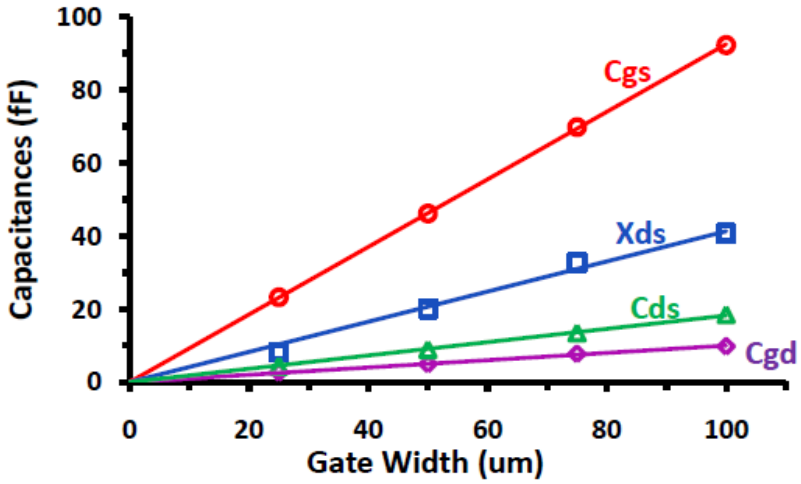


Figure 3.22: Extracted gate-source capacitance, C_{gs}, (circles, left axis), gate-drain capacitance, C_{gd}, (triangles, right), drain-source capacitance, C_{ds}, (diamonds, right), drain-source transcapacitance, X_{ds}, (squares, right) per finger for four HEMT widths. Lines show scaling.

50 GHz with 201 frequency points covering the frequency range in linear steps. Agilent E3646A and E3632A power supplies are used to supply the bias to the gate and drain of the DUT respectively, through the mm-wave head bias tees. A fine-step bias list file is created to control the SMU, with V_{DS} and V_{GS} swept from 0 to 28 V and -3 to +0.5 V respectively. On-wafer SOLT calibration method is used to accurately place the measurement reference planes at the DUT's input and output terminals. Keysight BenchVue software is used to automate the measurement.

Extraction of Access Resistance Values

The access resistances are initially estimated using the familiar cold-FET measurement procedure described in [67]. The values of these resistances are fine-tuned post-measurement to ensure minimal dispersion is observed in the extracted small-signal model parameters over the measured frequency range. Simultaneously, the two real terms; G_{gs} and G_{gd}, which are not included in the model formulation, are monitored across the measured frequency range. The terms, G_{gs} and G_{gd} arise from leakage through the gate junction and for an ideal intrinsic network, these terms are neglected as they are insignificant to the model accuracy for practical purposes. However, when

extracted, they are non-zero terms. This is another form of non-physical dispersion that arises from incorrect separation of the access network and the intrinsic model parameters.

Fine-tuning of the access resistances, and R_g in particular, are found to be effective in suppressing G_{gs} and G_{gd} and maintaining these values close to zero across the measurement frequency range. The final values for R_g, R_s and R_d obtained for 25, 50, 75 and 100 μm gate widths are shown in Fig. 3.23. Similarly, the access conductances, $(1/R_g)^2$, $(1/R_d)$ and $(1/R_d)$ are plotted in Fig. 3.24.

The square of the gate access conductance, R_g, is found to scale linearly with gate width, which reflects the distributed nature of the gate and the contribution of its end-effect. $(1/R_d)$ and $(1/R_g)^2$ scale linearly from 25 μm to 100 μm with zero offset, with the exception of $(1/R_s)$ which deviates from the linear fit at 25 μm gate width. The implication is that the scaling of the model to gate-widths of 25 μm and smaller may be inaccurate. This issue of imperfect scaling for R_s warrant further investigation, however, obtaining a perfect linear scaling of the access resistances at very short gate widths is of limited practical importance to most MMIC designs and not in the scope of this thesis. The effect of fine-tuning the access resistances; R_g, R_s and R_d on the extracted intrinsic small-signal terms is shown in Fig. 3.25.

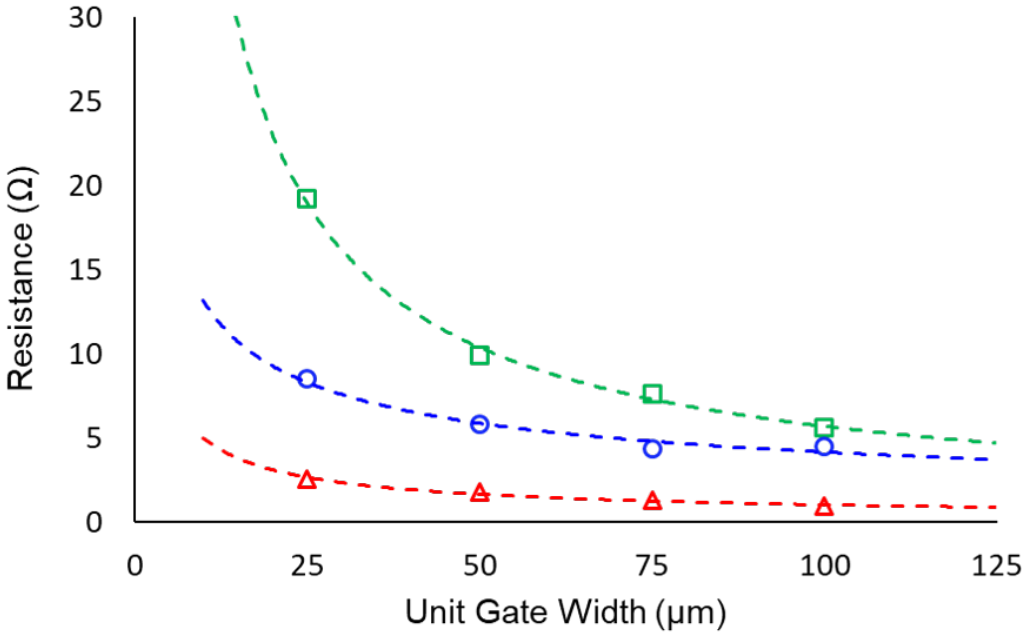


Figure 3.23: Access resistances, R_g (blue circles), R_s (red triangles) and R_d (green squares). Dashed lines are plotted as a guide.

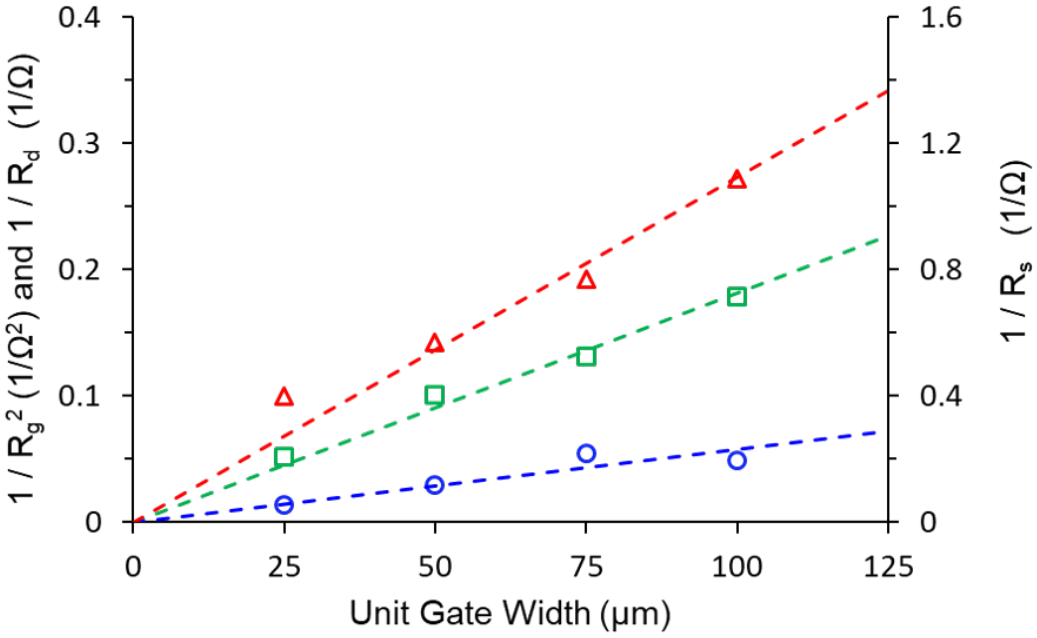
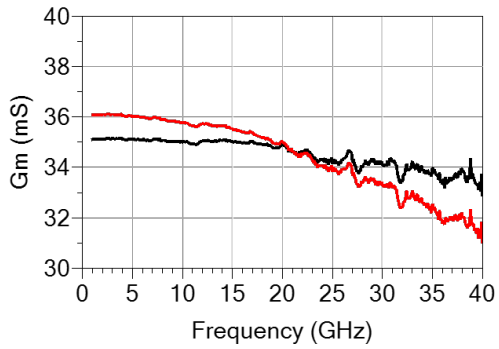
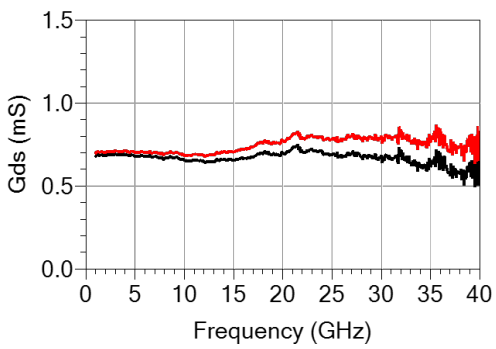


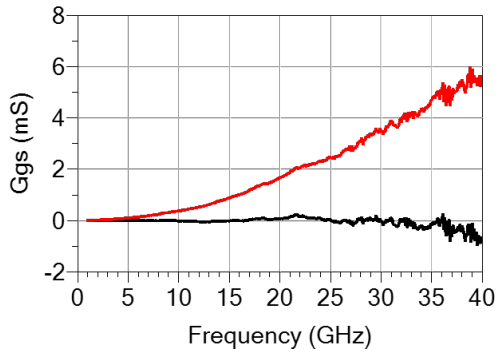
Figure 3.24: Access conductances, $1/R_g^2$ (blue circles), $1/R_s$ (red triangles) and $1/R_d$ (green squares). Dashed lines represent a linear fit to the data with zero offset.



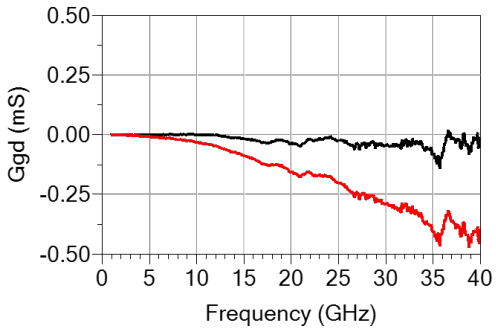
(a) G_m.



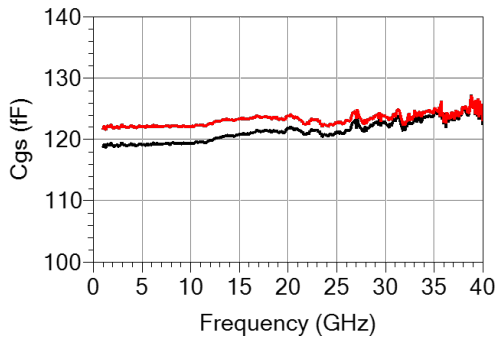
(b) G_{ds}.



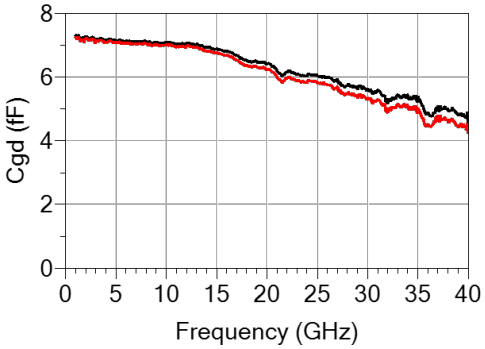
(c) G_{gs}.



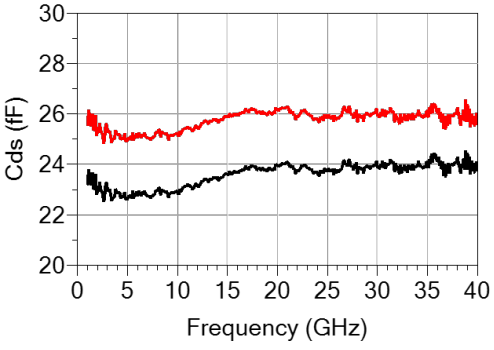
(d) G_{gd}.



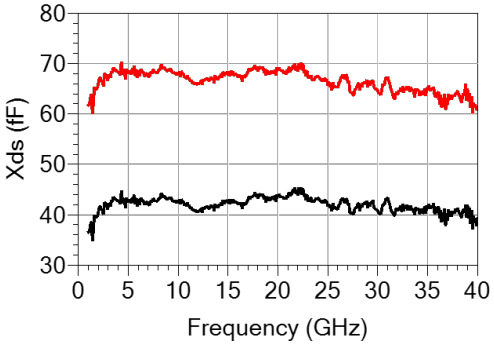
(e) C_{gs}.



(f) C_{gd}.



(g) C_{ds}.



(h) X_{ds}.

FIGURE 3.25: The extracted eight small-signal terms *without* tuning the cold-FET extracted access resistances (red) and *with* tuning the cold-FET extracted access resistances (black). The data shown is for 75 μm single-finger at V_{DS} = 20 V and V_{GS} = -1.5 V over frequencies from 1-40 GHz in 0.1 GHz steps.

EM Structure Setup

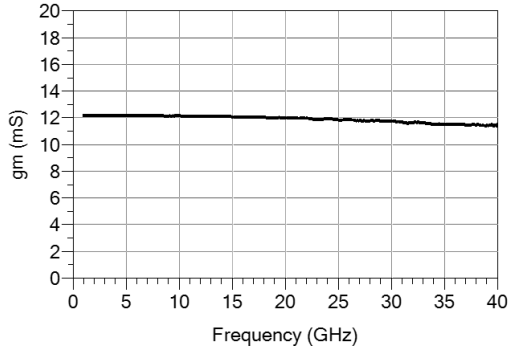
The EM model of a FET access metalisation is shown in Fig. 3.16, Fig. 3.17 and Fig. 3.18. The EM layout of the FET is an accurate representation of the measured device. The mesh density of the EM model is chosen to provide sufficient accuracy when modelling the smallest feature, i.e. the gate strip. The closed boundary of the Sonnet model is placed at least three times the substrate thickness away from any part of the analysed structure. This distance has been demonstrated to be adequate to make box wall coupling insignificant. In this case, ports 1 and 2 connect the extrinsic gate and drain of the FET to the Sonnet box through 50 Ω, 300 μm long microstrip lines. Sonnet automatically de-embeds these lines from the final simulation result. The EM structure is analysed at the same frequencies as the device measurements described earlier.

The Y_{int} matrix that results from the de-embedding of the extrinsic access network completely describes the intrinsic single finger of the FET. Using this matrix, alternative representations of the 3-port intrinsic network can be derived. For example, a common-gate representation can be derived by eliminating the row and the column that corresponds to the gate terminal in this matrix and similarly, a common-source representation network is achieved by by eliminating the row and the column that corresponds to the source terminal and so on for the common-drain. For familiarity, the common-source configuration is used to calculate the intrinsic parameters of the FET as described in section 3.3.2. The resultant 2×2 Y-parameters matrix can be precisely described by eight elements corresponding to four real and four imaginary parameters.

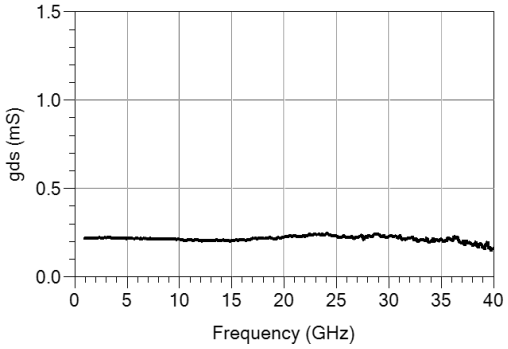
Extraction Verification

Dispersion-less Intrinsic Data

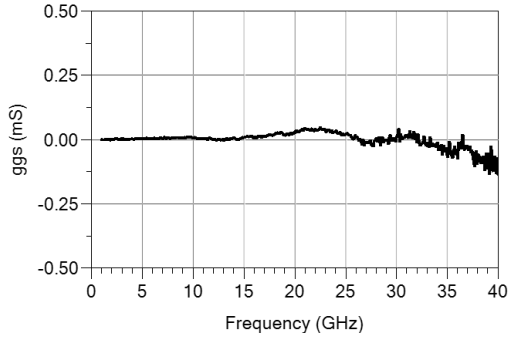
The extracted intrinsic model parameters scale linearly with device width, and at the same time provide good frequency-independent intrinsic model parameters as shown in Figures 3.26, 3.27 and 3.28 for 25, 50 and 75 μm intrinsic fingers respectively.



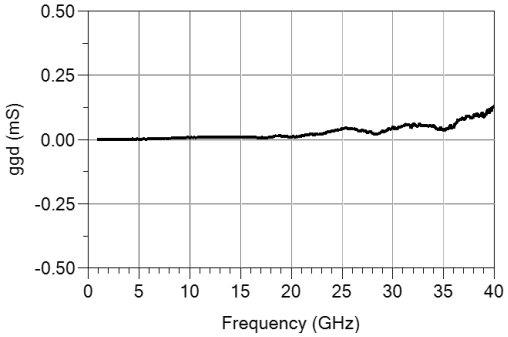
(a) G_m.



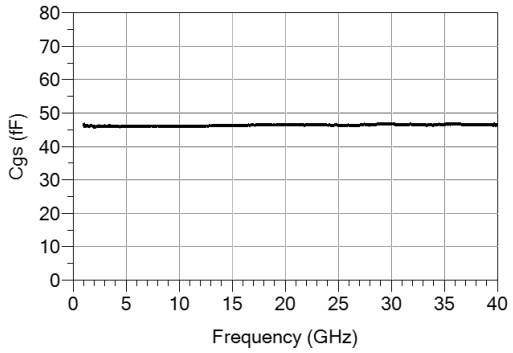
(b) G_{ds}.



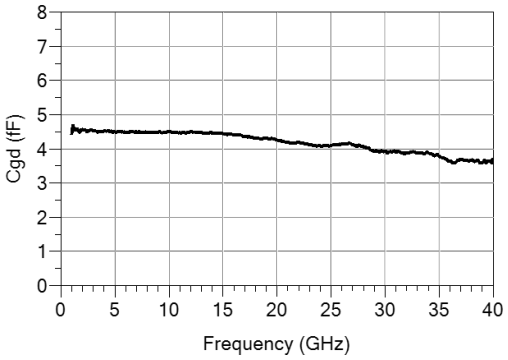
(c) G_{gs}.



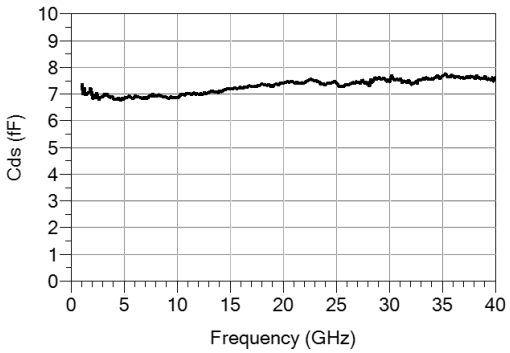
(d) G_{gd}.



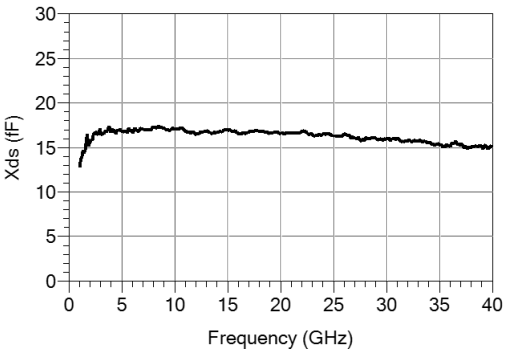
(e) C_{gs}.



(f) C_{gd}.

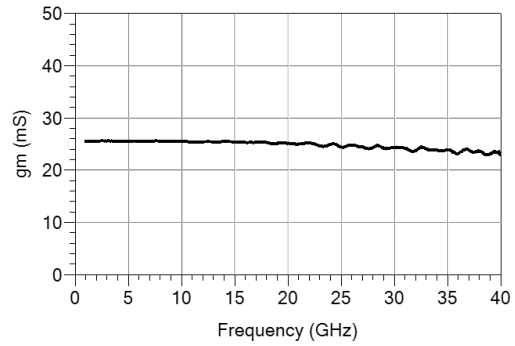


(g) C_{ds}.

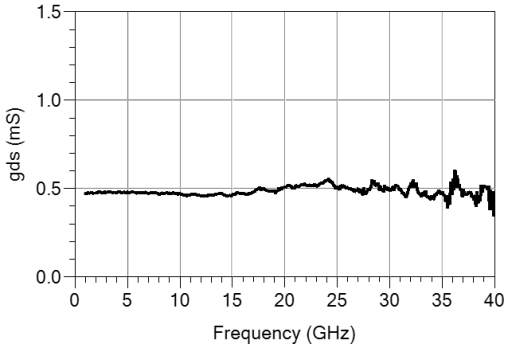


(h) X_{ds}.

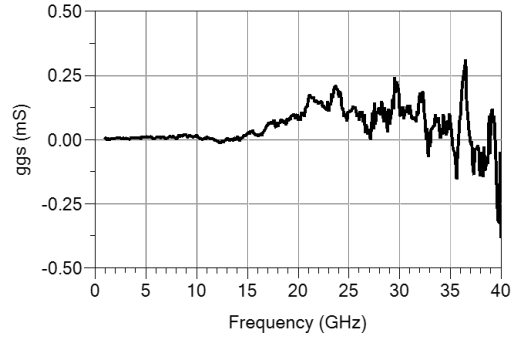
Figure 3.26: The extracted eight small-signal terms for the 25 μm single-finger linear model at V_{DS} = 20 V and V_{GS} = -1.5 V over frequencies from 1-40 GHz in 0.1 GHz steps.



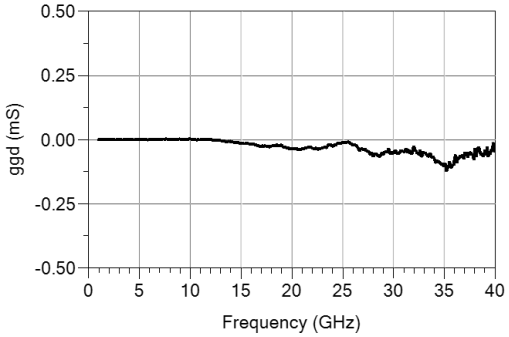
(a) G_m.



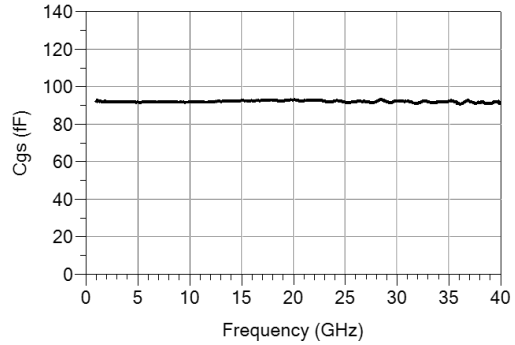
(b) G_{ds}.



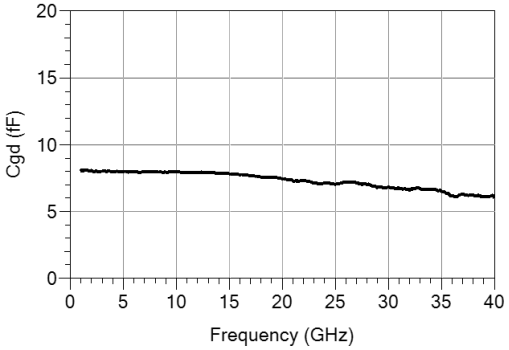
(c) G_{gs}.



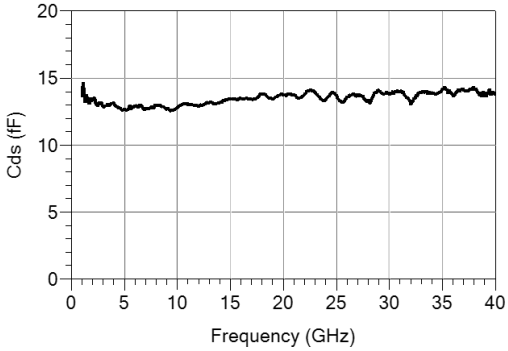
(d) G_{gd}.



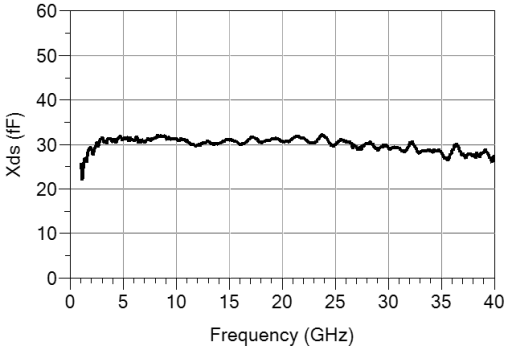
(e) C_{gs}.



(f) C_{gd}.

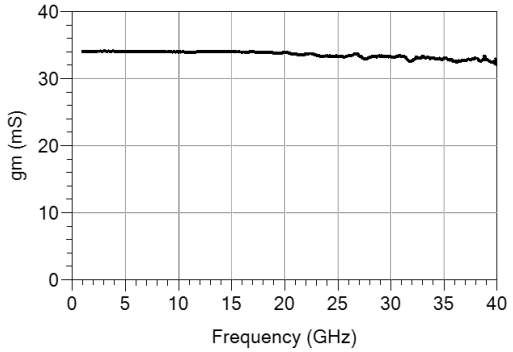


(g) C_{ds}.

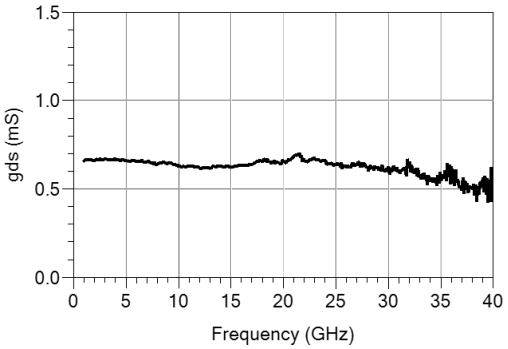


(h) X_{ds}.

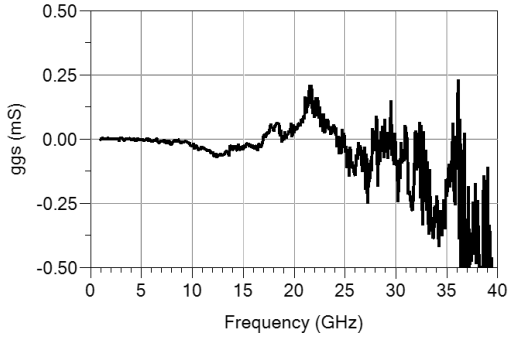
FIGURE 3.27: The extracted eight small-signal terms of the 50 μm single-finger at V_{DS} = 20 V and V_{GS} = -1.5 V over frequencies from 1-40 GHz in 0.1 GHz steps.



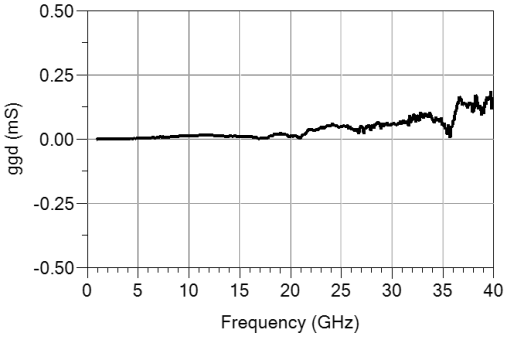
(a) G_m.



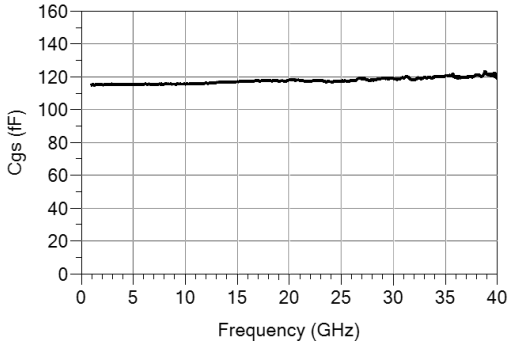
(b) G_{ds}.



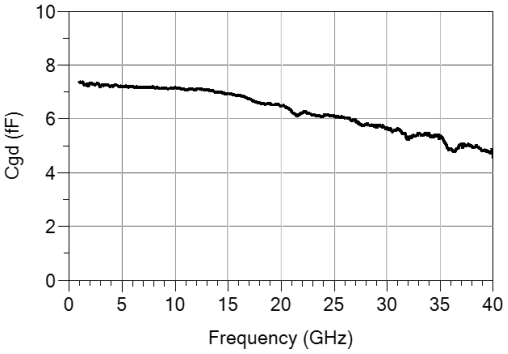
(c) G_{gs}.



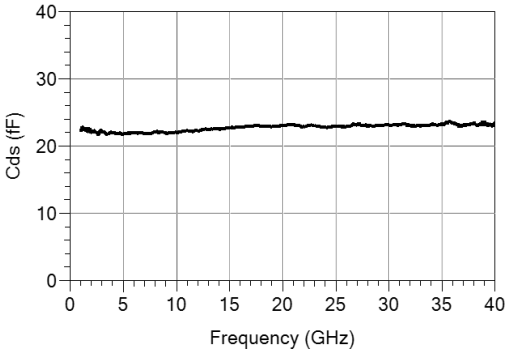
(d) G_{gd}.



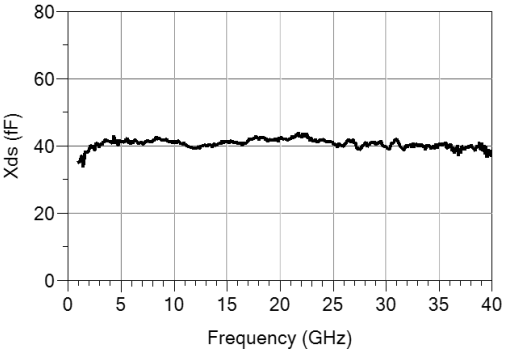
(e) C_{gs}.



(f) C_{gd}.



(g) C_{ds}.



(h) X_{ds}.

Figure 3.28: The extracted eight small-signal terms of the 75 μm single-finger at V_{DS} = 20 V and V_{GS} = -1.5 V over frequencies from 1-40 GHz in 0.1 GHz steps.

Scaling Intrinsic Data

The six intrinsic model parameters are plotted against the unit gate width. They scale linearly with the unit gate width of the FET, intersecting the Y-axis very close to zero unit gate width, indicating physical accuracy of the model formulation as shown in Fig. 3.29 and Fig. 3.30.

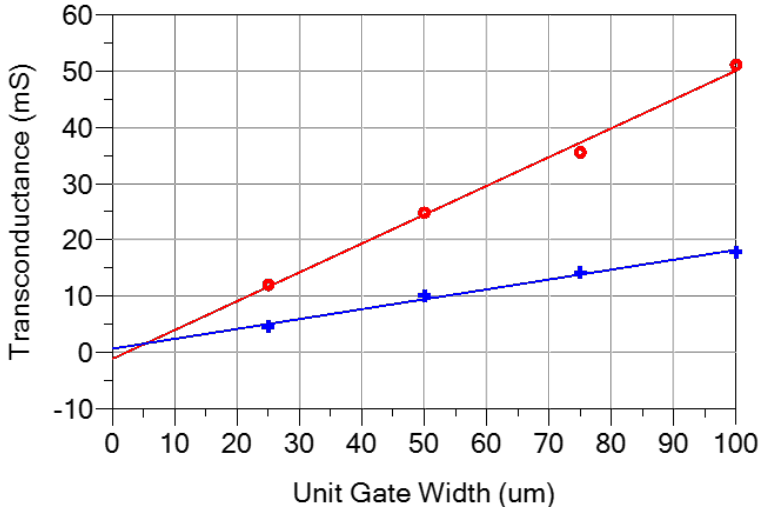


Figure 3.29: Extracted transconductance g_m (red) and output conductance g_{ds} (blue) per finger for four GaN HEMT widths. Solid lines show scaling fit.

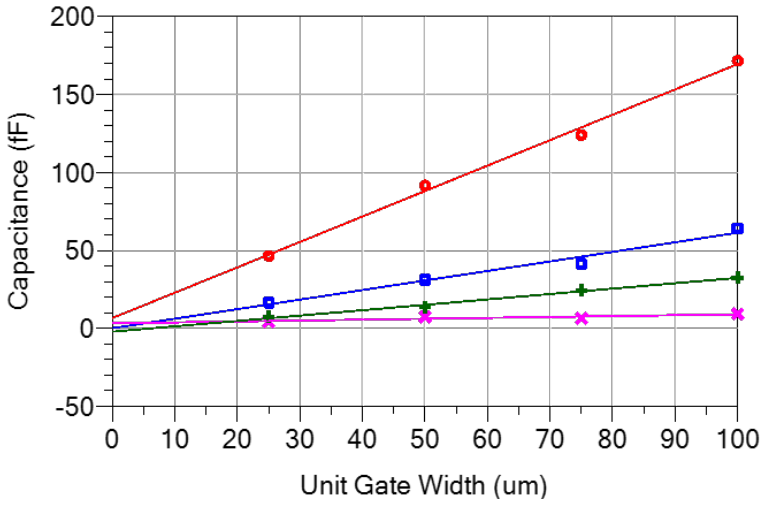


Figure 3.30: Extracted gate-source capacitance C_{gs} (red), gate-drain capacitance C_{gd} (magenta), drain-source capacitance C_{ds} (green) and drain-source transcapacitance X_{ds} (blue) per finger for four GaN HEMT widths. Solid lines show scaling fit.

The intrinsic model parameters are obtained in the previous section demonstrating a successful separation of the intrinsic core parameters from the access network. This is apparent from the linear scalability of the intrinsic model parameters with respect to the unit gate width, and also the near-zero intercept at zero unit gate width for each parameter. This implies a scalable core linear model is obtained which can be used to synthesise any arbitrary device and predict its small-signal performance. Fig.3.31 illustrates how the core model is electrically connected to EM metalisation in the schematic. Fig. 3.32 compares the simulated and the measured small-signal performance of 2×25, 2×50, 2×75 and 2×100 μm devices and showing excellent agreement between measured and predicted performance. Scaling the number of fingers of the devices, the model also exhibits a very good agreement with the measurements as shown in Fig. 3.33

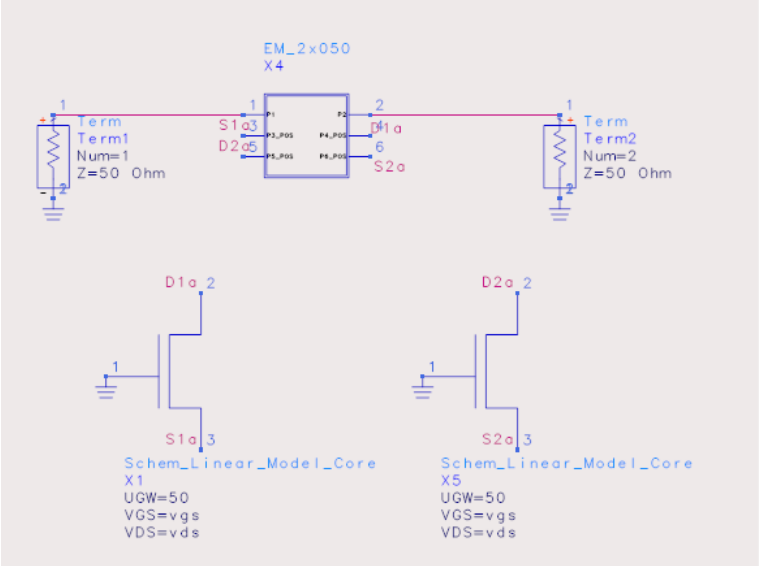
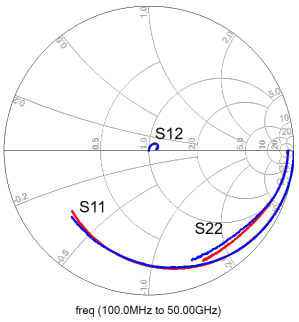
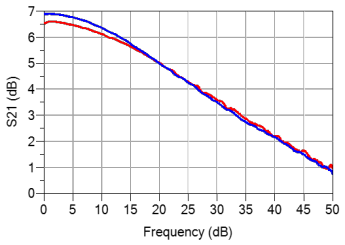


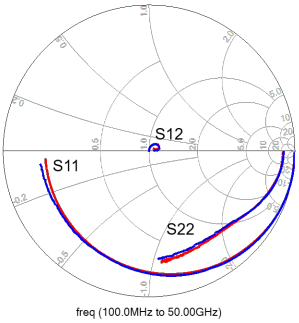
FIGURE 3.31: A schematic of a complete 2×50 μm showing the lumped-element thermal model connection to the thermal node of the model.



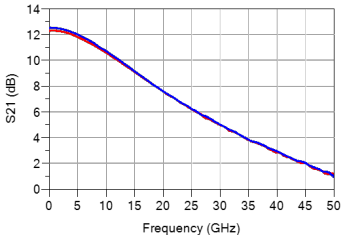
(a) 2×25 μm, S_{11}, S_{12}, S_{22}.



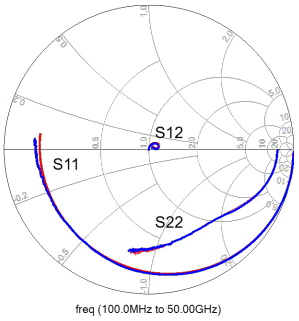
(b) 2×25 μm, S_{21}.



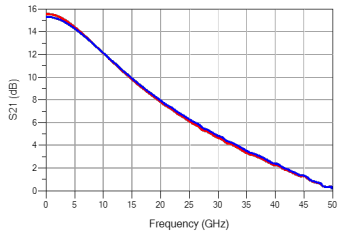
(c) 2×50 μm, S_{11}, S_{12}, S_{22}.



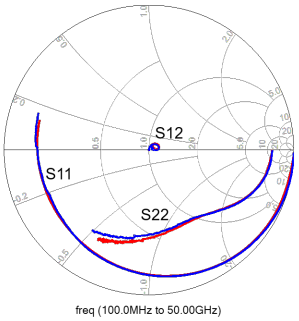
(d) 2×50 μm, S_{21}.



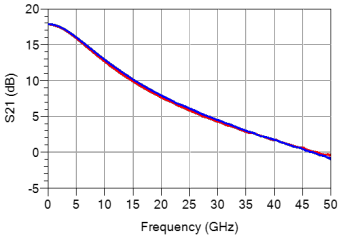
(e) 2×75 μm, S_{11}, S_{12}, S_{22}.



(f) 2×75 μm, S_{21}.

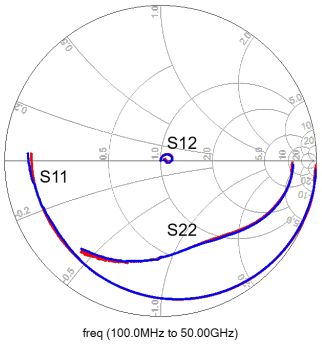


(g) 2×100 μm, S_{11}, S_{12}, S_{22}.

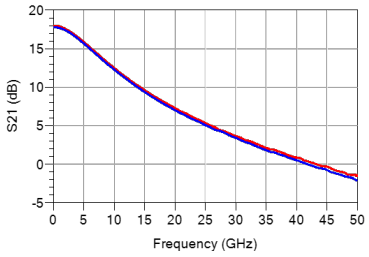


(h) 2×100 μm, S_{21}.

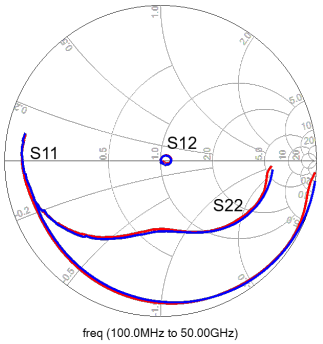
Figure 3.32: Modelled (blue) and measured (red) S-parameters performance from top to bottom for 2×25, 2×50 , 2×75 and 2×100 μm devices at V_{DS} = 20 V and V_{GS} = -1.5 V over frequencies from 1-50 GHz in 0.1 GHz steps.



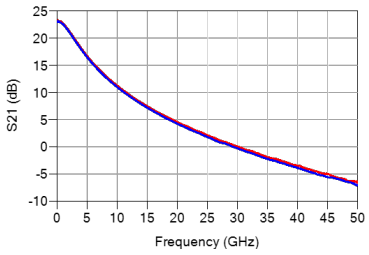
(a) 4×50 μm, S_{11}, S_{12}, S_{22}.



(b) 4×50 μm, S_{21}.



(c) 8×100 μm, S_{11}, S_{12}, S_{22}.



(d) 8×100 μm, S_{21}.

FIGURE 3.33: Modelled (blue) and measured (red) S-parameters performance from top to bottom for 4×50 μm and 8×50 μm devices at $V_{DS} = 20$ V and $V_{GS} = -1.5$ V over frequencies from 1-50 GHz in 0.1 GHz steps.

3.5 Summary

A rigorous method for the extraction of true intrinsic core-model parameters is described in this chapter. The resulting model exhibits linear scaling properties and the element values are dispersionless, so can be reliably used to extrapolate beyond measured data in terms of gate width and frequency. The intrinsic model parameters are not only bias-dependent, but they also depend on the temperature and the trap state during the measurement.

Small-signal models are convenient to use with of any simulator tool and enable very fast simulations. Linear models can be sufficient for the design of LNAs and even power amplifiers if the optimum load impedance is determined beforehand using

load-pull measurements or large-signal simulations of the unit cell device. However, extracted small-signal parameters give no insight into the dynamic behavior of a device, in other words, trap and thermal states. These dynamic effects are buried inside the small-signal data and cannot be separated. This limits the use of the small-signal models to steady-state applications at the bias they were extracted from.

A large signal model can describe the dynamic thermal effects and charge trapping on device operation. A large signal model can be extracted in a similar way to a small signal model. However, before an extraction of the core nonlinear model parameters can be attempted, the thermal and trapping states need to be determined. In the next two chapters, these dynamic effects are addressed, characterised and modelled in order to facilitate the fitting of the large-signal model.

4

Thermal Modelling and Model Implementation

A finite-element thermal model is presented as a tool to investigate the effects of self-heating on electrical performance and reliability. This model is implemented in SPICE so that it can be simplified and integrated into electrical design tools, enabling more accurate electrothermal simulations. The thermal resistance paths through the transistor are modeled using resistors, by considering the analogy between the flow of the heat and electric current. Nonlinear temperature-dependent thermal conductivity is implemented by representing the resistances as non-linear voltage controlled current sources. The model is able to predict the temperatures at any element of the transistor structure and can predict the radius of heat flow beyond the transistor layout. The model is calibrated and verified using gate resistance thermometry (GRT). It is then

scaled back to a convenient single-finger lumped-element thermal model that is used as a building block of arbitrary multifinger thermal network. The model is integrated into a microwave circuit design suite.

A 2D thermal model is developed, to be used together with the MQFET model that allows for electrothermal and dynamic simulation. A 3D thermal model is also developed to analyse the limitations of the 2D thermal model developed earlier. The 3D thermal model is then validated with a commercial FEM thermal simulator (Symmic).

In this chapter, the definition of local thermal state is presented in section 1. A thermal finite-element model and its SPICE implementation are presented in sections 2 and 3. The model is then calibrated and used to formulate a simple lumped-element thermal model.

4.1 Global and Local Thermal State

High power GaN HEMT devices usually have multiple gate fingers to boost the output power capability, and these fingers have a certain width which is ideally optimised for the frequency of interest. The summation of all gate widths is referred to as device periphery which is usually given in millimeter. The power capability of a process is defined as watts per millimeter (W/mm). This power capability is achieved when the device is appropriately matched for maximum power output and a general assumption is that all fingers are thermally and electrically identical. However, in practice, this simply does not happen due to reasons such as process variation, yield issues, sub-optimal matching to the gate fingers of the device due to combing loss and last but not least, the temperature variation amongst the different fingers. These factors result in different small and large-signal behaviour of individual gate fingers within a multifinger device.

For large-signal operation in particular, the temperature in each finger needs to be accurately modelled in order to assess its impact on the RF performance and the device reliability, the global temperature state for the whole multifinger device is simply not enough. In this chapter, the focus will be on understanding and modeling the heat-flow

Table 4.1: Analogy for equivalent thermal circuit.

Electrical Circuit	**Thermal Circuit**
Voltage (V)	Temperature (K)
Current (A)	Heat Flow (dissipated power) (W)
Electrical Conductivity $(A/m.V)$	Thermal conductivity $(W/m.K)$
Resistance (Ω)	Thermal Resistance (K/W)
Capacitance (F)	Thermal Capacitance (J/K)

in GaN HEMT multifinger devices.

4.2 Finite-element Model

A local thermal state is needed for each finger in a multifinger device. To model this state, a finite-element thermal model, that is able to capture the heat flow in the substrate as well as the mutual heating of adjacent gate fingers, is required.

The finite-element model developed, makes use of the popular analogy between the flow of electric current and heat by assigning voltage V as equivalent to temperature T, current to power dissipation, and electrical resistance r to thermal resistance R_{th}. Table 4.1 shows the analogy between electrical circuit and equivalent thermal circuit:

The value of the resistors used in the mesh network in Fig. 4.1 are defined as

in the x-direction

$$R_{th_x} = \rho \frac{\delta x}{\delta y \delta z}, \tag{4.1}$$

and similarly in y-direction

$$R_{th_y} = \rho \frac{\delta y}{\delta x \delta z}, \tag{4.2}$$

and in z-direction

$$R_{th_z} = \rho \frac{\delta z}{\delta x \delta y}. \tag{4.3}$$

ρ is the thermal resistivity the material. The capacitor, C, represents the thermal capacity of the 3D material volume shown in Fig. 4.1 and is defined as

$$C_{th} = c\rho\delta x\delta y\delta z. \tag{4.4}$$

where c is the heat capacity, and ρ (kg/m^3) is the density of the material.

For a multifinger transistor device, in order to accurately model the local thermal state, i.e., the finger temperature, a list of requirements are needed to be solved; the maximum or the average channel temperature of each finger, scale temperature correctly with dissipated power and ambient temperature (i.e., implement a non-linear temperature-dependent thermal conductivity), capture the mutual heating between the fingers (lateral heat-flow in the horizontal direction) and capture the heat flow in the vertical direction through the substrate stack-up, i.e., the heat flow from the channel to the epilayers through to the substrate and to the heat sink.

Solving for the temperature profile along each gate-finger is nice and could be very useful when performing failure analysis and identifying the exact point of failure in high power devices that are related to overheating. However, the scope of this thesis is limited to the formulation of a simplified lumped-element thermal network, which calculates a steady-state operating temperature to feed back to an electrical nonlinear model in a CAD simulator. The 2D electrical representation is shown in Fig. 4.2. In this case, δz in (4.1) to (4.4) becomes one where the third dimension that represents the width of the gate-finger is assumed to be infinite.

The two dimensions that are considered and modeled are; the x-dimensions which

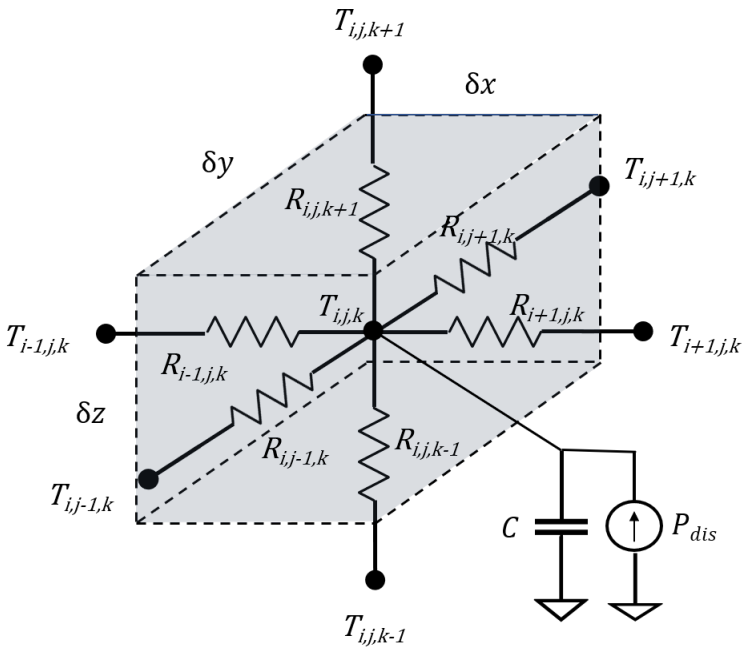


Figure 4.1: 3D representation of the SPICE finite-element thermal model. C represents the heat capacity of the volume highlighted.

represents the lateral heat flow between the gate-fingers of a device, and the y-dimension, which represents the heat flow through the substrate as illustrated in Fig. 4.2.

Fig. 4.3 shows the 2D model cross-section containing the channel region. where R_{th_x} is the thermal resistance that describes heat flow in the x-direction. δ_x and δ_y are chosen to provide sufficient spatial resolution without compromising simulation speed. Materials are treated as isotropic, however anisotropy can be implemented by specifying different thermal resistance values for x and y-direction. The full model includes the device substrate, epilayers and gate/source/drain metallization. Source vias, passivation layers, interfacial layers, air bridges and die-attach may also be incorporated.

The model is applicable to devices of any material system provided that the important thermal regions/parameters are modeled accurately. In GaAs devices, the epilayer region has been identified as the most-significant contributor to thermal resistance [82].

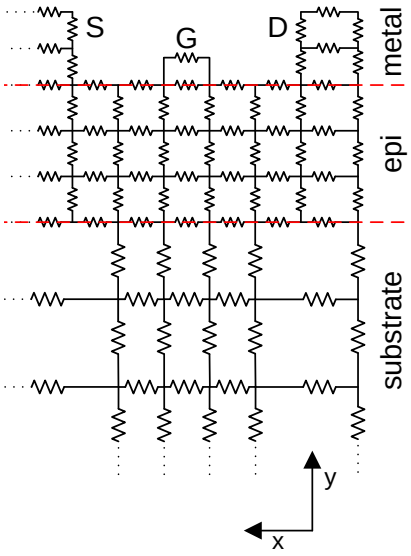


FIGURE 4.2: A simplified representation of the SPICE finite-element thermal model. Capacitors not shown here for simplicity.

4.3 SPICE Implementation

SPICE is a general purpose analog circuit simulator which is used to predict circuit behavior and to verify circuit designs. SPICE was originally used to develop integrated circuits by the Electronics Research Laboratory of the university of California, Berkeley (1975). SPICE program analyses circuits using a netlist-based description of the circuits' components.

The finite-element thermal model is implemented in SPICE. The advantages of using SPICE include the capability to perform both steady-state and transient simulations, open-source availability and the possibility of simplifying a dense mesh that represents the physical device to a lumped-element model. This model connects directly to the thermal node(s) of a nonlinear device model in any circuit simulator tool given that the model has an exposed thermal node. This also opens up the door to perform electrothermal simulations under RF input power drive which is very useful for studying the relationship between temperature and efficiency of each finger in a multifinger device.

The model takes advantage of device symmetry to reduce simulation time. The boundary conditions include an isothermal base plate, which is imposed using a dc

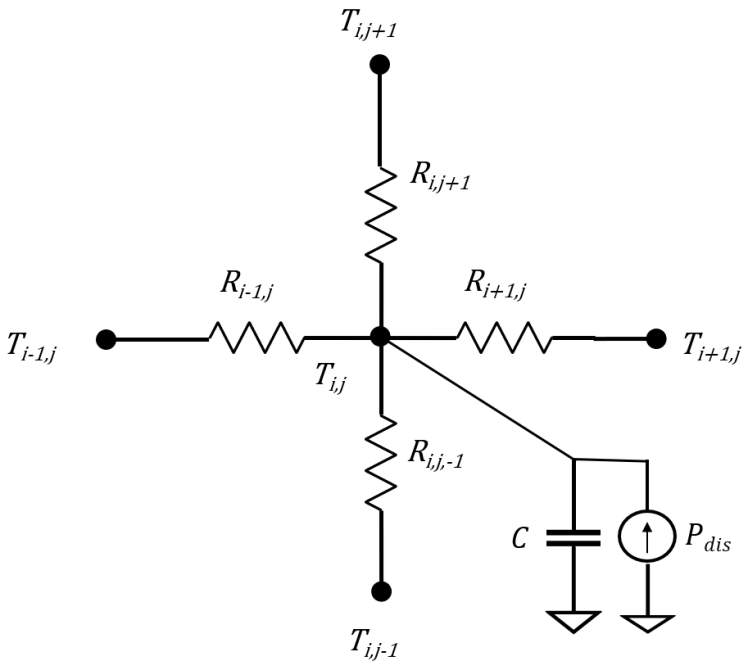


Figure 4.3: Simplified 2D representation of the SPICE finite-element thermal model. C represents the 2D heat capacity.

voltage source. All other surfaces are modeled as adiabatic.

Mesh density affects the simulated gate temperature and a reasonable mesh is chosen that enables an acceptable simulation time without compromising the accuracy of the results. A dense linear grid of resistors is used to achieve the precise epilayer thickness. The resistors defining the thickness through the substrate to the back-side heatsink are distributed logarithmically in space. This is reasonable since the thermal gradient in the substrate is low relative to the epilayer region. The SPICE netlist that describes the geometry and material composition of the transistor is generated via an AWK language script [83]. The AWK code is included in Appendix A.

The channel heat-source geometry has been demonstrated to affect operating temperature [82] [84]. The heat-source geometry in the SPICE model is defined by the grid size in the channel region, i.e. where the power is injected in the model.

TABLE 4.2: Semiconductor thermal parameters used in finite-element SPICE simulations [2]

Material	κ (W/mK)	α	Heat Capacity (J/kg.K)
GaN	150.0	0.49	490
AlGaN	25.0	0.43	490
SiC	450.0	1.49	670

4.3.1 Non-linear Temperature Dependent Thermal Resistance

Non-linear temperature-dependent thermal resistance is an important consideration for modeling self-heating. In semiconductors thermal resistance typically increases with temperature according to

$$R_{th}(T) = R_{th_0} \left(\frac{T}{300} \right)^{\alpha}, \tag{4.5}$$

where R_{th_0} is the thermal resistance at ambient temperature of 300 K, T is the local temperature and α is a material-dependent constant [85] [86].

An advantage of using SPICE is that each resistor in the mesh can be easily defined as a voltage-controlled current source. This makes it possible to apply a non-linear relationship between the current (power) flowing through each resistor (thermal resistance) and its terminal voltages (local temperature). Upon implementing (4.5) into SPICE, a resistor (r_x) between two nodes n and $n+1$ in the x-direction is defined as

$$r_x(V) = r_{x_0} \left(\frac{(V_{n+1} + V_n)/2}{300} \right)^{\alpha}, \tag{4.6}$$

The material thermal conductivity parameters used for the simulations is presented in Table 4.2 [2].

4.3.2 Heat Flow in the Third Dimension

The 2D model assumes the heat-source to be infinite in the third dimension (i.e. z-dimension along the gate finger). In order to model a finite gate width, one must account for the end effects that are associated with different gate widths. Fig. 4.4 shows the temperature profile across a 100 μm width finger simulated using the 3D SPICE finite-element thermal model. The 3D SPICE model is given in Appendix B and is used to simulate the temperature profile of a single gate-finger. The temperature is not constant across the finger and the edges are considerably cooler than the middle of the finger.

Accordingly, 3D simulations are performed to extract the channel temperature as a function of gate-finger width and substrate thickness. Fig. 4.5 shows that the maximum temperature rise is insignificant when the gate finger-width approaches five substrate thicknesses. This implies that when the gate-finger is significantly wider than the substrate thickness, i.e. 5×, most of the heat generated in that finger is flown vertically through the substrate which provides a much shorter path to the heat sink. The plateaued temperature value for each substrate thickness is considered to be the equivalent temperature rise of an infinite gate width.

Fig. 4.6 represents the normalised temperature rise values to the equivalent temperature rise of an infinite gate-finger width obtained from Fig. 4.5. Normalised temperature rise values in Fig. 4.6 are used to scale down the temperature rise for the finite gate-finger widths. SPICE model thermal simulations suggest that the normalised temperature values are almost independent of the substrate material used as shown in Fig. 4.7.

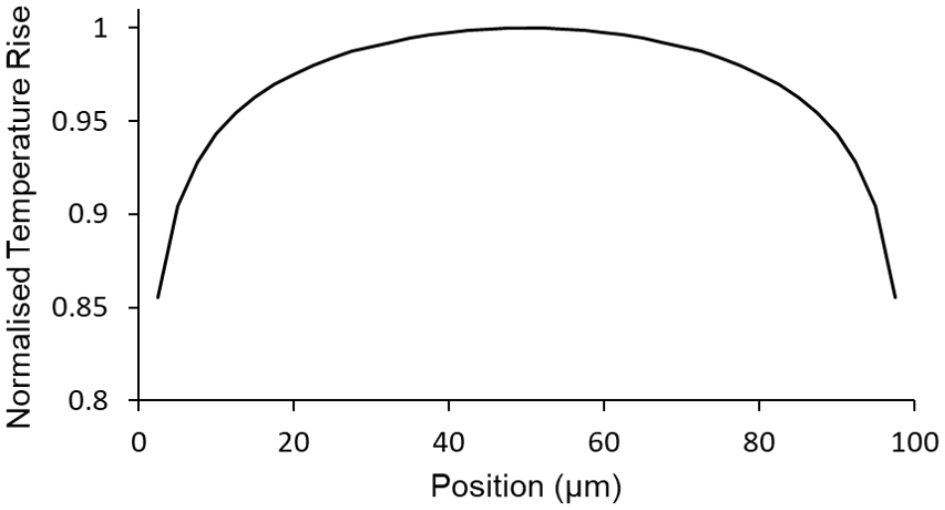


FIGURE 4.4: A normalised temperature rise in a 100 μm finger, simulated on a 100 μm SiC substrate using 3D SPICE implementation.

4.4 Application To GaN Technology

GaN HEMT devices are usually grown on foreign substrates such as Si, SiC and diamond and these substrates have excellent thermal conductivity. However, this results in introducing an interface layer which causes a temperature discontinuity when heat is conducted across an interface between two different materials and the thermal effect of this interface layer is called the thermal-boundary resistance (TBR). GaN transistors have high-power dissipation and the effect of this TBR is undesirable because it leads to elevated channel temperatures which impacts the reliability and RF performance of GaN devices. In GaN on SiC devices the transition layer is often composed of AlN with a thickness on the order of 100 nm. A value of 3.3×10^{-8} $\mu m^2 K W^{-1}$[87] is used in the SPICE model for the TBR region.

Fig. 4.8 presents a typical GaN on SiC substrate stackup illustrating the position of the AIN layer that forms the TBR interface layer. It is obvious that the distance between the TBR layer and the heat source is very crucial to near-junction thermal management and therefore, the GaN buffer layer may be optimised for a trade-off between electrical and thermal performance. [88].

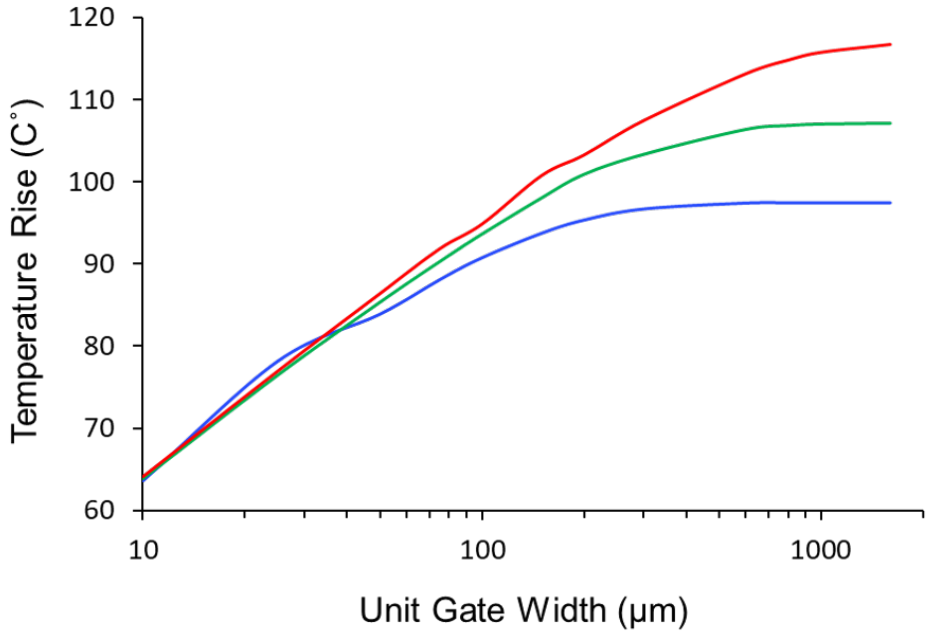


Figure 4.5: Peak temperature rise with respect to gate finger width, for various substrate thicknesses; 35 (blue), 75 (green) and 150 μm (red). A 100 μm SiC substrate is used with power dissipation of 5.2 W/mm and ambient temperature is 27°C.

The SPICE thermal modeling described in the previous section of this chapter is used to predict and model the thermal behavior for the high power GaN on SiC process of interest. The same GaN process used in the previous Chapter 3 is used in the following sections. See page 54 in Chapter 3 for the GaN process details.

4.4.1 Thermal Extraction

The same AWK script that was built previously is used for the new process. The script is generic and flexible where all of the important details of the substrate and the process including substrate thickness, "H", number of fingers, "numfing", gate-to-gate spacing, "G2G", dissipated power, "PWR_mm" and backside temperature, "va_K", are defined as variables where users have the choice to change the value of any variable when they run the script such as

awk [-v] [H=100] [-v] [numfing=6] [-v] [G2G=33] [-v] [PWR_mm=5.2] [-v] [va_K=300] -f thermal_script.awk

The line command above shows how the AWK script is run in the command line.

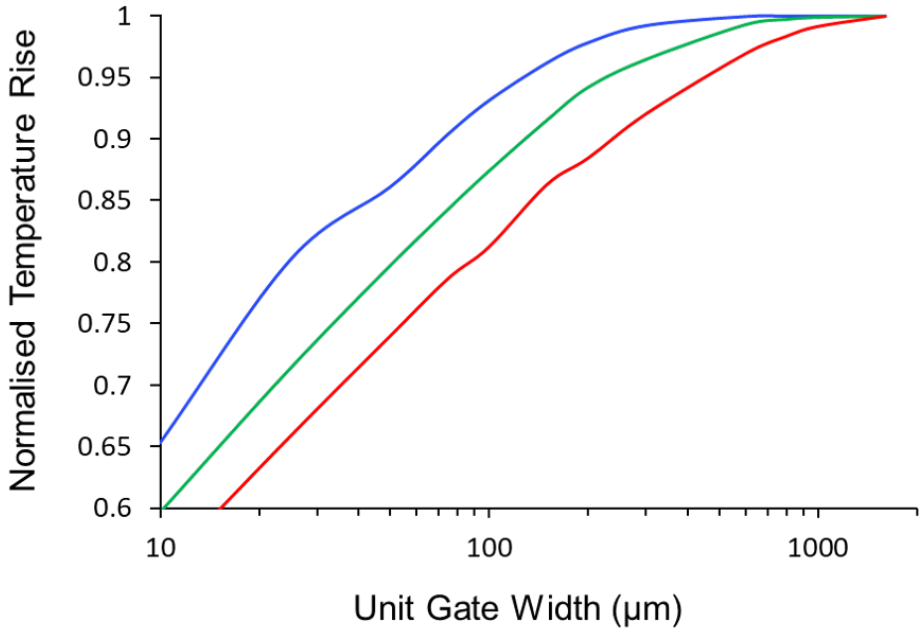


FIGURE 4.6: A normalised temperature rise (peak) with respect to gate finger width, for various substrate thicknesses; 35 (blue), 75 (green) and 150 μm (red). Such data is used to account for the finite gate finger width. A 100 μm SiC substrate is used with power dissipation of 5.2 W/mm and ambient temperature is 27°C.

The "awk" is required to run AWK script in Linux and "gawk" may be used in Windows. The [-v] is used when a variable is to be passed on to the script in the following argument, for instance, [H=100], is used as the first passed on variable, where "H" is a variable that is defined in the AWK scrip and is given a value of "100". Similarly, "numfing", "G2G" and "PWR_mm" and "va_K" values are entered. The "-f" argument is entered when a file gets passed in the following argument, and in this case this file is the AWK script that is used to generate the SPICE netlist file ".cir". Arguments between brackets are not mandatory fields in the command line and if they are omitted, default values defined in the AWK scrip will be used instead. The SPICE netlist generated by the AWK script can have as many as hundreds of thousands of lines depending on the geometry of the modelled device.

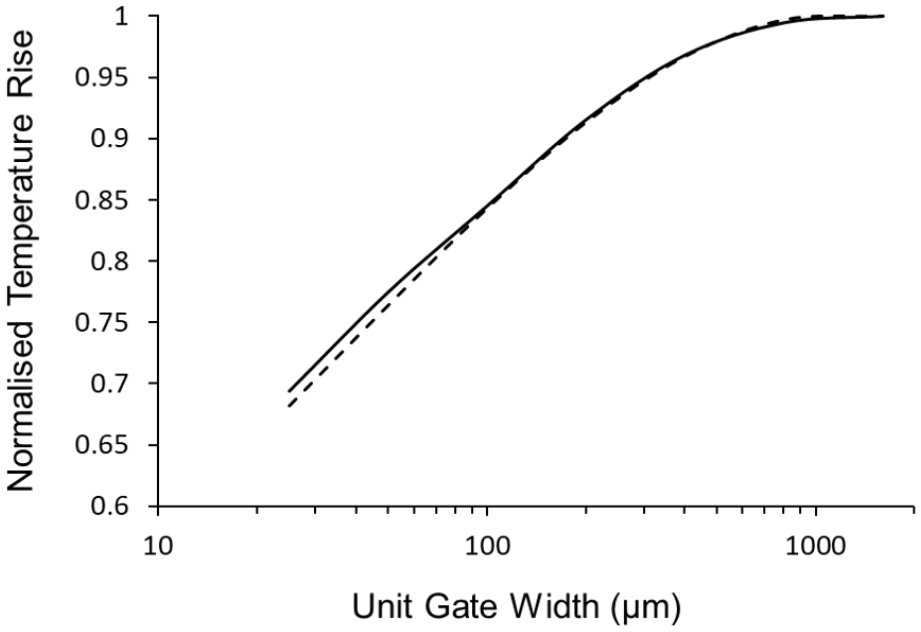


Figure 4.7: A normalised temperature rise (peak) with respect to gate finger width, for GaAs (dashed line) and SiC (solid line) substrates. Substrate thickness is 100 μm and ambient temperature is 85°C. Power dissipation of 0.52 W/mm and 5.2 W/mm are used for GaAs and SiC respectively.

4.5 SPICE Simulation Results

4.5.1 Model Calibration and Verification

The lumped-element SPICE thermal model developed in the previous sections needs to be calibrated and verified against a standard technique used by semiconductor industry. Default model parameters that are sourced from the literature including; material thermal conductivity values, epilayer thickness, TBR value and nonlinear temperature dependent coefficients for epilayers and substrate are kept the same. In addition, a scaling parameter, β, is introduced to (4.6) to account for the heat-flow in third dimension.

$$r_x(V) = \beta r_{x_0} \left(\frac{(V_{n+1} + V_n)/2}{300} \right)^{\alpha}, \tag{4.7}$$

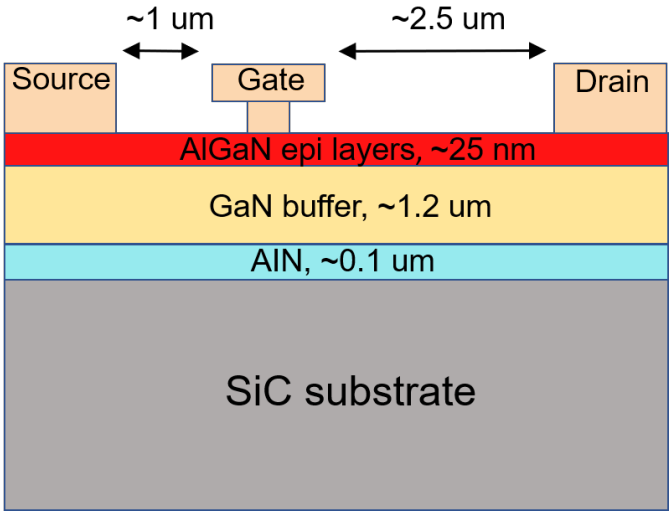


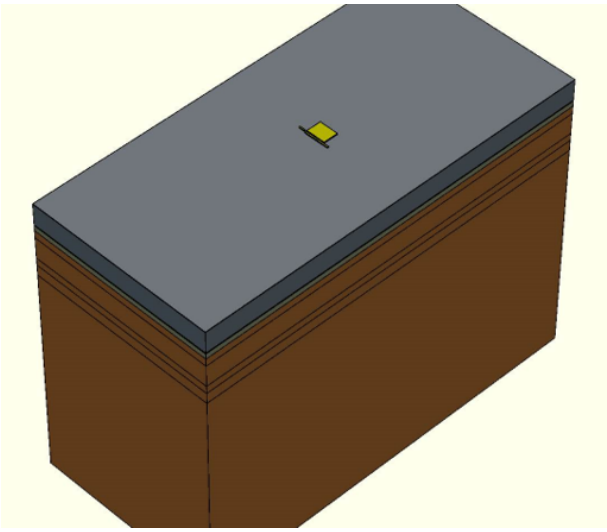
FIGURE 4.8: A basic example of GaN on SiC structure.

β is the scaling factor, where $0 \leq \beta \leq 1$.

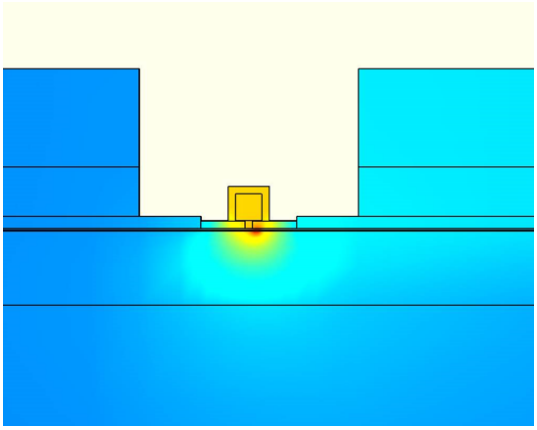
This implies that the physical thermal effects are correctly captured and the full functionality of the non-linear temperature dependent thermal resistivity is preserved: The heat-source dimensions, i.e. the grid size in the channel region, is adjusted in order to obtain simulation results to match the measurements. The heat-source geometry is held constant at 0.25 μm $\times$ 0.05 μm, which is found to be a reasonable assumption since the thermal analyses are conducted on devices biased into deep saturation where the heat-source and gate geometries are comparable.

A SPICE model is generated for an outside-source via (OSV) 6-finger GaN device on a 100 μm SiC thick and simulated for different power dissipation values. GRT steady-state measurements [82] [89] [90] for the 6 $\times$50 μm device are obtained from the semiconductor foundry. The GRT measurements provided were performed on one of the innermost fingers of an OSV configuration.

SYMMIC full 3D thermal tool is used to assess the end-effect on both; maximum and average temperature rise along the gate-finger. A detailed gate structure is implemented in SYMMIC including the gate feed and gate tab in order to capture a more accurate heat distribution along the gate-finger as shown in Fig. 4.9.



(a)



(b) Cross-section of the transistor.

Figure 4.9: SYMMIC simulations for a 100 μm gate-finger.

Fig. 4.10 shows the normalised gate-junction temperature rise for both maximum and average cases for different gate-finger widths. The SYMMIC simulations show end-effects become significant on relatively small gate-finger widths. Results also show the temperature rise is independent of power dissipated under the gate-finger.

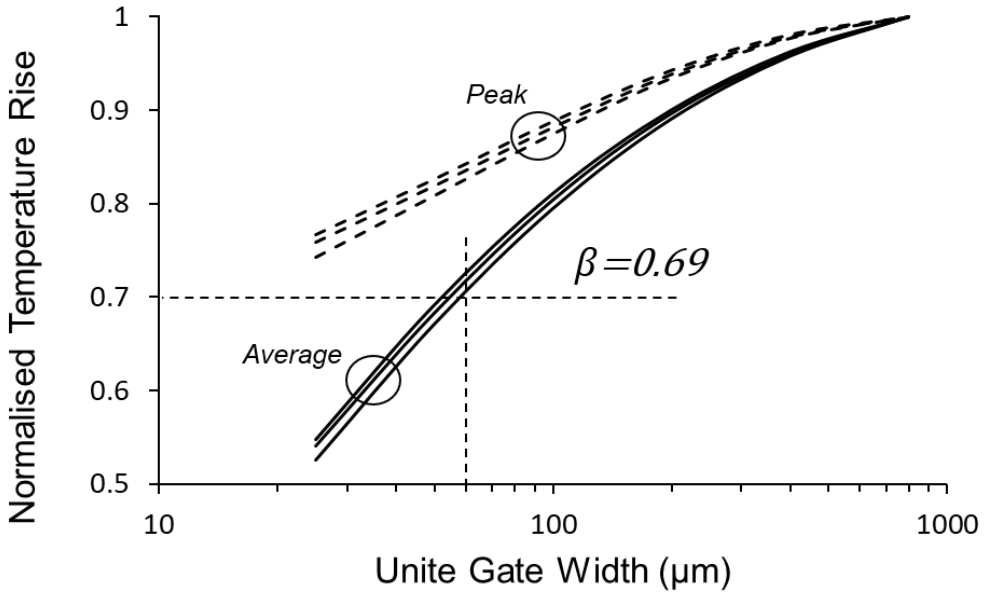


FIGURE 4.10: Simulated normalised maximum (dashed lines) and average (solid lines) gate-junction temperature rise versus gate-finger width. Three power densities, 0.5, 1 and 2 W/mm, are plotted for each case. The data shown is for a single gate-finger on a 100 μm GaAs substrate and 85 °C ambient temperature.

The GRT technique is based on measuring the change in the injected current into the gate metal due to the change in the temperature of the gate-junction. This means that the estimated temperature value by this technique represent the averaged temperatures along the gate-metal stripe. Hence, based on Fig. 4.10, a normalised avergae temperature rise value of "0.69" is used to calibrate the 2D SPICE model to the GRT measurements.

When $\beta = 1$, i.e. default values for model parameters are used, the temperatures are significantly overestimated by the model. The results are shown in Fig. 4.11. A very good agreement between modelled and measured temperatures is achieved when $\beta = 0.69$ is used as shown in Fig. 4.12. The model fits measured data at low power densities as well as at high power densities providing a good validation for the model. The scaling factor, β, in this case, represents a correction factor for the SPICE modelled temperatures which compensate for the unaccounted end-effects for finite gate-finger widths as illustrated in Figs. 4.5 and 4.10.

Fig. 4.12 also show the non-linear temperature dependent thermal resistivity effect

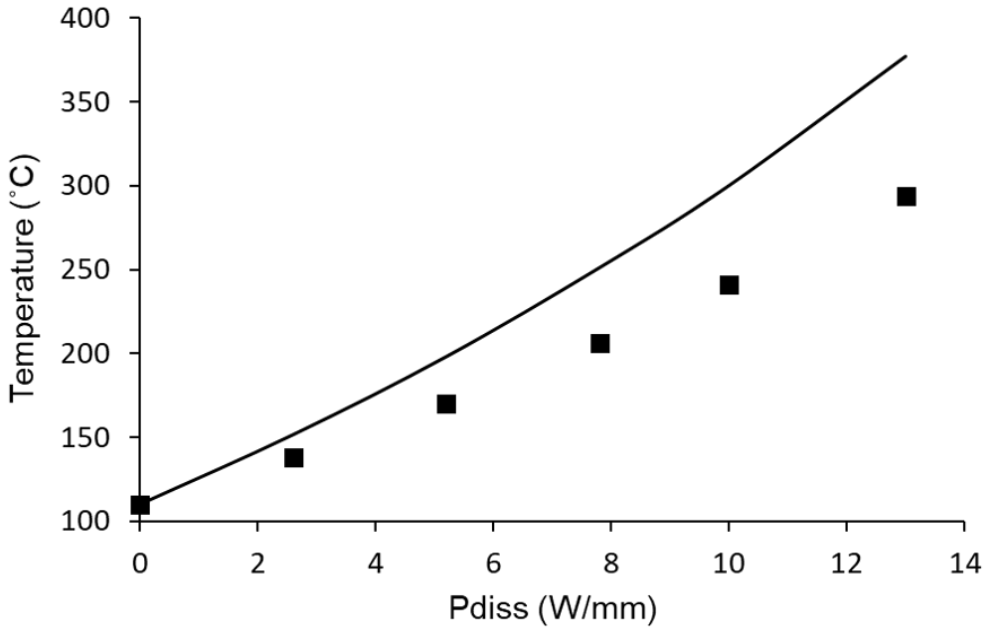


Figure 4.11: Gate junction temperature versus power density plotted for GRT measurements (squares) and SPICE model (solid line) with $\beta = 1$, i.e infinite gate-finger. The data shown is for a 6 $\times$50 μm OSV device on a 100 μm SiC substrate and 110 °C ambient temperature and 33 μm gate-to-gate spacing.

on the simulated temperatures of the SPICE model. When the non-linear temperature dependent thermal resistivity is ignored, the model is only able to predict the measured GRT data at a very low power densities, i.e., below 2 W/mm and the model deviates from the measured data quite rapidly at higher power densities. An error in the predicted temperature of more than 50°C can result at high power dissipation of 13 W/mm.

4.5.2 SPICE Model Results and Observations

A 6-finger device is extensively studied in this section where the SPICE thermal model is generated for different gate-to-gate spacings, substrates thicknesses, power dissipation, ambient temperatures. The SPICE models generated are executed for steady-states and transient solutions.

The effect of the thickness of the substrate on the temperature rise is stronger for

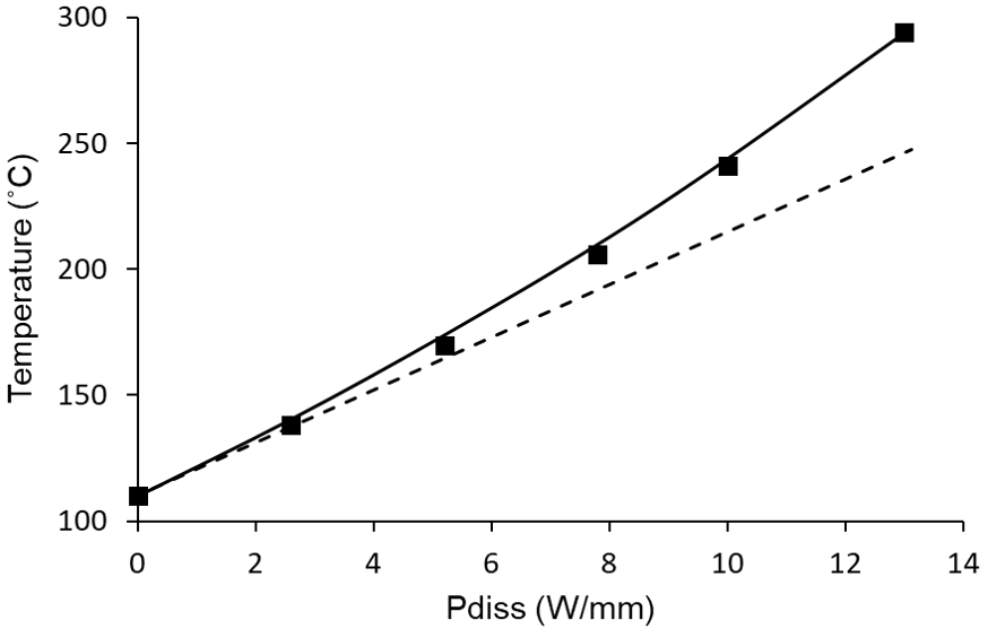


FIGURE 4.12: Gate junction temperature versus power density plotted for GRT measurements (squares) and SPICE model (solid line) with $\beta = 0.69$ which corresponds to 50 μm gate-finger. The data shown is for a for 6 $\times$50 μm OSV device on a 100 μm SiC substrate and 110 °C ambient temperature and 33 μm gate-to-gate spacing. The dashed line is the results of the SPICE model when the material temperature-dependent constants are set to zero.

bigger multifinger devices as shown in Fig. 4.13.

Fig. 4.14 shows the innermost finger temperature rise of a 6-finger device for different gate-to-gate spacings. The less the spacing between fingers is, the more temperature rise is expected due to stronger mutual heating between these fingers. The reduction in temperature rise becomes less of a strong function of gate-to-gate spacing beyond a substrate thickness, which is 100 μm in this case. The figure also suggests that gate-to-gate spacings effect on temperature rise becomes negligible beyond three substrates thicknesses.

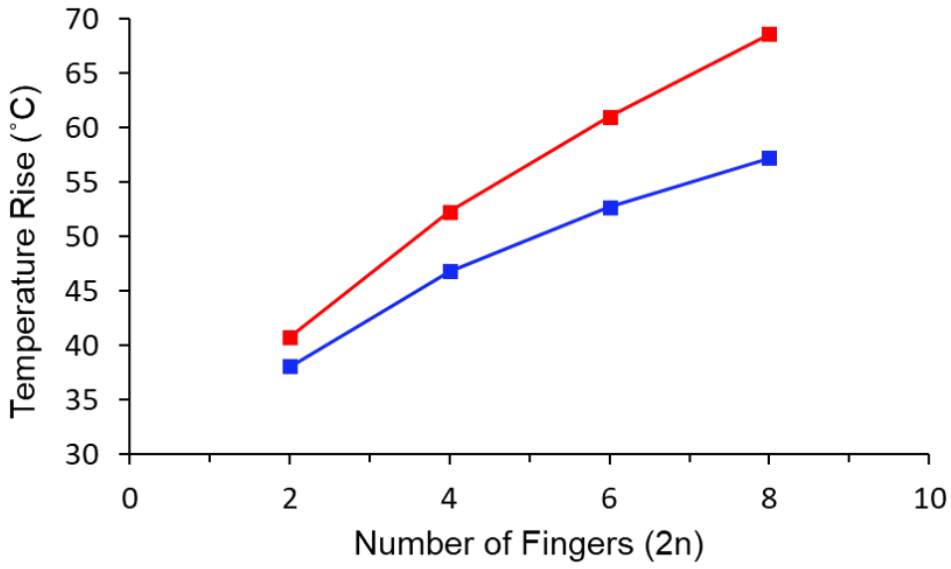


Figure 4.13: Substrate thickness effect on the temperature rise for different multifinger device sizes. Two SiC substrate thicknesses are shown; 50 μm (blue) and 100 μm (red) with 5.2 W/mm power dissipation and 110 °C ambient temperature.

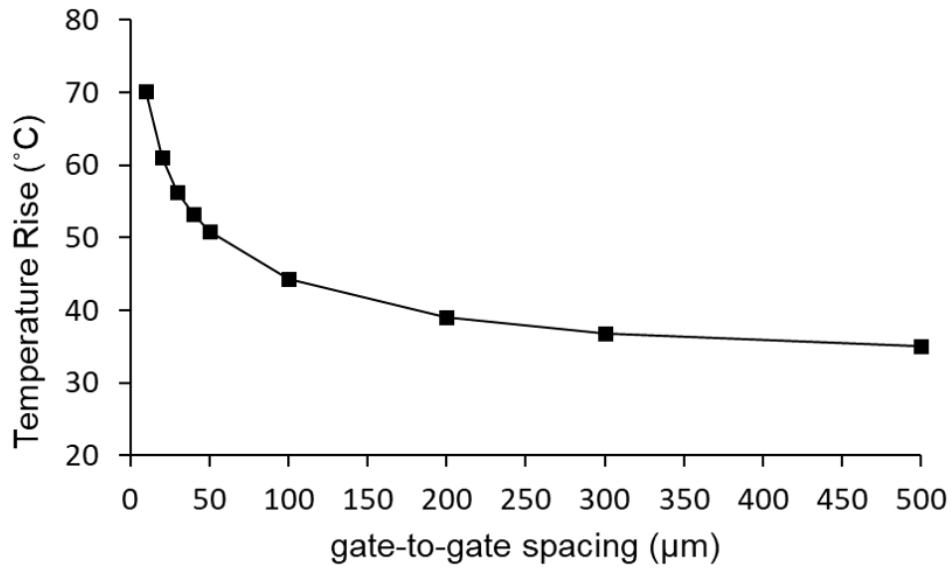


Figure 4.14: SPICE modeled temperature rise versus gate-to-gate spacing for a 6 $\times$50 μm device on 100 μm SiC substrate at 5.2 W/mm power dissipation and 110 °C ambient temperature.

Increased power densities leads to reduced uniformity of gate finger temperatures in

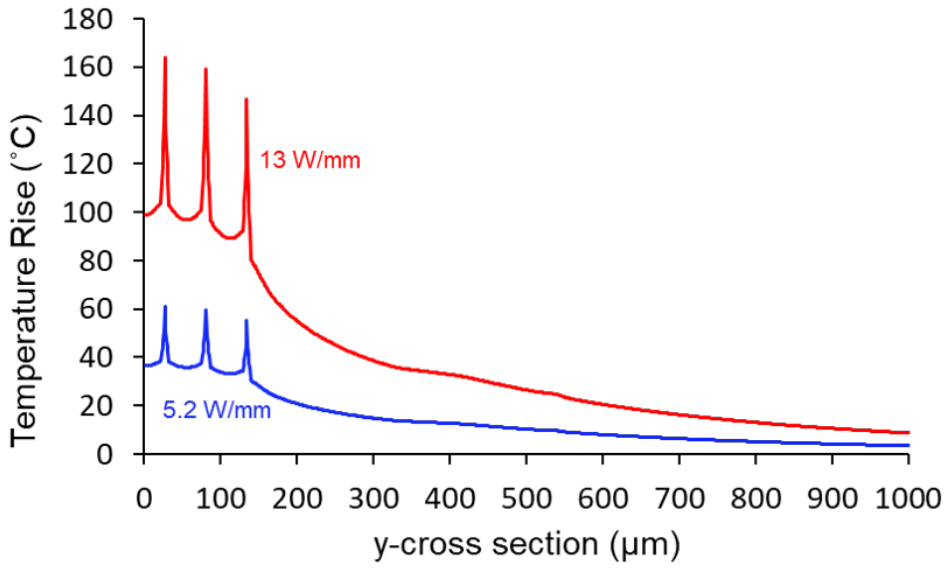


FIGURE 4.15: Channel temperature profile simulation of a 6 ×50 μm device for two different power densities for 100 μm SiC substrate and 110 °C ambient temperature.

a multfinger devices as shown in Fig. 4.15, where a significant difference in temperature-rise, of about 20 °C, is observed between the innermost and outermost fingers. Global temperature modelling of multifinger devices becomes insufficient in predicting the temperature rise in high power application circuits such as high power amplifiers, where the output stage can have several tens of gate fingers in parallel.

4.6 SPICE-based Gate-finger Lumped-element Model

In order to overcome the limitation of the global temperature node in multifinger devices, local thermal models are needed in order to capture the temperature rise in each finger and hence accurately predict the device's RF performance and reliability.

A lumped-element thermal model for a single gate-finger is developed. The model is considered a building unit that is used to construct any multifinger thermal network. The model fits in with the single-finger approach to the large-signal modelling that is discusses in Chapter 6.

4.6.1 Vertical Heat Flow

Transient thermal simulations help engineers understand how heat flows through a material stack-up. The transient temperature profiles taken at the channel of innermost finger, i.e., the hottest finger, for three different multifinger devices; 2-finger, 4-finger and 8-finger as shown in Fig. 4.16.

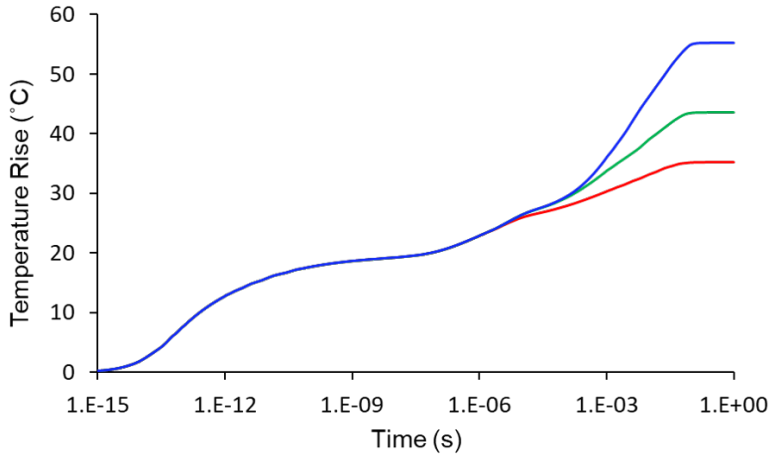


Figure 4.16: SPICE model's transient simulations for the innermost finger of 2-finger (red), 4-finger (green) and 8-finger (blue) devices. Simulations were performed at 5.2 W/mm power dissipation for 100 μm SiC substrate thickness with 20 μm gate-to-gate spacing and ambient temperature of 27 °C.

Temperature rise profile results capture three time constants which reflect the heat flow through the different materials in the stack-up. The first time constant is of the order of picoseconds and is attributed to the channel temperature rise, where the heat source is highly localised. The second time constant is due to the heat flow between the GaN buffer and the SiC substrate. The temperature rise in this region is influenced by the TBR. The third and the final time constant is due to the SiC substrate where the heat flows through the thickness of the substrate material and the time constant depends on the substrate material and its thickness and is found to be of the order of tens of milliseconds.

In practice, die attach and package layers also have significant effects on the steady-state temperature rise and transient profile. In high power GaN pulsed applications, circuits are more prone to thermally induced memory effects.

Fig. 4.17 results suggests that to construct the vertical thermal network, a minimum of three resistors are required in order to capture an accurate vertical heat flow through the substrate. The first resistor represents the temperature rise in the gate-junction, the second resistor represents the temperature rise at the interface between the GaN buffer layer and the TBR layer and the third resistor represents the temperature rise due to the SiC substrate. This vertical model represents an unmounted bare die device with an ideal heat sink and it is up to the MMIC designer to implement any die or package assembly arrangement or introduce any thermal resistance as backside boundary condition to capture effects of various assemblies.

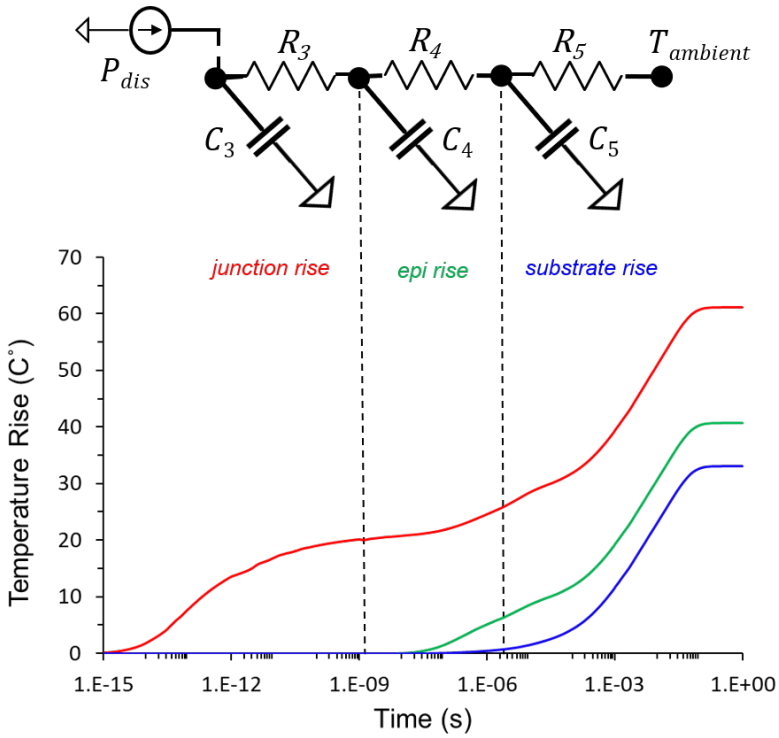


FIGURE 4.17: Lumped-element model vertical network formulation mapped to transient response of the finite-element SPICE thermal model at the different material interfaces. The junction/epi (red), GaN/TBR (green) and TBR/SiC (blue) interfaces. Simulations were performed on a 6-finger device at 5.2 W/mm power dissipation for 20 μm gate-to-gate spacing and 100 μm substrates thicknesses. Ambient temperature of 110 °C.

Fig. 4.18 shows that the first and second time constants are the same regardless of number of fingers or substrate thicknesses. Increased final steady-state temperature values and time constants are simulated for thicker substrates.

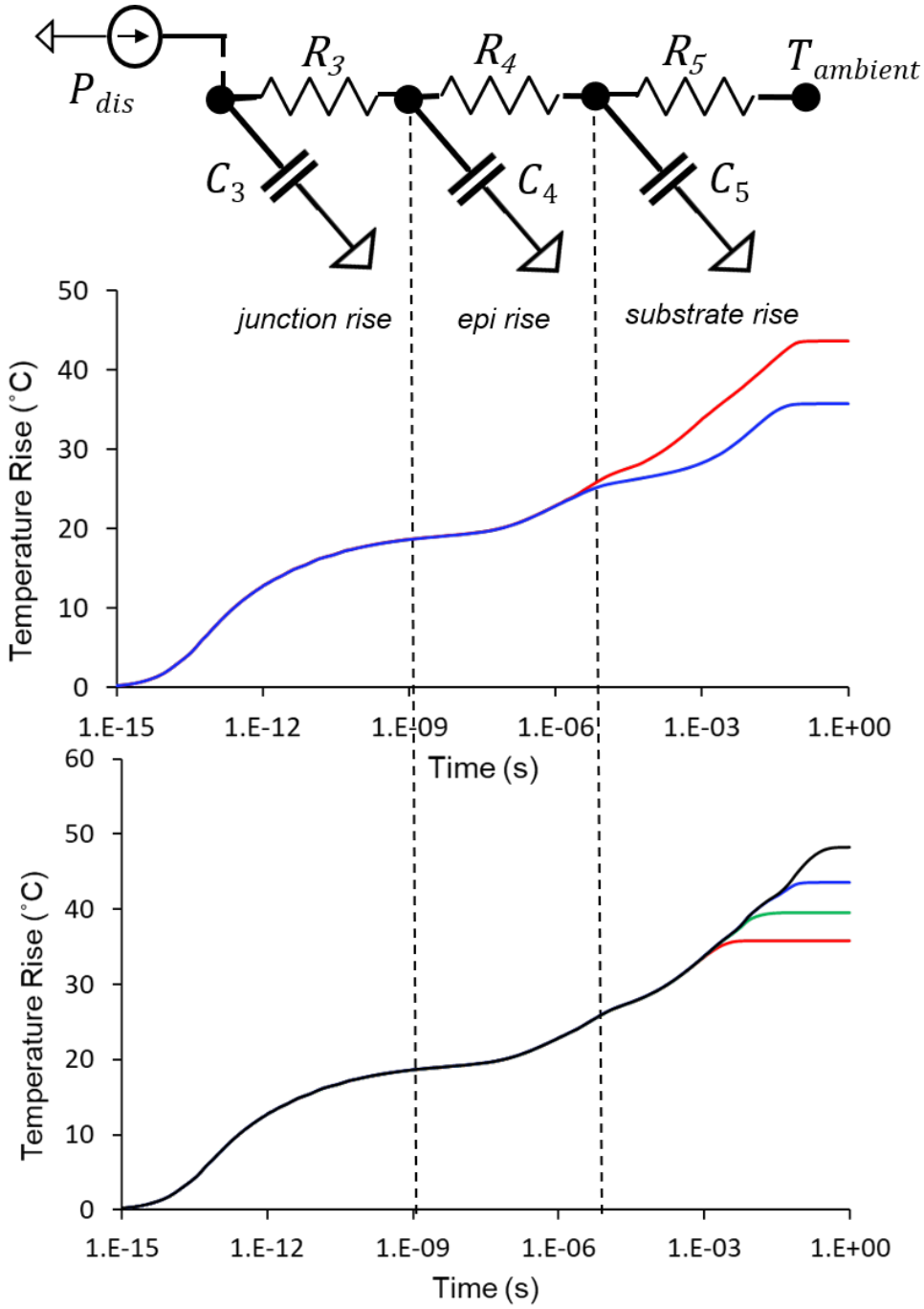


Figure 4.18: Lumped-element model vertical network formulation mapped to transient response of the finite-element SPICE thermal model. Simulations were performed on a 6-finger device at 5.2 W/mm power dissipation for 20 μm and 100 μm gate-to-gate spacing (top) and four different substrates thicknesses (25,50, 75 and 100 μm) (bottom). Ambient temperature of 27 °C.

For the purpose of this model, the interface thermal resistor and the substrate

resistor are combined and hence the number of resistors are reduced to two. Reducing the number of resistors from three to two is not found to affect the accuracy of the steady-state solution.The proposed vertical thermal network that is required to model the heat flow in the vertical dimension is shown Fig. 4.19.

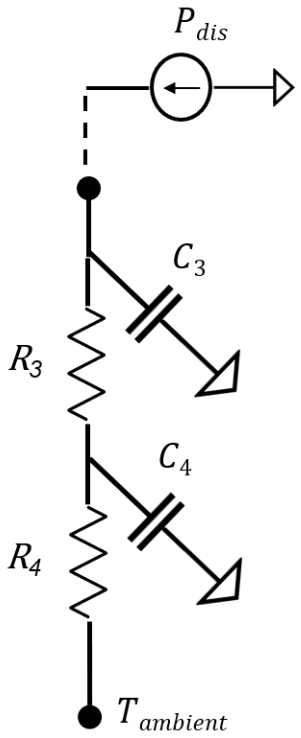


FIGURE 4.19: Lumped-element model minimum vertical network required.

4.6.2 Lateral Heat Flow

In a multifinger device, the vertical thermal ladder network is not enough to capture the temperature rise due to mutual heating between fingers where different fingers may be running at widely different temperatures which will affect the reliability of each individual finger differently. And since temperature is a nonlinear feedback mechanism that affects the drain current, especially in power amplifier circuits where high power densities are required, the overall optimum load-line for a large multifinger device may be affected due to nonuniform bias densities across the different fingers. Moreover, in a large-signal operation, and for large devices, individual fingers may see very different load impedance values which can affect what temperature each finger is running at.

It is shown from previous SPICE simulations in Fig. 4.14, that the maximum temperature rise in a multifinger device, is found to be a strong function of the gate-to-gate spacings. The figure suggests that a resistor, R_1, can be placed between each pair of adjacent fingers in the lumped-element model as shown in Fig. 4.20, to account for the mutual heating between fingers and in most cases, the gate-to-gate spacing chosen by a MMIC designer is the same across the whole multifinger device. This simplifies the proposed lumped-element model and leads to using the same resistor value either side of each finger where the power is dissipated.

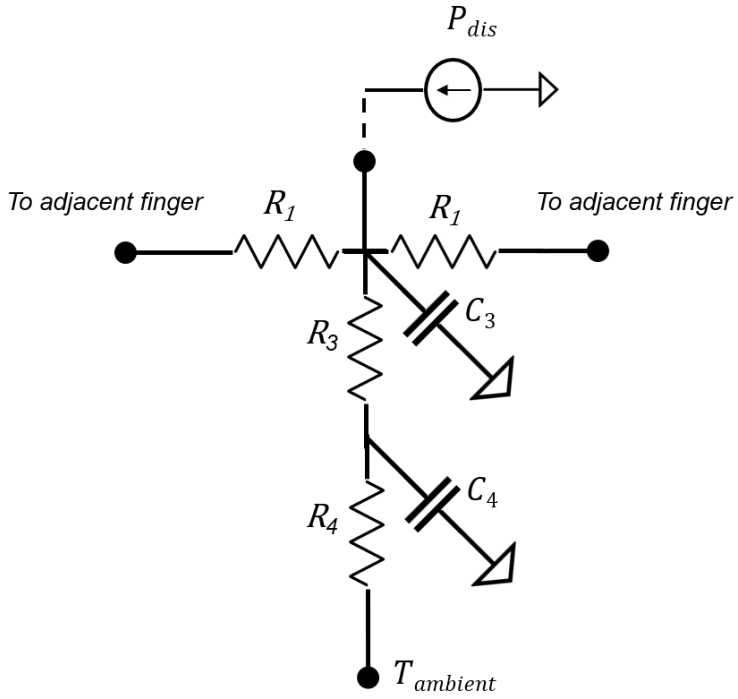
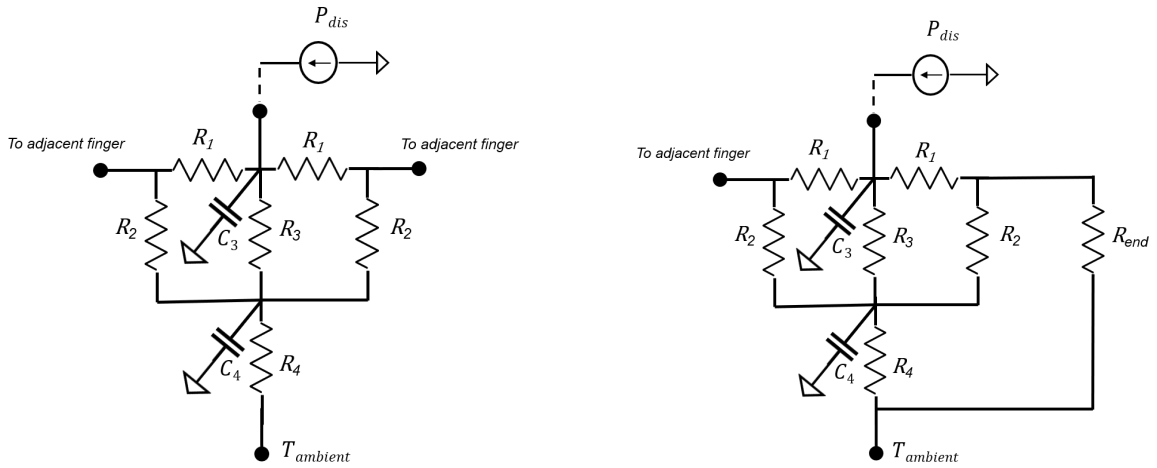


Figure 4.20: Lumped-element model minimum vertical network required, and with the resistor, R_1, added between two adjacent fingers.



(a) Inner finger. (b) Outermost finger.

FIGURE 4.21: Lumped-element thermal model used to fit SPICE data.

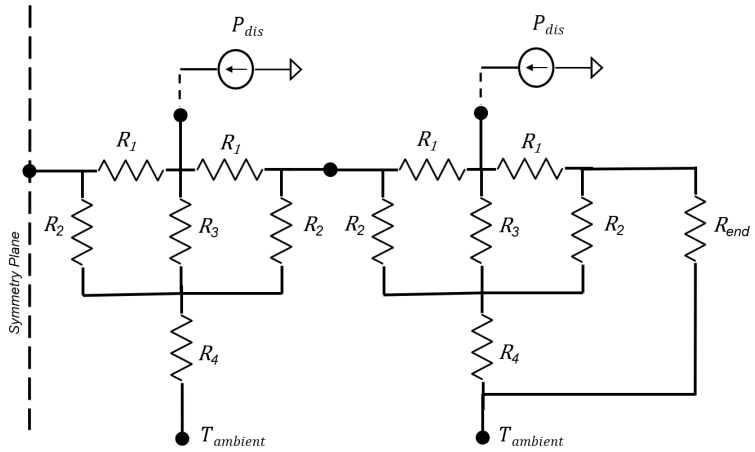
To complete the lumped-element thermal network, an additional resistor, R_2 is found to be necessary to model the vertical heat flow between two adjacent fingers. The complete model is shown in Fig. 4.21.

4.7 Lumped-Element Model

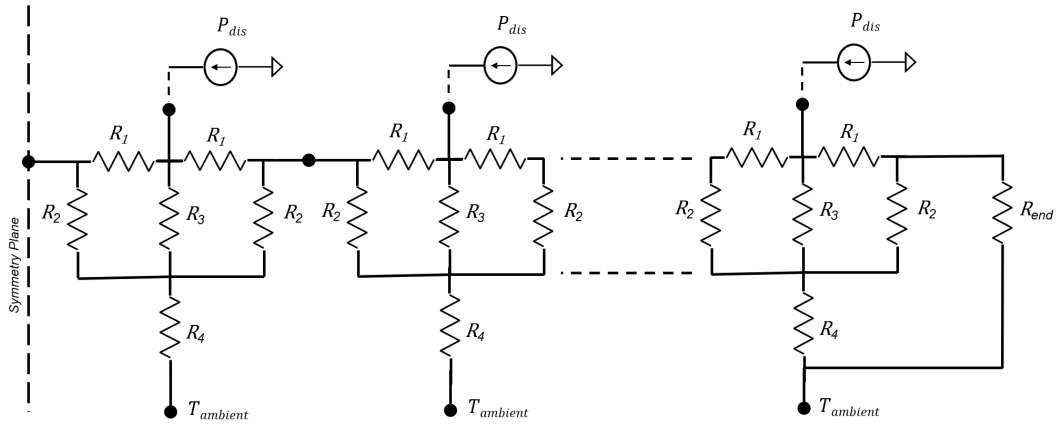
A complete, steady-state, lumped-element thermal network which is based on the results of a physical SPICE model is shown in Fig. 4.21. The lumped-element network has the minimum number of resistor elements that are required to obtain an accurate steady-state solution. This network is considered to be the building thermal model unit which can be cascaded to build a thermal network for an arbitrary multifinger device.

The lumped-element model is constructed as a building block unit which can be easily scaled up to any multifinger device. As shown in Fig. 4.21, the heat flow from the gate finger is symmetrical in the horizontal direction. R_1 represents the lateral thermal resistivity of the path between two fingers, R_2 and R_3 represents the heat flow vertically through the epilayers in the close vicinity of the heat source and R_4 is the thermal resistivity of the substrate.

The lumped-element model proposed has four exposed nodes as shown in Fig. 4.21 (a),



(a) A model for a 4-finger device.



(b) A generic model for a 2n-finger device.

Figure 4.22: Lumped-element thermal model. Capacitors not shown here for simplicity.

the top node one is connected to the thermal node of a nonlinear model (MQFET), the bottom node is connected to the ambient temperature or can be connected any custom thermal network and the two nodes either side of the thermal model are connected to the adjacent fingers in a multifinger device or in the case of outermost finger, only one node is required to be connected to adjacent finger and the other node is terminated with an end-effect resistor, R_e, as shown in Fig. 4.21 (b).

The single-finger lumped-element model is cascaded to construct a thermal lumped-element network for a 4-finger device and a generic multifinger device as shown in Fig. 4.22.

TABLE 4.3: Lumped-Element Model Normalised Resistor Values

Gate-to-Gate Spacing (μm)	10	20	30	40
R_1 ($\Omega.mm$)	280	98.5	63	42
R_2 ($\Omega.mm$)	0.26	0.26	0.26	0.26
R_3 ($\Omega.mm$)	5.66	5.66	5.66	5.66
R_4 ($\Omega.mm$)	9.6	9.6	9.6	9.6
R_{end} ($\Omega.mm$)	1.93	1.93	1.93	1.93

4.8 Fitting Lumped-Element Model to SPICE Data

The effort of fitting the lumped-element model in this section is focused on the steady-state temperatures only. Although transient simulations performed using the thermal code are used to formulate the lumped-element model, no effort is taken to fit the transient solutions as per the scope of this thesis.

SPICE models for 2, 4, 6 and 8-finger devices on a 100 μm thick SiC substrate are generated with 5.2 W/mm dissipated power which is similar to the bias used in power amplifiers. Each device size was simulated with four different gate-to-gate spacings; 10, 20, 30 and 40 μm. A perfect heat sink is connected to the backside of the substrate with an ambient temperature of 85 °C assumed when simulating the SPICE thermal model.

For each multifinger device simulated, the maximum channel temperature of each finger is recorded, for example, for a 4-finger device, the temperatures of the inner and the outer fingers are recorded. Half of the fingers are required because devices used here are symmetrical. The simulation of the different models mentioned above result in 40 temperature data points, these data points are used to optimise the finite-element models for each device. A Simplex gradient algorithm is used to fit the resistor values of the lumped-element model; R_1, R_2, R_3, R_4 and R_{end} to the temperature data points obtained from the SPICE model. The same models above are generated again using a 50 μm SiC substrate for verification.

Table 4.3 shows the resistor values of the lumped-element model, which are fitted to the SPICE data, given for commonly used gate-to-gate spacings. It is noted that all the resistor values of the lumped-element model are held constant for different gate-to-gate spacings except R_1 which represents the heat-flow path resistivity between gate fingers.

Fig. 4.23 shows the finite-element model for one finger of a 2-finger device configuration which also represent the building block for any multifinger device, so, for example, to construct a finite-element thermal model for a 4-finger device with 20 μm gate-to-gate spacing, four lumped-element unit cells shown Fig. 4.23 are cascaded to generate a full 4-finger lumped-element thermal model as shown in Fig. 4.24.

Fig. 4.25 shows R_1 values plotted for different gate-to-gate spacings where the data is well fitted to a power-law function which is consistent with the SPICE gate-to-gate data shown in Fig. 4.14 which also suggests that the temperature dependency on the spacing between gate fingers follows a similar trend.

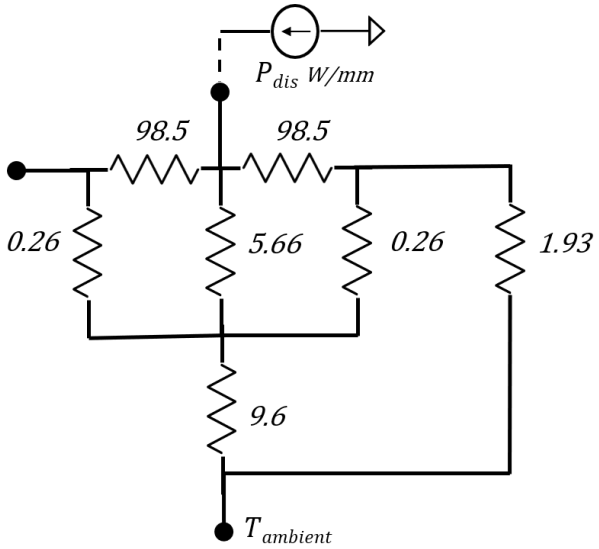


Figure 4.23: Lumped-element thermal model of a 2-finger device with 20 μm gate-to-gate spacing. This model is normalised, i.e., dissipated power (P_{dis}) unit is W/mm and the resistor values are given in Ω.mm.

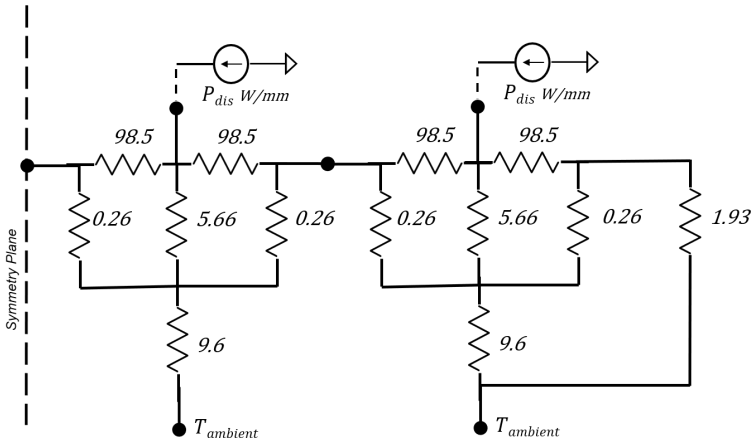


FIGURE 4.24: Lumped-element thermal model of a 4-finger device with 20 μm gate-to-gate spacing. Dissipated power (P_{dis}) unit in W/mm and the resistor values in Ω.mm.

The values for the finite-element resistors are fitted to normalised dissipated power values, i.e. W/mm. The values of the fitted resistors are converted to work with absolute power densities in order to match the output of the thermal node of the nonlinear model (MQFET). The thermal node of the MQFET passes a current that equals the instantaneous power dissipated in the device.

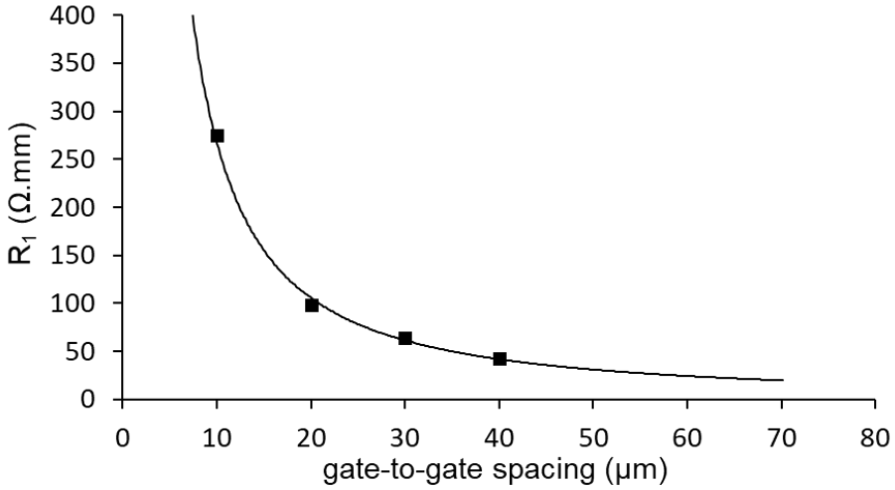


FIGURE 4.25: R_1 values of the lumped-element plotted for different gate-to-gate spacings (squares) and the fitted power-law function (solid line).

Fig. 4.26 illustrates how the single-finger lumped-element thermal model is connected in the electrical schematic of a multifinger device. A good agreement is achieved

and data verified even outside the SPICE data that was used to fit the model was shown in Fig. 4.27. The proposed lumped-element thermal model is a simple linear lumped-element network and was found to have no impact on simulation speed or model convergence.

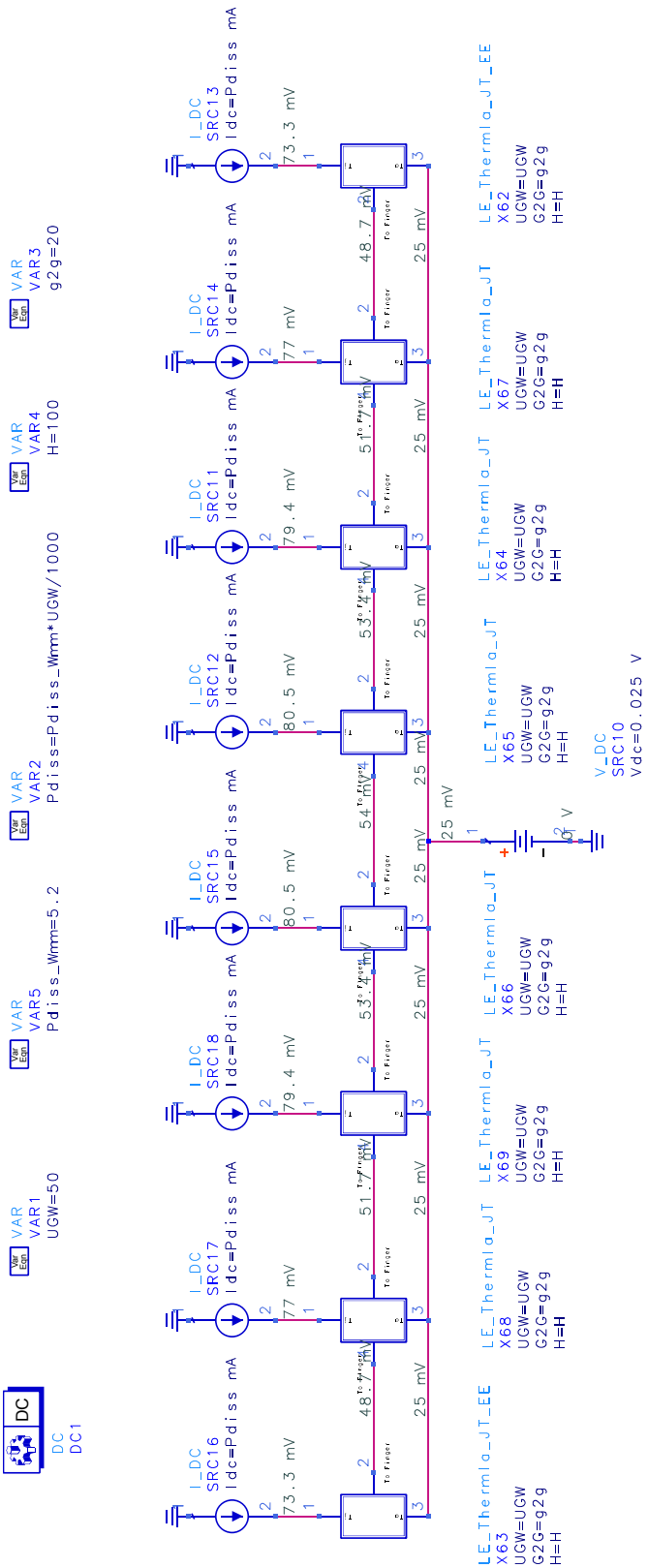
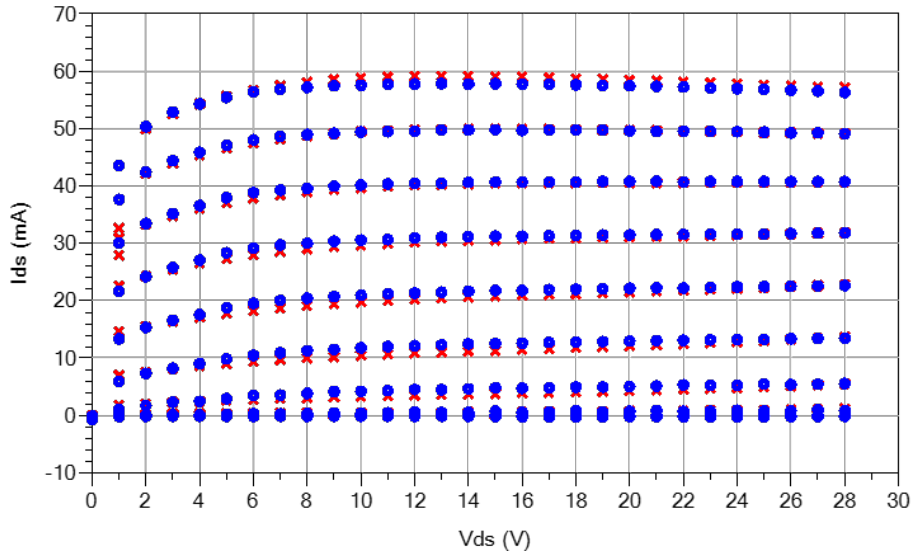
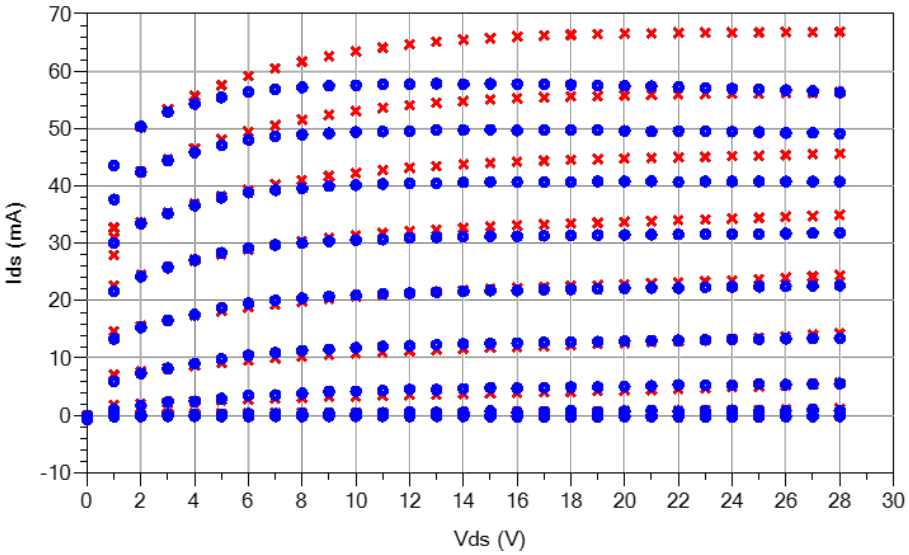


FIGURE 4.26: Lumped-element thermal model of an 8×50 μm device connected in an electrical schematic.



(a) Lumped-element model is enabled.



(b) Lumped-element model is disabled.

FIGURE 4.27: DCIV for data for a 2×50 μm.

4.9 Summary

In this chapter, a finite-element thermal model has been developed using SPICE to investigate device self-heating. Both steady-state and transient simulations have been demonstrated. The model incorporates temperature-dependent thermal conductivity

and accounts for gate finger end-effects. Good agreement with measurements is observed.

The model is then scaled back to a sparse scalable lumped element model that is suitable for integration into a microwave circuit design suite. In turn, this introduces the capability to perform electrothermal simulations. The proposed lumped-element thermal model is a simple linear lumped-element network that has no impact on simulation speed nor model convergence.

In the next chapter, the trapping effects in GaN devices are characterised and modeled.

5

Trap Characterisation and Model Implementation

A trap potential is highly sensitive to the device operating temperature, and therefore a thermal network is needed to feed into a trap model. An accurate estimate of thermal impedance is provided by the thermal network developed in Chapter 4. This thermal model will aid the characterisation of trapping in this chapter.

The generic trap-centre model depicted in Fig. 5.1 includes temperature and trap-state dependence to elegantly predict trapping rates in any state [1]. The trap state is modelled as a trap potential, v_T , across a charge storage capacitor, C_T , that is driven by charge capture, i_C, and emission, i_E, currents. The latter are controlled by the trap state and a bias-dependent control potential (analogous to the trap energy), v_I .

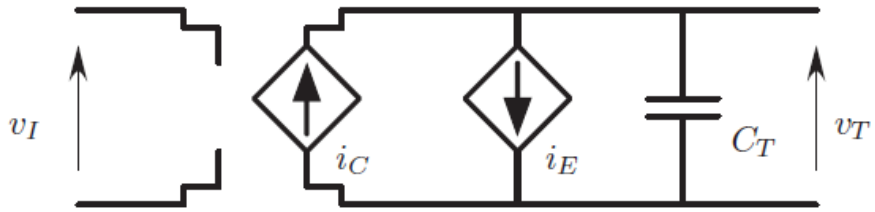


FIGURE 5.1: Circuit model of a trap center [1].

Section 5.1 describes the selection of a probe state and develops a model used to extract the trap-state potential. Section 5.2 and 5.3 describe the details of the extraction of trap-state potential and rate. Section 5.4 discusses the results and their consistency with theory and an application to small-signal characteristics. Finally, Section 5.5 presents an application to a commercial GaN proccess.

5.1 Trap State Probe

The probe condition is one in which the full gate-lag transient can be observed. That is, the initial and final states are measurable. The initial states are measured over a range of initial conditions. The result is a remarkable characterisation of trap-state variation from neutral to fully-ionised across the bias range.

Consider a device having one single-level trap affecting the drain current through the gate potential. Consider also that the device has been held at a bias point V_{GS}, V_{DS} for long enough to establish a steady-state temperature and trap potential V_T. For constant V_{DS}, a step change in the gate-source voltage to v_{GS} will produce a current, given to the first order, by

$$i_{DS} = g_m \cdot (v_{GS} + V_T - V_{Th}) \,, \tag{5.1}$$

where i_{DS} is the instantaneous drain-source current, g_m is a local transconductance, and V_{Th} the device threshold-voltage. The key assumption is that V_T has not changed

instantly. Fig. 5.2 shows a typical transfer characteristic of GaN HEMT used in this chapter.

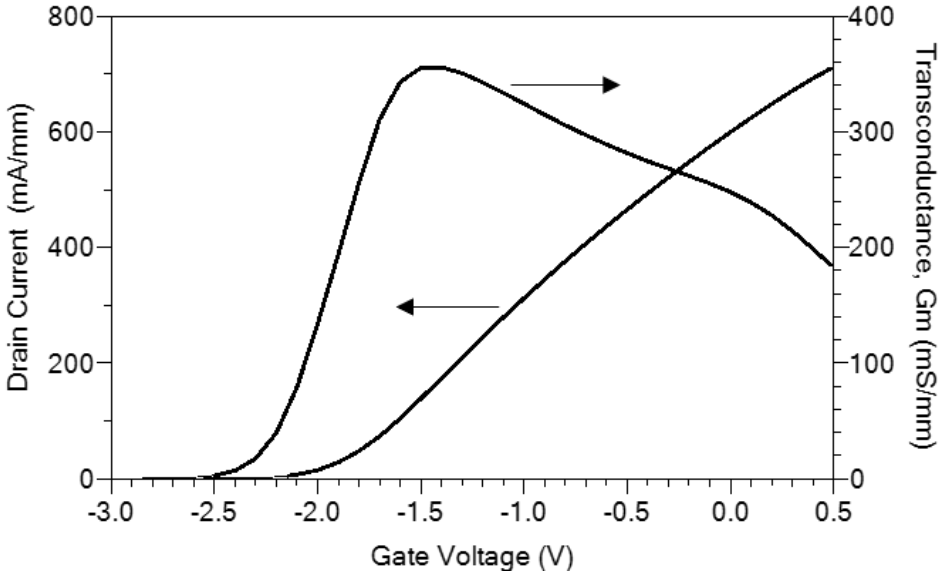


Figure 5.2: DC transfer characteristic of GaN HEMT.

Two such pulses will give $g_m = \Delta i_{DS}/\Delta v_{GS}$, which can be substituted into (5.1) to give

$$V_T = i_{DS} \cdot \frac{\Delta v_{GS}}{\Delta i_{DS}} - v_{GS} + V_{Th}. \tag{5.2}$$

The potential V_T is the steady-state trap-circuit potential at that particular bias point. So, for a grid of bias values V_{GS} and V_{DS}, V_T can be simply calculated for each bias point.

This two-pulse method allows arbitrary bias states to be probed, including states normally unobservable. The problem with this method, however, is that the current model restricts calculation to individual bias points because of its simplicity and that propagation of errors means that the uncertainty becomes too large when the trap voltage is small. Additionally, the temperature of the device, and hence of the trap-center, is different for each bias point.

5.2 Trap State Extraction

A downhill-simplex algorithm is used to minimise the fit of a more-complex model to 9 pulse-points at each of 33 bias points (11 $V_{DS} \times 3$ V_{GS}), giving 297 data points. The 9 data points, which form the probe cluster, are chosen to be uniformly distributed about a mean turned-on bias value; (v_{ds}, v_{gs}). The mean bias point needs to have minimal power dissipation and still produce a measurable drain current at the same time in order to eliminate or minimise the thermal impact on the behaviour of the device. The mean value chosen for the probe cluster is (4V,-1V) with a uniform step value of (0.5V, 0.1V).

The instantaneous drain current is given by

$$i_{DS} = I_{DS0} + \{g_{m_0}\,[v_{\acute{G}S} + (V_T - V_{Th})] + g_{ds} \cdot v_{\acute{D}S}\} \cdot \delta_P, \tag{5.3}$$

where I_{DS0} is a constant instrumentation current-offset, g_{m0} a global transconductance, $v_{\acute{G}S}$ and $v_{\acute{D}S}$ are intrinsic voltages due to access resistances r_S and r_D, g_{ds} is the drain-source conductance and $\delta_P = 1 - \delta \cdot P_Q$ is a power factor determined by parameter δ [W^{-1}] and the power at the bias point, $P_Q = V_{DS} \cdot I_{DS}$, with the assumption the device has been sitting on that bias for *long enough*.The constant δ, is a fitting parameter used to scale down the modelled current in relation to temperature, i.e., higher power dissipation. Note that (5.2) is not used for the complete device model, but merely to model the instantaneous current about the pulse-points for the purpose of finding V_T.

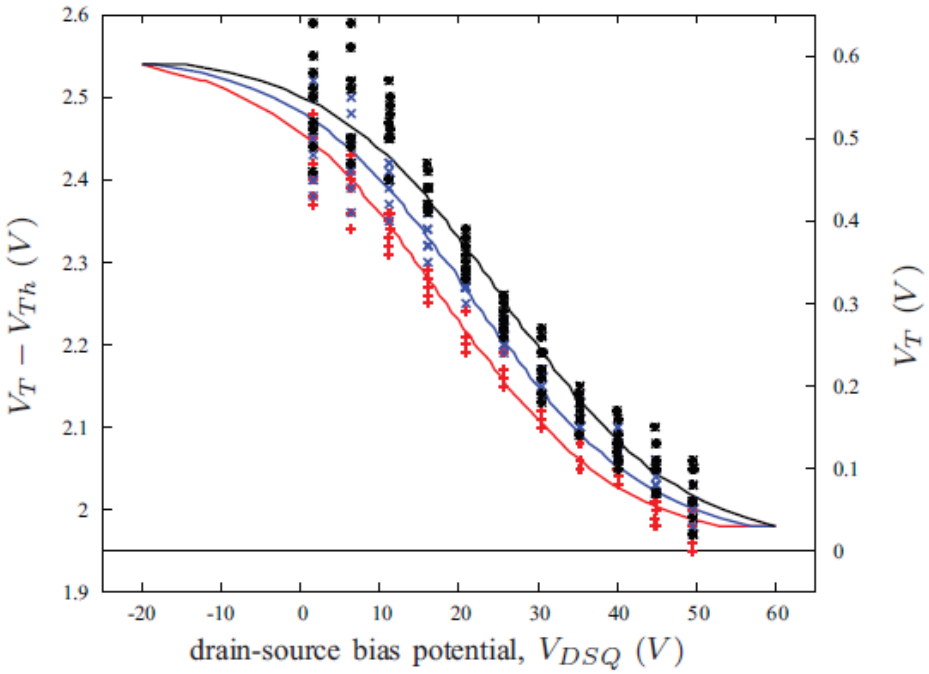


Figure 5.3: Extracted values of $V_T - V_{Th}$ (points) and fitted curves as a function of bias V_{DS} and $V_{GS} = -6.75$ (*red*), -4.45 (*blue*), -2.15 (*black*), lower to upper. Here, $\alpha = -0.00381, \beta = 0.00232, \gamma = -0.067$, $V_0 = 0.6V$ and $V_{Th} = -1.95V$.

The potential $(V_T - V_{Th})$ for individual bias points is plotted in Fig. 5.3, revealing an electron trap. This is then fitted for a relationship [1] between v_I and V_T (also plotted in Fig. 5.3);

$$v_I = \alpha \cdot \acute{V_{GS}} + \beta \cdot \acute{V_{DS}} + \gamma, \ and \tag{5.4}$$

$$(V_T - V_{Th}) = \frac{V_0}{1 + \exp(v_I / \hbar T)} - V_{Th}. \tag{5.5}$$

Here, α, β and γ are dimensionless fitting parameters relating intrinsic bias potentials to v_I, V_0 $[V]$ is the maximum trap voltage, $\hbar$ $[eV.K^{-1}]$ is Boltzmann's constant, and T $[K]$ temperature. The two parameters α and β can be directly related to gate lag and drain overshoot respectively.

In order to fit to these data points, temperature is modelled as

$$T = T_a + R_T \cdot P_Q, \tag{5.6}$$

where T_a $[K]$ is the ambient temperature and R_T $[K.W^{-1}]$ is the thermal resistance. Note that, in Fig. 5.3, measured points are at the bias temperatures whereas fitted curves are at a particular T_a. The close agreement between measured v_T and that modelled in (5.5) provides verification for the trap-center circuit model shown in Fig. 5.1 and detailed in [1].

For simplicity and quick trap-model extraction, cold quiescent biases may be used in the fitting process. In this case, $P_Q \to 0$, $\delta_P \to 1$ and $T \to T_a$.

5.3 Trap Rate

The characteristic frequency for the trap can be obtained from the time constant of a pulse profile. Emission of the trap center is chosen as this will be independent of the voltages involved, although it will be influenced by temperature. This transition may be iso-thermal in nature so that the emission frequency obtained is at ambient temperature (for convenience).

The time constant of the trap model in Fig. 5.1 is the product of the capacitance and dynamic resistances of the current source. The characteristic frequency of the trap-center is then given by [1] as

$$\omega = \omega_0 \left[1 + \exp\left(\frac{v_I}{\hbar T}\right)\right], \tag{5.7}$$

where the emission frequency is given as

$$\omega_0 = B \cdot T^2 \cdot \exp\left(\frac{E_{act}}{\hbar T}\right), \tag{5.8}$$

for a constant B $[rad \cdot s^{-1} \cdot K^{-2}]$ and activation energy E_{act} $[V]$.

Fig. 5.4 shows measurements of the time constants of gate-lag pulse profiles of the trap center over three different ambient temperatures. A model is fitted that incorporates one trap-center model and a heat-sink model that feeds into the trap model.

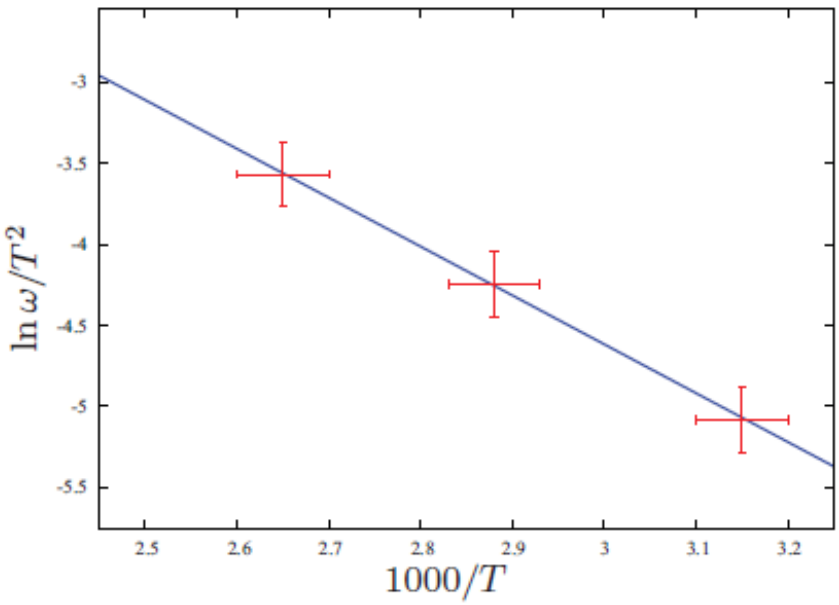


Figure 5.4: Measured (red bars) and modelled (blue line) emission frequencies, for three different temperatures, with a target of $v_{GS} = -1.6V$, $v_{DS} = 10V$ and a bias of $V_{GS} = -6.0V$, $V_{DS} = 40V$. Here, $E_a = -0.26V$ and $B = 63.7$.

The rest of the HEMT model is extracted in conventional ways [91]. This then completes the trap model of Fig. 5.1, with current sources (for normalised capacitance value) given by [1] and the signs reflecting the fact that it is an electron trap:

$$i_C = -\omega_o \cdot v_T \cdot \exp\left(\frac{v_I}{kT}\right), \text{ and} \tag{5.9}$$

$$i_E = -\omega_o \cdot (V_o - v_T). \tag{5.10}$$

5.4 Discussion

Consider the dispersion shown in Fig. 5.5 in the context of the results seen in Fig. 5.3. In both data sets of Fig. 5.5, the bias is at $V_{DSQ} = 40V$, which is a near-neutral trap state as shown in Fig. 5.3. The very-fast capture process is dominant in this state, so a brief period at the bias is sufficient to establish the neutral state. When the drain potential of the transistor is reduced to a low potential ($\sim 10V$), there is significant

current lag evident in Fig. 5.5. This is because, as shown in Fig. 5.3, the trap will be moving to an almost fully-ionised state, where slow emission is the dominant process. Hence, 50 μ s is not sufficient time for the trap to become fully-charged, whereas 1 s is. When the transistor is reduced to a moderate potential ($\sim 25V$), the trap state is only half-ionised, with both emission and capture processes competing. Hence, at this point, 50 μs is almost the time required for the trap to charge. It would require a shorter time ($\sim 1\ \mu\ s$) to show significant dispersion in this state.

Fig. 5.5 can also be considered for its implications for gate lag and drain overshoot. For constant V_{DS}, a positive change in v_{GS} results in a positive change in v_T over time and hence an slow increase in current. This is normally referred to as gate lag. Similarly, for constant V_{GS}, a positive change in v_{DS} results in a decrease in v_T over time and hence a slow decrease in current. This is normally referred to as drain overshoot. Most real-world changes involve both v_{GS} and v_{DS}, nonetheless Fig. 5.3 allows us to relate the before and after terminal voltages to the changes in v_T.

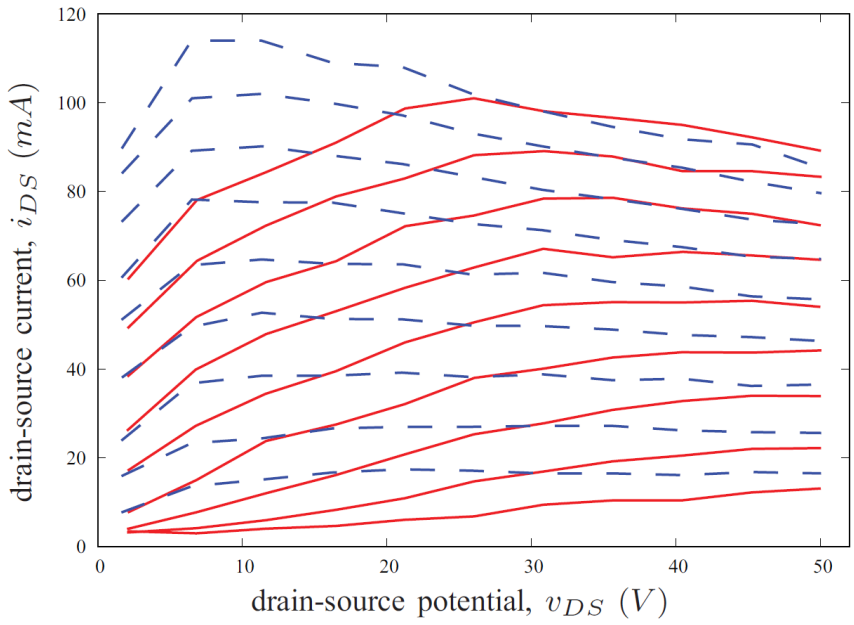


FIGURE 5.5: Pulsed-I/V of a 2x100 μm GaN device, measured at two different times. Bias is $V_{GSQ} = -6V$ and $V_{DSQ} = 40V$, duty cycle 10%, pulse time: blue dash 50 μs, red solid 1 s.

The complete HEMT device model is extracted in conventional ways [91]. To this

is added the trap-centre circuit of Fig. 5.1. Such a device model that incorporates one trap-centre model and a heat-sink model that feeds into the trap model is then used to simulate gate-lag transients. The results are shown in Figs. 5.4 and 5.7.

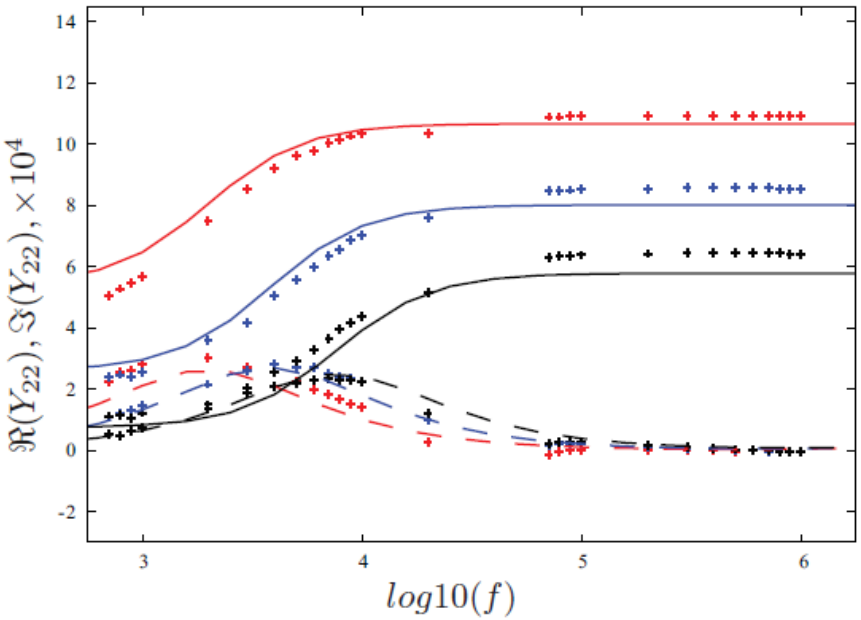


Figure 5.6: Measured (points) and modelled (line) $\Re(Y_{22})$ (full) and $\Im(Y_{22})$ (dash), at V_{GSQ}/V_{DSQ} = -2/11V (red), -1.7/16V (blue), -1.5/21V (black), top to bottom.

Y-parameters of the device at biases that evoke trap effects [65] are shown in Fig. 5.6. This shows good agreement between the simulated performance and measured responses, for a range of biases. These simulations are able to accurately predict the dispersion in the Y-parameters due to trap-induced current changes and the temperature-induced trap changes. This result is a good verification of both the trap-centre model and of the trap parameter-extraction method.

The extraction method can then be described as:

1. Extract basic device parameters in the usual manner, including g_{m0}, g_{ds}, δ, r_S, r_D and R_T,

2. Measure a data set that includes a cluster of pulse voltages for each of enough bias points V_{GS} and V_{DS} to give adequate coverage over the range of interest,

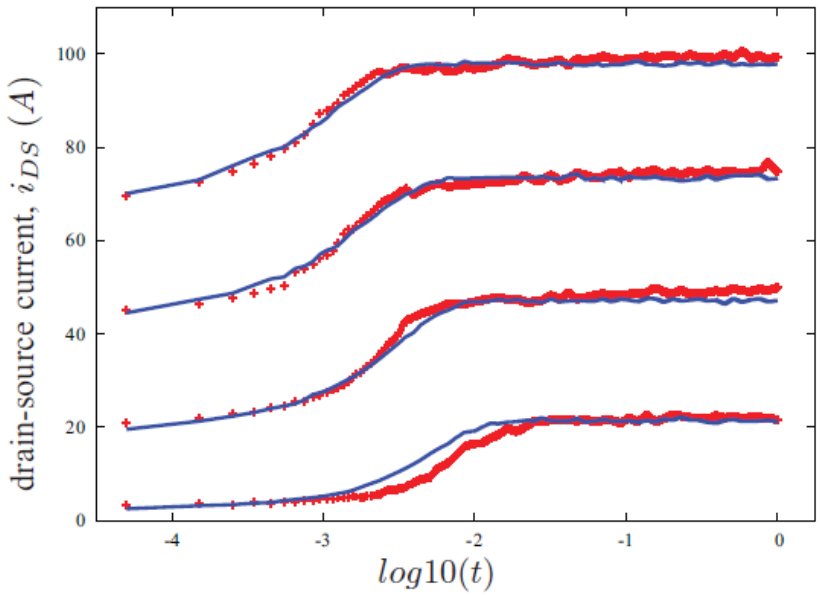


FIGURE 5.7: Measured (red dots) and modelled (blue lines) transient drain current at $v_{DS} = 11V$ and $v_{GS} = -2.5, -2, -1.5, -1.0V$, originating from quiescent condition of V_{GSQ}/V_{DSQ} = -6/40V.

while observing the timing considerations of *long* quiescent time and *short* pulse time,

3. Fit a current model to this data set, solving for $\alpha, \beta, \gamma, V_{Th}$ and V_0. Whether this is done as a one- or two-stage process is not important, and

4. Measure the time constant of the transient response of an emission event, to get the characteristic frequency ω_0.

For devices that have more than one trap and/or multiple-level traps, it is a simple matter to fit for a combination of effects. Similarly, for knee-walkout, for which the trap is thought to act on access resistances [92] rather than v_{GS} in controlling current. Another consideration is impact ionisation, acting on drain current indirectly by the supply of charge carriers to a trap. Again, an expanded current model, that includes a term in $exp(v_{DS})$, would be needed, along with a suitable choice of the voltages to which one pulses. Note that the device used here was chosen as having only one noticeable trap and no obvious impact ionisation.

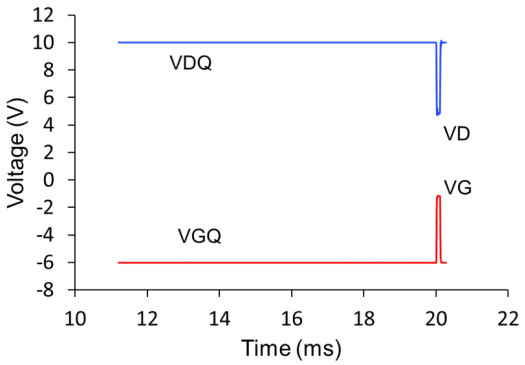
5.5 Application to GaN Process Technology

The same GaN process used in the previous chapters is used in the following sections. See page 54 in Chapter 3 for the process details.

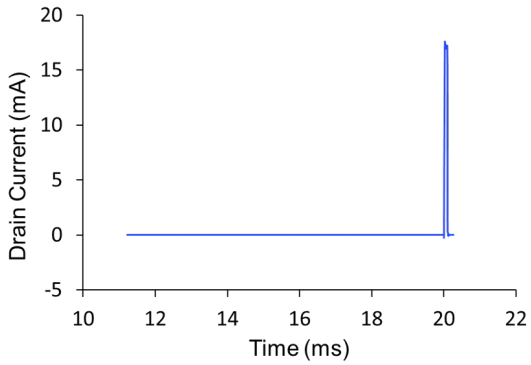
5.5.1 Trap Extraction

A Keysight commercial pulsed IV system called "MCSMU" is used to make these pulsed measurements on a 2×100 μm device. A 100 μs pulse width is used to sample the drain the current and 10 ms soak time is implemented on each bias point which is found to be enough to establish the trap state before applying the pulse. When the gate and drain voltage pulses are applied to the device, the drain current is then sampled after 2 μs.

A pulse example is shown in Fig. 5.8 (a), showing gate and drain being pulsed and Fig. 5.8 (b) shows the measured drain current over time. A closer look at these pulses are shown in Fig. 5.9.

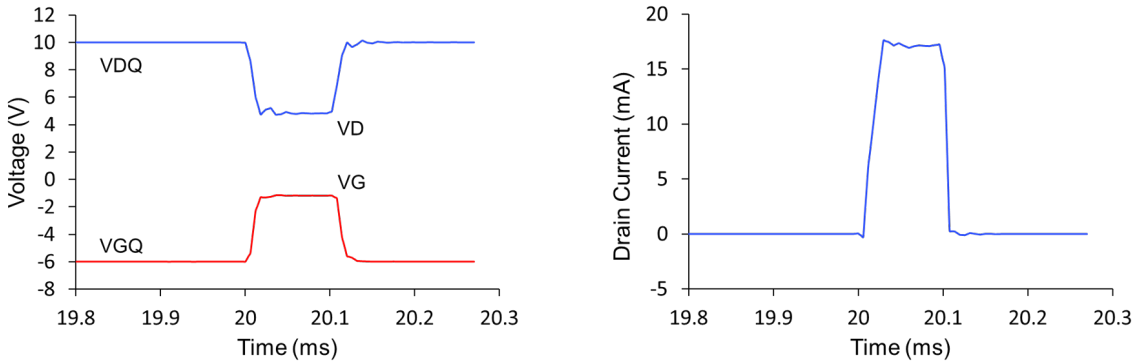


(a) Applied pulses to the gate (red) and drain (blue) terminals.



(b) Measured drain current over time.

Figure 5.8: A pulse width of 100μs is used to characterise the trapping in a 2×100 μm device.



(a) (b)

FIGURE 5.9: Same as figure. 5.8, but with a closer look at the pulse region.

A total of 12 pulse points for 28 bias points (7 $V_{DS} \times 4$ V_{GS}) giving a total number of 336 data points to fit. The instantaneous drain current is given by:

$$i_{DS} = I_{DS0} + \{g_{m_0}[v_{\acute{G}S} + (V_T - V_{Th})] + g_{ds} \cdot v_{\acute{D}S}\} \cdot \delta_P, \tag{5.11}$$

In this extraction, the trap voltage at each probe pulsed points is forced to have the same trap potential which is believed to be a better approach as it is forcing the fit to be averaged across the probe space which is a more realistic assumption given that these probe points have low power dissipation and the current sampling time of these pulse points is quicker than any significant thermal or trap time constants associated with these probe points.

Fig. 5.10 shows the measurement plan for trap characterisation.

The black dots represent the 28 bias points in which they are biased for 10 seconds to get the trap state fully established, i.e., fully ionised states. After establishing the trap state, each point of the probe cluster of the 12 points (in red diamonds) is pulsed with 100 μs pulse width where the drain current is sampled at 2 μs rate and after that, the bias is returned to the same bias point for another 10 seconds to reset the trap state in case it has changed during the pulsing process. The process is repeated until all of the probe points in the clusters are measured and then the bias is moved to the next bias point to repeat the whole process again until all the bias points completed.

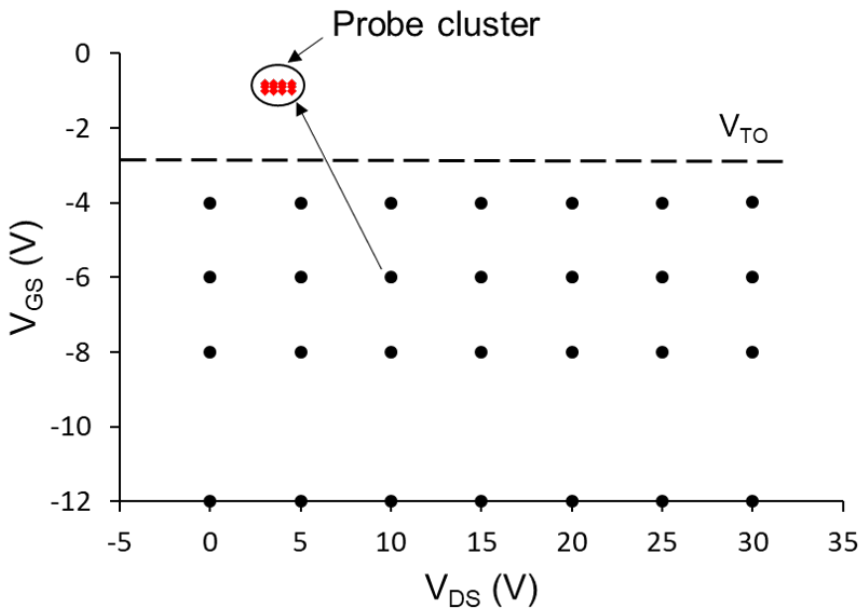


Figure 5.10: Trap measurement plan showing biases to be characterised (black dots) and the pulse cluster probes (red diamonds).

The pinch-off of this process is about -2 V and the gate bias points are -12, -8, -6 and -4 V. Drain voltage is swept from 0 to 30 V in 5 V steps. It is worth mentioning that the all the gate bias points are chosen to be below pinched-off voltage of the process so that no power dissipation is generated at the biases we are characterising for traps and in this case thermal effects can be easily separated from traps and hence there are less unknowns to solve.

The measured data is post processes and rearranged in a certain way so that it can be imported and read in Keysight ADS. An optimisable trap voltage vector which represents $(V_T - V_{Th})$ that contains a total number of 336 variables is created and all the 12 points in the probe cluster are forced to have the same variable (trap voltage). The 12 points that form the probe cluster are generated using the nested values of V_{DS} = 3, 3.5, 4 and 4.5V and V_{GS} = -1.2, -1.1, -1 and -0.9V. The modelled drain current equation (5.11) is optimised to fit the measured current profile. Reasonable initial guess value for the current model are given as good starting point to start the optimisation process. A "Gradient Minmax" optimisation method is found to be robust for this

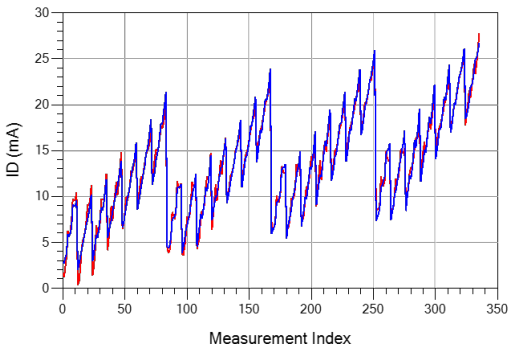
kind of problems..

Initial conditions for the access resistances of (5.11) are used and fixed during the optimisation process as 2.3 and 6.2 Ω for r_s and r_d respectively. The intrinsic values are estimated based on the linear extraction values described in Chapter 3 where $g_{m_0} = 5$ mS and $g_{ds} = 2.5$ mS. The thermal coefficient δ_P is set to 1 since all the 28 bias points we are measuring are cold and have no dc power dissipation associated. I_{DS0} is set to zero initially assuming no current offset in the instruments used.

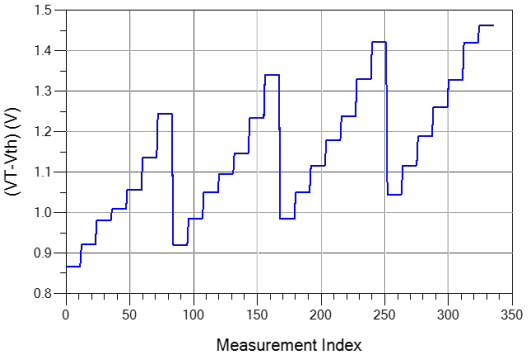
The goal of the optimiser is set so that the root-mean-square error (RMSE) is equal to zero as follows:

$$i_{error} = \sqrt{(i_{DSmodeled} - i_{DSmeasured})^2} \tag{5.12}$$

The optimiser is run until the minimum error (5.12) is achieved. The final results of the current fit is given in Fig. 5.11(a) where a very good agreement is achieved across the whole bias range. The extracted trap voltages that give this current fit are shown in Fig. 5.11(b). The values of the instantaneous drain current model parameters used to achieve the fit are given in table 5.1.



(a) The drain current model fit (red) to the measured current (blue) for total of 336 bias points.



(b) The corresponding extracted $(V_T - V_{Th})$ voltages.

FIGURE 5.11: Optimised drain current and extracted steady-state trap potentials.

Table 5.1: Final values for drain currents' parameters given in (5.11).

Parameter	Value
I_{DS0}	-0.0004
g_{m_0}	0.0480
g_{ds_0}	0.0025
r_s	2.3400
r_d	6.2000
δ_P	1.0000

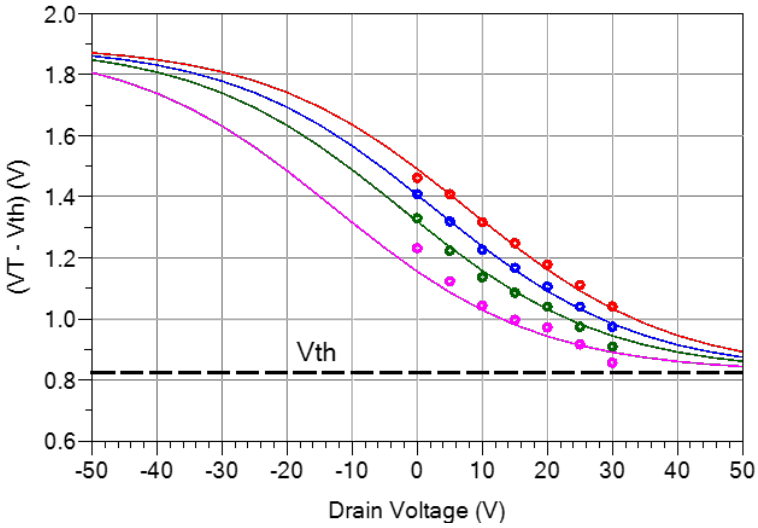


Figure 5.12: Extracted values of $(V_T - V_{Th})$ (points) and fitted curves as a function of bias V_{DS} and V_{GS}=-12 (magenta), -8 (green), -6 (blue) and 4 (red), lower to upper. Here, α = -0.00412, β = 0.00162, γ = -0.029, V_0 = 1.07V and V_{Th} = -0.8V.

Fig. 5.12 shows the extracted trap voltages and the fitted model to those extracted values based on the relationship in (5.5). The model fits the trap voltages very well the measured bias range, although it deviates at V_{GS}=-12 V which is expected due to the bigger i_{error} values at this bias. The bigger error values are attributed to a measurement error that arises from the reading of smaller current values, see graph Fig. 5.11 up to measurement index = 84.

5.6 Summary

This Chapter has presented a useful technique for extracting circuit parameters for modeling a trap center in GaAs and GaN. This consists of extracting the steady-state trap potentials of a model for a representative range of bias voltages. The characteristic frequency for emission is also measured from the time constant of a suitable transient response. The model is then used to accurately simulate the low-frequency dispersion in the device. Additionally, this provides verification of the model of trapping used.

6

Fitting and Verification of a Complete Large-signal Model, Including Thermal and Trapping Effects

In principle, the large-signal model should differentiate to a small-signal model at a quiescent bias point, which should eliminate the need to have a separate small-signal model. This requires the large-signal model to have a topology that correctly accounts for dispersion and dynamic effects. It also means that the core nonlinearity of the large-signal model needs to be mathematically conservative, so the small-signal parameters can correctly integrate to large-signal parameters.

The implication is that the large-signal model must consist of a nonlinear lumped-element network with non-dispersive parameters; conductance, transconductance, capacitance and transcapacitance. These parameters are expected to scale linearly with zero offset in proportion to the device width.

In this chapter, the thermal and trap models which are extracted in Chapters 4 and 5 respectively, are added to the large-signal model (MQFET). The current and charge derivatives of the large-signal model are fitted to the core linear model data obtained in Chapter 3. Beginning with a brief introduction to the MQFET in section 6.1, then the fitting process is discussed in section 6.2. In section 6.3, the large-signal model is verified over a range of device sizes under small-signal and large-signal operating conditions.

6.1 Modelling Approach

The intrinsic multi-bias data extracted in Chapter 3, contains all the information of the device including the nonlinear dynamic behavior of the FET device; thermal and trap charge. In the linear model extraction, this data is treated as a black box leading to inaccuracies in the model when scaled aggressively to multifinger devices because the mutual heating between fingers is significant and temperature distribution across the different fingers is not equal. Moreover, the trap charge behavior is highly dependent on the channel temperature and consequently inaccuracies in the thermal model will also cause inaccurate trap charge dynamics.

There are two ways to approach the modelling and the fitting of the nonlinear large-signal model. The first approach obtains non-dispersive intrinsic data that is free of dynamic effects. In this case, the DCIV and small-signal measurements must be acquired under pulsed conditions, i.e. using pulse lengths that are shorter than the thermals and trapping time constants. Based on the time constants for self-heating and trapping that are extracted in Chapters 4 and 5, the pulsed excitation should be of the order of picoseconds to avoid thermals and traps. This is impractical, considering the high voltage and current requirements.

In the second approach, the nonlinear dynamic effects of the device are modelled first and separated from the small-signal intrinsic multi-bias data. The dynamic models are added to the large-signal model which together form the complete large-signal model. The complete model is then fitted to the intrinsic multi-bias data.

In practice, the DCIV and small-signal measurements of a device are taken at steady-state, that is applying the bias long enough to ensure that thermals and trap charge states have reached steady-state. In this case, the extracted intrinsic data will include the nonlinear dynamic effects. The dynamic thermal and trapping effects, which are characterised and modelled in Chapters 4 and 5 respectively, are added to the relevant nodes the MQFET then the MQFET nonlinear model is fitted to the intrinsic data obtained from the small-signal extraction which has the nonlinear dynamic effects buried inside. The second approach is adopted in this chapter. The model acquisition process is illustrated in Fig. 6.1.

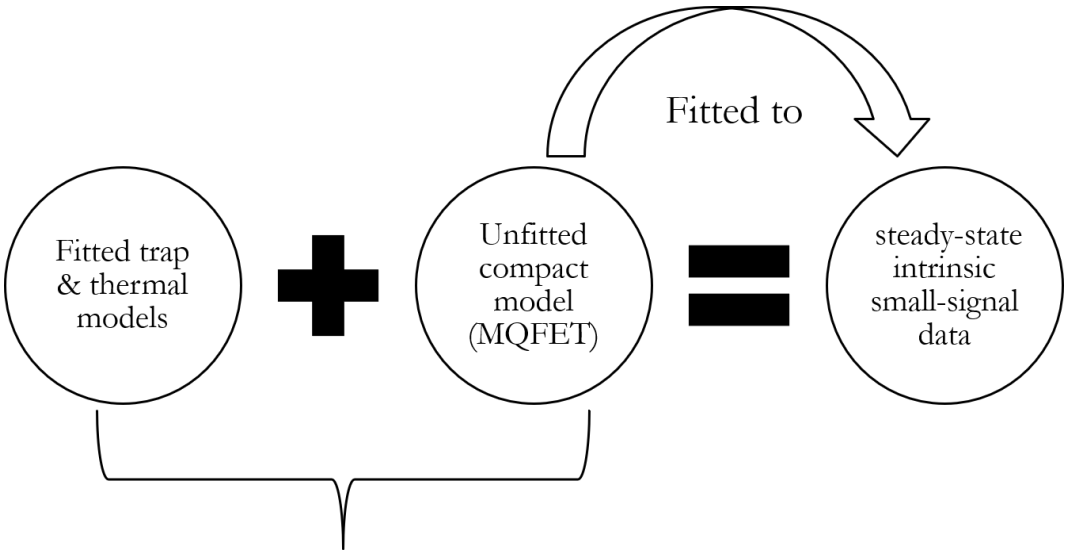
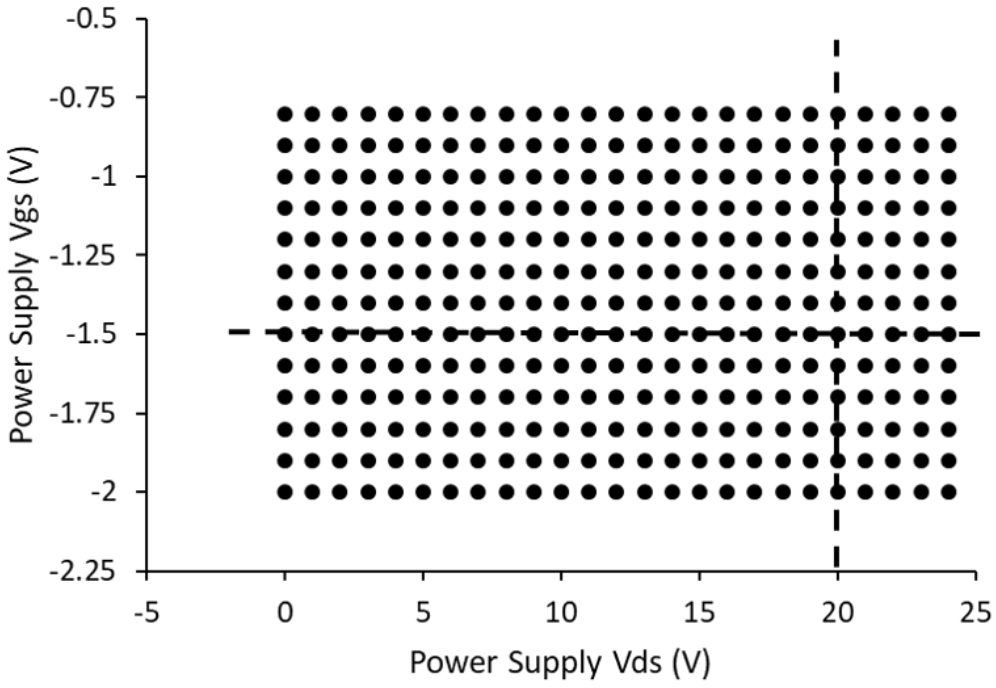
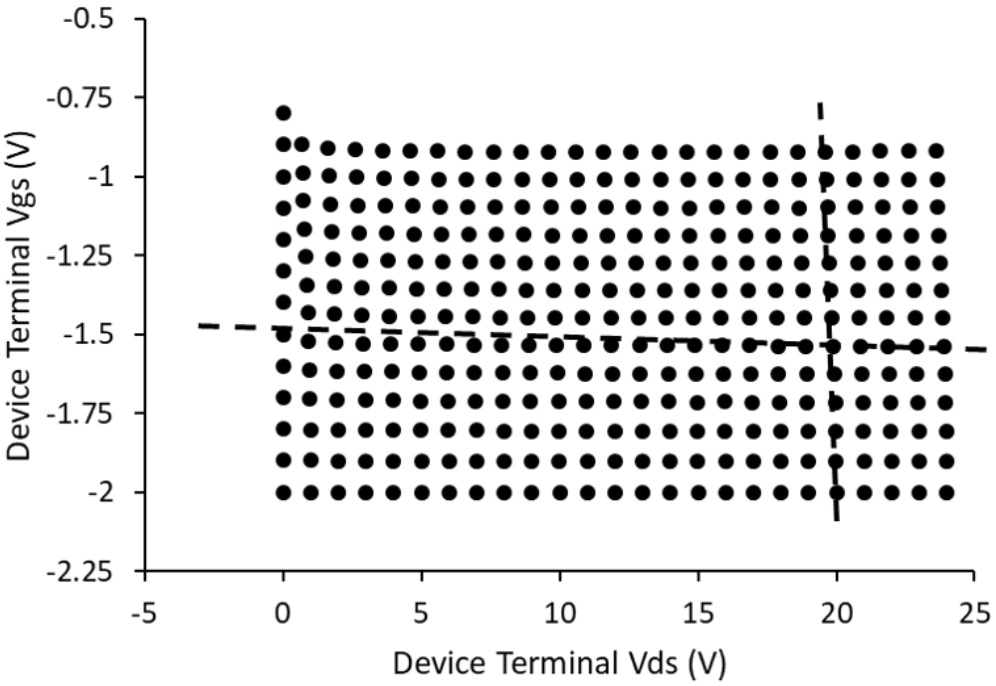


Figure 6.1: Illustration of the acquisition process of a complete large-signal model.

To characterise the small-signal and large-signal RF response of the HEMT, multi-bias S-parameters data is measured over the range of bias points shown in Fig. 6.2 (a). To ensure the measured data includes the trap and thermal information, a time delay of 1 second is chosen as a bias soak time. That is, for each bias applied to the device, a one second delay (which is selected according to the trap response observed in Chapter 5) is implemented before recording any measurement. Hence the measured small-signal data represents the steady-state response of the device under test.



(a) At the power supply terminals.



(b) At the intrinsic device terminals.

Figure 6.2: Measured bias points used for large-signal model extraction. Gate and drain bias slices used in the fitting process are shown.

6.2 Application to GaN Process Technology

The same GaN process used in the previous chapters is used in the following sections. See page 54 in Chapter 3 for the process details.

6.2.1 Small-Signal Measurement Details

A Keysight N5290A, 900 Hz to 110 GHz mm-wave 2-port network analyser system is used to perform small-signal S-parameters measurements. The VNA is calibrated from 50 MHz to 50 GHz with 201 frequency points in linear steps. Agilent E3646A and E3632A power supplies are used to bias the gate and drain of the DUT respectively, through bias tees incorporated in the mm-wave converter heads. A fine bias list file is created to supply bias voltages to the power supplies, with V_{DS} and V_{GS} swept from 0 to 28 V and -3 to +0.5 V respectively. On-wafer SOLT calibration method is used to accurately extend the measurement reference plane to the DUT's input and output terminals. Keysight BenchVue software is used to automate the measurement with bias sweeping.

6.2.2 Model Fitting

The thermal and trap models obtained from Chapters 4 and 5, are added to the unfitted MQFET large-signal model in order to form a complete large-signal model. The MQFET model parameters are tuned so that the current, current derivatives and charge equations of the complete large-signal model are fitted to the small-signal intrinsic model parameters obtained in Chapter 3. Ideally, the parameters of the large-signal model fit well across the whole bias plane, however, it is generally not feasible to obtain an accurate fit across all the regions of operations without making compromises. Instead, a gate bias slice and a drain bias slice which best represent of the intended region of operation and design application, are chosen to fit the large-signal model parameters. The bias slices are chosen to ensure the best model fit and accuracy over a wide range of amplifier applications with more focus on power amplifiers. For the GaN process used here, $V_{DS} = 20$ V is chosen since it is the highest qualified voltage

by the foundry which makes it an obvious bias choice for power amplifiers. The G_m peaks around V_{GS} = -1.5 V which corresponds to about 10% I_{dss}. See Fig. 5.2 for a typical transfer characteristic of GaN HEMT used in this thesis.

An accurate DCIV fit is necessary to predict the large-signal operation. Fig. 6.2 (b) shows the supply voltages mapped to the intrinsic gate and drain nodes for typical GaN power amplifier bias conditions. The graph also shows the gate and drain bias slices chosen for fitting the large-signal model.

To simplify the fitting process, the task is divided into two steps; starting with fitting the current model and its derivatives, followed by fitting the charge derivatives.

Current Model

The parameters that describe the drain current model in the MQFET, are used to fit the DCIV data and the current derivatives to the measured data. An excellent agreement between the modelled and measured DCIV characteristic is achieved as shown in Fig. 6.3. The model accurately tracks the knee region which is largely due to the inclusion of the trap model fitted in Chapter 5. In addition, the model fits the high power dissipation biases accurately with the help of the thermal network extracted in Chapter 4. A good agreement between the modelled and measured transconductance, G_m, and drain conductance, G_{ds}, is shown in Fig. 6.4 for both V_{GS} and V_{DS} slices.

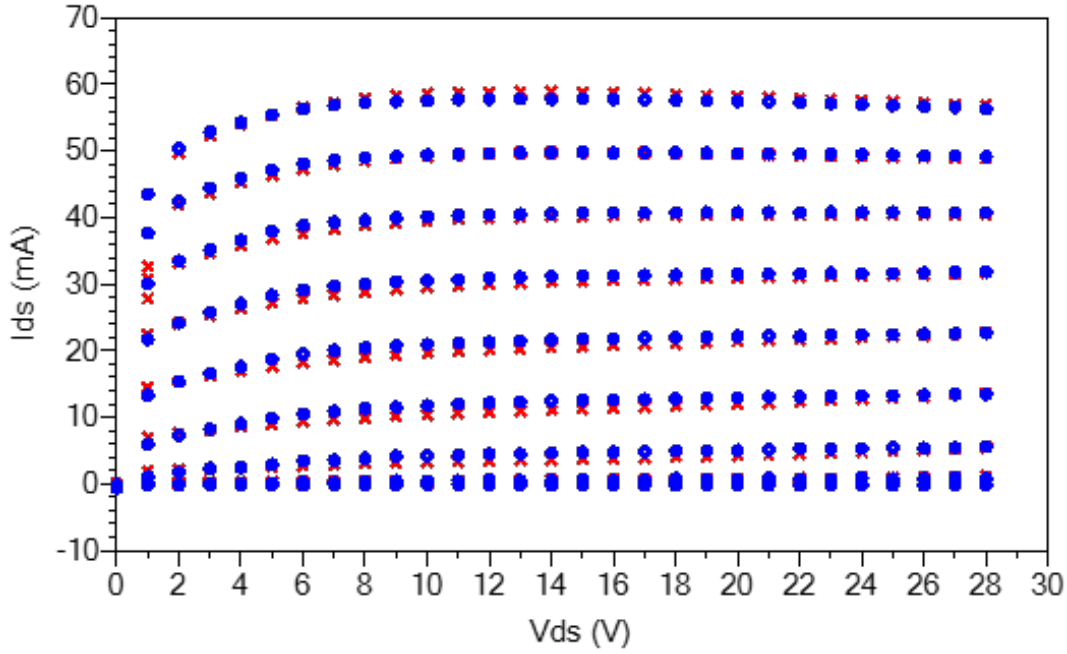
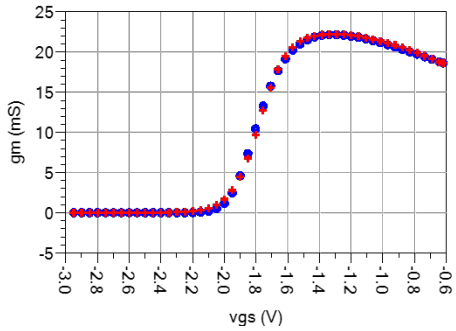
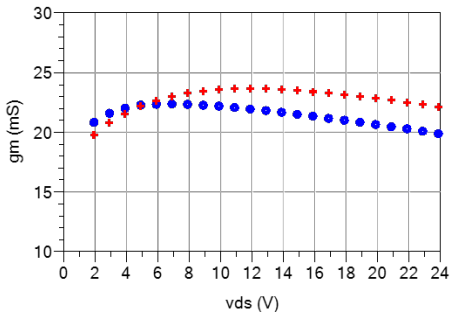


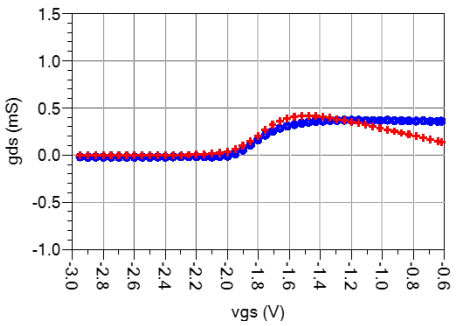
Figure 6.3: Measured (blue) and modelled (red) DCIV curves for a 2 × 50 μm GaN HEMT device.



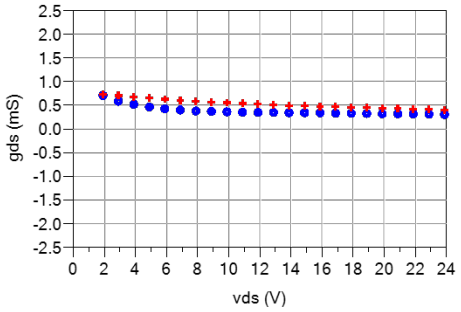
(a) G_m vs V_{GS}.



(b) G_m vs V_{DS}.



(c) G_{ds} vs V_{GS}.

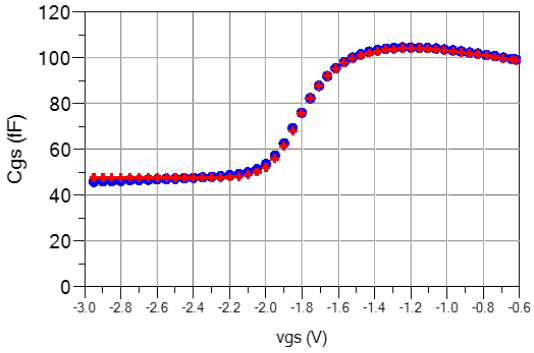


(d) G_{ds} vs V_{DS}.

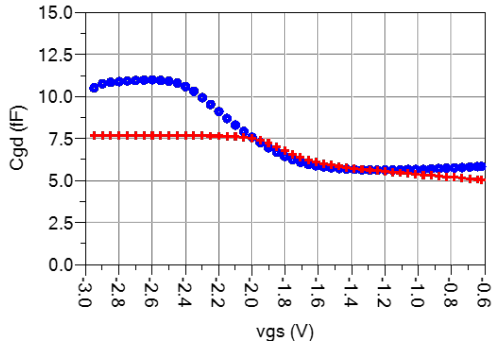
Figure 6.4: Measured (blue) and modelled (red) intrinsic de-embedded model parameters for drain current first derivatives, G_m and G_{ds}, versus slices at V_{GS} and V_{DS}= -1.5 V and 20 V respectively. Frequency of extraction 29 GHz.

Charge Model

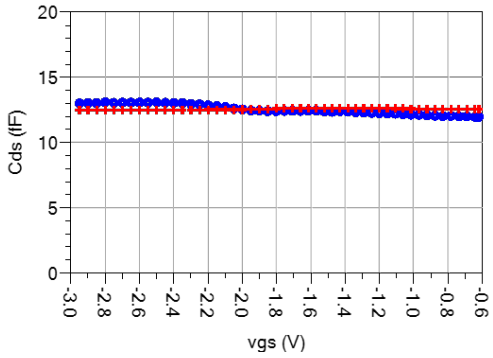
Similarly, the MQFET charge fitting parameters given in Fig. 6.7 are used to fit the measured dispersion-free intrinsic multi-bias capacitance data as shown in Figs. 6.5 and 6.6. A good fit is achieved for C_{gs}, C_{ds}, X_{ds}, although the modelled C_{gd} deviates from the measurement at V_{GS} and V_{DS} below 2 V and 16 V respectively.



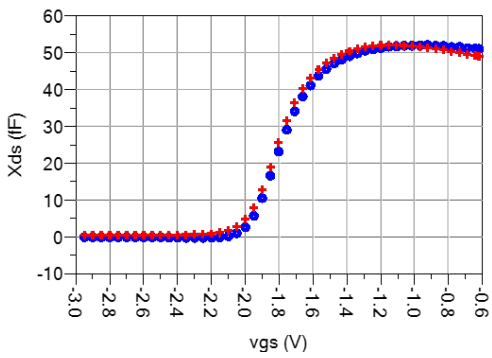
(a) C_{gs}



(b) C_{gd}

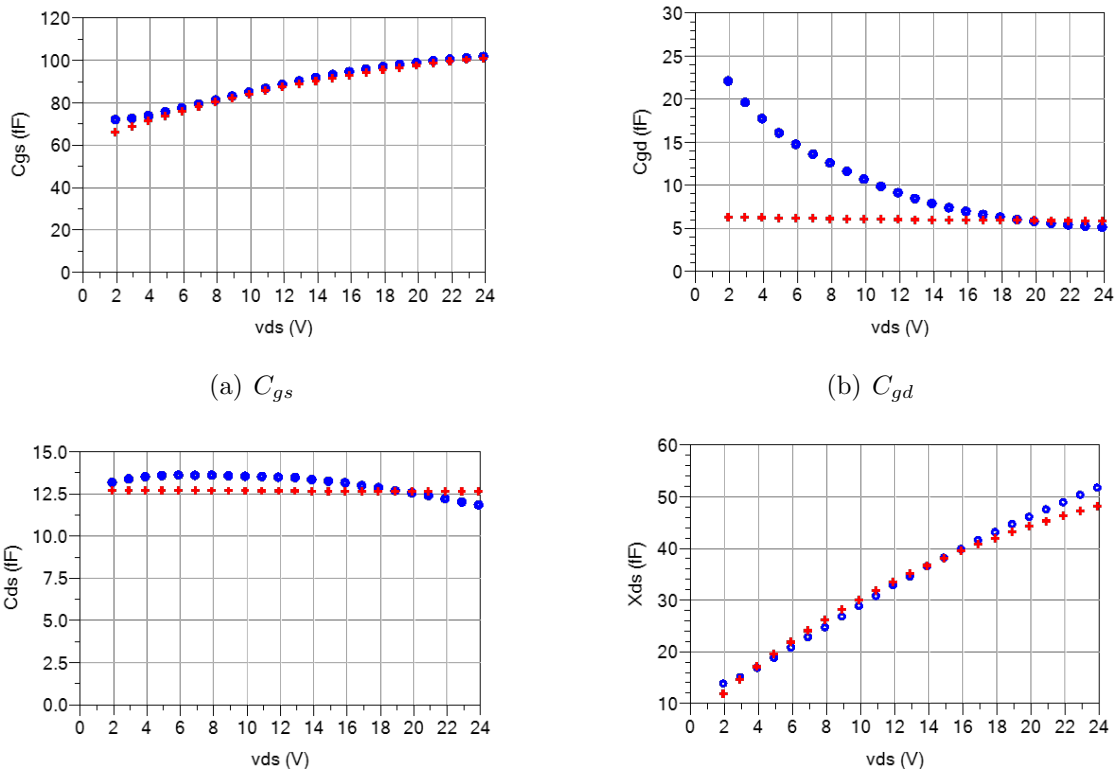


(c) C_{ds}



(d) X_{ds}

Figure 6.5: Measured (blue) and modelled (red) intrinsic de-embedded model parameters for charge derivatives, at V_{DS}= 20 V. Frequency of extraction is 29 GHz.



(a) C_{gs} (b) C_{gd}

(c) C_{ds} (d) X_{ds}

FIGURE 6.6: Measured (blue) and modelled (red) intrinsic de-embedded model parameters for charge derivatives, at V_{GS}= -1.5 V. Frequency of extraction is 29 GHz.

The MQFET model parameters used to achieve the final fit are given in Fig. 6.7.

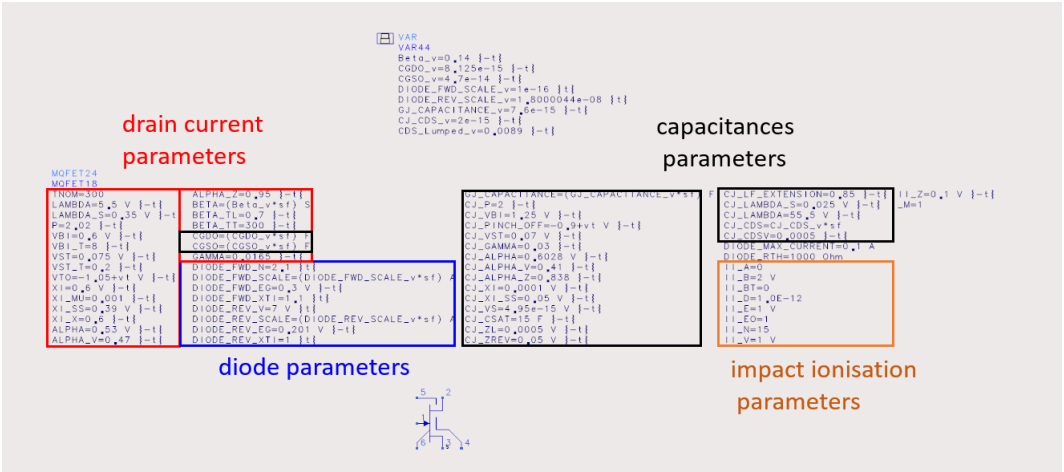


FIGURE 6.7: The values of the fitting parameters of the MQFET large-signal model.

6.3 Model Verifications

The extracted large-signal model for 50 μm single-finger device is used to assemble a complete 2×50 μm model including the extrinisc access network as shown in Fig. 6.8. A good agreement between the complete device model and the measurement of the same device is achieved, see Fig. 6.9.

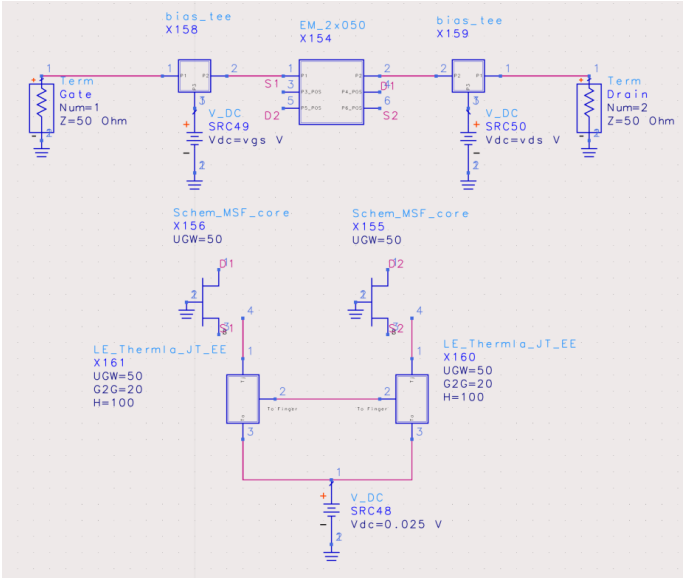
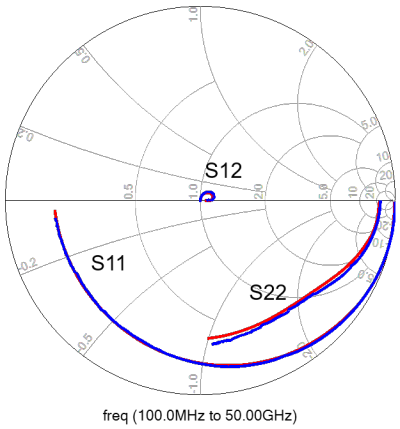
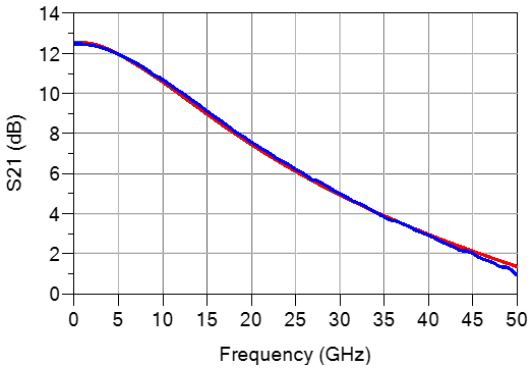


FIGURE 6.8: A schematic of a complete 2×50 μm showing the lumped-element thermal model connection to the thermal node of the model.



(a) 2×50 μm, S_{11}, S_{12}, S_{22}.

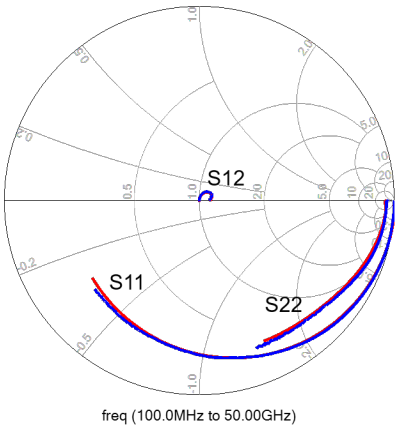


(b) 2×50 μm, S_{21}.

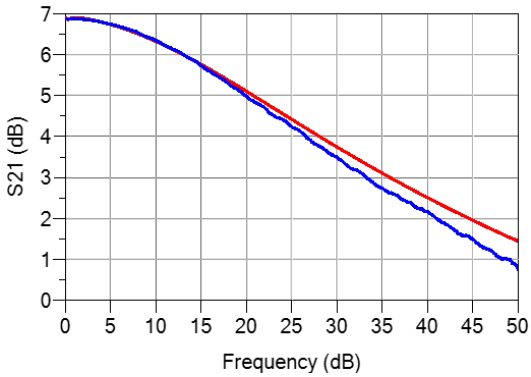
FIGURE 6.9: Measured (blue) and modelled (red) S-parameters for 2×50 μm device, at V_{DS} = 20 V and V_{GS} = -1.5 V over frequencies from 1-50 GHz in 0.1 GHz steps.

6.3.1 New Device Synthesis

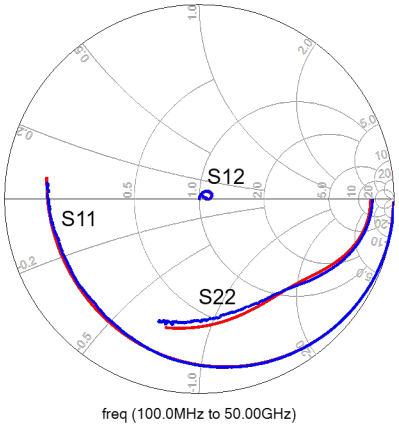
The single-finger, large-signal model is linearly scaled with the gate width and used with new EM simulations to synthesise, 2×25 μm, 2×75 μm and 2×100 μm devices. Excellent agreement between measured and synthesised devices is achieved as shown in Fig. 6.10.



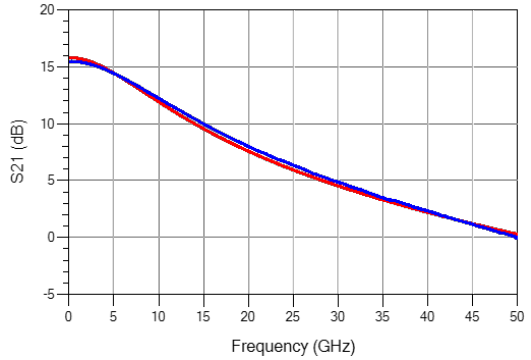
(a) 2×25 μm, S_{11}, S_{12}, S_{22}.



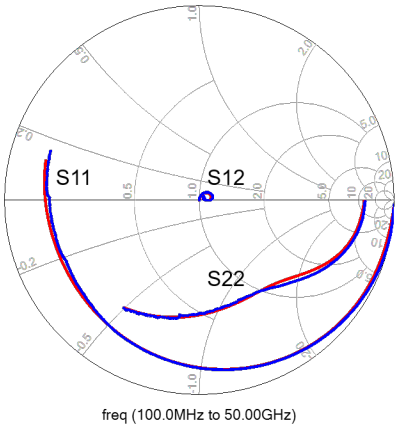
(b) 2×25 μm, S_{21}.



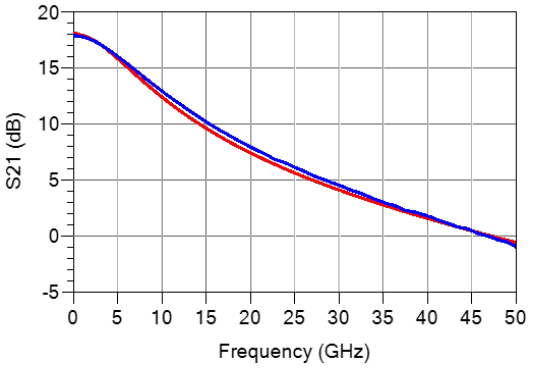
(c) 2×75 μm, S_{11}, S_{12}, S_{22}.



(d) 2×75 μm, S_{21}.



(e) 2×100 μm, S_{11}, S_{12}, S_{22}.



(f) 2×100 μm, S_{21}.

Figure 6.10: Measured (blue) and modelled (red) S-parameters for several 2-finger devices, at V_{DS} = 20 V and V_{GS} = -1.5 V over frequencies from 1-50 GHz in 0.1 GHz steps.

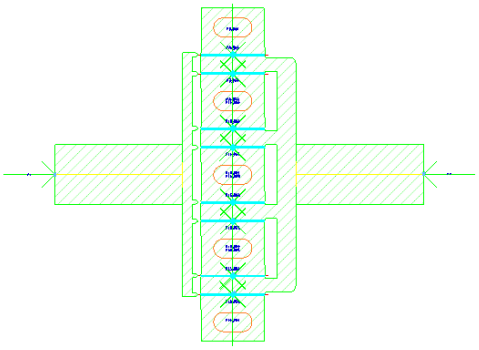


FIGURE 6.11: A Momentum EM layout of an 8×100 μm device.

The large-signal model is used to accurately predict the performance of devices that have not been measured or modelled before. Fig. 6.12 shows a complete large-signal model of an 8×100 μm device including the lumped-element thermal network and trap model which is connected to the MQFET trap node one level down in the schematic hierarchy. The metalisation of the device is analysed using Keysight ADS Momentum, the EM layout is shown in Fig. 6.11. The combined model incorporating electromagnetic passive and intrinsic active components is able to accurately predict the small-signal performance of the device as shown in Fig. 6.13.

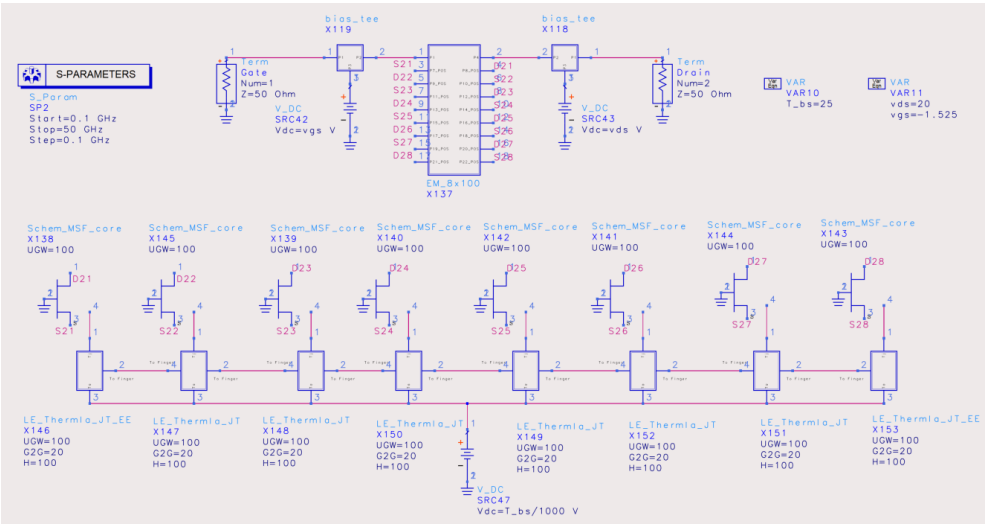
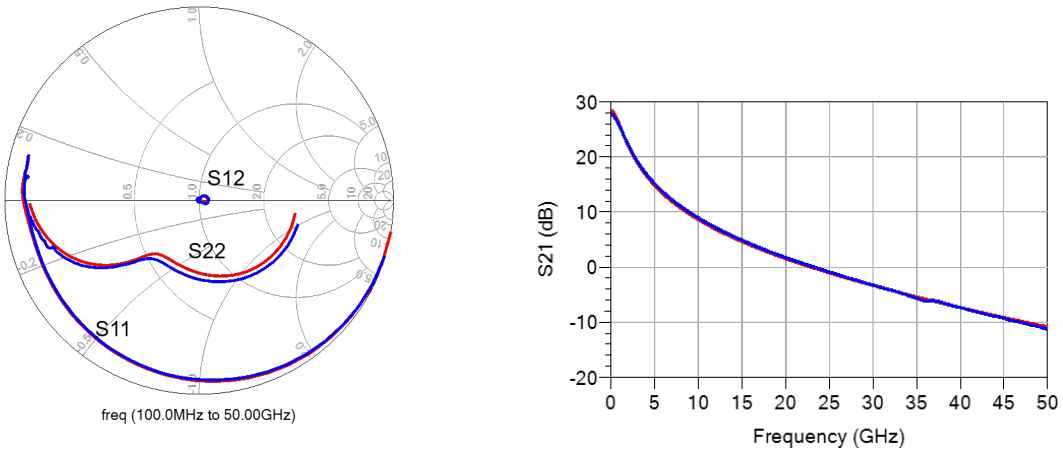


FIGURE 6.12: A schematic of a complete 8×100 μm device showing the lumped-element thermal model connection to the thermal node of the model.



(a) S_{11}, S_{12}, S_{22}. (b) S_{21}.

Figure 6.13: Measured (blue) and modelled (red) S-parameters for an 8×100 μm device at V_{DS} = 20 V and V_{GS} =-1.5 V over frequencies from 1-50 GHz in 0.1 GHz steps.

6.3.2 Large-signal Verification

The large-signal performance of the model is verified against load-pull measurements. A simulated load-pull test bed schematic is constructed to simulate a 4×50 μm device model as shown in Fig. 6.14. The simulation is performed at 29 GHz to match the load-pull data provided by the foundry. Excellent agreement is achieved between the measurement and simulated load-pull target for maximum output power and nearby contours as shown in Fig. 6.15. The simulated maximum output power the load-pull target is 3.5 W/mm with 52% PAE while the measurement has maximum output power and PAE of 3.3 W/mm and 50% respectively.

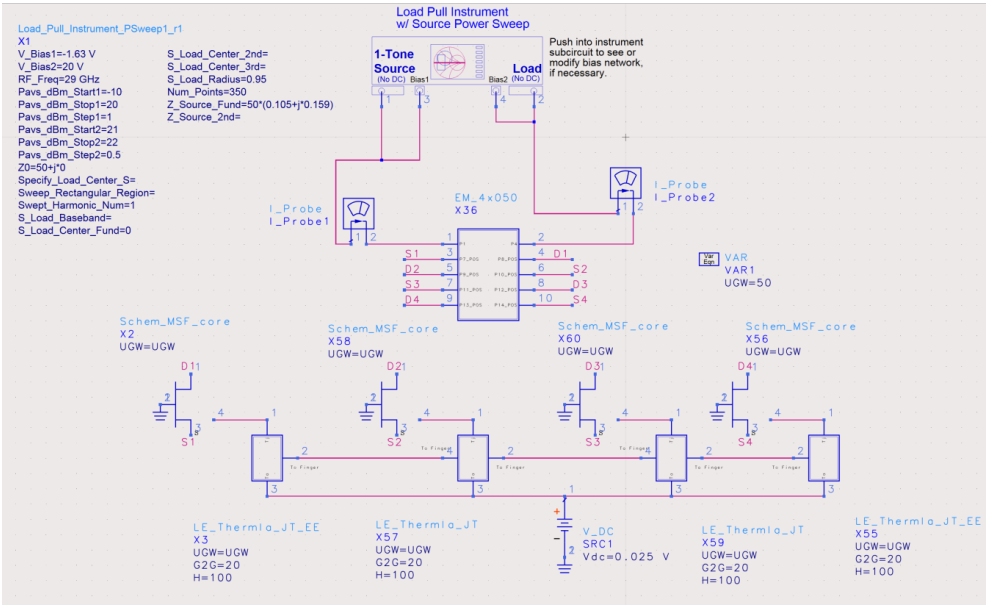
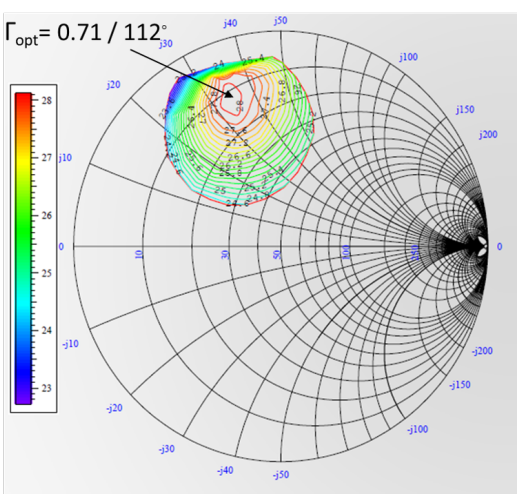
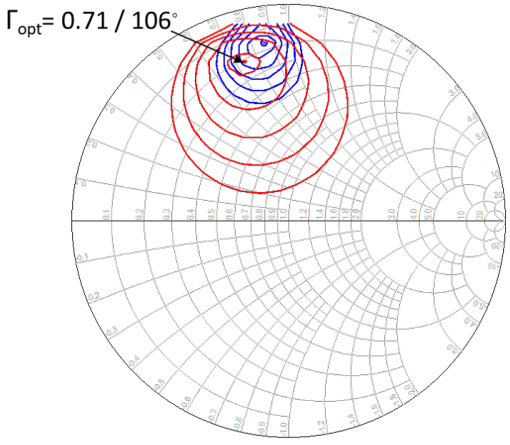


FIGURE 6.14: A load-pull schematic used to simulate power and PAE contours for a 4×50 μm device.



(a) Measured load-pull contours.



(b) Simulated load-pull contours for maximum power (red) and maximum PAE contours (blue).

FIGURE 6.15: Measured and simulated load-pull contours at 29 GHz taken at quiescent bias of V_{DS} = 20 V and V_{GS} = =-1.5 V.

6.3.3 Scaling Limits

Scaling factor of 1:8 is demonstrated which resulted from scaling the gate-finger from 50 μm to 100 μm and scaling the number of fingers from 2 to 8. In principle, the number of fingers can scale to as many as required. EM tools, in general, can handle up to hundreds of these fingers. However, the scaling limitation may arise from scaling the gate-finger which is bound by the maximum frequency of operation. This limit may be approximated by 5% of the wavelength at the maximum frequency of operation according to [93], i.e., at 40 GHz, the maximum width for a single finger that can be used is 375 μm. Investigating instability at higher frequencies might be a limitation to what can be achieved in terms of finger scaling. In this case, the gate-finger may be divided into smaller segments as shown in [94].

6.4 Summary

A complete large-signal intrinsic model that incorporates thermal and trap feedback networks is presented in this chapter. The model scales linearly with the width of the device and is able to accurately predict the small-signal performance devices with a range of sizes and geometries. The model is consistent with the small-signal model and can therefore replace it. The model is also able to accurately predict the load-pull target for a synthesised device quite accurately. The utility of this model is demonstrated in Chapter 7 where it is used to design a wideband high power amplifier.

7

Case Study

In Chapter 6, a complete large-signal intrinsic model is developed which scales linearly with device sizes, in terms of small-signal and large-signal performance.

In this chapter, the complete large-signal intrinsic model, is used to design a wideband nonuniform distributed power amplifier (NUDPA). The main goal in this design is to achieve more than 10 watts of saturated output power and to cover X, Ku and Ka bands which means covering the frequency band from 8 to 40 GHz with small-signal gain of more than 20 dB. This circuit is considered to be a complex and very challenging design given the requirement of delivering 10 W over a very wide bandwidth and it is believed that the combination of these specifications have not been addressed before. A list of existing state-of-the-art wideband high power amplifiers are given in table 7.1.

This design is chosen to validate the nonlinear modeling approach described in

TABLE 7.1: Existing wideband high power amplifiers.

Frequency Range (GHz)	Power (W)	Reference (#)
16-40	7-16	[95]
6-37	1-1.6	[96]
17-43	10-16	[97]
17-36	3-5	[98]

this thesis in every possible aspect including, scaling the model with device width and scaling load-pull targets with frequency.

7.1 Distributed Power Amplifier Design Challenges

The principle of distributed amplifier (DA) is to extend the gain-bandwidth product of devices by embedding multiple transistors between two artificial transmission lines, one connected to the gate terminals and the other to the drain terminals. In such a configuration, gate and drain capacitances are absorbed into the shunt capacitance of the artificial line and the bandwidth can be extended to the cutoff frequency of the line. Distributed amplification is very effective for applications that require broadband operation but unfortunately, distributed amplifiers have limited power and efficiency capabilities and they can only deliver a fraction of the theoretical combined power capability of the transistors used. Several power limiting factors can be identified for this topology [99], [100]. More efficient power combining techniques have been already demonstrated in both GaAs and GaN technologies by using the nonuniform distributed power amplifier topology [101] [102]. This topology facilitates broadband combining but with more efficient power combing over the conventional distributed amplifiers.

According to the maximum power transfer theorem, a power source with internal resistance, R_p, delivers maximum power into a load resistance of R_L when $R_L = R_p$. The load impedance R_L is typically fixed by convention, e.g. 50 or 75 Ω. The maximum

ac voltage swing at the transistor output terminal is limited by the breakdown voltage of the transistor. The process that is used in this design has a breakdown voltage in excess of 100 V and is qualified to operate reliably at maximum drain voltage of 20 V. The combination of the system impedance and maximum operating voltage limits the maximum output power that can be achieved.

To scale up the output power capability, more parallel transistors are needed or bigger transistors which results in R_p being much lower than the system load impedance (50 Ω in this case). In order to exceed the maximum power limitation, impedance transformation is required so that a lower load impedance is presented to the transistor-based amplifying device. However, for an acceptable return-loss bandwidth, impedance transformation has fundamental bandwidth limitations, as described by the Bode-Fano criterion [103]. In order to simultaneously meet the design bandwidth and power requirements, a high ratio wideband impedance transformer is required.

Generally, the optimum load target for a device needs to be determined in the early stages of a design, or even before it is started, in order to guarantee best possible performance. The optimum load target for operation may be determined by performing load-pull measurements, large-signal model simulations or theoretical calculations. Traditionally, at microwave and millimeter-wave frequencies, measured targets are preferred and more trusted by design engineers over simulated or calculated targets. This is mainly due to the lack of an accurate large-signal model that scales with device size and converges reliably when heavily saturated, or the difficulty in developing such a model. However, load-pull systems operating at the required frequencies are not always available to designers, or they can be expensive to set up, and even when a load-pull system is available, they tend to be time-consuming and cumbersome to calibrate and operate. Calibration of load-pull tuners or systems is a lengthy process which may take days of effort depending on the number of impedances and frequency points required.

Load-pull of a single device sample over a range of bias conditions and frequency points could take several days. Usually there are several devices of interest to the designer, which means the measurement process is repeated for different device sizes and layouts, leading to a lengthy and costly measurement exercise. In addition, bandwidth

and power handling capability are common limitations in load-pull systems.

Active and hybrid-active load-pull systems are capable of presenting high reflection coefficients to the DUT terminals, but this capability comes at the expense of other challenging and complex requirements. Examples of these requirements include a dedicated 4-channel VNA, signal generators to required number of harmonics, high power laboratory amplifiers to achieve high reflection coefficients and couplers. A common rule of thumb is that the laboratory amplifiers used for active load-pull must be capable of delivering ten times the output power of the DUT.

7.1.1 Intrinsic Load-pull Target

One of the major advantages of the nonlinear single-finger model developed in this thesis, is that it can be scaled in width and embedded in an arbitrary device geometry, extending the model utility to devices that have never been fabricated or not available in the PDK to the circuit designer. The model shows good agreement with measurements over a wide range of biases, and extrapolate accurately in frequency beyond the original range of characterisation data.

It is widely accepted, based on theoretical analysis, see Cripps, [104], and experimental measurements of FETs, that the conjugate of the optimum power-matched load, as observed at the intrinsic controlled current source, is equivalent to a constant conductance in parallel with a constant capacitance over a very wide frequency range. This concept is especially useful for low-frequency applications, where the parasitics of the device are insignificant or small and thus, they can be accurately measured and modelled, without needing to de-embed the device parasitics. The large-signal single-finger model described here is a key enabler for this concept to be extended to microwave frequencies where device parasitics have a strong influence on the device behaviour.

Having reduced the non-linear behaviour to the pure intrinsic device model, the optimum load-pull target can be described simply as a frequency invariant conductance in parallel with a frequency invariant capacitance both scaling linearly with gate width.

Assuming that dynamic thermal and trapping effects are negligible at the operating

frequency, a measured load-pull target can be de-embedded to the intrinsic device plane, or deduced from nonlinear simulations directly at the same circuit node [68]. The de-embedded intrinsic target can then be transformed to the output accessible terminal of an arbitrary device layout inclusive of the parasitic effects of the access network and the interaction of multiple gate fingers, thereby accurately, predicting its load-target.

The load-pull target for maximum drain efficiency is obtained from a load-pull measurements taken on a 4×50 μm device at the bias conditions of V_{DS} = 20 V, Id = 100 mA/mm and a frequency of 29 GHz. The measured load-pull target is then transformed to the intrinsic device plane similar to what is shown in [105]. The target transformation is done using the electromagnetic model of the extrinsic access network and the common-gate large-signal intrinsic model extracted in previous chapters. The load-pull target transformation is done as follows:

- A model for the measured load-pulled device is created using the EM of the extrinsic access network with internal ports and the single-finger intrinsic model which can be a linear or a nonlinear model in this case. Then the measured optimum load impedance is presented at the extrinsic drain terminal.
- The impedance looking out of each common-gate single finger is calculated using the reflection coefficients at the intrinsic drain terminal.
- The average complex impedance of all the fingers is then converted to admittance to get the G_{opt} and C_{opt}.

The optimum impedance to be presented at the intrinsic device drain terminal is

$$Z_{opt} = R_{opt} + jX \tag{7.1}$$

$$Y_{opt} = \frac{1}{R_{opt} + jX} \tag{7.2}$$

$$Y_{opt} = \frac{R_{opt}}{R_{opt}^2 + X^2} - j\frac{X}{R_{opt}^2 + X^2} \tag{7.3}$$

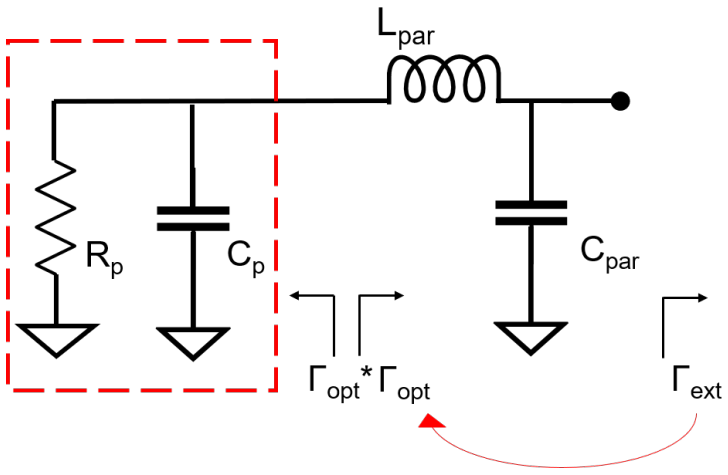


FIGURE 7.1: Equivalent R_p and C_p representation of the intrinsic large-signal model.

The conjugate of 7.3 gives the admittance looking into the device

$$Y_{opt}{}^{*} = G_{opt} + jB_{opt} \tag{7.4}$$

Where G_{opt} equals to $R_{opt}/(R_{opt}^2 + X^2)$and B_{opt} equals to $X/(R_{opt}^2 + X^2)$.

This leads to a simplified representation of the large-signal optimum loading conditions as shown in Fig. 7.1 where $R_p = 1/G_{opt}$ and $C_p = B_{opt}/\omega$.

R_p and C_p should scale linearly with gate width since they represent the the intrinsic device with no parasitic effects. Therefore a common way of describing these two values normalised to the units of gate width such as

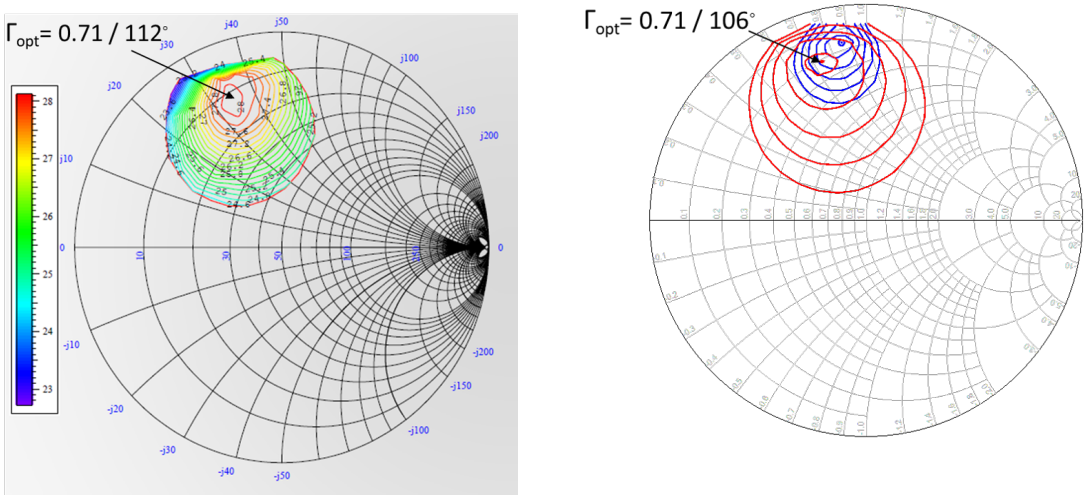
$$R_p = \frac{W}{G_{opt}}(\Omega.mm) \tag{7.5}$$

$$C_p = \frac{B_{opt}}{\omega.W}(pF/mm) \tag{7.6}$$

The measured load-pull target for the 4×50 μm device shown in Fig. 7.2, is transferred to the single-finger common-gate intrinsic drain target and then converted to a common-source representation, giving the optimum intrinsic load-pull target for a 50 μm finger of $175 + j298$ Ω.

7.1.2 Load-pull Target Scaling

The nonlinear model is verified against measured load-pull data which has been provided by the semiconductor foundry. Only one device has been measured and provided by the foundry and this devise is a 4×50 μm FET. Good agreement is obtained between the optimum power-matched loads provided by the foundry and that obtained from nonlinear simulations as shown in Fig. 7.2.



(a) Measured power contours.

(b) Simulated contours of maximum power (red) and PAE (blue).

Figure 7.2: Measured and simulated load-pull power contours at 29 GHz for 4×50 μm device. Quiescent bias is: $V_{DS} = 20$ V and $I_{DS} = 100$ mA/mm.

The optimum load target shown in Fig. 7.2 is converted to the device intrinsic drain terminal in order to determine R_P and C_P. For the purpose of this distributed amplifier design, only the real part, R_P, must be known so that it can be used to determine the

characteristic impedance of each drain line section which is tapered to achieve a near optimum load for all the transistor cells. The lengths of each segment of the drain line are adjusted such that the transistor currents combine in phase and the optimum load capacitance C_P is absorbed in the artificial transmission line.

Fig. 7.3 shows the simulated dynamic load-lines for the outermost finger of a 4×50 μm device at 29 GHz when the optimum load target is presented accessible drain terminal of the device.

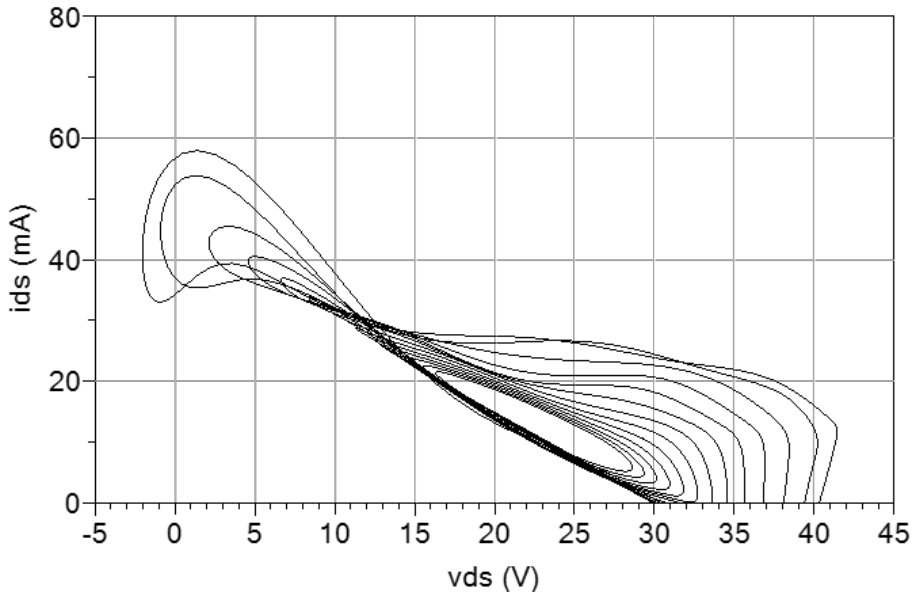


FIGURE 7.3: Simulated dynamic load-lines for the outermost finger of a 4×50 μm device at 29 GHz. Quiescent bias is: $V_{DS} = 20$ V and $I_{DS} = 100$ mA/mm.

Based on [102], the characteristic impedance for optimum load is given as

$$\frac{R_P(\Omega.mm)}{R_L} = \sum_{i=1}^{N} W_{Q_i} \tag{7.7}$$

7.1.3 Cripps Optimal Load line

Maximum power transfer occurs when the the load impedance R_L equals the source impedance R_s, assuming the source reactance is negated, i.e conjugally matched. The maximum output power delivered to the load is given by

$$P_{max} = \frac{V^2}{2R_L} \tag{7.8}$$

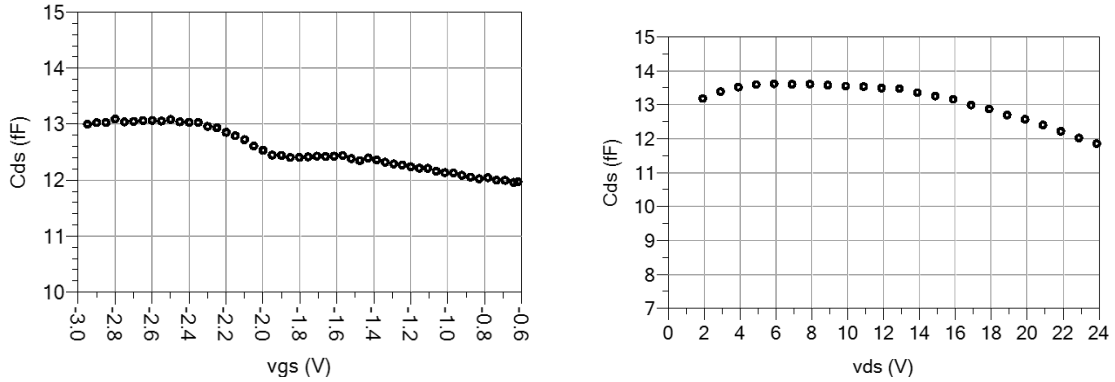
According to Cripps load-line theory [104], the optimum load line for maximum output power for class A operation is achieved when the load impedance R_L is equal to R_{opt} where R_{opt} is the internal resistance of the source and the source in this case is the FET device. This R_{opt} is given by

$$R_{opt} = \frac{2(V_{dc} - V_{knee})}{I_{max}} \tag{7.9}$$

For $V_{DC} = 20$ V, V_{knee} of 2 V and I_{max} of 0.9 A/mm, equation 7.9 gives normalised R_{opt} of 40 $\Omega.mm$. C_p can be approximated by the intrinsic value of drain capacitance, C_{ds} which was already extracted for different device widths in Chapter 3. A C_{ds} value of 14 fF per 50 μm is obtained form Fig. 3.27 (g) in Chapter 3, which gives a normalised value of 0.28 pF/mm.

The assumption here that C_{ds} is constant with input power and this approximation seems reasonable given that C_{ds} is almost constant with gate-source V_{GS} and drain-source V_{DS} potentials as shown in Fig. 7.4.

$$Z_{opt} = \frac{1}{Y_{opt} \parallel G_{ds}} \tag{7.10}$$



(a) C_{ds} vs v_{gs} at v_{ds}=20 V. (b) C_{ds} vs v_{ds} at v_{gs}=-1.5 V.

FIGURE 7.4: Extracted output drain-source capacitance, C_{ds} fo 50 μm gate-finger.

and in terms of R_{opt} and C_p, the optimum impedance Z_{opt} can be written as

$$Z_{opt} = \frac{R_{opt}}{1 + G_{ds}R_{opt} - j\omega C_{ds}R_{opt}} \tag{7.11}$$

For 50 μm total device periphery, G_{ds} is extracted as 0.5 mS per 50 μm finger, Z_{opt} at 29 GHz is calculated to be *176 + j281* Ω.

To cross-check with the measured load-pull target that is supplied by the foundry for 4×50 μm device, the Cripps load-pull target for maximum output power obtained above is transformed to the extrinsic drain terminal, giving Γ_{opt} of $0.71\angle 115°$ which is almost identical to the measured load-pull target shown in Fig. 7.2 (a). The extrinsic Cripps load-pull target of the 4×50 μm device predicts the measured load-pull target very well which gives confidence in using the measured load target and scale it up or down for for different device geometries used in the design.

7.2 Design

In order to achieve the design targets of power, gain and efficiency simultaneously over more tha two octaves of bandwidth, a detailed trade-off analysis is done in order to identify the optimum transistor device geometry for each unit cell. For a broadband

distributed amplifier, the gain-bandwidth product is constant which means gain will be reduced for wider bandwidths.

A rough estimate of the total FET periphery needed to achieve 10 W of output power can be made using the known limitations of the process technology and some idealised assumptions such as a 20 V drain supply, Class A operation and sinusoidal excitation. Under these conditions, and assuming a system load impedance of 50 Ω, It is found that the maximum achievable power is only 6 W, which falls well short of our design target.

By looking closely at equation 7.9, two options are available to increase the output power to increase the supply voltage or reduce the load impedance. Increasing the drain voltage is not possible since the process is only qualified up to 20 V operation. Operating at higher drain voltage may lead to inconsistent circuit performance or premature device degradation and failure. The only option remaining is to reduce the load resistance to approximately 15 Ω in order to achieve 10 W from the 20 V supply voltage. Assuming the amplifier external load impedance must remain as 50 Ω, this necessitates a broadband and low-loss impedance transformer. The necessary bandwidth and impedance transformation ratio poses considerable challenges for the implementation in planar MMIC form in a compact die area. Reducing R_L means reducing R_p of the whole DA by increasing the size of each unit cell transistor. However, doing so can have the undesirable effect of reducing the achievable gain at high frequencies. This is another challenge to be overcome in the design.

A single-ended cascade of three distributed gain stages is chosen for this design in order to achieve the desired gain where each stage is a NUDPA on its own. Each stage consists of a NUDPA is designed separately with internal 50 Ω interfaces between stages and 6 to 8 dB of gain per stage. The final stage with 10 W output power is designed first. Ten transistor cells were found necessary in order to achieve the power, gain and bandwidth requirements. A idealised analysis is shown in table 7.2 which estimates the total gate periphery needed to achieve the required power as well as the characteristic impedance at each drain terminal. The total periphery is the divided

TABLE 7.2: Calculated characteristic impedance of each drain line section in the NUDPA which then is used as a starting value during in the early stages of the design.

NUDPA Design Parameters	Element (i)	W_Q (mm)	$\sum W_i$ (mm)	Z_{0i} (Ω)	W_{0i} (μm)
R_p **(Ω.mm) = 40**	1	0.25	0.25	160	5
V_{dc} **(V) = 20**	2	0.25	0.5	80	26
V_{knee} **(V) = 2**	3	0.25	0.75	53	82
Total Periphery (mm) = 2.5	4	0.25	1	40	145
Number of Elements = 10	5	0.25	1.25	32	213
Maximum Power (W) = 10	6	0.25	1.5	27	287
	7	0.25	1.75	23	350
	8	0.25	2	20	425
	9	0.25	2.25	18	488
	10	0.25	2.5	16	569

into parallel elements to maximise the total gain that can be achieved in the NUDPA. Ten transistor elements is found to be the best trade-off between power and gain with each element is 4×62.5 μm (i.e., 250 μm of gate periphery).

7.2.1 Transistor Unit Cell Optimisation

The large-signal intrinsic model is used in a trade-off study to determine the optimum device size for the design. The trade-off study includes, but is not limited to, merits such as power, gain , efficiency, temperature, and die area.

Fig. 7.5 shows the maximum available gain for different device unit cells. At 40 GHz, the 4×62.5 μm device has one dB more gain than the 2×125 μm and gives very similar gain to the 8×31.25 μm. Theoretically, the three devices should be capable of delivering the same output power, however, the aim here is to use the optimum device for power without compromising gain, efficiency and die area.

The results suggest that either the 4×62.5 μm and the 8×31.25 μm offer similar

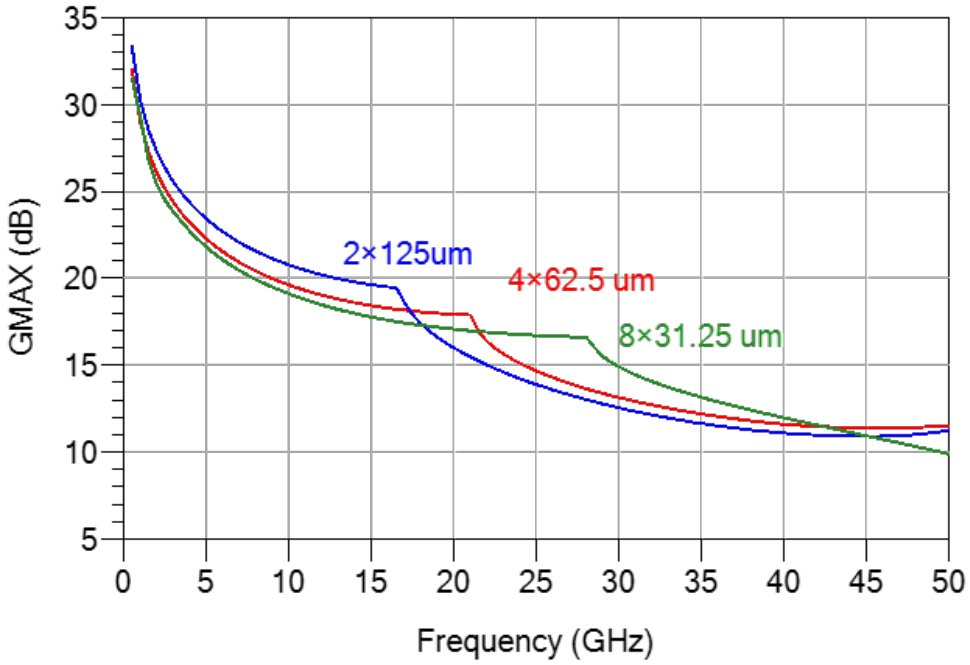


Figure 7.5: Maximum available gain comparison for three devices with 0.25 mm total gate periphery.

available gain around the upper frequency limit of the design, however, the 4-finger device is chosen for this design over the 8-finger for its compact layout.

7.2.2 Broadband Impedance Transformer

Fig. 7.6 shows simulated insertion loss and return loss for microstrip quarter-wave transformers with input impedances of 15, 25 and 35 ohms and an output impedance of 50 Ω. The bandwidth can be achieved with 10 dB return loss is less than an octave making it unsuitable for use in this wideband design. in this design. A wideband, low loss and compact planar impedance transformer is needed to transform the 50 Ω to 15 Ω over 8 to 40 GHz. There are a few planar monolithic wideband transformers suitable for MMIC designs reported in the literature such as the Ruthroff with 4:1 transformation ratio used in [95] and Trifilar with 2.25:1 ratio used in [106]. Unfortunately, these transformers do not meet the bandwidth requirements of this design and besides this,

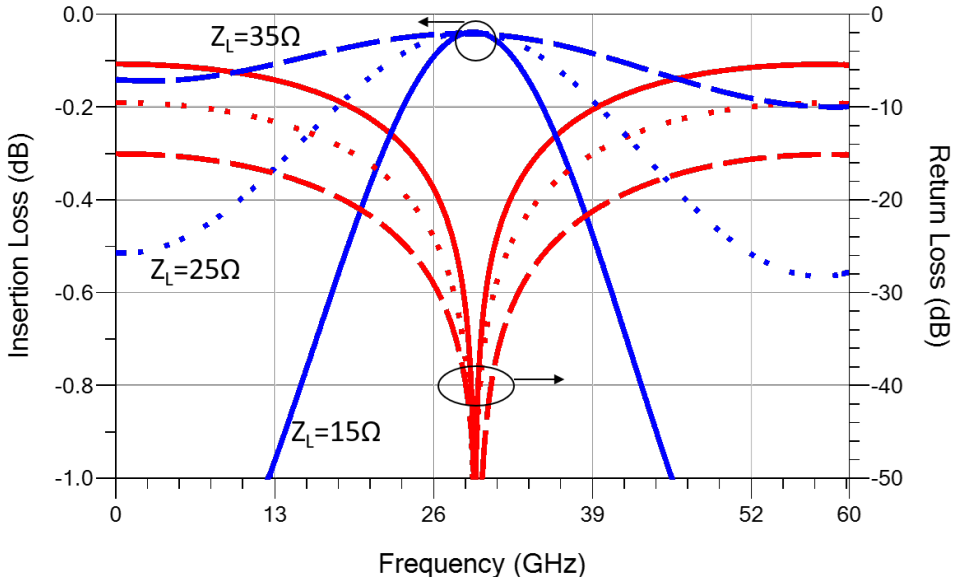


FIGURE 7.6: Quarter-wave microstrip transformer with different load impedance transformation ratios based on 50 Ω system impedance.

they are protected by patents which restrict their use.

A transformer is required that is wideband and capable of high transformation ratio such as 4:1. The outcome of the research has resulted in a novel wideband, planar and low loss impedance transformer capable of very high power handling called the "Folded Patches Transformer" (FPT) (patent pending). The FPT consists of two asymmetrical coupled patches, the input port is connected to a central line and this middle line that is tightly coupled to the patch below it and loosely coupled to the patch above it. The middle line is connected to the far corner of the upper patch through a short, high impedance line, and the upper and lower patched are joined together near the input port by an air-bridge connection. The output port is taken from the end of the bottom patch through a short section of a low-impedance transmission line.

The FPT is very compact and this example measures 1 mm $\times$0.7 mm, making it an attractive and cost-effective solution for use in MMICs as a wideband impedance transformer or a matching element.

Fig. 7.7 shows a photograph of fabricated test structure of the of 4:1 FPT covering the frequency range of 5-40 GHz and fabricated on a 100 μm SiC substrate.

Fig. 7.8 show measured results of three FTP samples demonstrating high uniformity and low sensitivity to manufacturing variations. The measured results also show excellent agreement with the ADS Momentum electromagnetic simulations as shown in Fig. 7.9.

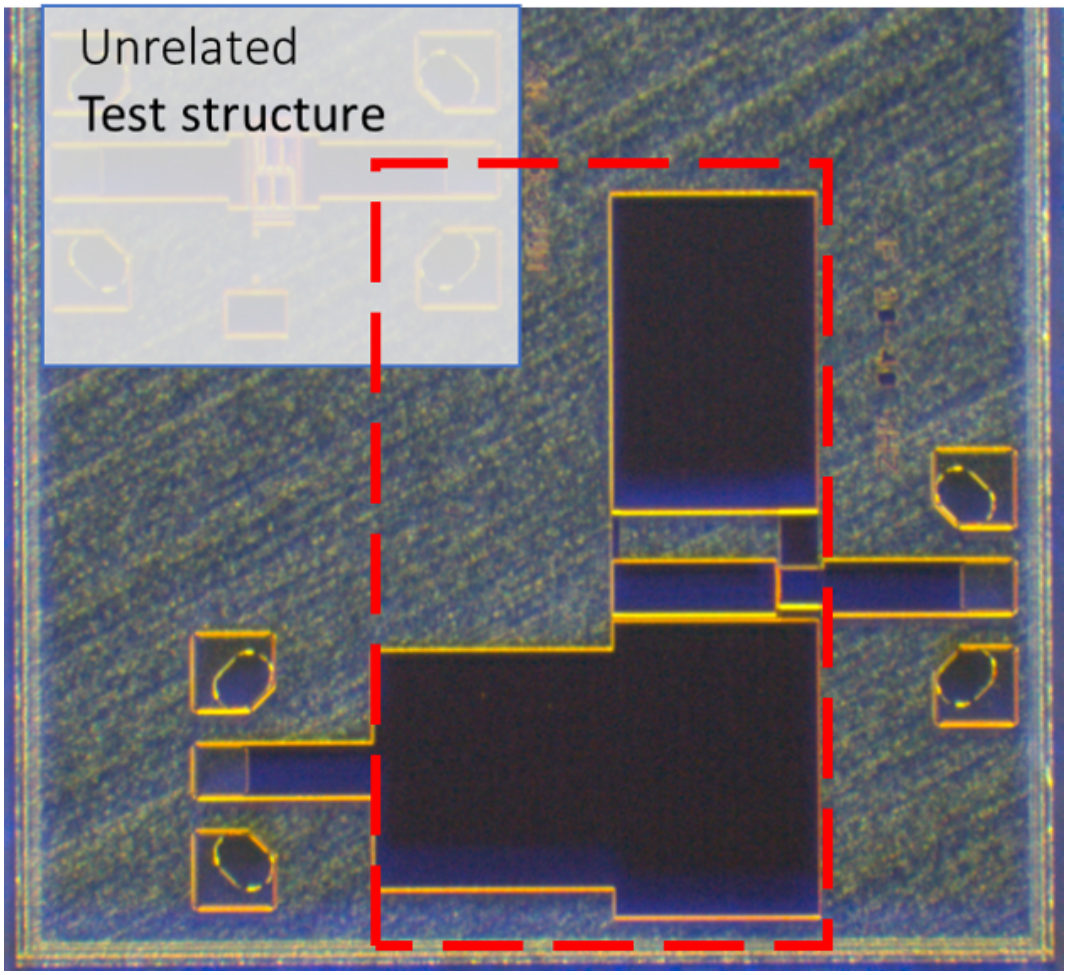


Figure 7.7: FPT structure fabricated on 100 μm SiC wafer.

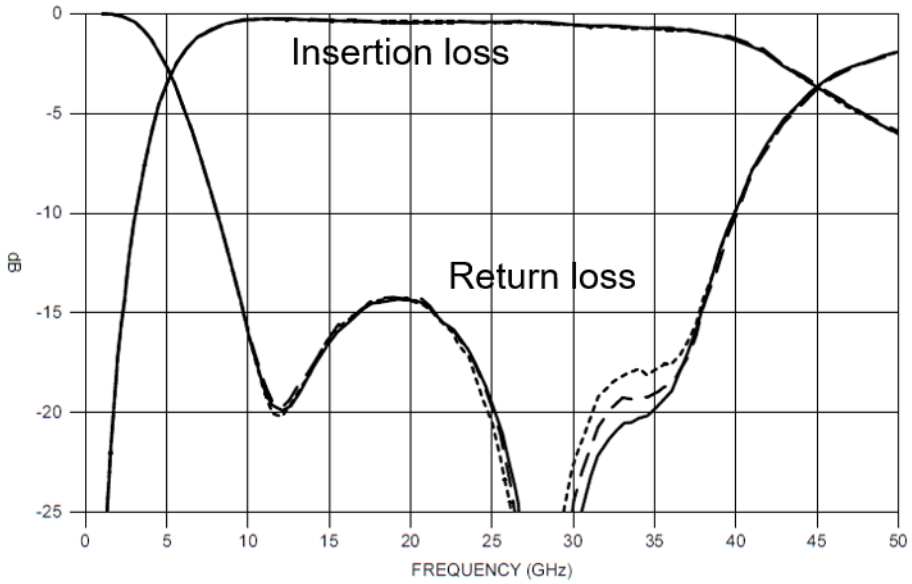


FIGURE 7.8: Measured insertion loss and return loss for three samples of the FPT fabricated on 100 μm SiC wafer.

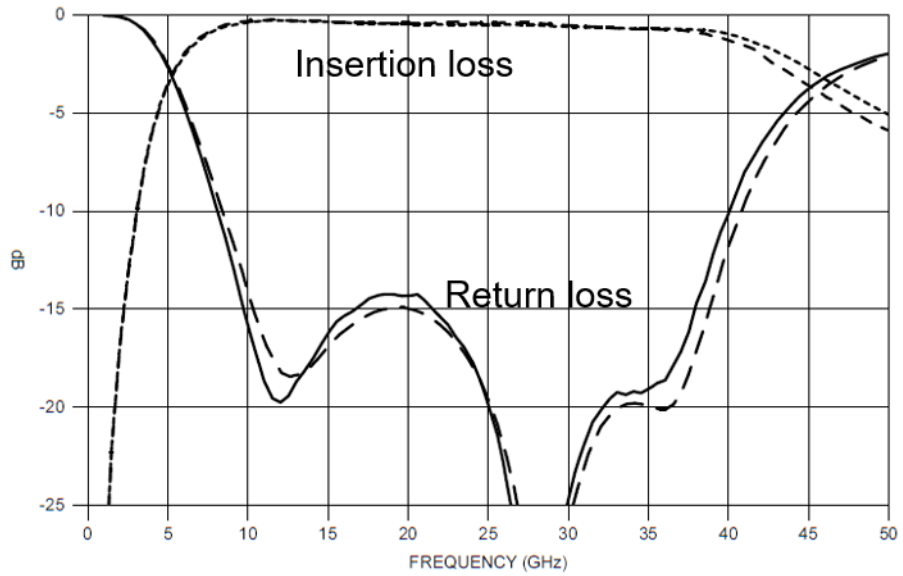


FIGURE 7.9: Measured (dashed line) and simulated (solid line) results of 4:1 FPT fabricated on 100 μm SiC wafer.

The maximum power estimated intable 7.2 is ideal and does not account for losses such as drain line losses, the insertion loss of the impedance transformer and transition

loss including bond wires. Therefore, in order to achieve more than 10 W of output power at the customer board and across the full band of interest, almost 3 dB more power, is needed at the drain terminal of the last element to overcome 3 dB of output loss. The 3 dB might seem pessimistic, however, simulations tend to underestimate losses, and from the measurement of the FPT, the insertion loss is about 1 dB, another 1 dB can be attributed to the die transition including bond wires and 1 dB margin is included to allow for manufacturing variations and modelling error.

To increase the output power by 3 dB, the total gate periphery needs to be doubled, i.e. the R_p becomes 7.5 Ω instead of 15 Ω. An 8:1 transformer with more than two octaves of bandwidth is extremely difficult to implement in a compact planar form for MMIC integration. Having smaller R_p also means the unit cell devices will need to be doubled in size and will have much less gain. A more practical approach is to combine two of NUDPAs with half the desired total power, however, given the bandwidth of this NUDPA, it is not straightforward.

A Lange coupler is commonly used for planar power combining at microwave frequencies. However, a Langer coupler based power combiner typically has bandwidth of around one octave, which falls far short of the target for this design.

What is needed is a wideband, low loss, compact planar power combiner that can present a constant impedance to each NUDPA over the full operating bandwidth. The input power splitter is less critical in this particular case, since the output power is found to be less sensitive to the presented input impedance, whose variation over the operating band can be compensated in other ways. This has led to a novel idea of combining two broadband folded patch transformers in parallel in a configuration similar to a Wilkinson power combiner, but with impedance transforming properties. The resulting impedance transforming power combiner has almost the same bandwidth as the single folded patch transformer. The layout of this impedance transforming power combiner and its simulated performance are shown in Fig. 7.10 and Fig. 7.11 respectively.

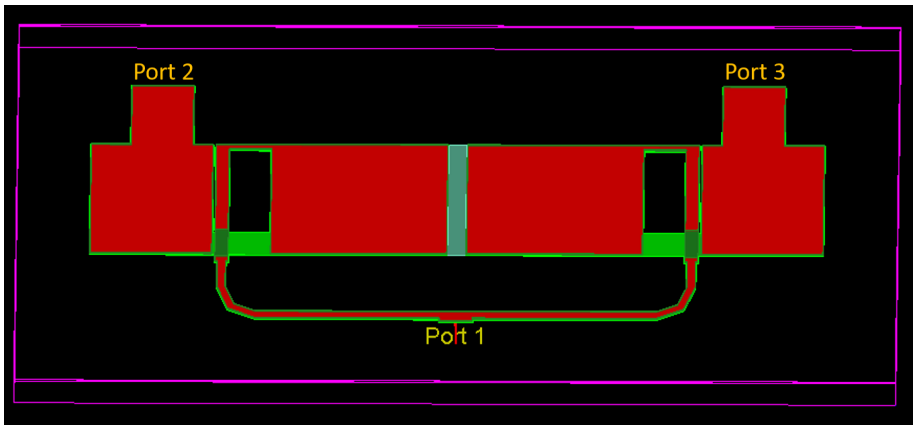


FIGURE 7.10: An 8 to 40 GHz broadband power combiner with 4:1 impedance transformation used to combine two NUDPAs.

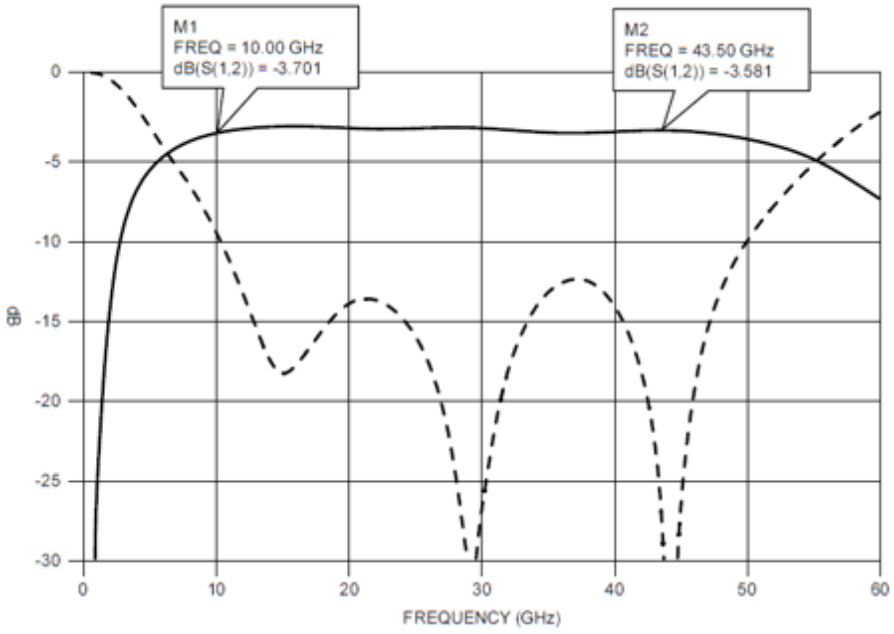


FIGURE 7.11: Simulated insertion loss (solid line) and return loss (dashed line) for the proposed combiner and 4:1 impedance transformer used to combine two NUDPAs.

The design architecture is shown in Fig. 7.12.

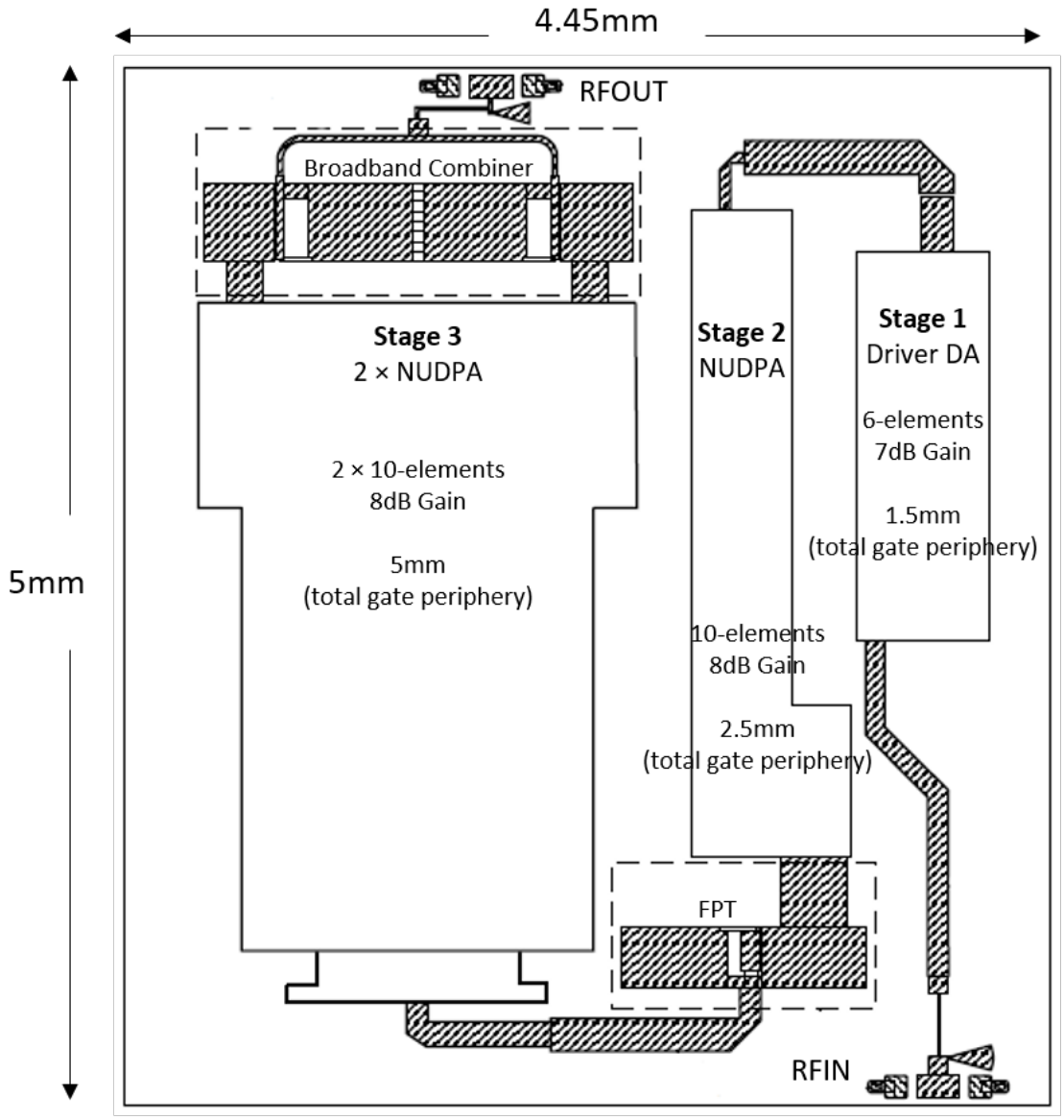


Figure 7.12: The NUDPA circuit architecture.

The aim of this chapter and this particular design exercise is to validate the developed nonlinear model and demonstrate its usefulness along with the modelling techniques developed in challenging, complicated and innovative circuit design.

7.3 Simulations

Simulated dynamic load-lines for the outer fingers of the transistor elements in the NUPDA design at 23 GHz are shown in 7.13. It can be observed that all of the elements are almost ideally power matched except the first element which is not matched for power. This arises from not being able to realise the required high characteristic impedance on its drain line. See table 7.2. Simulated small-signal S-parameters are shown in Fig. 7.14 (a). The typical small-signal gain is about 22 dB, the input return loss is better than 10 dB and the output return loss is better than 8 dB across the 8 to 40 GHz bandwidth. Ten watts of saturated output power is achieved at about 16 dB of power gain and with power-added efficiency of about 13-18% across the 8 to 40 GHz bandwidth as shown in Fig. 7.14 (b).

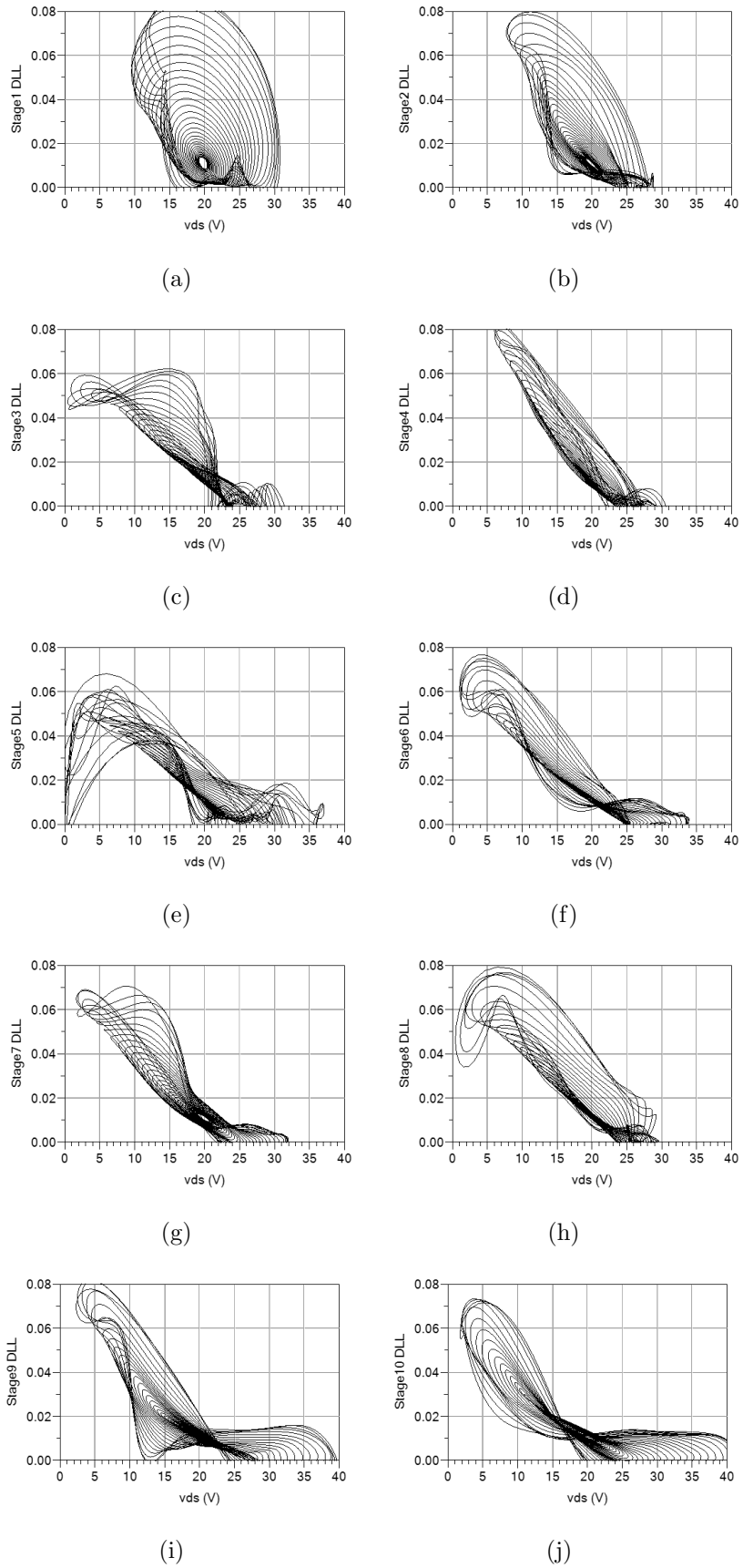
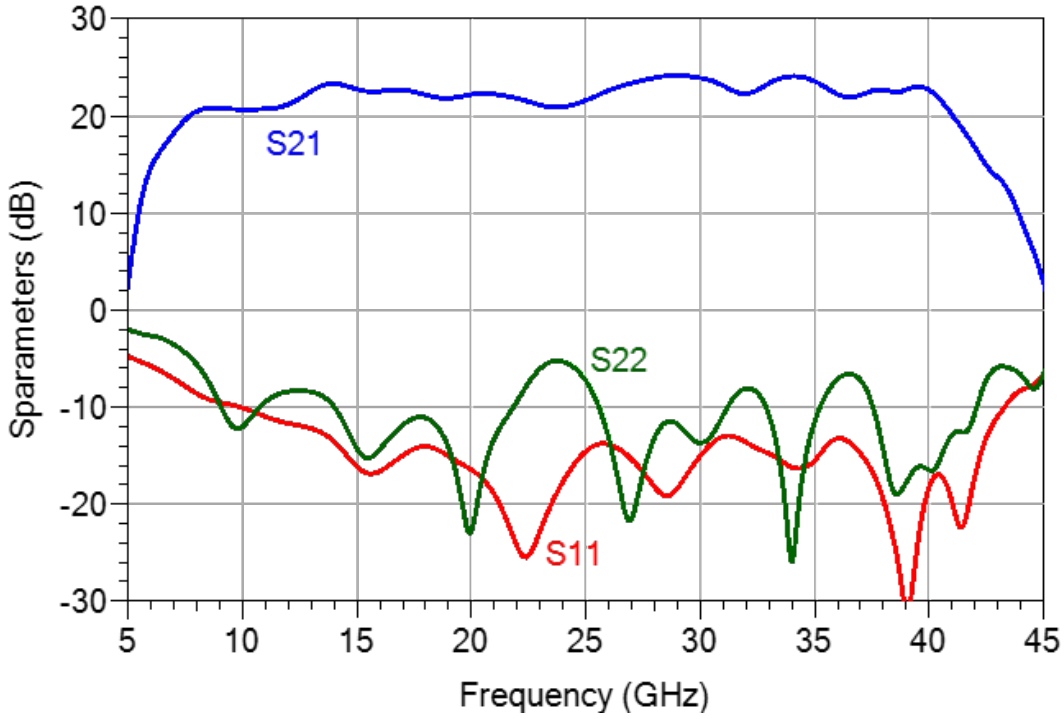
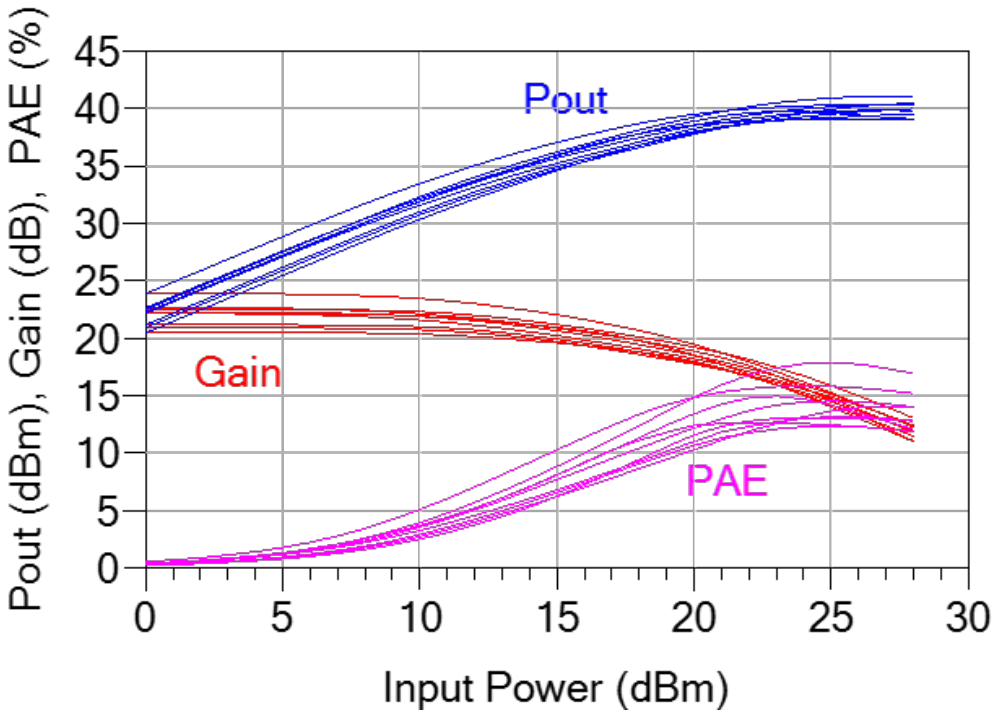


Figure 7.13: Simulated dynamic load-lines for outer finger (62.5 μm) of each transistor element (4×62.5 μm) in the 10-stage NUDPA at 23 GHz with input power swept from -10 to 23 dBm.



(a) Small-signal performance.



(b) Large-signal performance. Input power swept from 0 to 28 dBm in 0.5 dBm steps. The different traces represent the different frequencies where the frequency is swept from 8 to 40 GHz in 4 GHz steps.

FIGURE 7.14: Quiescent bias is: V_{DS} = 20 V and V_{GS} =-1.3 V. Ambient temperature is 27C°.

7.4 Summary

A 10 W nonuniform distributed power amplifier is designed using GaN/SiC process technology. The design relies heavily on the large-signal intrinsic model developed in this thesis which is used to optimise the transistor unit cell for the design and to accurately scale and predict the optimum load-pull target for the circuit. A novel broadband 4:1 impedance transformer and power combiner is designed and fabricated, and then used in the design in order to meet the power and bandwidth requirements under the constraints of the process technology. Excellent simulated results are demonstrated using MQFET with no convergence issues.

8

Conclusion and Future Opportunities

Specific achievements are highlighted after each chapter. This chapter provides a conclusion to the dissertation with a discussion of the main outcomes and suggestions for future work.

8.1 Outcomes

The technical contributions in this dissertation are presented in Chapters 3-7. The main goal of this work was to develop a new approach to scalable, large-signal modelling of GaAs and GaN microwave HEMT devices, that can be used to accurately synthesise arbitrary device geometries and that is consistent with the small-signal model. Chapter 3 presented a formulation of an intrinsic small-signal model that is consistent with the associated large-signal model. The extracted small-signal parameters of the

equivalent model linearly scaled with device width and are independent of frequency in the non-dispersive operating regions. Memory effects, i.e. thermal and trap states, are embedded in the steady-state small-signal intrinsic parameters, and for the large-signal model to scale accurately, these effects needed to be separated from the extracted small-signal intrinsic data which led to Chapters 4 and 5.

In Chapter 4, a thermal FEM SPICE model was developed to model the local temperature rise in multifinger devices taking into account self-heating, mutual heating and end effects. A lumped-element thermal model was formulated that can accurately model the local temperature rise, i.e. at the individual gate finger, and scales correctly with number of fingers. The lumped-element thermal model was fitted to SPICE thermal model data, whose results were verified using GRT measurements. Chapter 5 presented a newly-developed trap-state characterisation technique that was used to fit an adequate trap circuit model over a wide bias range. The thermal and trap circuit models form part of the complete large-signal model, in which the interaction of the thermal and trap models are critical to the model completeness, scalability and accuracy, as well as the consistency with the small-signal model.

The complete model was fitted to the extracted multi-bias small-signal intrinsic parameters in Chapter 6, which were shown to scale linearly with the device size. The model was shown to predict the small-signal and large-signal performance of arbitrary synthesised device geometries. Chapter 7 presented a case study power amplifier design using GaN HEMT technology that was based on the complete large-signal modelling techniques and procedures developed in this dissertation. The design benefited from the scalable model in optimising the transistor unit cell layout to achieve best electrical performance and facilitating electromagnetic analysis of all passive circuit features, including FET access networks, in a single model. The design also benefited from the built-in electrothermal simulation capability ensuring accurate device scaling and allowing local temperature rise to be monitored under small-signal as well as large-signal excitation and under a range of bias, temperature and mounting conditions.

8.1.1 Non-dispersive Scalable Small-signal Characterisation

The first step of the procedure started with the extraction of the true intrinsic linear model parameters. A non-dispersive small-signal model equivalent circuit was introduced in Chapter 3 in which the model consists of four capacitance terms needed to fit the four imaginary parts of the intrinsic Y-parameters. The use of internal ports in EM tools were then discussed in order to accurately model the metalisation of the device and de-embedd it from the measured small-signal parameters to reveal to the intrinsic small-signal parameters. The resulting model exhibited linear scaling properties with device width and the element values were dispersionless. The extraction method is proven to be a powerful technique that has enabled MMIC design engineers to reliably design high-performance circuits using models the bounds of the measured data used for model extraction beyond measured data.

8.1.2 Single-finger Thermal Characterisation

A lumped-element thermal model was formulated at the level of the individual gate finger of a multifinger device in Chapter 4. The structure of the model was based on transient simulations performed with FEM SPICE model that was developed to capture the heat-flow in the vertical dimension as well as the lateral heat flow, mutual heating and end effects. Four resistors in total were needed to construct the model, two resistors were needed vertically to account for the heat-flow through the substrate and one resistor either side of the gate junction where the power is assumed to be injected, another resistor was needed to model the suppress the lateral heat flow between fingers. For the outermost finger, an end effect resistor was needed. A multifinger temperature data obtained from SPICE simulations, including several gate-to-gate spacings and substrate thicknesses was used to optimise the lumped-element finger model. The optimised model was verified for scalabilty with gate-to-gate spacings and substrate thicknesses. A complete single-finger large-signal model was fitted in Chapter 6. The model incorporates a trap-centre with a thermal node that is connected to the lumped-element thermal model. The single-finger large-signal model including trapping and the

lumped-element thermal model combine to form a powerful but user-friendly and accessible electrothermal simulation that can be conveniently implemented into a MMIC design flow.

8.1.3 Trap-state Extraction

In Chapter 5, a technique for extracting parameters for a trap centre model in GaAs an GaN was developed. The basic device parameters including g_m, g_{ds}, R_s, R_d and R_T were extracted, as explained in Chapter 3. A cluster of pulse voltages with sufficient bias points V_{GS} and V_{DS} were measured to give coverage over the operating range of interest, while observing the timing consideration of long quiescent time and short pulse time. The data was then fitted to a current model in order to extract the steady-state trap voltages. The charactersitic frequency of the trap, ω_0 was extracted by measuring the time constant of the transient response of an emission event. The model was used to accurately simulate the low-frequency dispersion in the device.

8.2 Broader Adoption

The non-dispersive scalable small-signal modelling technique described in Chapter 3, was used by many others in applications that are outside the scope of this thesis. Some related publications are listed below:

J. Tarazi, M. C. Rodriguez, A. Dadello, M. G. McCulloch, A. P. Fattorini, S. Hwang, R. Clement, A. E. Parker, J. T. Harvey, and S. J. Mahon, "GaAs E band radio chipset," in *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2013, pp. 1–4.

A. Bessemoulin, M. C. Rodriguez, S. J. Mahon, A. E. Parker, and M. C. Heimlich, "150 GHz GaAs amplifiers in a commercial 0.1-μm GaAs pHEMT process," in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, 2016, pp. 552–555.

A. Bessemoulin, J. Tarazi, M. Rodriguez, M. G. McCulloch, A. E. Parker, and S. J.

Mahon, "Reduced-size E-band GaAs power amplifier MMIC," in *2015 10th European Microwave Integrated Circuits Conference (EuMIC)*, 2015, pp. 25–28.

M. C. Rodriguez, J. Tarazi, A. Dadello, E. R. O. Convert, M. G. McCulloch, S. J. Mahon, S. Hwang, R. G. Mould, A. P. Fattorini, A. C. Young, J. T. Harvey, A. E. Parker, M. C. Heimlich, and W. Wang, "Full ETSI E-band doubler, quadrupler and 24 dBm power amplifier," in *2012 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2012, pp. 1–4.

S. J. Mahon, A. Dadello, P. Vun, J. Tarazi, A. C. Young, M. C. Heimlich, J. T. Harvey, and A. E. Parker, "LNA design based on an extracted single gate finger model," in *2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct 2010, pp. 1–4.

A. Bessemoulin, J. Tarazi, M. G. McCulloch, and S. J. Mahon, "0.1-μm GaAs phemt W-band low noise amplifier MMIC using coplanar waveguide technology," in *2014 1st Australian Microwave Symposium (AMS)*, 2014, pp. 1–2.

B. K. Schwitter, J. Tarazi, A. E. Parker, and S. J. Mahon, "Assessing the effects of field plates in an AlGaN/GaN-on-SiC HEMT model extraction," in *2014 1st Australian Microwave Symposium (AMS)*, 2014, pp. 17–18.

8.3 Future Opportunities

8.3.1 Further Model Improvement

The lumped-element thermal network used in the large-signal model is only fitted to steady-state operation, and it would be desirable to incorporate the transient response and dynamic thermal effects. Adding the correct dynamics to the thermal model in addition to the trap model, would result in more accurate system level simulations with amplitude modulated waveforms and associated linearisation techniques. Intermodulation product are often related to the interaction of heating and trapping dynamics. Performing two-tone measurements with swept tone-spacing would be a simple way to

verify or improve the model and the modelling technique. More extensive measurements using other modulated waveforms, perhaps under load-pull conditions, might also be explored to improve the dynamic thermal model.

As for the intermodulation distortion effects, it would be also desirable to incorporate the transient response and dynamic thermal effects in the model in order to investigate the pulse recovery time and effects in high power pulsed applications. Performing DC pulsed and RF pulsed measurements on devices could be sufficient to verify or improve the modelling technique.

It would be desirable and convenient to have noise embedded in the intrinsic large-signal model. Noise modelling is not in the scope of this thesis, however, it is briefly discussed in Chapter 3 where it is linked to the intrinsic region of the FET. Having a non-dispersive large-signal core model that accurately scales with device size, is a key enabler for the eventual implementation of an accurate and scalable noise model to the core large-signal model. In return, the simulated noise can be compared with measurements in order to verify its scalability with device size and bias and terminating impedances. Moreover, if successful, the need of a separate small-signal model could be eliminated entirely.

8.3.2 Application Perspective

The complete large-signal intrinsic model can be used to develop highly optimised application-specific transistor cells. The model scales electrically and thermally with device width, facilitating the synthesise of arbitrary device geometries optimised to deliver specific performance requirements. Such work may result in novel transistor layouts that can be promoted by semiconductor foundries and used by MMIC design engineers to help improve their designs and extract the best possible performance from a given process technology. Some of the common practical applications that could be explored include; extremely compact layouts, high frequency operation with maximum gain, lowest noise figure, improved thermal characteristics leading to better reliability and unconditionally stable transistor cells. The model can be used as the basis to build up a database of worldwide semiconductor technologies.

A

Appendix A

A.1 2D FEM SPICE CODE

```
############################## AWK SCRIPT FOR 2D SPICE MULTI-FINGER THERMAL MODEL ##########################
######################################### JABRA TARAZI - June 2020 ########################################


  function MultiFinger() {

for (m=0;m<numfing/2;m++){
for (j = 0; j < ynodes; j++) {
for (i = 0; i < xnodes; i++) {
if ( (j == 0)){# && (i*dx >= DrainPad/2  + (SourcePad +ChanneLength*dc )*int((m+1)/2)+ (
DrainPad + ChanneLength*dc)*int(m/2)  )  && (i*dx < DrainPad/2   + ChanneLength*dc+ (
SourcePad +ChanneLength*dc)*int((m+1)/2) + (DrainPad + ChanneLength*dc)*int(m/2)) ) {
rr = repi*dx/ 2^j/dc ; alpha = alpha_algan ;
}else if ( (j == 5) )  {
rr = tbr*dx;
```

```
}else if ( (j >= 0) && (j <= 4))  {
rr = rganx/ 2^j ; alpha = alpha_gan;
}else {
rr = rx/ 2^j ; alpha = alpha_sic;
}
printf "Bx%03d%03d  n%03d%03d  n%03d%03d I= (V(n%03d%03d,n%03d%03d))  /
( %g * ( ((V(n%03d%03d)+V(n%03d%03d))/2 + %g) / (%g) )^%g )  \n",
i,  j,     i, j,    i+1,  j,     i+1,   j,   i,  j,
-1.0*beta*rr,   i+1, j,     i, j , 1e-6, 300, 1.0*alpha > OutFileName
}
     printf "\n"  > OutFileName
  }

for (i = 0; i < xnodes; i++) {
for (j = 0; j < ynodes; j++) {
if ( (j == 0)){# && (i*dx >= DrainPad/2  + (SourcePad +ChanneLength*dc )*int((m+1)/2)+ (
DrainPad + ChanneLength*dc)*int(m/2)  )  && (i*dx < DrainPad/2   + ChanneLength*dc+ (
SourcePad +ChanneLength*dc)*int((m+1)/2) + (DrainPad + ChanneLength*dc)*int(m/2)) ) {
rr = rgany * 2^j*dc ;  alpha = alpha_gan;
}else if ( (j >= 0) && (j <= 4))  {
rr = rgany * 2^j ;  alpha = alpha_gan;
}else {
rr = ry* 2^j ; alpha = alpha_sic;
}
printf "By%03d%03d  n%03d%03d  n%03d%03d I= V(n%03d%03d,n%03d%03d) /
( %g * ( ((V(n%03d%03d)+V(n%03d%03d))/2 + %g) / (%g) )^%g )\n",
i,  j,     i, j,    i,  j+1,     i,   j+1,   i,  j,
-1.0*beta*rr,   i, j+1,     i, j , 1e-6, 300, alpha  > OutFileName
}
     printf "\n" > OutFileName
  }

  print "\n* ambient nodes" > OutFileName

for (i = 0; i < xnodes; i++) {
printf "va%03d%03d  n%03d%03d  0 %f\n", i, j, i, j, va > OutFileName
}
printf "\n" > OutFileName
for (j = 0; j < ynodes; j++) {
printf "va%03d%03d  n%03d%03d  0 %f\n", i, j, i, j, va > OutFileName
}


 print "\n* power input" > OutFileName
```

```
  ii = ii / xpnodes;

for (m=0;m<numfing/2;m++){
for (i = 0; i < xnodes; i++) {

if (i*dx == DrainPad/2   + ChanneLength*dc/2+ (SourcePad +ChanneLength*dc)*int((m-1)/2+1)
+ (DrainPad + ChanneLength*dc)*int(m/2))  {

printf "ia%03d%03d  0 n%03d%03d %g pwl 0 0 10n %g\n", i, 0, i, 0, ii, ii > OutFileName
}
}
}



  printf ".control\n" > OutFileName
  printf "   op\n" > OutFileName
   for (m=0;m<numfing/2;m++){
for (i = 0; i < xnodes; i++) {
j =0;
if (i*dx == DrainPad/2   + ChanneLength*dc/2+ (SourcePad +ChanneLength*dc)*int((m-1)/2+1)
+ (DrainPad + ChanneLength*dc)*int(m/2))  {
printf "   print n%03d%03d\n",  i, 0 > OutFileName
}
}
}



################################### Transient Simulation ##############################################
  if (AC) {

   printf "   tran 10n 1000u 200n\n" > OutFileName
    printf "   write %s.raw  all\n ", BaseFileName > OutFileName
    printf "   plot n%03d%03d",  (G2G/2/dx + (ChanneLength*dc/dx)/2 +1 ), 0 > OutFileName
printf " xlog\n" > OutFileName

}
 ################################### Transient Simulation ##############################################

#################################### Printing out nodes of j = 0 ##########################################



for (k = 0; k < LineNum; k++) {
printf " print " > OutFileName
for (i = (k)*xnodes/LineNum; i < (k+1)*xnodes/LineNum ; i+=1)  {
for (j = 0; j < 1; j+=1) {
```

```
printf " V(n%03d%03d)",  i, j > OutFileName
}
}
if ( k == 0) {printf " > " BaseFileName ".txt\n" > OutFileName } else {printf " >> " BaseFileName ".txt\n"
> OutFileName}
 }
  printf "\ndestroy all\n" > OutFileName
  printf ".endc\n" > OutFileName
}
}

 BEGIN {

  ################################### dx/dy/dz dimensions ######################################
  X = 370 ; # dimension of substrate in x-dimension
  Y = H ; # Substrate thickness in um
  dx = 0.25 ;     # x-grid in um
  dy = 0.05 ;     # y-grid in um
  dz = 1 ;      # Fixed z-dimension in 2-D analysis
  dc = 1 ; # channel grid in um ( 10 grids for 1um)
  hc = 1  ; # number of injected points in the channel
  AC = AC ; # 0/1 Transient Analysis Switch
  beta = 0.68 ; # Normalised Temperature Scaling Factor based on Substrate Thickness
  ################################### End of dx/dy/dz dimensions ################################


  ################################### Materials Properties ######################################
  alpha_gan = 0.49; # Thermal Nonlinear conductivity Factor of GaN = 0.49
  alpha_sic = 1.49; # Thermal Nonlinear conductivity Factor of SiC = 1.49
  alpha_algan = 0.43; # Thermal Nonlinear conductivity Factor of AlGaN = 0.43
  rganx =  5555 * dx / dy / dz ;    # Thermal conductivity of GaN = 150-180 W/m.K
  rgany =  5555 * dy / dx / dz ;    # Thermal conductivity of GaN = 150-180 W/m.K
  rsicx =  2128 / dz ;       # Thermal conductivity of SiC in X,Y = 470 W/m.K
  rsicz =  1675 / dz ;       # Thermal conductivity of SiC in Z = 370 W/m.K
  r_air =  37000000 / dz;    # Thermal conductivity of Air = 0.027 W/m.K
  c_air =  1.1055e-15 * dz;  # Heat Capacity of Air = 1.005 J/Kg.C, and Density = 1.1 g/cm^3
  c_gan = 3.0135e-12 * dz;   # Heat Capacity of GaN = 490 J/Kg.C, and Density = 6.15 g/cm^3
  c_sic = 2.144e-12 * dz;  # Heat Capacity of SiC = 670 J/Kg.C, and Density = 3.2 g/cm^3
  MetThick = 5.3 ; # Metalisation Thickness in um
  ChanneLength = 3; # Channel length in um
  DrainPad = G2G - ChanneLength; # Drain Pad size
  SourcePad = G2G - ChanneLength; # Source Pad size
  rgold = 3144 ; # Thermal conductivity of Gold = 318 W/m.K
  epi1 = 4e4 /dz ; # Thermal conductivity of AlGaN = 25 W/m.K
  tbr = 3.3e4/0.1; # Thermal conductivity of TBR material 3.3*10^-8 W/m^2.K
```

```
va = 383 ;            # Ambient Temp in Kelvin.
LineNum = 100 ; # Dividing the Print-out statement into small portions to suit WinSpice
###################################### End of Materials Properties ##############################


###################################### ON/OFF Switches ##########################################
Metal = 1 ; # 0/1, OFF/ON Switch for Metalisation of the transistor
Bvia = 0 ;  # 0/1, OFF/ON Switch for BackVia
BV_hollow = 1 ; # 0/1, OFF/ON Switch for solid/hollow backvia
Channel = 1 ;   # 0/1, OFF/ON Switch for InGaAs/AlGaAs
###################################### End of ON/OFF Switches ###################################


###################################### Dimensions ###############################################
xnodes = X / dx ;      # Number of elements in the x-direction
ynodes1 =(log(Y/dy)) ;      # Number of elements in the y-direction
ynodes = ynodes1/log(2)+1; # Number of nodes in y-direction
xpnodes = 1 ;       # Number of fingers where the power is dissipated
G2G = G2G ;        # gate-to-gate Spacing between fingers in um
MetEdge = (G2G/2+ ChanneLength*dc + BV2Pad  + BViaL)/dx ;
xnodes_2 = MetEdge + ynodes + 2 ;
###################################### End of Dimensions ########################################


###################################### Power Dissipation ########################################
finger = numfing ; # Number of gate fingers in transistor
pp = PWR  ;       # Power dissipated into the device in W/mm
ii = pp*xpnodes/1000 ; # Power per finger in W/um
###################################### Power Dissipation ########################################


###################################### CIR Output Filename ######################################
BaseFileName = finger"_Fingers\\"finger"_Fin_G2G_"G2G"_um_H_"H;
OutFileName = finger"_Fin_G2G_"G2G"_um_H_"H".cir";
###################################### End of CIR Output Filename ###############################


print "* 2-d thermal model for spice\n" > OutFileName

print "* RC reference\n" > OutFileName
printf "Cr  ref  0 %g\n", c_sic > OutFileName
printf "Rr  ref  varef %g\n", rsicx > OutFileName
```

```
  printf "Vr  varef 0 %g\n", va > OutFileName
  printf "Ir  0 ref %g pwl 0 0 10n %g\n", ii, ii > OutFileName

  print "* 2-d thermal model for spice\n" > OutFileName

  rx = rsicx * dx / dy ;          # Resistance in x-dimension
  ry = rsicz / dx * dy ;          # Resistance in y-dimension
  c =  c_sic * dx * dy ;         # Total capacitance
  rgoldx = rgold * dx / MetThick / dz ;  # Resistance og Metal in x-dimension
  repi = epi1/0.025 ; # Channel layer Resistance

    print "\n* mirror plane" > OutFileName

  for (j = 0; j < ynodes; j++) {
     printf "Em%03d%03d  m%03d%03d        0  n%03d%03d  0  1\n", 0, j, 0, j, 1, j > OutFileName
 if (j == 0){
 printf "Rm%03d%03d  m%03d%03d  n%03d%03d  %f\n", 0, j, 0, j, 0, j, repi*dx/ 2^j/dc  > OutFileName;
 }else if ((j > 0)&&( j <= 4)){
 printf "Rm%03d%03d  m%03d%03d  n%03d%03d  %f\n", 0, j, 0, j, 0, j, rganx / 2^j > OutFileName;
 }else if (j == 5){
 printf "Rm%03d%03d  m%03d%03d  n%03d%03d  %f\n", 0, j, 0, j, 0, j, tbr*dx / 2^j > OutFileName;
 }else {
 printf "Rm%03d%03d  m%03d%03d  n%03d%03d  %f\n", 0, j, 0, j, 0, j, rx / 2^j > OutFileName; }
  }

  print "\n* capacitors at each node" > OutFileName

for (j = 0; j < ynodes; j++) {
for (i = 0; i < xnodes; i++) {
for (m=0;m<numfing/2;m++){
if ( (j == 0) && (i*dx >= DrainPad/2  + (SourcePad +ChanneLength*dc )*int((m-1)/2+1)+ (
DrainPad + ChanneLength*dc)*int(m/2)  )  && (i*dx < DrainPad/2   + ChanneLength*dc+ (
SourcePad +ChanneLength*dc)*int((m-1)/2+1) + (DrainPad + ChanneLength*dc)*int(m/2)) ) {
cc = c * 2^j*dc;
} else {
cc = c * 2^j
}
}
printf "Cx%03d%03d  n%03d%03d  0 %g\n", i, j, i, j, cc > OutFileName
}
}
  print "\n* resistor grid" > OutFileName

################################### Call The MultiFinger Function ##############################
```

```
  MultiFinger() ;

}
```

B

Appendix B

B.1 3D FEM SPICE CODE

```
############################ AWK SCRIPT FOR 3D SPICE SINGLE-FINGER THERMAL MODEL ########################
######################################### JABRA TARAZI - June 2020 ######################################


BEGIN {

xnodes = 40 ;  # Dimension of substrate in x-dimension in um (dx*xnodes)
ynodes = 12 ; # Substrate thickness in um (dy*2^12)
znodes = 14 ; # Substrate extension in um (dz*2^12)
xpnodes = 5 ; # Width of the gate-finger in um (dx*xpnodes)
shift = 0 ; # Used to Shift the heat-source
dx = 75 ; # x-grid along the gate-finger in um
dy = 0.05 ; # y-grid through the substrate in um
dz = 0.125 ; # z-grid either side of the gate-finger in um
rsicx =  2128  ;        # Thermal Conductivity of SiC in X,Y = 470 W/m.K
```

```
  rsicz =  1675  ;        # Thermal Conductivity of SiC in Z = 370 W/m.K

rx = rsicx * dx / dy / dz ;
ry = rsicz * dy / dx / dz ;
rz = rsicx * dz / dx / dy ;

rxp = rx ;
va = 383; # Ambient Temp in Kelvin.
alpha = 1.49 ; # Thermal Nonlinear Conductivity Factor of SiC = 1.49
beta = 1; # Normalizsed Temperature Scaling Factor based on Substrate Thickness
ii = 5.2/1000 ; # Power per finger in W/um

BaseFileName = "3D_W_"xpnodes*dx*2"_H_"ynodes;
OutFileName = BaseFileName ".cir" ;


printf "\n * 2-d odd/even symmetry experiment\n" > OutFileName


printf "\n * y-symmetry plane\n" > OutFileName

for (j = 0 ; j < ynodes ; j++) {
for (k = 0; k < znodes ; k++) {

printf "Rmy%03d%03d%03d  my%03d%03d%03d  n%03d%03d%03d  %f\n", 0, j, k, 0, j, k,  0, j, k, rx/2^(j-k) > OutFileName
     printf "Emy%03d%03d%03d  my%03d%03d%03d 0  n%03d%03d%03d  0  1\n", 0, j, k, 0, j, k, 1, j, k > OutFileName


      }
     }

printf "\n * z-symmetry plane\n" > OutFileName

for (i = 0 ; i < xnodes ; i++) {
for (j = 0; j < ynodes ; j++) {

printf "Rmz%03d%03d%03d  mz%03d%03d%03d  n%03d%03d%03d  %f\n", i, j, 0, i, j, 0,  i, j, 0, rz*2^(k-j) > OutFileName
     printf "Emz%03d%03d%03d  mz%03d%03d%03d 0  n%03d%03d%03d  0  1\n", i, j, 0, i, j, 0, i, j, 1 > OutFileName


      }
     }


printf "\n * resistances in x-direction\n" > OutFileName
```

```
for (k = 0 ; k < znodes ; k++) {
for (j = 0 ; j < ynodes ; j++) {
for (i = 0 ; i < xnodes ; i++) {

printf "Bx%03d%03d%03d  n%03d%03d%03d  n%03d%03d%03d I=V(n%03d%03d%03d,n%03d%03d%03d)/
( %g * (((V(n%03d%03d%03d) + V(n%03d%03d%03d))/2 + %g)/ (%g) )^%g )\n",
i,  j,  k,  i, j, k,  i+1,  j, k,  i+1,   j, k,   i,   j,  k,
-1.0*beta*(rx*2^(-j-k)),  i+1, j, k, i, j , k, 1e-6, 300, alpha  > OutFileName

}
}
}


printf "\n * resistances in y-direction\n" > OutFileName

for ( k = 0; k < znodes ; k++) {
for (i = 0 ; i < xnodes ; i++) {
for (j = 0 ; j < ynodes ; j++) {

printf "By%03d%03d%03d  n%03d%03d%03d  n%03d%03d%03d I=V(n%03d%03d%03d,n%03d%03d%03d)/
( %g * (((V(n%03d%03d%03d) + V(n%03d%03d%03d))/2 + %g)/ (%g) )^%g )\n",
i,  j,  k,  i, j, k,  i,  j+1, k, i, j+1, k,   i,   j,  k,
-1.0*beta*(ry*2^(j-k)), i, j+1, k, i, j , k, 1e-6, 300, alpha   > OutFileName

}
}
}

printf "\n * resistances in z-direction\n" > OutFileName

for ( i = 0; i < xnodes ; i++) {
for (j = 0 ; j < ynodes ; j++) {
for (k = 0 ; k < znodes ; k++) {

printf "Bz%03d%03d%03d  n%03d%03d%03d  n%03d%03d%03d I=V(n%03d%03d%03d,n%03d%03d%03d)/
( %g * (((V(n%03d%03d%03d) + V(n%03d%03d%03d))/2 + %g)/ (%g) )^%g )\n",
i,  j,  k,   i, j, k,  i,  j, k+1, i, j, k+1,   i,   j,  k,
-1.0*beta*(rz*2^(k-j)), i, j, k+1, i, j , k, 1e-6, 300, alpha  > OutFileName

}
}
}
```

```
printf "\n * ambient nodes\n" > OutFileName

#j = ynodes ;

for (i = 0 ; i < xnodes ; i++) {
for (k = 0; k < znodes; k++) {
printf "va%03d%03d%03d  n%03d%03d%03d  0 %f\n", i, j, k, i, j, k, va > OutFileName

}
}


printf "\n * ambient nodes\n" > OutFileName

#k = znodes ;

for (i = 0 ; i < xnodes ; i++) {
for (j = 0; j < ynodes; j++) {
printf "va%03d%03d%03d  n%03d%03d%03d  0 %f\n", i, j, k, i, j, k, va > OutFileName

}
}

printf "\n * ambient nodes\n" > OutFileName

#i = xnodes ;

for (j = 0 ; j < ynodes ; j++) {
for (k = 0; k < znodes; k++) {
printf "va%03d%03d%03d  n%03d%03d%03d  0 %f\n", i, j, k, i, j, k, va > OutFileName

}
}

printf "\n * power nodes\n" > OutFileName

j = 0 ;
k = 0;

for (i = shift; i < xpnodes+shift ; i++) {

printf "ia%03d%03d%03d  0 n%03d%03d%03d %g pwl 0 0 10n %g\n", i, j, k, i, j, k, ii*dx, ii*dx > OutFileName

}
```

```
printf ".control\n" > OutFileName
printf "op\n" > OutFileName

printf "\n * print temperature at the nodes\n" > OutFileName

for (i = 0; i < xpnodes ; i++) {

printf "print n%03d%03d%03d\n",  i, 0, 0 > OutFileName

}

printf "print " > OutFileName
for (i = 0; i < xpnodes; i++) {
for (j = 0; j < 1; j++) {
printf " V(n%03d%03d%03d)",  i, j, 0 > OutFileName

}
}

printf " > " BaseFileName"_X.txt\n" > OutFileName

printf "destroy all\n" > OutFileName
printf ".endc\n" > OutFileName

}
```

List of Abbreviations

ac	Alternating Current
AlGaAs	Aluminium Gallium Arsenide
AlGaN	Aluminium Gallium Nitride
ANN	Artificial Neural Network
CAD	Computer-aided Design
DA	Distributed Amplifier
dc	Direct Current
DUT	Device Under Test
EM	Electromagnetic
FEM	Finite Element Method
FET	Field Effect Transistor
FFT	Fast Fourier Transform
FPT	Folded Patches Transformer
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GRT	Gate Resistance Thermometry
HEMT	High Electron Mobility Transistor
LNA	Low Noise Amplifier
MMIC	Monolithic Microwave Integrated Circuit
NUDPA	Nonuniform Distributed Power Amplifier
NVNA	Nonlinear Vector Network Analyser

OSV	Outside Source Via
PA	Power Amplifier
PAE	Power-added Efficiency
PDK	Process Design Kit
RF	Radio Frequency
RMSE	Root Mean Squared Error
pHEMT	pseudomorphic High Electron Mobility Transistor
SiC	Silicon Carbide
SMU	Source Measure Unit
TBR	Thermal Boundary Resistance
TFR	Thin-film Resistor
VNA	Vector Network Analyser
2-DEG	Two-Dimensional Electron Gas

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Statement of Candidate

I certify that the work in this thesis entitled "**Nonlinear Modelling of GaAs and GaN High Electron Mobility Transistors**" has not previously been submitted for a degree, nor has it been submitted as part of requirements for a degree to any other university or institution other than Macquarie University.

Except where acknowledged in the customary manner, the material presented in this thesis is, to the best of my knowledge, original and written by me.

In addition, I certify that all information sources and literature used are indicated in the thesis.

Jabra Tarazi
November 2020